SGM6617

23V V_{IN}, 25V V_{OUT}, 4.5A Boost Converter with ±1.6% (MAX) Accuracy Input Average Current Limit and True Load Disconnection

GENERAL DESCRIPTION

The SGM6617 is a high-voltage non-synchronous Boost converter with a wide input voltage range from 2.9V to 23V while delivering adjustable output voltages between 4.5V and 25V. The device also has the input average current limit and true load disconnect functions. The input average current limit can be programmed from 0.1A to 3A by adjusting the external resistor connected to the ILIM pin. The integrated 35mΩ (TYP) isolation FET between the VP and SW pins ensures complete input-output disconnection when the device is disabled.

The SGM6617 utilizes the constant off-time peak current control topology to achieve enhanced dynamic performance. The device operates in PWM mode under heavy load conditions and automatically switches to PFM mode at light load, maintaining high conversion efficiency across the entire load range.

The SGM6617 implements various protection features, such as output over-voltage protection (OVP), cycle-by-cycle over-current protection (OCP), short-circuit protection and thermal shutdown to improve device robustness.

The SGM6617 is available in a Green TQFN-2.5×2-13L package.

FEATURES

- **Wide Input Voltage Range: 2.9V to 23V**
- **Wide Output Voltage Range: 4.5V to 25V**
- **0.1A to 3A Programmable Input Average Current Limit**
- **4.5A (TYP) Peak Switching Current Limit**
- **1.2MHz (TYP) Switching Frequency**
- **Integrated MOSFETs**
  - **ISO MOSFET: 35mΩ (TYP)**
  - **Low-side MOSFET: 40mΩ (TYP)**
- **True Load Disconnection when EN Shuts Down**
- **Output Over-Voltage Protection (OVP)**
- **Cycle-by-Cycle Over-Current Protection (OCP)**
- **Under-Voltage Lockout (UVLO)**
- **Thermal Shutdown**
- **External Loop Compensation**
- **Available in a Green TQFN-2.5×2-13L Package**

APPLICATIONS

Loudspeakers
Electric Appliances
POS Machines
Barcode Scanner

SIMPLIFIED SCHEMATIC

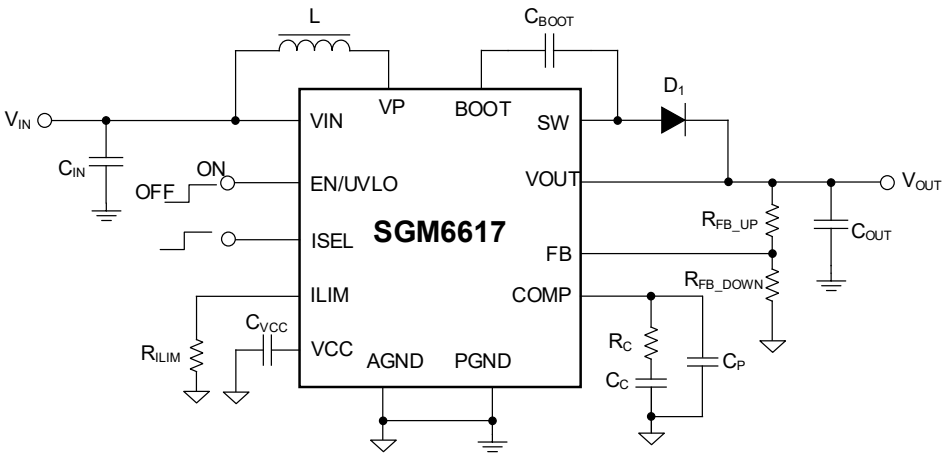


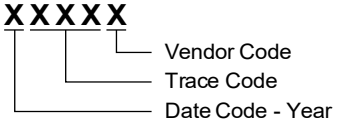
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6617	TQFN-2.5×2-13L	-40℃ to +125℃	SGM6617XTXG13G/TR	6617 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltage
- VIN, EN/UVLO ..... -0.3V to 25V
- SW, VOUT, VP ..... -0.3V to 30V
- BOOT ..... -0.3V to V_{SW} + 6V
- ISEL, FB, ILIM, VCC, COMP ..... -0.3V to 6V

Package Thermal Resistance
- TQFN-2.5×2-13L, θ_{JA} ..... 59.8℃/W
- TQFN-2.5×2-13L, θ_{JB} ..... 4.8℃/W
- TQFN-2.5×2-13L, θ_{JC} ..... 52.6℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±5000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.9V to 23V
Output Voltage Range, V_{OUT} ..... 4.5V to 25V
Effective Inductance Range, L .. 2.2μH to 10μH, 4.7μH (TYP)
Effective Input Capacitance Range, C_I ..... 22μF (TYP)
Effective Output Capacitance Range, C_O ..... 10μF to 2000μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

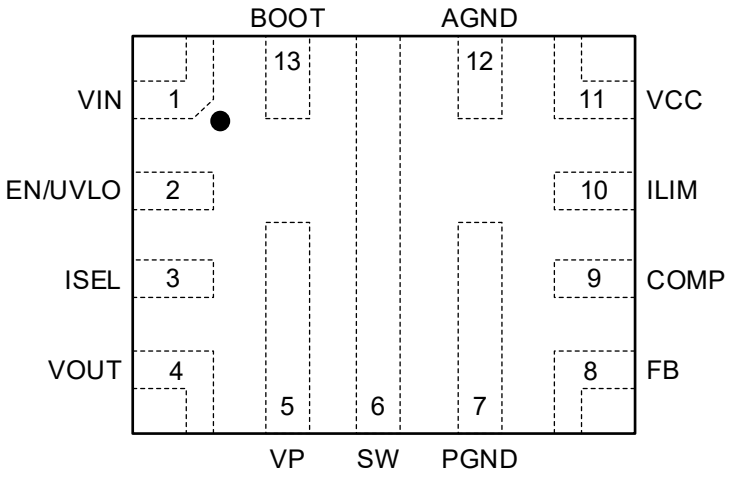
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2.5×2-13L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VIN	I	Power Supply Input of the IC.
2	EN/UVLO	I	Enable Input and Under-Voltage Lockout Pin. Logic high enables the device. Logic low shuts down the device. Connecting this pin to VIN through a resistor divider can program the start-up and shutdown levels of the device. This pin must not be left floating.
3	ISEL	I	Scale the ISO MOSFET to improve input average current limit accuracy and adjust peak switching current limit value. ISEL is high when I_{LIM} > 750mA. ISEL is low when I_{LIM} ≤ 750mA.
4	VOUT	P	Output of the Boost Converter.
5	VP	P	Drain of the Internal ISO MOSFET.
6	SW	P	Switching Node Pin. Connect to the drain of the internal low-side power MOSFET and the source of the internal ISO MOSFET.
7	PGND	P	Power Ground.
8	FB	I	Voltage Feedback Pin. Connect to the resistor divider to program the output voltage.
9	COMP	O	Output of the Internal Error Amplifier. Put the loop compensation network between this pin and the AGND.
10	ILIM	I	Input Average Current Limit Setting Pin. A resistor is placed between ILIM and AGND to program the input average current limit.
11	VCC	O	Output of the Internal Regulator. Connect this pin to AGND with a capacitor more than 1.0μF effective.
12	AGND	P	Analog Signal Ground.
13	BOOT	O	Gate Driver Supply of ISO MOSFET. Connect this pin to SW pin with a 0.47μF to 1μF ceramic capacitor.

NOTE: I = input, O = output, I/O = input/output, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, L = 4.7μH, V_{IN} = 5V and V_{OUT} = 12V, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply							
Input Voltage Range		V_{IN}		2.9		23	V
VIN Under-Voltage Lockout Threshold		V_{IN_UVLO}	V_{IN} rising		2.8	2.9	V
Quiescent Current into VOUT Pin		I_Q	IC enabled, no load, no switching, V_{IN} = 2.9V to 5.25V, V_{OUT} = 25V, V_{FB} = V_{REF} + 0.1V		80	120	μA
			IC enabled, no load, no switching, V_{IN} = 5.5V to 23V, V_{OUT} = 25 V, V_{FB} = V_{REF} + 0.1V		25	40	μA
Quiescent Current into VIN Pin			IC enabled, no load, no switching, V_{IN} = 2.9V to 5.25V, V_{FB} = V_{REF} + 0.1V		0.25	1	μA
			IC enabled, no load, no switching, V_{IN} = 5.5V to 23V, V_{FB} = V_{REF} + 0.1V		55	76	μA
VCC UVLO Threshold		V_{CC_UVLO}	V_{CC} rising		2.75		V
VCC UVLO Hysteresis		V_{CC_HYS}	V_{CC} hysteresis		170		mV
VCC Regulation		V_{CC}	I_{VCC} = 4mA, V_{OUT} = 12V		4.9		V
Shutdown Current into VIN Pin		I_{SD}	IC disabled, V_{IN} = 2.9V to 23V, EN = GND			2.6	μA
Leakage Current into SW		I_{SW_LKG}	IC disabled, V_{OUT} = V_{SW} = 25V,V_P floating			2	μA
Leakage Current into VP		I_{VP_LKG}	IC disabled, V_{OUT} = V_P = 25V,V_{SW} floating			2	μA
Leakage Current into FB		I_{FB_LKG}	IC disabled, V_{FB} = 1V			100	nA
Output Voltage							
Output Over-Voltage Protection Threshold		V_{OVP}	V_{OUT} rising	25.9	27.0	28.2	V
Output Over-Voltage Protection Hysteresis		V_{OVP_HYS}	OVP threshold		0.9		V
Reference Voltage							
Reference Voltage at FB Pin		V_{REF}		0.985	1	1.015	V
Power Switch							
Low-side MOSFET On-Resistance		R_{DSON}	V_{CC} = 4.9V		40		mΩ
ISO MOSFET On-Resistance			V_{CC} = 4.9V, ISEL = high		35		mΩ
ISO MOSFET On-Resistance (Scale)			V_{CC} = 4.9V, ISEL = low		130		mΩ
Current Limit							
Peak Switching Current Limit		I_{LIM_SW}	T_J = +25℃, R_{LIM} = 14.4kΩ, ISEL = high ,V_{IN} = 2.9V to 23V	3.50	4.50	5.65	A
			T_J = +25℃, R_{LIM} = 14.4kΩ, ISEL = low, V_{IN} = 2.9V to 23V	2.00	2.50	3.10	
Input DC Current Limit	0.75A to 3.0A	$I_{LIM\_DC\_ACCURACY}$	T_J = +25℃, V_{IN} = 5V, V_{OUT} = 12V, initial accuracy, ISEL = high	-1.6		1.6	%
	0.75A to 3.0A		T_J = -40 to +125℃, V_{IN} = 2.9V to 23V, V_{OUT} = 4.5V to 25V, initial accuracy, ISEL = high	-4.5		4.5	%
	0.2A to 0.75A		T_J = -40 to +125℃, V_{IN} = 2.9V to 23V, V_{OUT} = 4.5V to 25V, initial accuracy, ISEL = low	-7.0		12.0	%
	0.1A to 0.2A		T_J = -40 to +125℃, V_{IN} = 2.9V to 23V, V_{OUT} = 4.5V to 25V, initial accuracy, ISEL = low	-17.0		23.0	%

ELECTRICAL CHARACTERISTICS (continued)

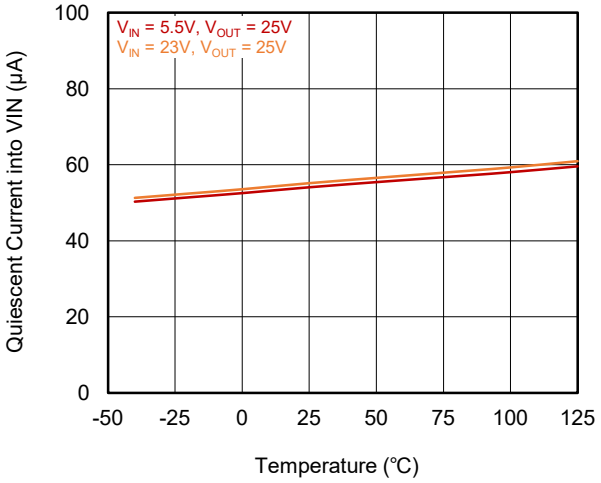
(T_J = -40℃ to +125℃, L = 4.7μH, V_{IN} = 5V and V_{OUT} = 12V, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 2.9V to 23V, V_{OUT} = 4.5V to 25V		1200		kHz
Soft-Start Time	t_{SS}			4		ms
Minimum Off-Time	t_{OFF_MIN}			110		ns
Minimum On-Time	t_{ON_MIN}			90		ns
Error Amplifier						
COMP Pin Sink Current	I_{SINK}			19		μA
COMP Pin Source Current	I_{SOURCE}			18		μA
COMP Pin High Clamp Voltage	V_{CCLPH}			1.7		V
COMP Pin Low Clamp Voltage	V_{CCLPL}			0.5		V
Error Amplifier Trans-Conductance	G_{EA}			250		μS
Logic Interface						
EN Logic High Threshold	V_{EN_H}				0.812	V
EN Logic Low Threshold	V_{EN_L}		0.3			V
EN Threshold Hysteresis	V_{EN_L}			50		mV
UVLO Rising Threshold	V_{UVLO}		0.75	0.813	0.88	V
Sourcing Current at the EN/UVLO Pin	I_{UVLO_HYS}		1.55	2.00	2.35	μA
ISEL Pin Logic High Threshold	V_{IH}				0.8	V
ISEL Pin Logic Low Threshold	V_{IL}		0.4			V
ISEL Pin Internal Pull-Down Resistor	R_{DOWN}			700		kΩ
Thermal Shutdown						
Thermal Shutdown Rising Threshold	t_{SD_R}	T_J rising		150		℃
Thermal Shutdown Falling Threshold	t_{SD_F}	T_J falling		130		℃

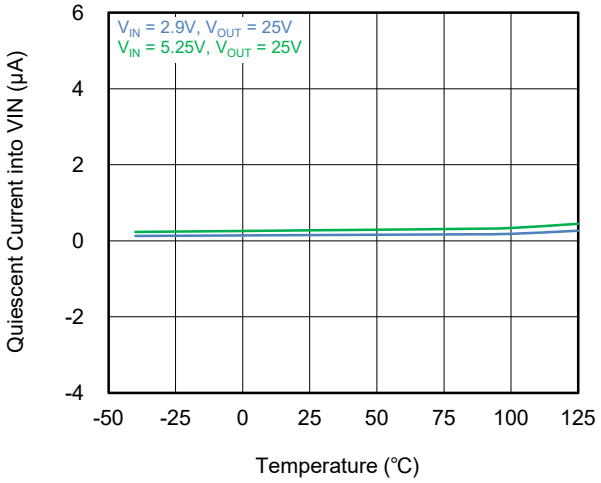
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, f_{SW}= 1.2MHz, unless otherwise noted.

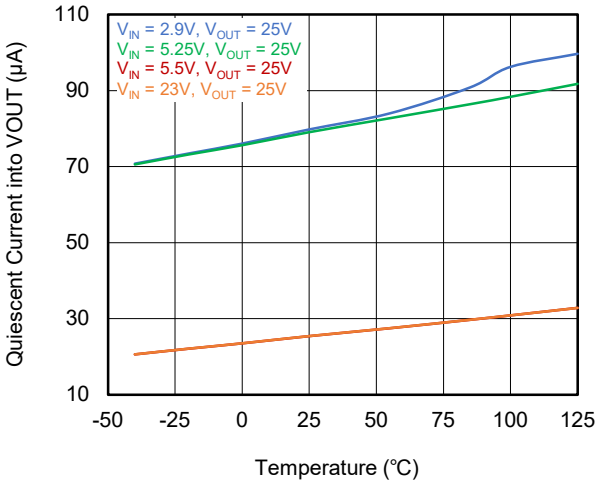
Quiescent Current into VIN vs. Temperature



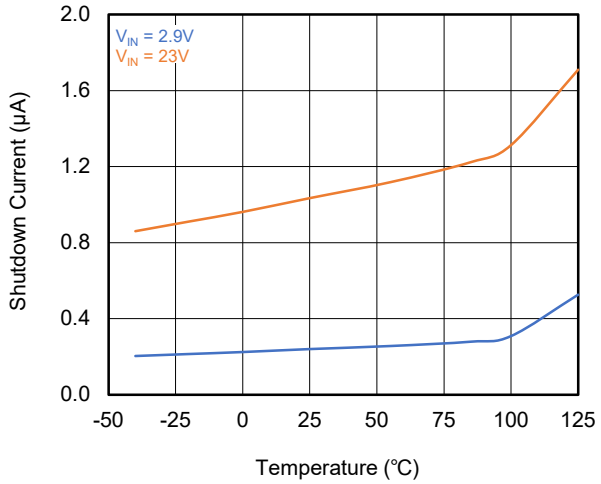
Quiescent Current into VIN vs. Temperature



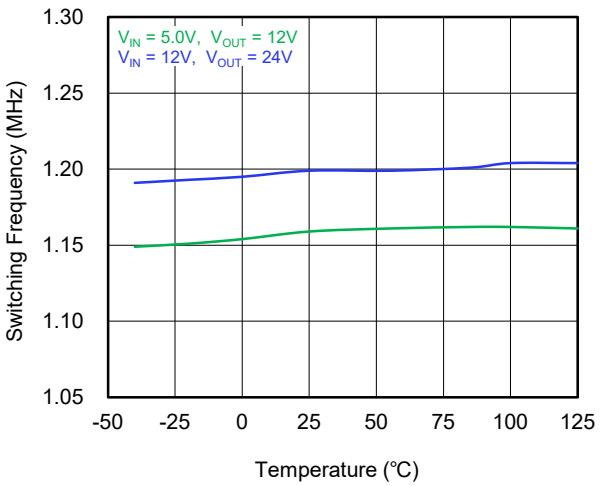
Quiescent Current into VOUT vs. Temperature



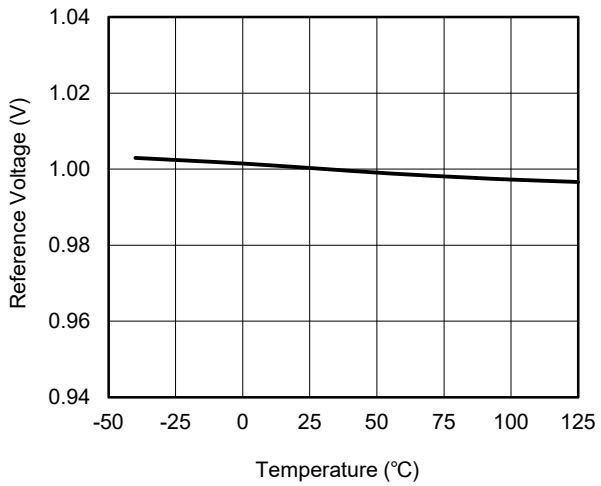
Shutdown Current vs. Temperature



Switching Frequency vs. Temperature



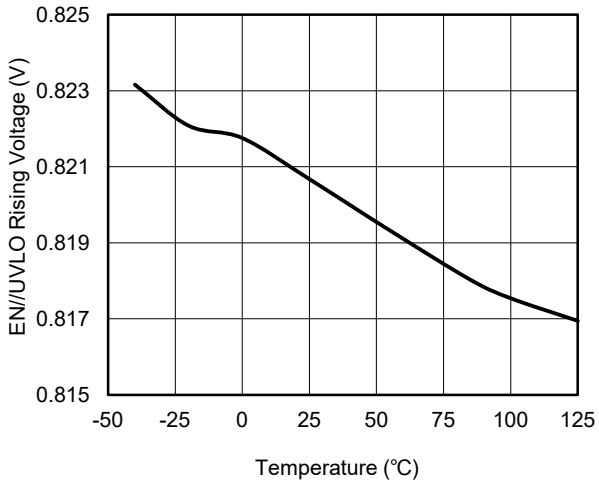
Reference Voltage vs. Temperature



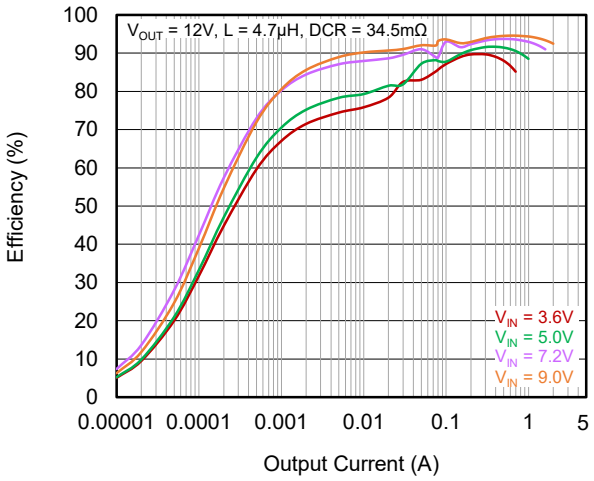
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f_{SW}= 1.2MHz, unless otherwise noted.

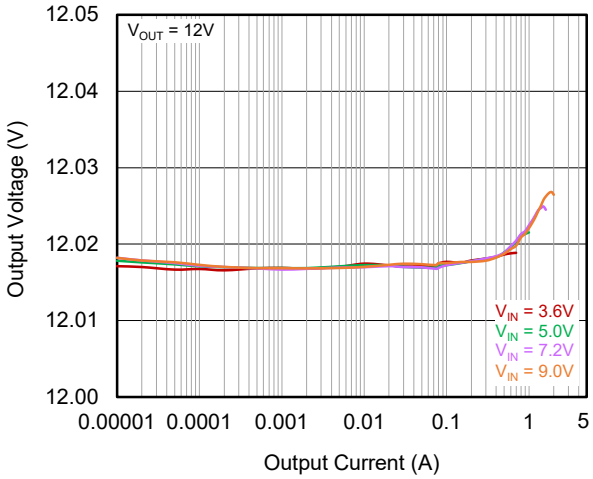
EN/UVLO Rising Voltage vs. Temperature



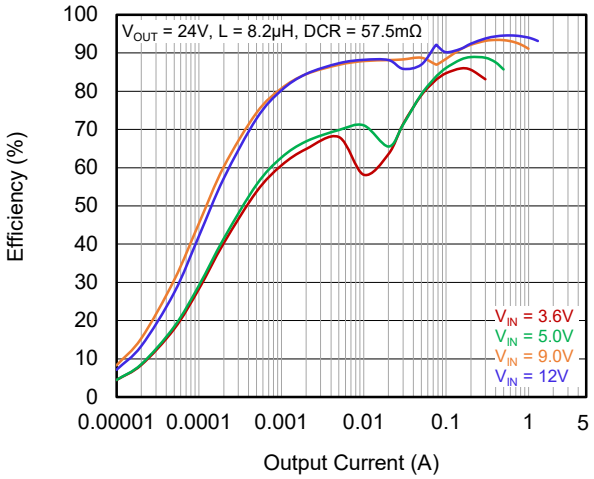
Efficiency vs. Output Current



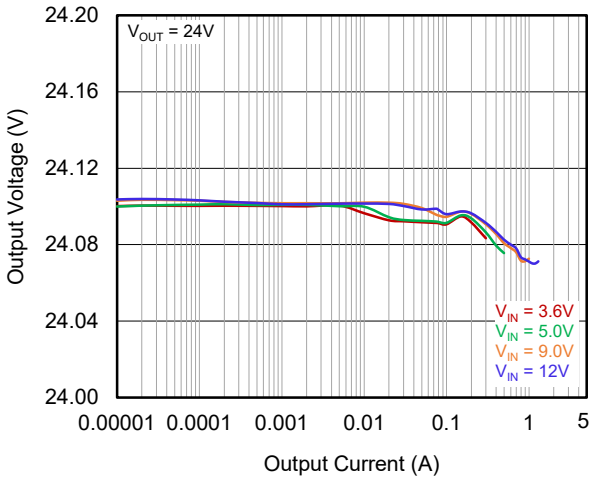
Output Voltage vs. Output Current



Efficiency vs. Output Current



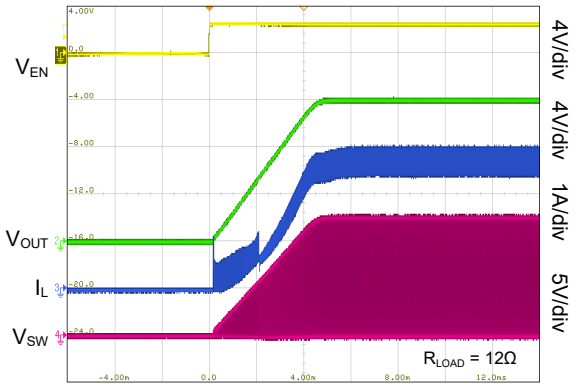
Output Voltage vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

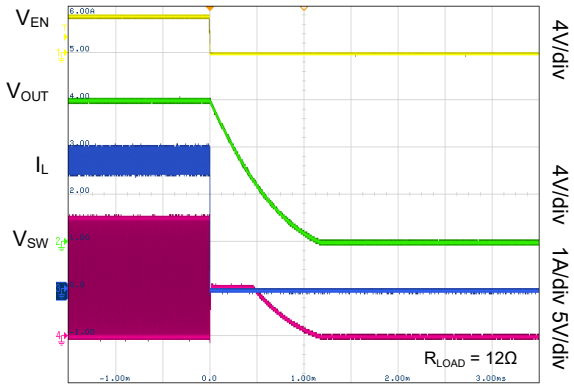
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 12V, C_{OUT} = 67μF, I_{CL} = 3.0A, f_{SW}= 1.2MHz, unless otherwise noted.

Start-up



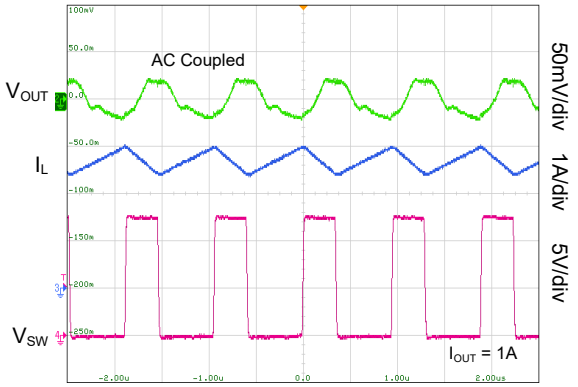
Time (2ms/div)

Shutdown



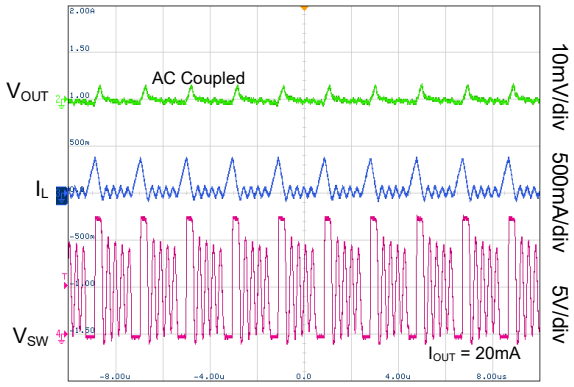
Time (500μs/div)

Switching Waveforms in CCM



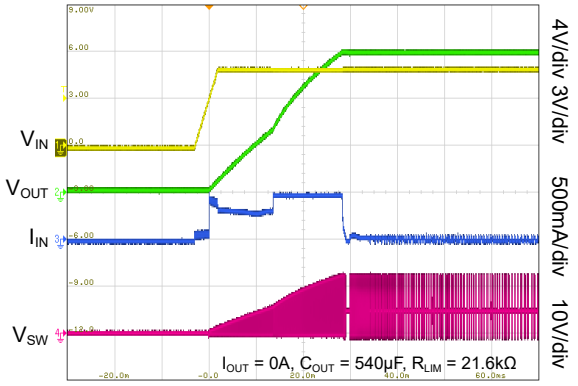
Time (500ns/div)

Switching Waveforms



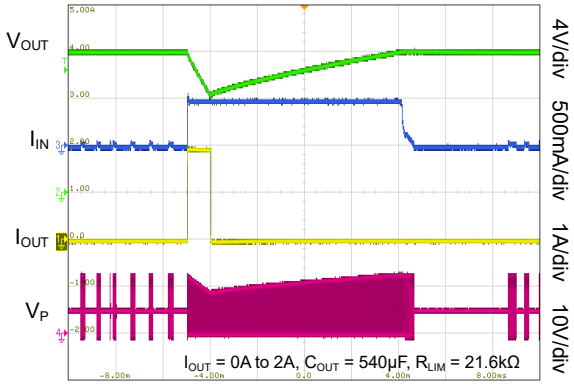
Time (2μs/div)

Start-up with I_{CL} 500mA



Time (10ms/div)

2A Load Pulse with I_{CL} 500mA

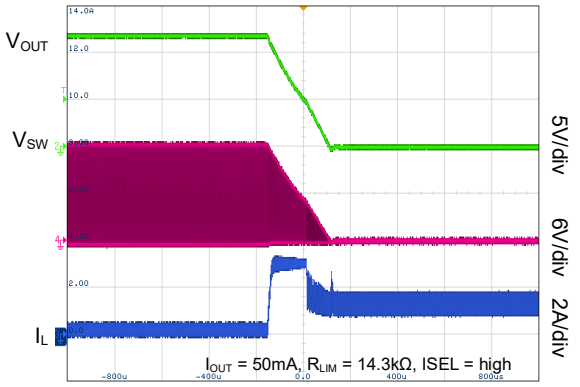


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

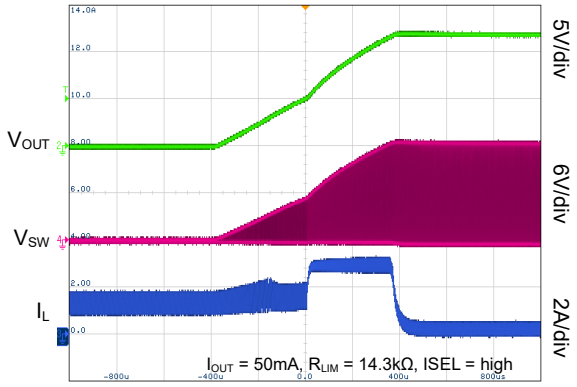
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 12V, C_{OUT} = 67μF, I_{CL} = 3.0A, f_{SW}= 1.2MHz, unless otherwise noted.

Short-Circuit Protection



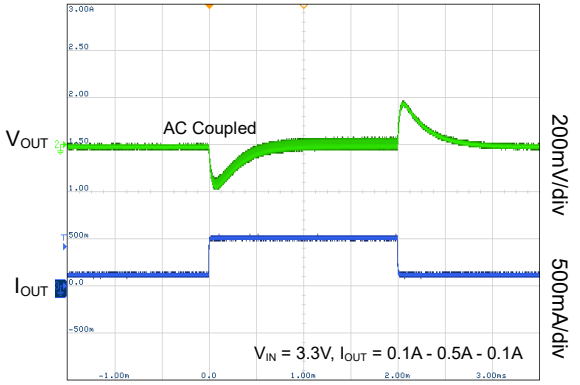
Time (200μs/div)

Short-Circuit Recovery



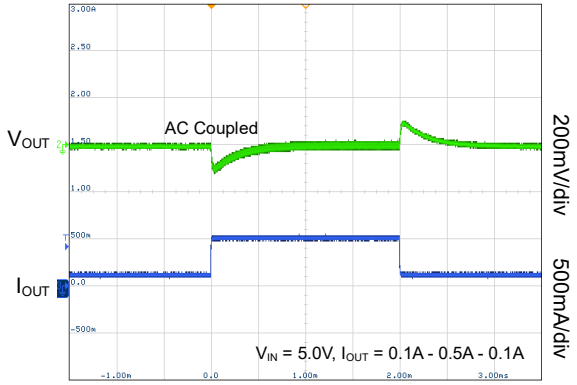
Time (200μs/div)

Load Transient



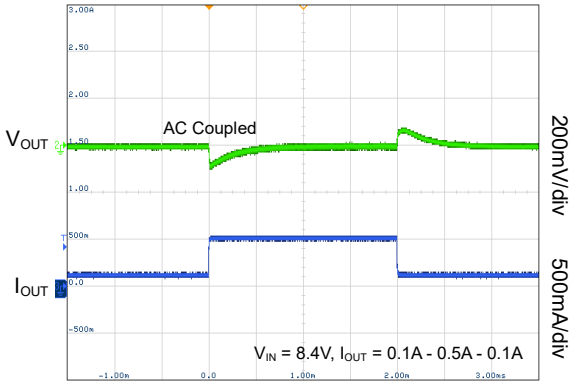
Time (500μs/div)

Load Transient



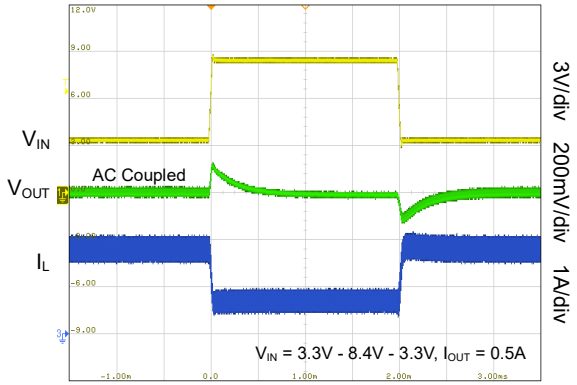
Time (500μs/div)

Load Transient



Time (500μs/div)

Line Transient



Time (500μs/div)

FUNCTION BLOCK DIAGRAM

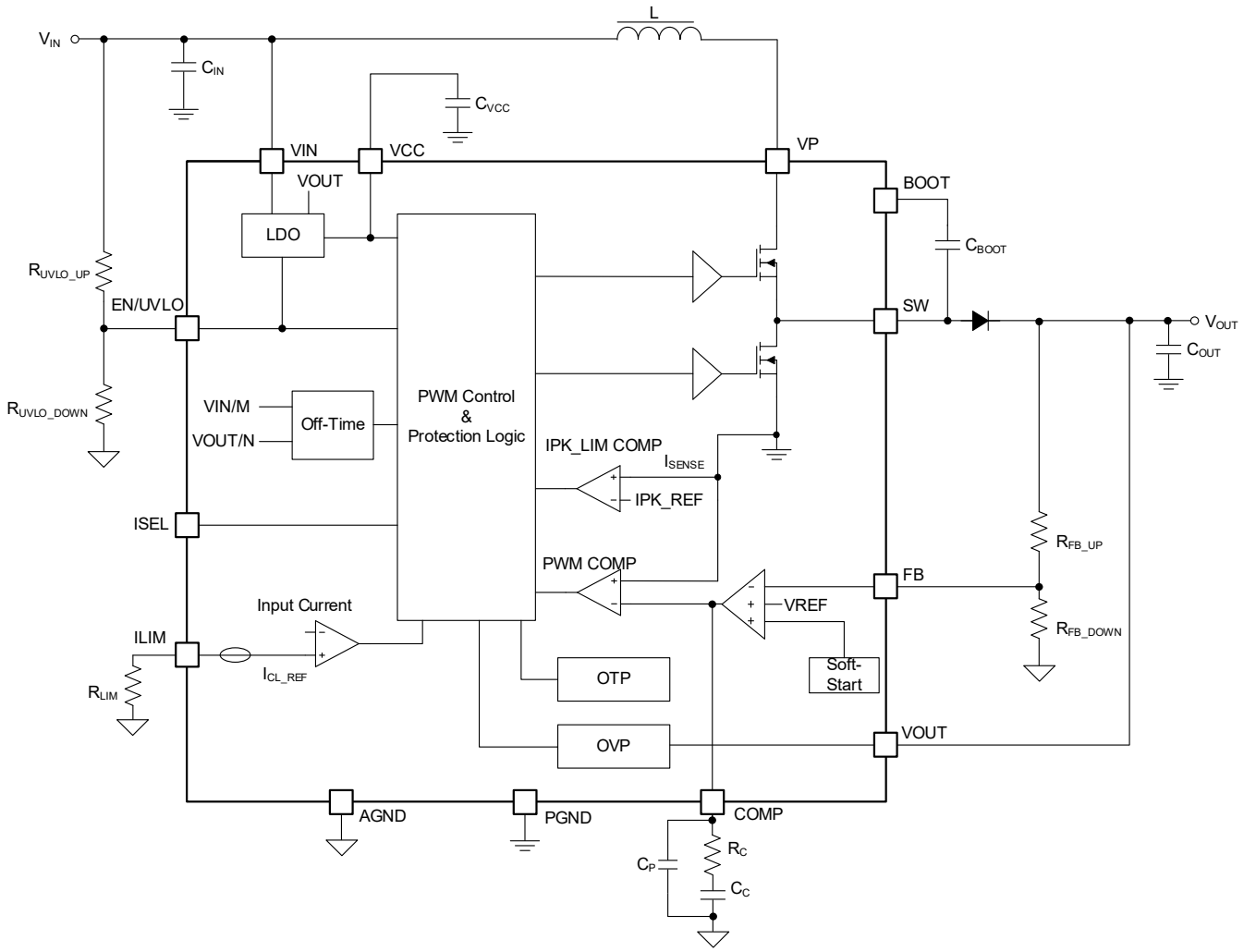


Figure 2. Function Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6617 is a high-voltage non-synchronous Boost converter with a wide input voltage range from 2.9V to 23V while delivering adjustable output voltages between 4.5V and 25V. The device also has the input average current limit and true load disconnect functions. The input average current limit can be programmed from 0.1A to 3A by adjusting the external resistor connected to the ILIM pin. The integrated isolation FET between the VP and SW pins ensures complete input-output disconnection when the device is disabled. The SGM6617 utilizes the constant off-time peak current control topology to achieve enhanced dynamic performance. When the ISEL pin is logic high, the peak switching current limit is 4.5A (TYP). When the ISEL pin is logic low, the peak switching current limit will change to 2.5A (TYP). The device operates in PWM mode under heavy load conditions and automatically switches to PFM mode at light load, maintaining high conversion efficiency across the entire load range.

The SGM6617 implements various protection features, such as output over-voltage protection (OVP), cycle-by-cycle over-current protection (OCP), short-circuit protection and thermal shutdown to improve device robustness.

Feature Description

VCC Power Supply

The internal LDO of SGM6617 generates a regulated 4.9V output with a 10mA current capability. When the VIN pin voltage is below 5.25V, the LDO is powered from the VOUT pin. When V_{IN} exceeds 5.5V, it switches to the VIN pin for power. A ceramic capacitor of at least 1μF effective must be connected between the VCC and AGND pins to stabilize and decouple the VCC voltage. A capacitor with an X7R or X5R dielectric and a voltage rating of 10V or higher is recommended.

Enable and Programmable UVLO

The SGM6617 features a combined enable and under-voltage lockout (UVLO) circuit. The device is enabled and begins switching when the VIN voltage exceeds its UVLO rising threshold of 2.8V (TYP) and the EN/UVLO pin is pulled above its own rising threshold. The EN/UVLO pin incorporates an accurate internal voltage reference and sources a hysteresis current (I_{UVLO_HYS}) to implement a programmable input UVLO with hysteresis, thereby preventing on/off chattering from input noise.

By using resistor divider as shown in Figure 3, the turn-on threshold can be calculated by using Equation 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where, V_{UVLO} is the UVLO threshold of 0.813V (TYP) at the EN/UVLO pin.

The hysteresis voltage is determined by the value of the upper resistor (R_1) in the EN/UVLO divider, thus setting the difference between the turn-on and turn-off thresholds, as given by Equation 2.

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R_1 \quad (2)$$

where, I_{UVLO_HYS} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}.

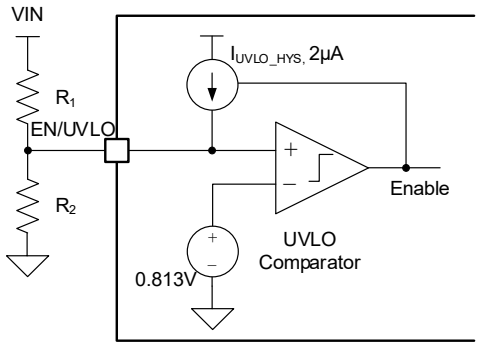


Figure 3. Programmable UVLO with Resistor Divider at EN/UVLO Pin

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DETAILED DESCRIPTION (continued)

Soft-Start and Inrush Current Control during Start-up

The SGM6617 incorporates soft-start and input average current limit functions to prevent excessive inrush current during start-up. When the EN pin is pulled high, the SGM6617 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to the reference voltage within 4ms (TYP). During the initial start-up phase when V_{IN} is higher than V_{OUT}, the current through the inductor is limited by the internal ISO MOSFET under a dual constraint: it is modulated by the down mode, increasing linearly with the decreasing VIN-to-VOUT differential, while simultaneously being limited by the ILIM pin's average current limit. Once V_{OUT} > V_{IN} × 1.05 + 0.2V (TYP), the converter transitions to standard boost operation, where the input current regulation is determined exclusively by the ILIM pin setting.

Switching Frequency

The SGM6617 regulates the output voltage using an adaptive constant off-time peak current control topology. It operates in pulse width modulation (PWM) mode at moderate to heavy loads, with a quasi-constant switching frequency of 1.2MHz (TYP). Under light-load conditions, the SGM6617 automatically enters a power-save mode that employs pulse frequency modulation (PFM) to maintain high efficiency.

Adjustable Input Average Current Limit

The SGM6617 features an integrated input average current limit function. The average current limit is configured via a resistor from the ILIM pin to AGND and can be programmed from 0.1A to 3A. For input average current limit settings below 750mA, setting the ISEL pin to logic low is recommended. This action increases the ISO MOSFET's on-resistance to enhance current accuracy and simultaneously reduces the peak switching current limit from 4.5A (TYP) to 2.5A (TYP).

The relationship between the input average current limit and the resistor is shown in Equation 3 and Equation 4.

$$I_{LIM} = \frac{43.2k\Omega}{R_{LIM}} \quad \text{with ISEL pin logic high} \qquad (3)$$

$$I_{LIM} = \frac{10.8k\Omega}{R_{LIM}} \quad \text{with ISEL pin logic low} \qquad (4)$$

where, R_{LIM} is the resistance between the ILIM pin and the AGND pin. I_{LIM} is the input average current limit.

For instance, the input average current limit is 3A if the R_{LIM} is 14.4kΩ with ISEL pin logic high. The ILIM pin cannot be left floating or connected to VCC.

Shutdown and Load Disconnect

When the input voltage falls below the UVLO threshold or the EN pin is pulled low, the SGM6617 enters shutdown mode, disabling all internal functions. The SGM6617 integrates a load disconnect function; when disabled, the internal ISO MOSFET between the VP and SW pins completely cuts off the path between input and output.

Over-Voltage Protection

The SGM6617 provides an output over-voltage protection (OVP). When the voltage at the VOUT pin is detected above 27V (TYP), the device immediately stops switching to prevent output over-voltage and protect downstream circuits. Switching remains disabled until V_{OUT} falls below the OVP threshold by the hysteresis value.

Output Short Protection

The SGM6617 includes output short-circuit protection. If the output voltage falls below V_{IN} × 1.05 + 0.2V (TYP), or even to ground during a fault condition, the device enters down mode. In this mode, the VP pin is regulated to approximately 2.5V above V_{IN}. This voltage differential across the inductor allows its current to ramp down, while limiting at a relatively low level to protect the device from damage. Normal operation automatically resumes once the short is removed and V_{OUT} rises above the V_{IN} × 1.05 + 0.2V (TYP) threshold.

Thermal Shutdown

A thermal shutdown circuit is provided to prevent damage from excessive heat and power dissipation. The protection is typically triggered at a junction temperature of 150℃ (TYP), which stops the device from switching. It recovers automatically and resumes operation once the junction temperature falls below 130℃ (TYP).

DETAILED DESCRIPTION (continued)

Device Functional Modes

PWM Mode

The SGM6617 operates in quasi-constant frequency pulse-width modulation (PWM) under moderate to heavy loads until the input average current limit is triggered. For each cycle, a circuit predicts the required off-time based on the VIN-to-VOUT ratio. The cycle begins by turning on the low-side N-MOSFET switch (as shown in Figure 2), and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. Once this peak current is detected by the current comparator, the low-side N-MOSFET switch is turned off. The inductor current then commutates to the Schottky diode and ramps down, as V_{OUT} is higher than V_{IN}. Until the calculated off-time is reached, the low-side switch turns on again and the switching cycle is repeated.

Auto PFM Mode

The SGM6617 seamlessly transits between PWM and PFM operation via its smooth on/off-time and automatic pulse-skipping modes, achieving high efficiency across a wide load range. As the load current decreases or V_{IN} increases, the output of the internal error amplifier drops, thereby reducing the inductor peak current and the power delivered to the load. Once this error amplifier output falls to a level corresponding to a peak current of approximately 330mA, the peak current is clamped at this threshold and stops decreasing. To further regulate the output voltage, the SGM6617 then extends the switching off-time, thereby reducing the energy per cycle delivered to the output.

In addition, the output voltage ripple is also small at light load due to low peak current. Refer to Figure 4.

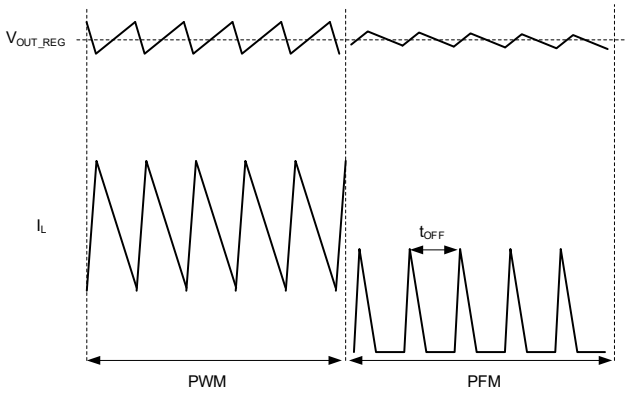


Figure 4. Auto PFM Mode Diagram

APPLICATION INFORMATION

The SGM6617 is a Boost converter supporting output voltages up to 25V and input average current limits up to 3A. It features quasi-constant frequency PWM operation for medium/heavy loads and high-efficiency PFM mode for light loads. The adaptive constant off-time peak current control architecture ensures excellent line and load transient response with minimal output capacitance. The SGM6617 also offers design flexibility, allowing the use of various inductor and output capacitor combinations through external compensation.

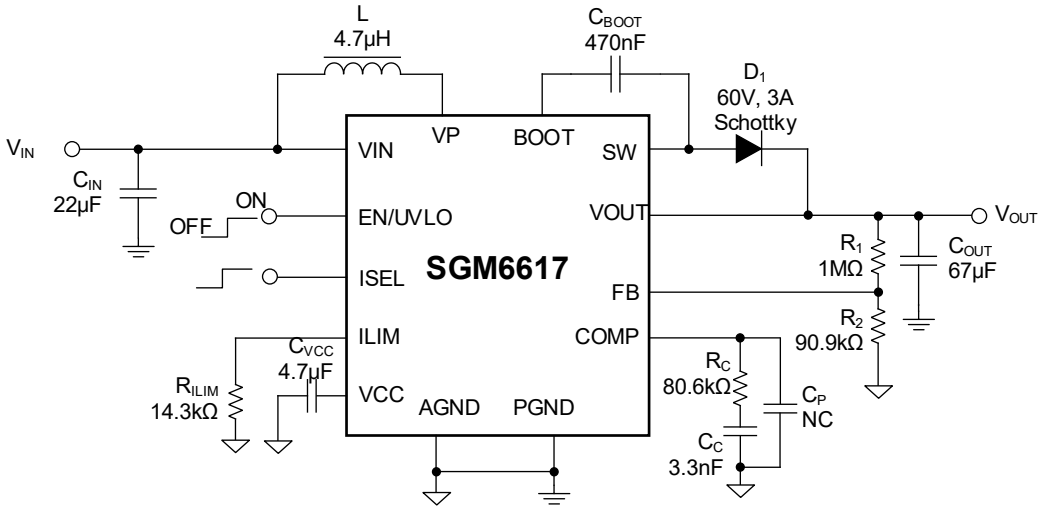


Figure 5. SGM6617 Typical Application Circuit

Design Requirements

Table 1. Design Parameters

Design Parameters	Example Values
Input Voltage Range	3.3V to 8.4V
Output Voltage	12V
Output Voltage Ripple	100mV Peak-to-Peak
Output Current Rating	0.5A

Detailed Design Procedure

Output Voltage Setting

The output voltage is set by an external resistor divider (R_1, R_2 in the Figure 5 circuit diagram). For optimal accuracy, R_2 should be less than 500kΩ to ensure the divider current is at least 100 times greater than the FB pin leakage current. While a lower value for R_2 improves noise immunity, a higher value reduces the quiescent current, thereby increasing light-load efficiency.

Once R_2 is selected, the value of R_1 can be calculated as:

$$R_1 = \left(\frac{V_{OUT} - V_{REF} \times R_2}{V_{REF}} \right) \quad (5)$$

Inductor Selection

The inductor is the most critical component in a DC/DC switching converter design. Its selection defines the key performance of the converter, including steady-state operation, transient response, loop stability, and overall efficiency. The three most important inductor specifications are inductance value, DC resistance (DCR), and saturation current.

The SGM6617 is designed to operate with inductor values ranging from 2.2μH to 10μH. A 2.2μH inductor offers a size advantage, while a 10μH inductor provides lower current ripple, presenting a size/performance trade-off. Furthermore, if the converter's output current is limited by the internal peak current protection, selecting a higher inductance value within this range can help maximize the output current capability.

Consider both the initial tolerance (±20% to ±30% at 0 A) and the drop in inductance (20% to 35%) that occurs as the current approaches the saturation point. Consequently, the selected inductor must have a rated saturation current that is higher than the converter's peak inductor current in all cases.

APPLICATION INFORMATION (continued)

For maximum output current, it is recommended to limit the inductor peak-to-peak ripple current to less than 40% of the average inductor current. The worst-case condition's peak-to-peak inductor current can be calculated with Equation 6 to 8: minimum V_{IN}, maximum V_{OUT}, and maximum load current.

To ensure sufficient design margin, perform this calculation using the minimum switching frequency, the inductor's minimum value (accounting for -30% tolerance), and a conservative estimate for power conversion efficiency.

In a Boost converter, calculate the inductor DC current as in Equation 6.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where,
• V_{OUT} is the output voltage of the Boost converter.
• I_{OUT} is the output current of the Boost converter.
• V_{IN} is the input voltage of the Boost converter.
• η is the power conversion efficiency.

Calculate the inductor peak-to-peak ripple current as in Equation 7.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (7)$$

where,
• I_{PP} is peak-to-peak ripple current of the inductor.
• L is the inductance.
• f_{SW} is the switching frequency.
• V_{OUT} is the output voltage.
• V_{IN} is the input voltage.

Therefore, the inductor peak current (I_{LPEAK}) can be calculated using Equation 8.

$$I_{LPEAK} = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

With ISEL logic high, the peak switching current limit is 4.5A (TYP); with ISEL logic low, the peak switching current limit is reduced to 2.5A (TYP). Accordingly, the peak inductor current must always remain below the inductor saturation current.

It should be noted that higher current ripple increases both DC and AC losses. For higher efficiency, an inductor with lower DCR is generally recommended. However, this often trades off against a larger component footprint. A list of recommended inductors is provided in the table below.

Table 2. Recommended Inductors

Part Number	L (μH)	DCR TYP (mΩ)	Saturation Current (A)	Size (L × W × H mm)	Vendor
74438367022	2.2	16.1	10.2	5.4×5.4×3.1	WURTH
74438367047	4.7	34.5	6.5	5.4×5.4×3.1	WURTH
74438367082	8.2	57.5	6.6	5.4×5.4×3.1	WURTH
7443321000	10	16.7	11.3	12.1×11.4×9.5	WURTH

Bootstrap Capacitor Selection

The bootstrap capacitor (connected between BOOT and SW) provides the gate drive current for the ISO MOFFET during the turn-on of each cycle. Therefore, a low-ESR ceramic capacitor with a value between 0.47μF and 1μF is recommended. It must be placed close to the device pins to minimize potentially damaging voltage transients caused by trace inductance. For this design example, a 0.47μF capacitor is used.

Input Capacitor Selection

Multilayer ceramic capacitors (MLCCs) are excellent choice for input decoupling due to their very low ESR and compact size. They must be placed as close as possible to the device. While a 22μF capacitor is typically sufficient, a larger value can be used to further reduce input current ripple.

When using only ceramic capacitors at the input with a power source connected via long leads (e.g., a wall adapter), a load step can cause ringing at the VIN pin due to interaction with the lead inductance. This ringing may couple to the output and could be misinterpreted as loop instability or potentially damage the device. To suppress this ringing, place additional bulk capacitance (electrolytic/tantalum) between the power source leads and the local ceramic input capacitor (C_{IN}).

APPLICATION INFORMATION (continued)

Output Capacitor Selection

The output capacitor is selected to meet both steady-state and load-transient requirements, with its value influencing the compensation design. The output voltage ripple is primarily determined by the capacitor's Equivalent Series Resistance (ESR) and its capacitance. For a theoretical capacitor with zero ESR, the minimum required capacitance for a target ripple can be calculated using Equation 9.

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (9)$$

where,

• C_{OUT} is the output capacitor.
• I_{OUT} is the output current.
• V_{OUT} is the output voltage.
• V_{IN} is the input voltage.
• ΔV is the output voltage ripple required.
• f_{SW} is the switching frequency.

The additional output voltage ripple component due to the capacitor's ESR is given by Equation 10:

$$\Delta V_{ESR} = I_{LPEAK} \times R_{ESR} \quad (10)$$

where,

• ΔV_{ESR} is the output voltage ripple caused by ESR.
• R_{ESR} is the equivalent series resistance of the output capacitor.

While the ESR of ceramic capacitors is not negligible, the ESR of tantalum or electrolytic capacitors must be considered in ripple calculations.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 11:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times V_{TRAN}} \quad (11)$$

where,

• ΔI_{STEP} is the transient load current step.
• ΔV_{TRAN} is the allowed voltage dip for the load current step.
• f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero).

The DC bias derating characteristic of ceramic capacitors must be carefully considered in design. Capacitance can decrease by as much as 70% at its rated voltage. Therefore, enough margins on the voltage rating must be considered to guarantee that sufficient capacitance is maintained at the actual output voltage.

Diode Selection

A Schottky diode is recommended for D1 primarily due to its low forward voltage and fast recovery characteristics. Key selection parameters include low reverse leakage current, a voltage rating exceeding the maximum output voltage plus switching-node overshoot, and a current rating sufficient for the average output current.

Loop Stability

The SGM6617 features external compensation for customizable loop optimization. The COMP pin serves as the output of the internal error amplifier. An external compensation network - comprising resistor R_C and ceramic capacitors (C_C and C_P), is connected to this pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by Equation 12.

$$G_{PS}(S) = K_{COMP} \times \frac{R_O \times (1-D)}{2} \times \frac{\left(1 + \frac{S}{2\pi f_{ESRZ}}\right) \times \left(1 - \frac{S}{2\pi f_{RHPZ}}\right)}{1 + \frac{S}{2\pi f_P}} \quad (12)$$

where,

• D is the switching duty cycle.
• R_O is the output load resistance.
• K_{COMP} is power stage trans-conductance (inductor peak current/comp voltage), which is 5.77A/V.

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (13)$$

where, C_O is effective output capacitance.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (14)$$

APPLICATION INFORMATION (continued)

where, R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (15)$$

The COMP pin is the output of the internal transconductance amplifier. Equation 16 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1+\frac{S}{2\pi f_{COMZ}}\right)}{\left(1+\frac{S}{2\pi f_{COMP1}}\right) \times \left(1+\frac{S}{2\pi f_{COMP2}}\right)} \quad (16)$$

where,

• G_{EA} is the transconductance of the amplifier, which is 250μS (TYP).

• R_{EA} is the output resistance of the amplifier, which is 16MΩ.

• V_{REF} is the reference voltage at the FB pin.

• V_{OUT} is the output voltage.

• f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.

• f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. A higher crossover frequency generally yields a faster transient response. As a general guideline, f_C should not exceed the lower of either one-tenth of the switching frequency (f_{SW}/10) or one-fifth of the right-half-plane zero frequency (f_{RHPZ}/5).

Then set the value of R_C, C_C, and C_P (in Figure 5) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1-D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (17)$$

where, f_C is the selected crossover frequency.

The value of C_C can be calculated by Equation 18.

$$C_C = \frac{R_O \times C_O}{2R_C} \quad (18)$$

The value of C_P can be calculated by Equation 19.

$$C_P = \frac{R_{ESR} \times C_O}{R_C} \quad (19)$$

If the calculated value of C_P is less than 10pF, it can be left open.

Designing the control loop for a phase margin greater than 45° and a gain margin greater than 10dB ensures the stable operation by preventing output voltage ringing during line and load transients.

APPLICATION INFORMATION (continued)

Layout Guidelines

PCB layout is vital for stability and noise performance, especially in high-frequency, high-current designs like this switching power supplies. Consequently, to maximize efficiency, the switch node rise and fall times are minimized, which requires careful management of the high-frequency switching path to prevent unwanted radiation (for example, EMI). Therefore, minimize the length and area of all SW pin traces and employ a ground plane beneath the regulator to reduce inter-plane coupling.

Place the input capacitor as close as possible to the VIN and PGND pins to minimize input supply ripple. Additionally, keep all high-current power paths, including SW, D1, the output capacitor and PGND, as short and wide as possible to reduce parasitic inductance.

Thermal management must be carefully considered in the layout due to the SGM6617's high power density. To enhance thermal performance, connect the high-current pins (VP, SW, VOUT, and PGND) to large copper polygons. Additionally, placing thermal vias underneath the SW pin to further improve heat dissipation.

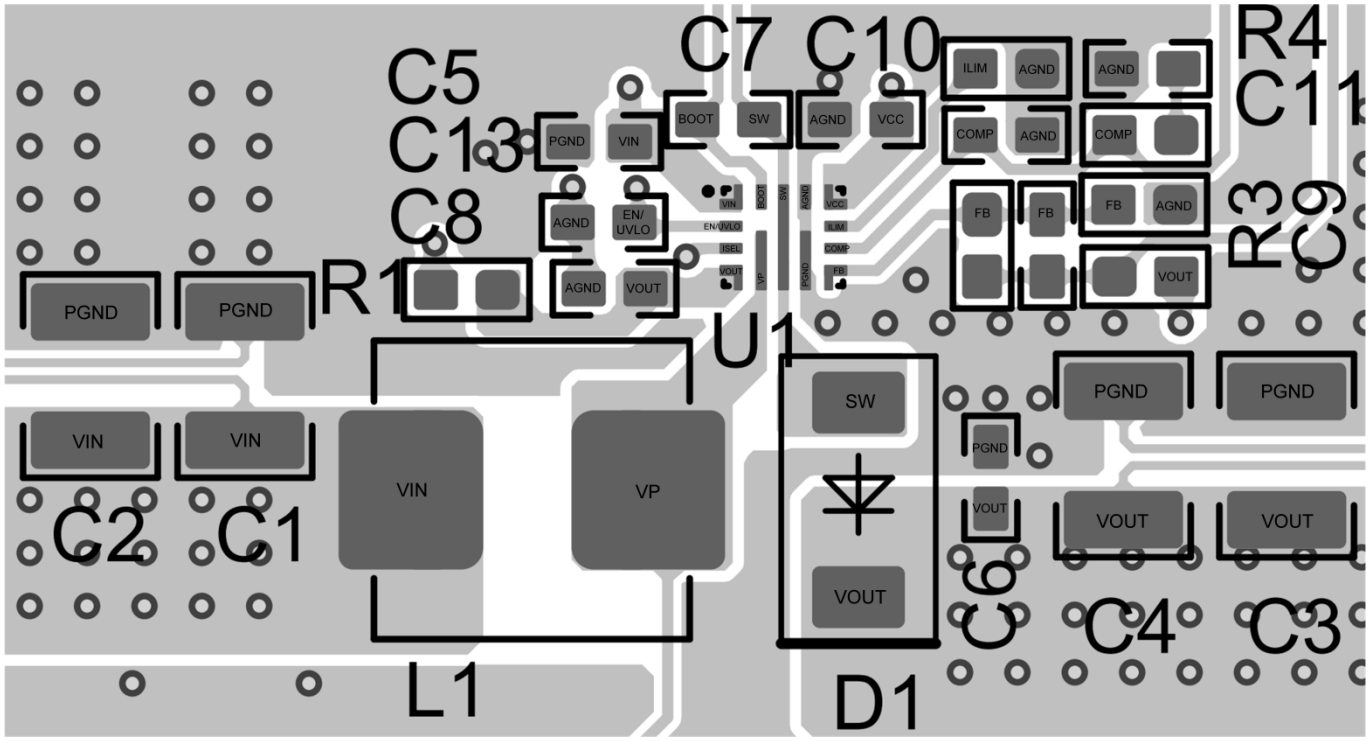


Figure 6. Layout Example

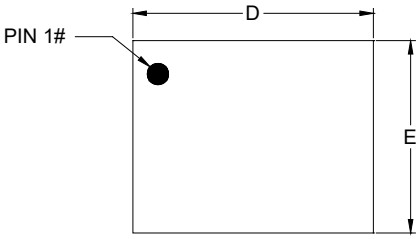
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

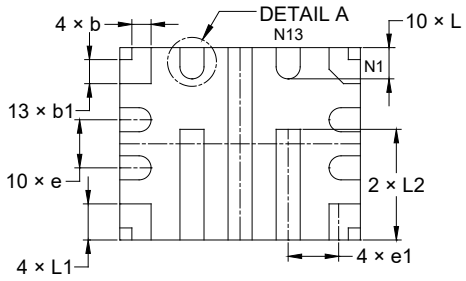
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

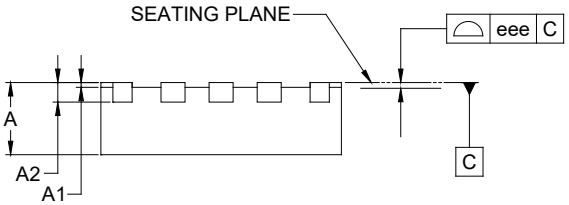
TQFN-2.5×2-13L



TOP VIEW



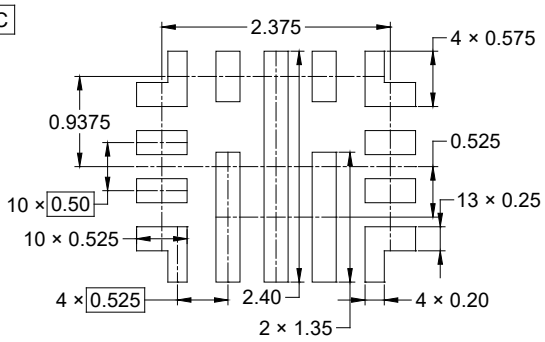
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



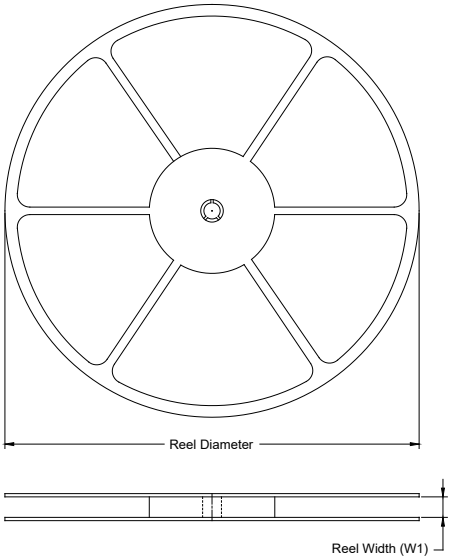
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
b1	0.200	-	0.300
D	2.400	-	2.600
E	1.900	-	2.100
e		0.500 BSC	
e1		0.525 BSC	
L	0.225	-	0.425
L1	0.275	-	0.475
L2	1.050	-	1.250
eee		0.080	

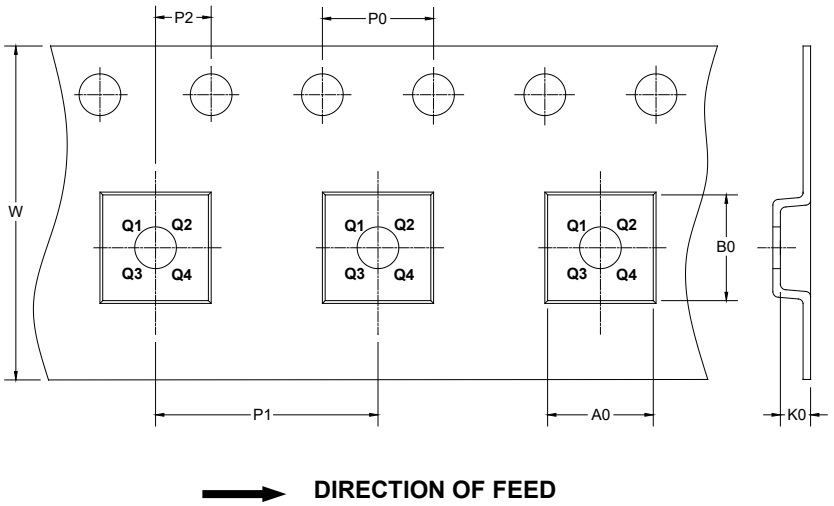
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



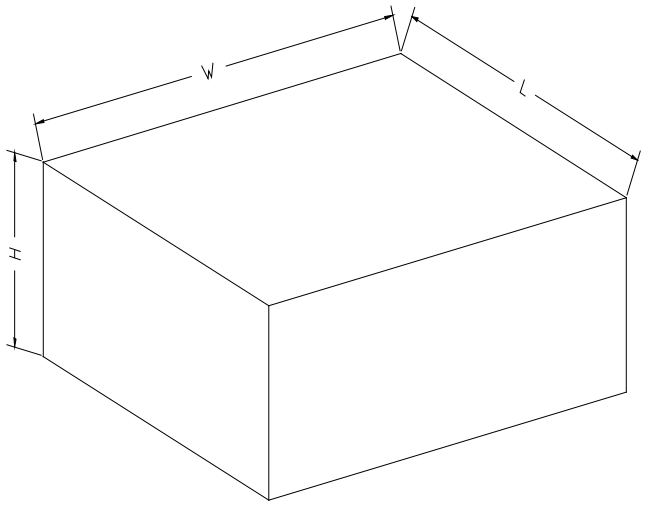
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.5×2-13L	7"	9.5	2.25	2.80	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002