

GENERAL DESCRIPTION

The SGM48218 is a half-bridge E-mode GaN HEMT driver with 1.7A peak source and 5.2A peak sink output current capability. High-side and low-side drivers are controlled independently by their own inputs.

The high-side power supply of the SGM48218 is powered by a bootstrap charging method with an integrated bootstrap switch, and supports a maximum operating voltage up to 100V. To prevent the bootstrap capacitor voltage from exceeding the maximum gate-source voltage rating of the E-mode GaN HEMT, smart charging technology is used to ensure that the high-side supply voltage does not exceed V_{CC} .

The SGM48218 high-side and low-side all adopt split outputs architecture. The split outputs allow separate adjustment of turn-on and turn-off speed for GaN HEMT by configuring the respective turn-on and turn-off resistors.

The SGM48218 supports operation at several MHz.

The SGM48218 is available in Green TQFN-3×3-14L and WLCSP-1.65×1.65-12B packages.

FEATURES

- TTL Logic Threshold Inputs
- Maximum Blocking Voltage: 100V DC
- Split Outputs Allow for Adjusting of Turn-On and Turn-Off Speed of GaN HEMT
- Smart Internal Bootstrap Charging for High-side Power Supply
- Operating VCC Voltage Range: 4.5V to 6.0V
- 1.7A Peak Source Current and 5.2A Peak Sink Current
- Fast Propagation Time: 18ns (TYP)
- Delay Matching: 1.5ns (TYP)
- -40°C to +125°C Operating Ambient Temperature Range
- Available in Green TQFN-3×3-14L and WLCSP-1.65×1.65-12B Packages

APPLICATIONS

Power Converters in 48V or Lower Systems Used in Telecom, Datacom, Portable Storage, etc.

Half-Bridge, Full-Bridge, Push-Pull, Synchronous Buck and Forward Converters

Synchronous Rectifiers

Class-D Audio Amplifiers

SIMPLIFIED SCHEMATIC

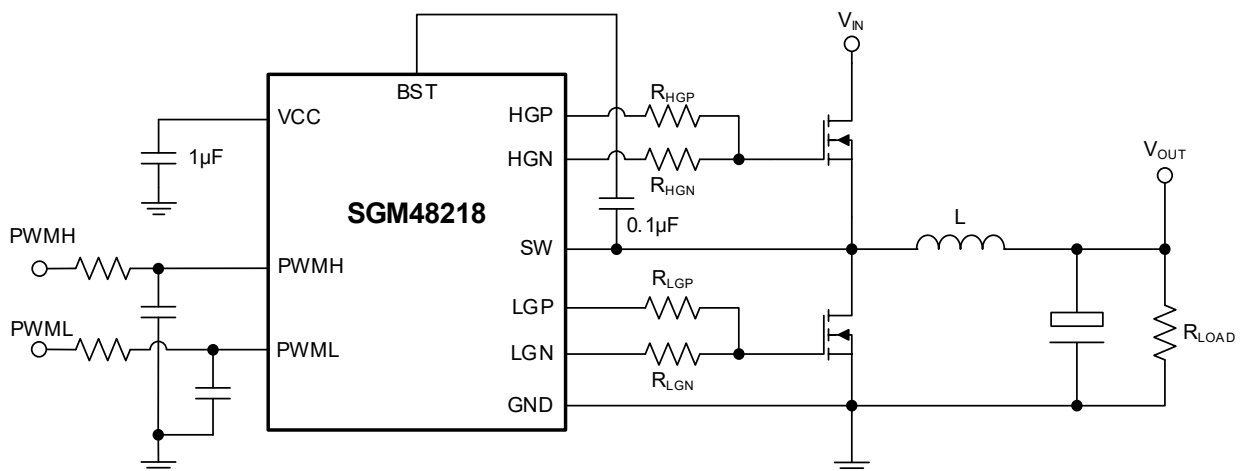


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

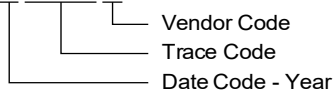
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48218	TQFN-3×3-14L	-40°C to +125°C	SGM48218XTXV14G/TR	48218 TXV14 XXXXX	Tape and Reel, 4000
	WLCSP-1.65×1.65-12B	-40°C to +125°C	SGM48218XG/TR	48218 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

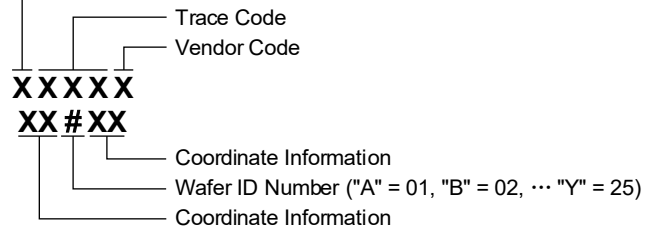
TQFN-3×3-14L

XXXXX



WLCSP-1.65×1.65-12B

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}

DC -0.3V to 7.0V
20ns 7.5V

 V_{BST_SW}

DC -0.3V to 7.0V
20ns 7.5V

 V_{SW}

DC -5V to 105V
20ns -10V to 110V

SW Slew Rate 50V/ns

V_{BST} -0.3V to 110V
20ns 118V

 V_{HGP}, V_{HGN} SW - 0.3V to $V_{BST} + 0.3V$ 20ns SW - 3V to $V_{BST} + 2V$ V_{LGP}, V_{LGN} -0.3V to $V_{CC} + 0.3V$ 20ns -3V to $V_{CC} + 2V$

PWMH, PWML, OVD -0.3V to 7.0V

Package Thermal Resistance

TQFN-3×3-14L, θ_{JA} 59.1°C/WTQFN-3×3-14L, θ_{JB} 8.5°C/WTQFN-3×3-14L, θ_{JC} 43.8°C/WWLCSP-1.65×1.65-12B, θ_{JA} 102.6°C/WWLCSP-1.65×1.65-12B, θ_{JB} 22.9°C/WWLCSP-1.65×1.65-12B, θ_{JC} 24.6°C/W

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10s) +260°C

ESD Susceptibility ^{(1) (2)}

HBM ±2000V

CDM ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} 4.5V to 6.0V

PWMH, PWML 0V to 5.0V

OVD 0V to V_{CC}

SW -3.5V to 100V

BST 1V to 105V

Operating Ambient Temperature Range -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

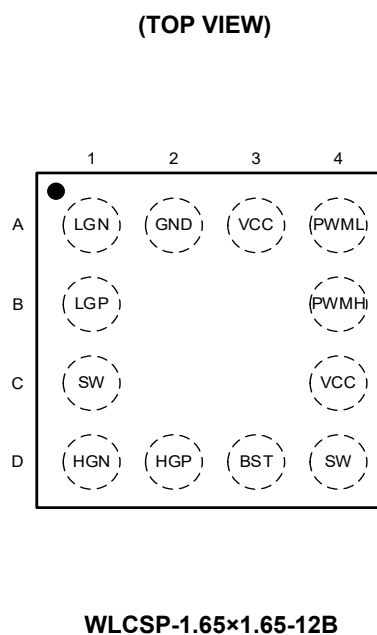
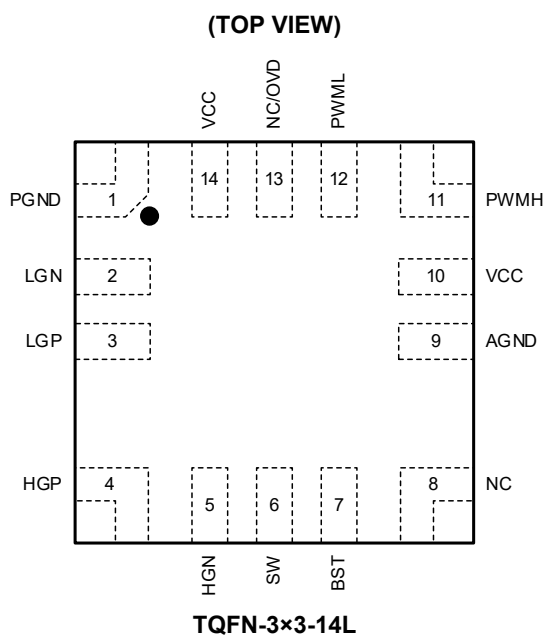
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		NAME	FUNCTION
TQFN-3×3-14L	WLCSP-1.65×1.65-12B		
1	—	PGND	Power Ground.
2	A1	LGN	Sink Current Output of Low-side. Connect a resistor to the gate of the low-side GaN HEMT to adjust the turn-off speed.
3	B1	LGP	Source Current Output of Low-side. Connect a resistor to the gate of the low-side GaN HEMT to adjust the turn-on speed.
4	D2	HGP	Source Current Output of High-side. Connect a resistor to the gate of the high-side GaN HEMT to adjust the turn-on speed.
5	D1	HGN	Sink Current Output of High-side. Connect a resistor to the gate of the high-side GaN HEMT to adjust the turn-off speed.
6	C1, D4	SW	Reference Ground of the High-side Output Stage.
7	D3	BST	High-side Bootstrap Supply. A bootstrap capacitor is required to connect between BST and SW pins. The capacitor value varies with the total gate charge of external GaN HEMT, the switching speed, as well as the voltage ripple criteria.
8	—	NC	No Connection.
9	—	AGND	Signal Ground.
10, 14	A3, C4	VCC	Power Supply. A decoupling capacitor is connected between VCC and GND pins.
11	B4	PWMH	Input of High-side Driver.
12	A4	PWML	Input of Low-side Driver.
13	—	NC/OVD	The VCC over-voltage detection pin for open-drain output needs to be pulled up to VCC through a resistor when in use. If not used, it can be left floating.
—	A2	GND	Reference Ground.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V$, $PGND = AGND = 0V$, typical values are measured at $T_J = +25^\circ C$, minimum and maximum values are measured at $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply						
VCC Quiescent Current	I_Q	PWMH = PWML = 0		100	170	μA
VCC Operation Current	I_{CC}	$f = 500kHz$, $C_{LOAD} = 0$		2	4	mA
VCC Under-Voltage Lockout Threshold	V_{CC_VTH}	V_{CC} rising	3.6	4	4.4	V
VCC Under-Voltage Lockout Threshold Hysteresis	V_{CC_HYS}			300		mV
VCC UVLO Blank Time	t_{BLANK}			40		μs
VCC Over-Voltage Detection Threshold	V_{OVD_VTH}	V_{CC} rising		6.6		V
VCC Over-Voltage Detection Threshold Hysteresis	V_{OVD_HYS}			300		mV
VCC Over-Voltage Detection Delay Time	t_{DELAY_OVD}			5		μs
PWM Inputs (PWMH, PWML)						
PWM Logic High Voltage	V_{H_PWM}			2.07	2.35	V
PWM Logic Low Voltage	V_{L_PWM}			360		mV
PWM Threshold Hysteresis	V_{HYS_PWM}		1.45	1.71		V
PWM Input Pull-Down Resistance	R_{PWM_IN}		100	200	300	k Ω
High-side Driver Supply						
V_{BST_SW} Under-Voltage Lockout Threshold	V_{BST_VTH}	BST rising	3.1	3.6	4.1	V
V_{BST_SW} Under-Voltage Lockout Threshold Hysteresis	V_{BST_HYS}			350		mV
Bootstrap Function						
VCC-BST Dynamic Resistance	R_{BST_RES}	$I_{VCC_BST} = 100mA$	1	3	5.2	Ω
High- and Low-side Gate Driver (HGP, HGN, LGP, LGN)						
Peak Source Current	I_{SOURCE}			1.7		A
Peak Sink Current	I_{SINK}			5.2		A
Source Resistance	R_{SOURCE}	$I_{SOURCE} = 100mA$		1.1	2	Ω
Sink Resistance	R_{SINK}	$I_{SINK} = 100mA$		0.22	0.5	Ω
High- and Low-side Gate Driver Timing Characteristics						
HGP Rise Time (0.5V - 4.5V) ⁽¹⁾	t_{R_HS}	1nF load		4.5		ns
HGN Fall Time (4.5V - 0V) ⁽¹⁾	t_{F_HS}	1nF load		2.5		ns
LGP Rise Time (0.5V - 4.5V) ⁽¹⁾	t_{R_LS}	1nF load		4.5		ns
LGN Fall Time (4.5V - 0.5V) ⁽¹⁾	t_{F_LS}	1nF load		2.5		ns
HGP Turn-On Propagation Delay	t_{HPH}	1nF load, PWMH rising to HGP rising		18	30	ns
HGN Turn-Off Propagation Delay	t_{HPL}	1nF load, PWMH falling to HGN falling		18	30	ns
LGP Turn-On Propagation Delay	t_{LPH}	1nF load, PWML rising to LGP rising		18	30	ns
LGN Turn-Off Propagation Delay	t_{LPL}	1nF load, PWML falling to LGN falling		18	30	ns
LGP On & HGN Off Delay Matching	t_{OFF_M}			1.5	6	ns
LGN Off & HGP On Delay Matching	t_{ON_M}			1.5	6	ns
Minimal Input PWM Pulse ⁽¹⁾	t_{PWM_MIN}			5		ns
Minimal Gate Output Pulse ⁽¹⁾	t_{GATE_MIN}			5		ns
Thermal Protection						
Thermal Shutdown ⁽¹⁾	T_{SD}			171		$^\circ C$
Thermal Shutdown Hysteresis ⁽¹⁾	T_{SD_HYS}			21		$^\circ C$

NOTE: 1. Specified by design and characterization, not production tested.

TIMING DIAGRAM

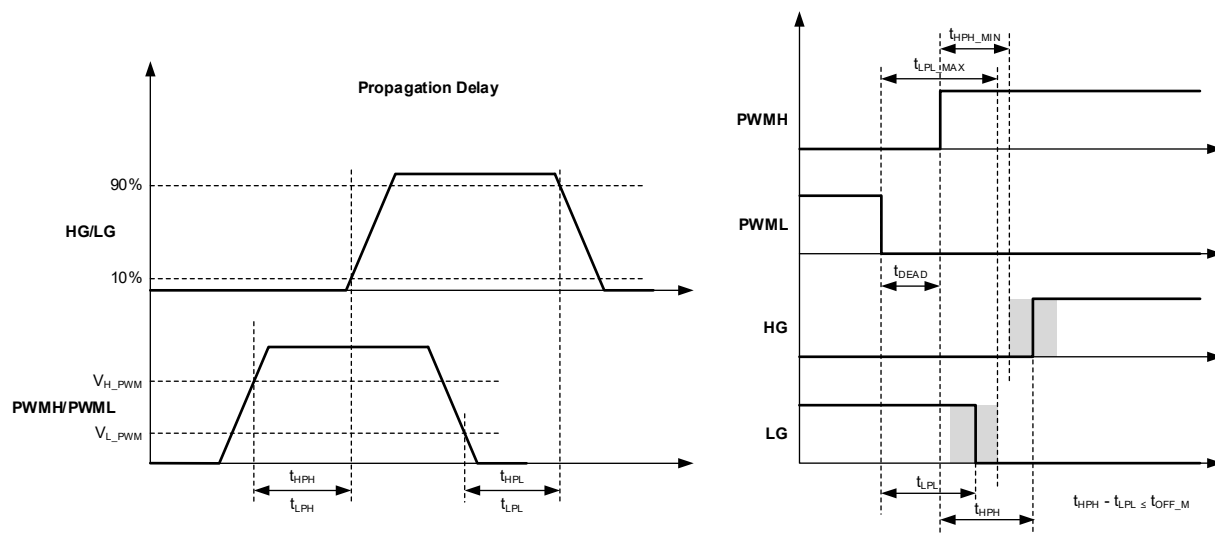


Figure 2. Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

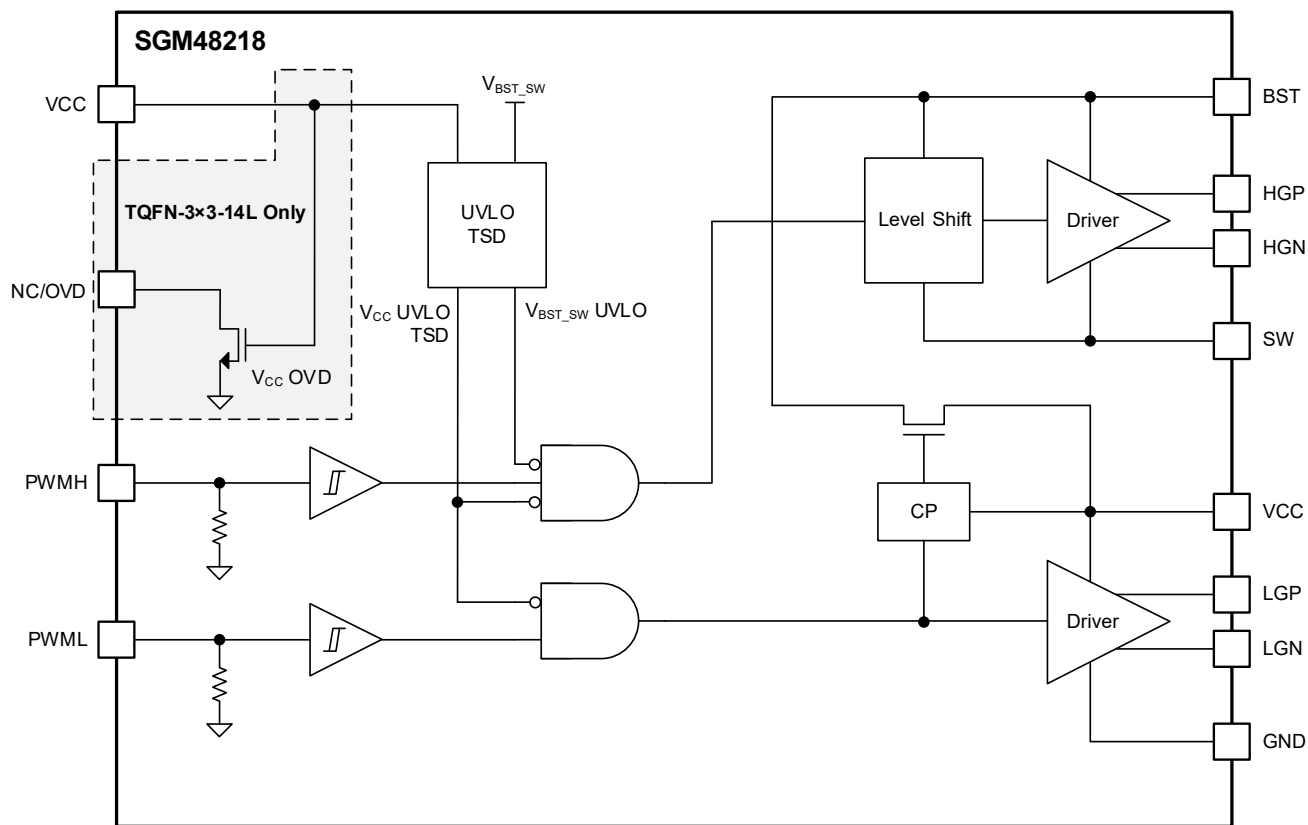
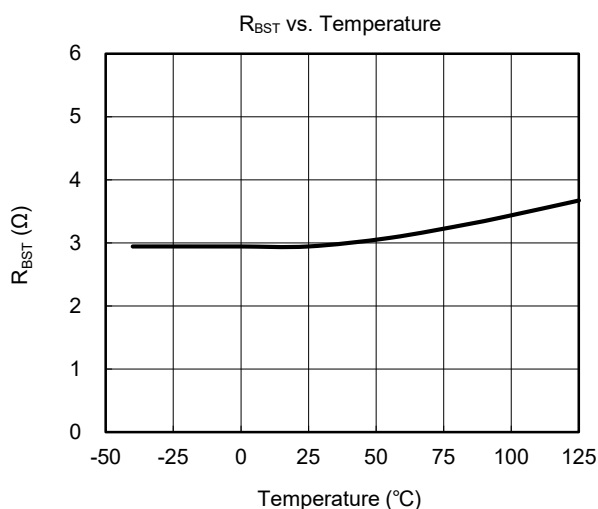
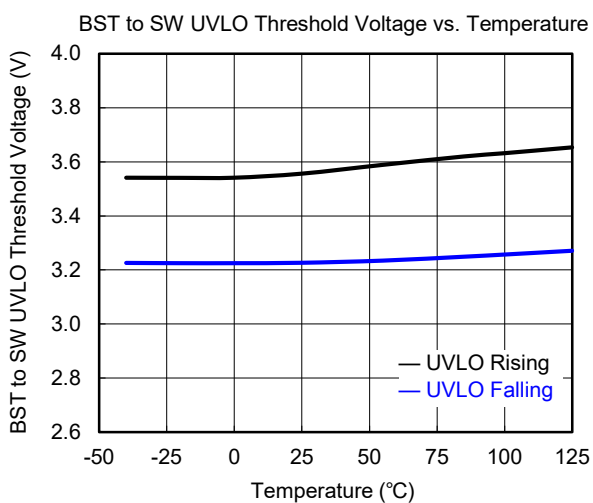
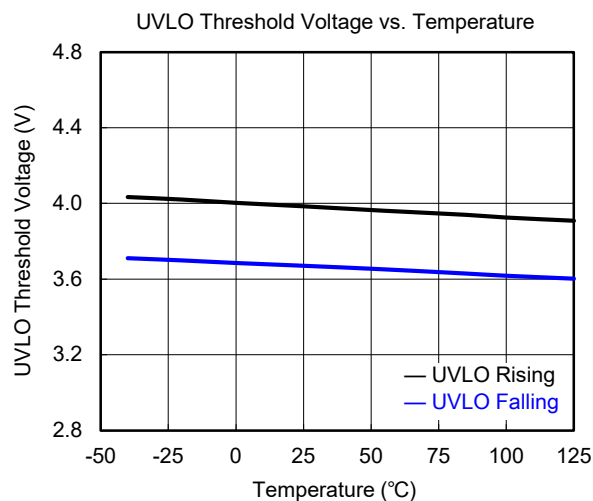
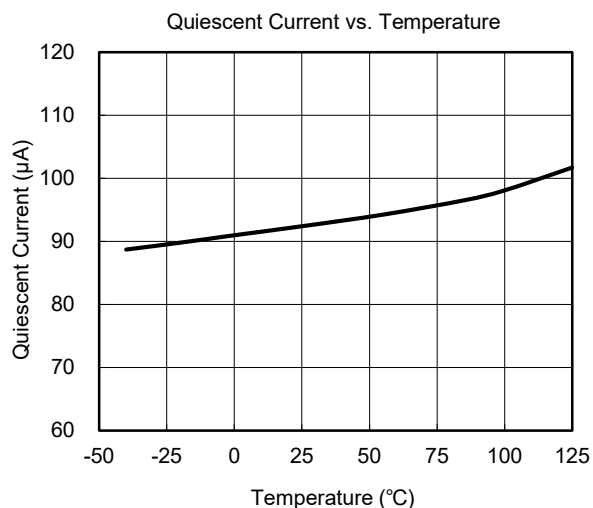
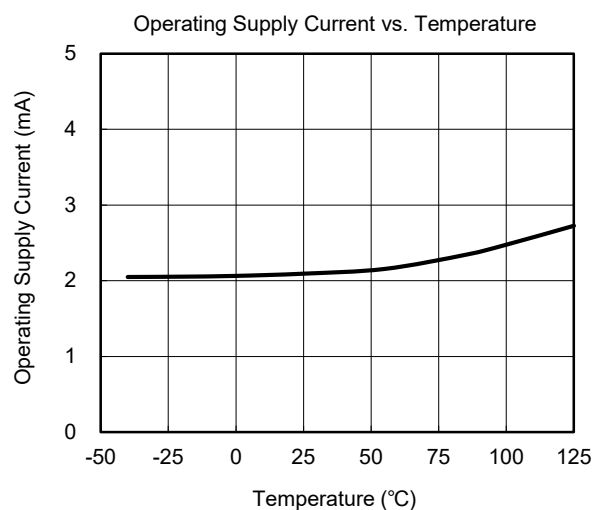
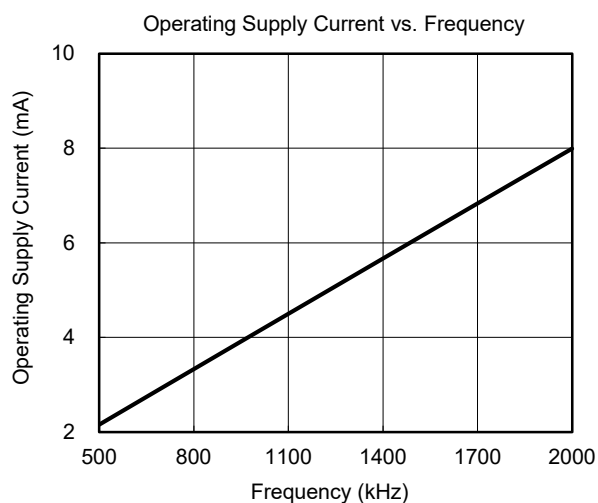
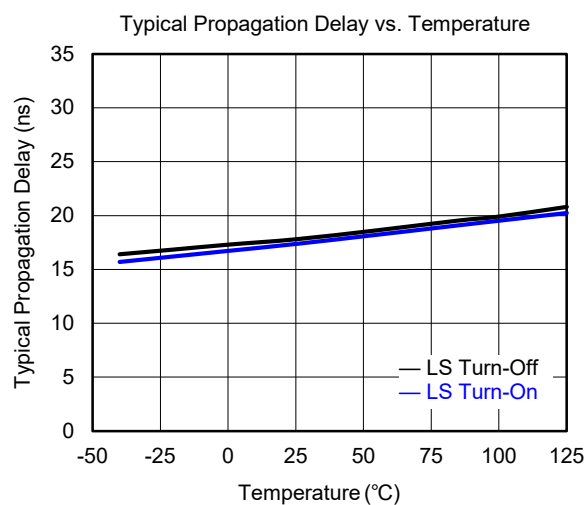
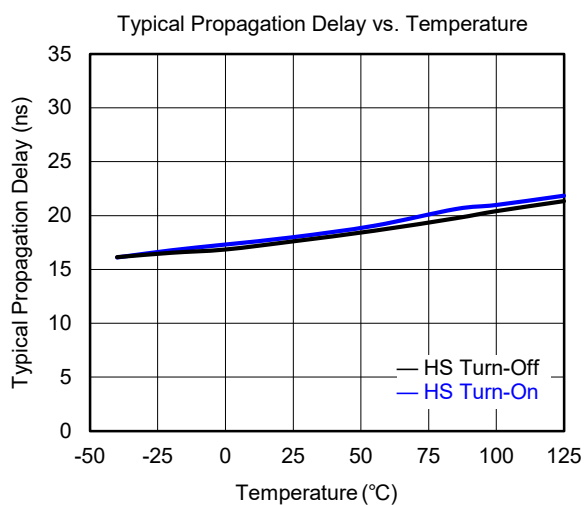


Figure 3. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $T_A = +25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued) $V_{CC} = 5V$, $T_A = +25^\circ C$, unless otherwise noted.

DETAILED DESCRIPTION

Table 1. HG and LG True Table

PWMH	PWML	HGP	HGN	LGP	LGN
High	Low	High	Open	Open	Low
Low	High	Open	Low	High	Open
High	High	High	Open	High	Open
Low	Low	Open	Low	Open	Low

Operation

The SGM48218 is designed to drive enhancement-mode (E-Mode) GaN HEMTs in half-bridge configurations and supports systems with a DC 100V bus. Its integrated active bootstrap charging circuit prevents the bootstrap capacitor voltage from exceeding V_{CC} , ensuring that the gate-to-source voltage for the high-side GaN HEMT does not surpass its maximum ratings.

UVLO Protection

The SGM48218 features under-voltage lockout (UVLO) protection for both the high-side and low-side power supplies. If the $V_{CC} < V_{CC_VTH} - V_{CC_HYS}$, the outputs of both the high-side and low-side are disabled. If the $V_{BST} < V_{BST_VTH} - V_{BST_HYS}$, only the high-side output is disabled. Once both the V_{CC} and BST voltages are above their respective thresholds, the driver outputs normally. Please refer to Table 2 for details.

PWM Input and Output

The PWMH and PWML logic input signals can be controlled independently. When PWMH and PWML are used to drive the high-side and low-side GaN HEMTs in the same bridge circuit respectively, sufficient dead time must be incorporated between PWMH and PWML to avoid conduction overlap. An individual low-pass RC filter is strongly recommended and should be placed closely to PWMH/PWML pin.

Once V_{CC} powers up and the low-side GaN HEMT is turned on, the bootstrap capacitor voltage begins to be charged to V_{CC} . Additionally, for the high-side channel, after both V_{CC} and $BST-SW$ have exceeded their respective UVLO thresholds, normal switching operation begins only after the first PWMH completes its transition from low to high. This ensures that the pulse width of the first output cycle exactly matches the signal pulse width.

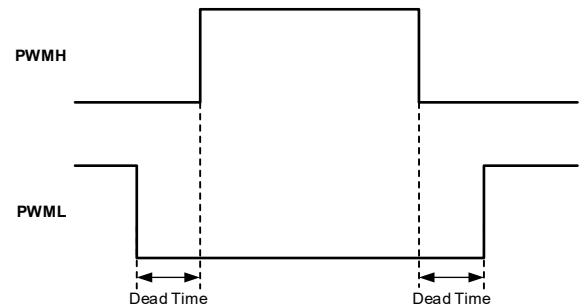


Figure 4. Dead Time Timing

If unused, the PWMH and PWML pins can be left floating, or connected to GND for better noise immunity.

Split outputs of SGM48218 means that it is flexible to adjust the turn-on and turn-off speed by using individual resistors between xGP/xGN and gate of GaN HEMTs. The output has $0.24\Omega/1\Omega$ internal pull-down/pull-up resistance. 0.24Ω pull-down resistance is used to prevent the gate-source voltage of GaN HEMT from exceeding the threshold voltage during high dV/dt case.

OVD Function

For the SGM48218 TQFN-3×3-14L package, pin 13 is the drain of an open-drain MOSFET and provides a V_{CC} over-voltage detection function. If this function is not used, the pin can be left floating or connected to ground. If this function is used, pin 13 must be connected to V_{CC} or an external DC supply through a pull-up resistor (e.g., $10k\Omega$). When V_{CC} exceeds V_{CC_VTH} , the open-drain MOSFET turns on after approximately $5\mu s$ and pulls this pin low, while the gate driver continues to operate normally without shutting down.

DETAILED DESCRIPTION (continued)**Table 2. V_{CC} and V_{BST_SW} UVLO PWM Distribution Logic**

VCC Condition	V _{BST_SW} Condition	PWMH	PWML	HG	LG
V _{CC} < V _{CC_VTH} during start-up	DNC	1	0	0	0
		0	1	0	0
		1	1	0	0
		0	0	0	0
V _{CC} < V _{CC_VTH} - V _{CC_HYS} after start-up		1	0	0	0
		0	1	0	0
		1	1	0	0
		0	0	0	0
V _{CC} > V _{CC_VTH}	V _{BST_SW} < V _{BST_VTH} during start-up	1	0	0	0
		0	1	0	1
		1	1	0	1
		0	0	0	0
	V _{BST_SW} < V _{BST_VTH} - V _{BST_HYS} after start-up	1	0	0	0
		0	1	0	1
		1	1	0	1
		0	0	0	0

Bootstrap Clamping

Due to the intrinsic characteristics of GaN HEMTs, the source-to-drain voltage of the bottom switch often exceeds a diode's forward voltage drop when its gate is pulled low, resulting in a negative voltage at the SW node. Furthermore, PCB layout and the device's drain/source parasitic inductances can exacerbate this negative voltage transient. In a high-side driver using a floating bootstrap supply, a negative SW voltage can overcharge the bootstrap capacitor, potentially damaging the high-side GaN HEMT.

The SGM48218 incorporates a bootstrap charging circuit that presents very high impedance when PWML = 0, preventing the bootstrap capacitor from being overcharged during dead time.

APPLICATION INFORMATION

Typical Application

The SGM48218 can be used to drive GaN HEMTs configured in a half-bridge for Buck converter, Boost converter or motor driver. Thanks to its internal active bootstrap path, the gate-source voltage of the high-side GaN HEMT can be prevented from exceeding its maximum rating. Split outputs provide the simplest way to fine-tune the turn-on and turn-off speed, and help reduce the area of the drive loop.

Selection of VCC Bypass Capacitor

To make the SGM48218 operate normally and drive GaN HEMTs properly, the VCC bypass capacitor must be sized and its minimum capacitance is given by:

$$C_{VCC} > \frac{Q_{gT} + Q_{gB}}{\Delta V_{CC}} \quad (1)$$

where:

Q_{gT} and Q_{gB} are the gate charge of top and bottom GaN HEMTs respectively.

ΔV_{CC} is the maximum allowable transient voltage drop of VCC.

A 1 μ F or larger X7R ceramic capacitor is recommended and should be placed as close as possible between VCC and AGND/GND pins.

Selection of Bootstrap Capacitor

C_{BST} should be able to provide sufficient gate charge for the top GaN HEMT and keep the bootstrap voltage well above the V_{BST_SW} UVLO threshold, the minimum capacitance can be calculated by:

$$C_{BST} > \frac{Q_{gT} + I_{GSS} \times t_{ON}}{\Delta V_{BST}} \quad (2)$$

where:

Q_{gT} is the gate charge of the top GaN HEMT.

I_{GSS} is the maximum gate leakage current of the top GaN HEMT.

t_{ON} is the maximum on-time period of the top GaN HEMT.

ΔV_{BST} is the maximum allowable transient voltage drop of external C_{BST} .

A 100nF or larger X7R ceramic capacitor is recommended and should be placed as close as possible between the BST and SW pins. When the Q_{gT} of the high-side GaN HEMT and the switching frequency increase, a larger bootstrap capacitor is required to maintain a stable high-side gate drive voltage. The total capacitance of C_{BST} should not exceed 1 μ F.

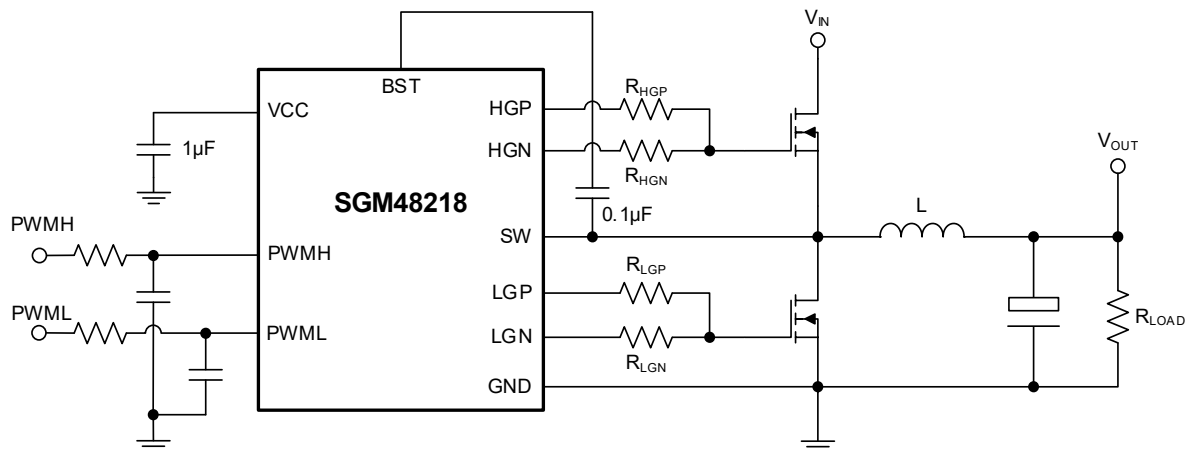


Figure 5. Typical Application Circuit

APPLICATION INFORMATION (continued)

Power Dissipation and Junction Calculation

When driving GaN HEMTs, low-resistance gate resistors are normally used. Most of the total driving power will be consumed by the driver especially when a 0Ω external gate resistor is used.

The total driving power can be roughly calculated by:

$$P_{\text{driver}} = (Q_{\text{gT}} + Q_{\text{gB}}) \times V_{\text{CC}} \times f_{\text{SW}} \quad (3)$$

where:

f_{SW} is the maximum switching frequency of the PWM signal.

Then the maximum junction temperature can be calculated by:

$$T_J = P \times \theta_{JA} \times T_A \quad (4)$$

Power Supply

The SGM48218 is designed to operate with a 4.5V to 6V power bias supplied to VCC. The actual power bias should be chosen according to the maximum V_{GS} of the GaN HEMT to be driven.

UVLO is designed in both the VCC-GND and BST-SW blocks.

Local bypass capacitors should be placed between VCC and AGND/GND pins with the shortest possible trace loop; the same applies to BST and SW pins. It is recommended to place at least one 100μF capacitor in parallel with one 1μF ceramic SMT capacitor as close as possible between the VCC and AGND/GND pins.

A low-temperature coefficient ceramic capacitor, such as X7R, is preferable.

Layout Guidelines

1. The gate driver should be placed as close as possible to the GaN HEMTs. Reducing the area of the drive loops lowers the loop's parasitic inductance, delivers sufficient peak current, and reduces switching noise and ringing.
2. The bootstrap path from BST to the external bottom GaN HEMT should be minimized.
3. Gate resistors or optional ferrite beads can be used to damp the potential ringing caused by LCR resonance of parasitic inductance, gate-source capacitance and resistance of the loop.

4. Low-ESR/ESL capacitors should be selected for the bypass capacitor.

5. A better bus loop will greatly favor to the driving quality of GaN HEMTs. For example, minimize the physical area of top and bottom power loops to lower the negative SW transient voltage during low-side current freewheeling, and place low-ESR/ESL ceramic capacitors adjacent to the GaN HEMTs to decouple excessive ringing on the power bus.

6. For the SGM48218 in the TQFN-3×3-14L package, AGND and PGND are recommended to be connected at a single point through a 0Ω resistor in the PCB layout.

Figure 6 and Figure 7 show the example PCB layout of the gate drive circuit consisting of the SGM48218, gate resistors, the VCC decoupling capacitor, the bootstrap capacitor, and the external GaN HEMTs.

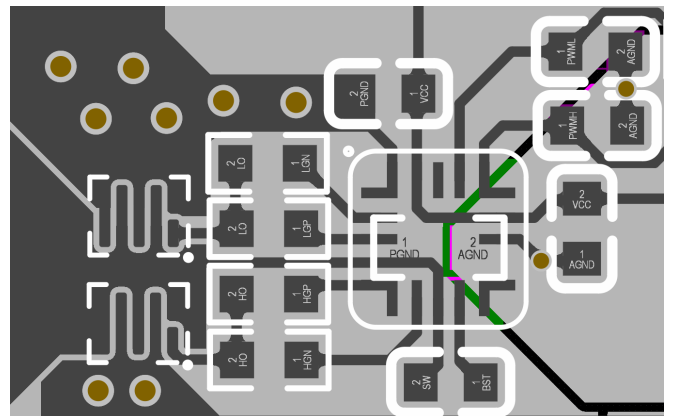


Figure 6. Recommended PCB Layout (TQFN-3×3-14L)

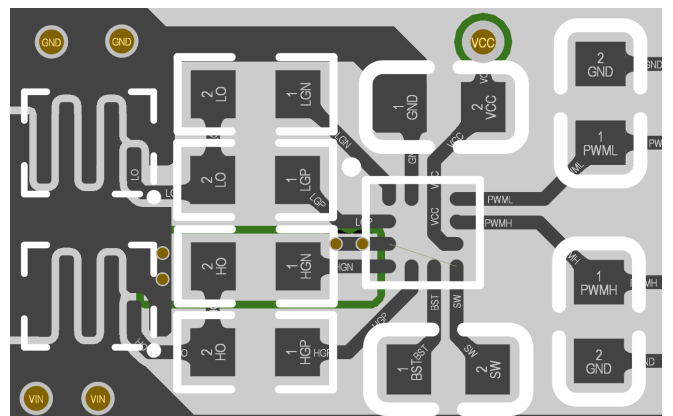


Figure 7. Recommended PCB Layout (WLCSP-1.65×1.65-12B)

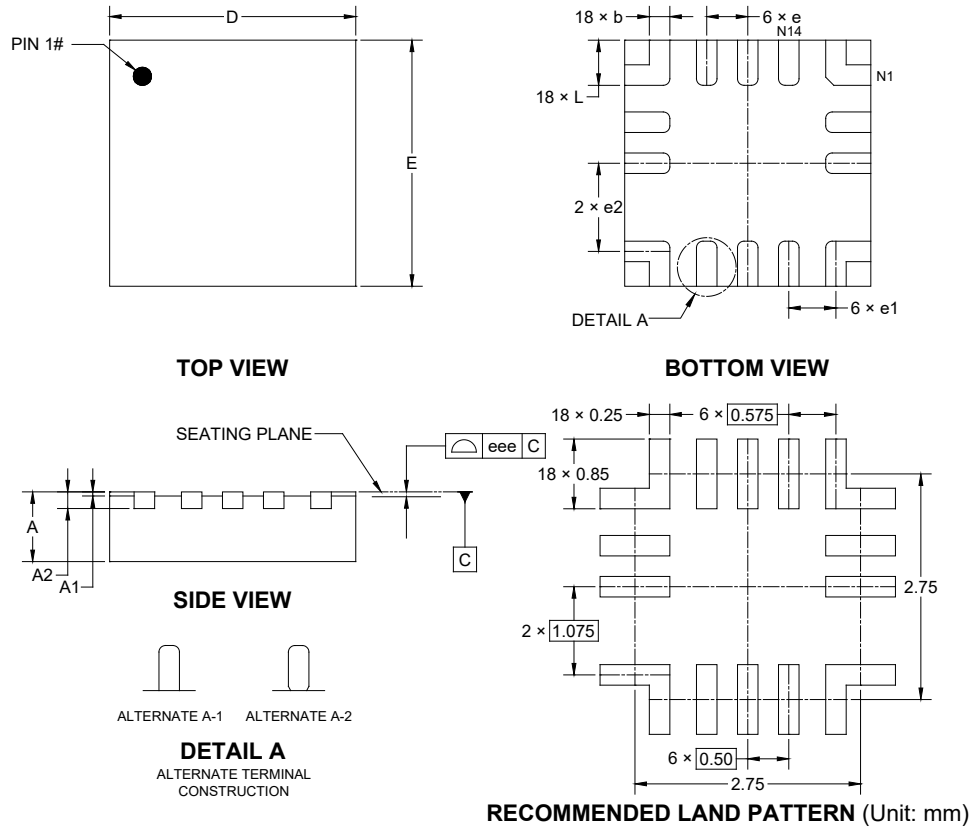
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (SEPTEMBER 2026)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

TQFN-3×3-14L



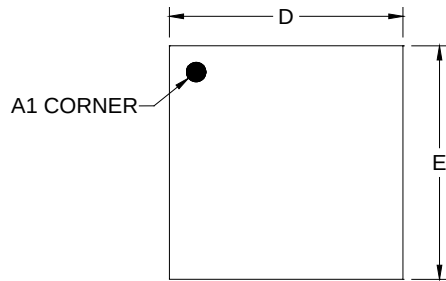
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
e	0.500 BSC		
e1	0.575 BSC		
e2	1.075 BSC		
L	0.450	-	0.650
eee	0.080		

NOTE: This drawing is subject to change without notice.

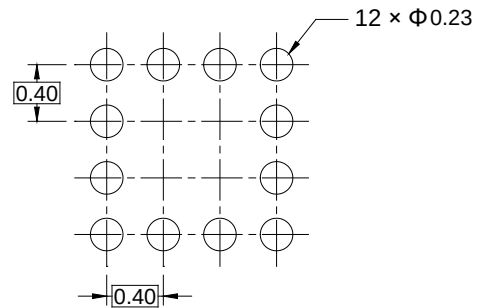
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

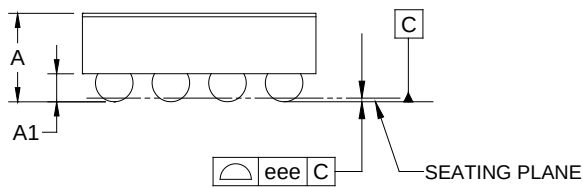
WLCSP-1.65×1.65-12B



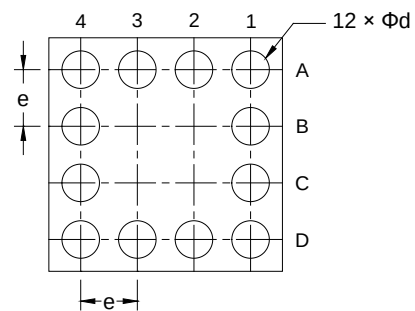
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

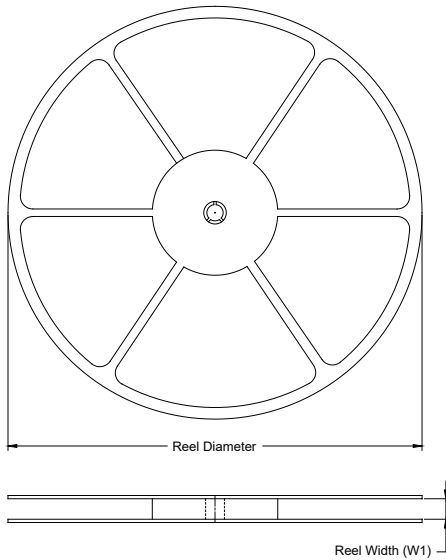
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.675
A1	0.178	-	0.218
D	1.620	-	1.680
E	1.620	-	1.680
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

NOTE: This drawing is subject to change without notice.

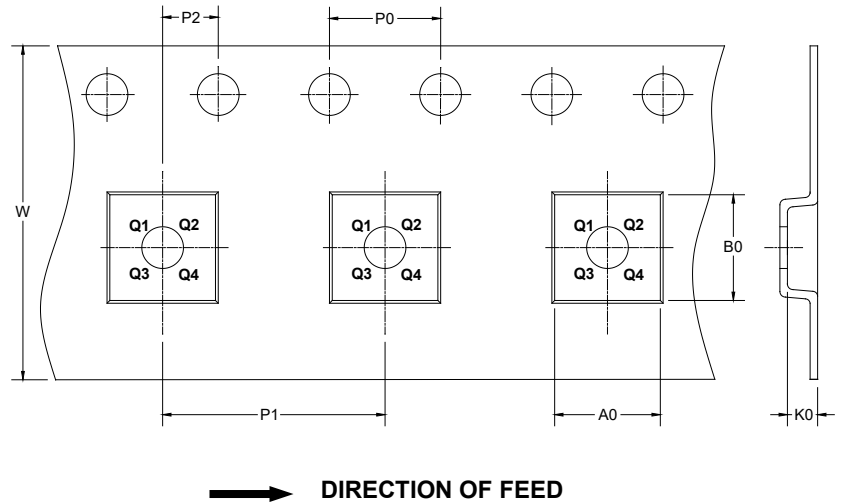
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

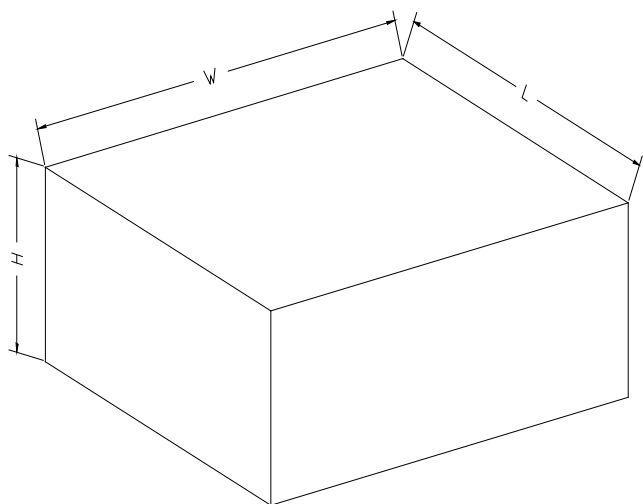
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-14L	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q1
WLCSP-1.65×1.65-12B	7"	9.5	1.80	1.80	0.88	4.0	4.0	2.0	8.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18
13"	386	280	370	5

DD0002