TD93C46/TD93C56/TD93C66/TD93C76/TD93C86
1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit and 16-Kbit (8-bit or 16-bit Wide) Microwire Serial Access EEPROM

GENERAL DESCRIPTION

The TD93C46 (1-Kbit), TD93C56 (2-Kbit), TD93C66 (4-Kbit), TD93C76 (8-Kbit) and TD93C86 (16-Kbit) are Microwire serial access EEPROM (electrically erasable programmable memory) devices. The internal memory array supports dual organization modes: byte (×8 bit) or word (×16 bit).

The TD93Cx6 features a single supply voltage range from 1.7V to 5.5V. All aforementioned components support a maximum operating clock frequency of 3MHz.

The TD93Cx6 is available in Green UTDFN-2×3-8AL, SOIC-8 and TSSOP-8 packages. The TD93Cx6 series operate over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Single Supply Voltage: 1.7V to 5.5V**
- **Industry Standard Microwire Bus**
- **Dual Organization Modes: by Byte (×8 bit) or Word (×16 bit)**
- **Programmable Command Supports for Byte, Word and Full Array-Level Operations**
- **Integrated Self-Timed Programming Cycle with Automatic Erase, Rated at 3ms**
- **Built-in READY/$\overline{\text{BUSY}}$ Status Indicator during Programming Execution**
- **Clock Frequency: 3MHz (MAX)**
- **Sequential Read Operation**
- **Optimized ESD Protection and Latch-up Immunity Performance**
- **More than 1 Million Write Cycles at T_A = +25℃**
- **More than 100-Year Data Retention at T_A = +25℃**
- **Available in Green SOIC-8, UTDFN-2×3-8AL and TSSOP-8 Packages**

Table 1. Memory Size Versus Organization

DEVICE	NUMBER OF BITS	NUMBER OF 8-BIT BYTES	NUMBER OF 16-BIT WORDS
TD93C86	16384	2048	1024
TD93C76	8192	1024	512
TD93C66	4096	512	256
TD93C56	2048	256	128
TD93C46	1024	128	64

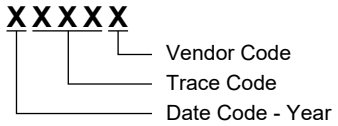
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TD93C46	SOIC-8	-40℃ to +125℃	TD93C46XS8G/TR	TD 93C46XS8 XXXXX	Tape and Reel, 4000
	UTDFN-2×3-8AL	-40℃ to +125℃	TD93C46XUJN8G/TR	34SJN8 XXXXX	Tape and Reel, 3000
	TSSOP-8	-40℃ to +125℃	TD93C46XTS8G/TR	TD 93C46XTS8 XXXXX	Tape and Reel, 5000
TD93C56	SOIC-8	-40℃ to +125℃	TD93C56XS8G/TR	TD 93C56XS8 XXXXX	Tape and Reel, 4000
	UTDFN-2×3-8AL	-40℃ to +125℃	TD93C56XUJN8G/TR	34TJN8 XXXXX	Tape and Reel, 3000
	TSSOP-8	-40℃ to +125℃	TD93C56XTS8G/TR	TD 93C56XTS8 XXXXX	Tape and Reel, 5000
TD93C66	SOIC-8	-40℃ to +125℃	TD93C66XS8G/TR	TD 93C66XS8 XXXXX	Tape and Reel, 4000
	UTDFN-2×3-8AL	-40℃ to +125℃	TD93C66XUJN8G/TR	34UJN8 XXXXX	Tape and Reel, 3000
	TSSOP-8	-40℃ to +125℃	TD93C66XTS8G/TR	TD 93C66XTS8 XXXXX	Tape and Reel, 5000
TD93C76	SOIC-8	-40℃ to +125℃	TD93C76XS8G/TR	TD 93C76XS8 XXXXX	Tape and Reel, 4000
	UTDFN-2×3-8AL	-40℃ to +125℃	TD93C76XUJN8G/TR	34VJN8 XXXXX	Tape and Reel, 3000
	TSSOP-8	-40℃ to +125℃	TD93C76XTS8G/TR	TD 93C76XTS8 XXXXX	Tape and Reel, 5000
TD93C86	SOIC-8	-40℃ to +125℃	TD93C86XS8G/TR	TD 93C86XS8 XXXXX	Tape and Reel, 4000
	UTDFN-2×3-8AL	-40℃ to +125℃	TD93C86XUJN8G/TR	34WJN8 XXXXX	Tape and Reel, 3000
	TSSOP-8	-40℃ to +125℃	TD93C86XTS8G/TR	TD 93C86XTS8 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

SOIC-8/UTDFN-2×3-8AL/TSSOP-8



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Output Voltage Range (DOUT = V_{OH} or Hi-Z),
V_{OUT} ..... -0.5V to (V_{CC} + 0.5V)
Input Voltage Range, V_{IN} ..... -0.5V to (V_{CC} + 1V)
Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Ambient Operating Temperature, T_A ..... -40℃ to +130℃
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 1.7V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

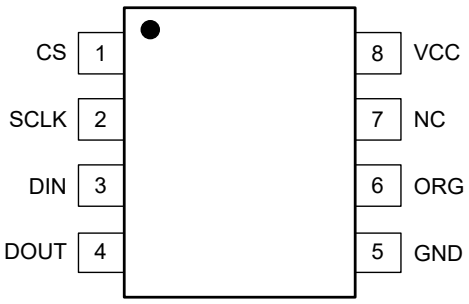
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

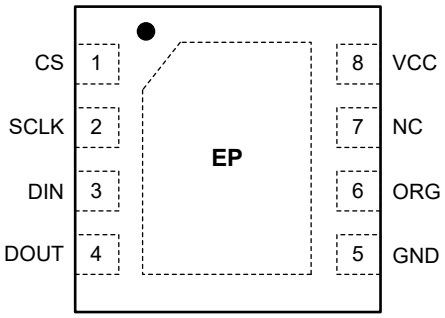
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8/TSSOP-8

(TOP VIEW)



UTDFN-2×3-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CS	Input	Chip Select Control Pin.
2	SCLK	Input	Serial Clock Input Pin.
3	DIN	Input	Serial Data Input Pin.
4	DOUT	Output	Serial Data Output Pin.
5	GND	Power	Ground.
6	ORG	Input	Organization Select Input Pin.
7	NC	-	No Connection. This pin can be left floating, tied to VCC or GND.
8	VCC	Power	Power Supply Voltage Pin.
Exposed Pad	EP	-	Exposed Pad. Connect it to GND or left it floating.

FUNCTIONAL BLOCK DIAGRAM

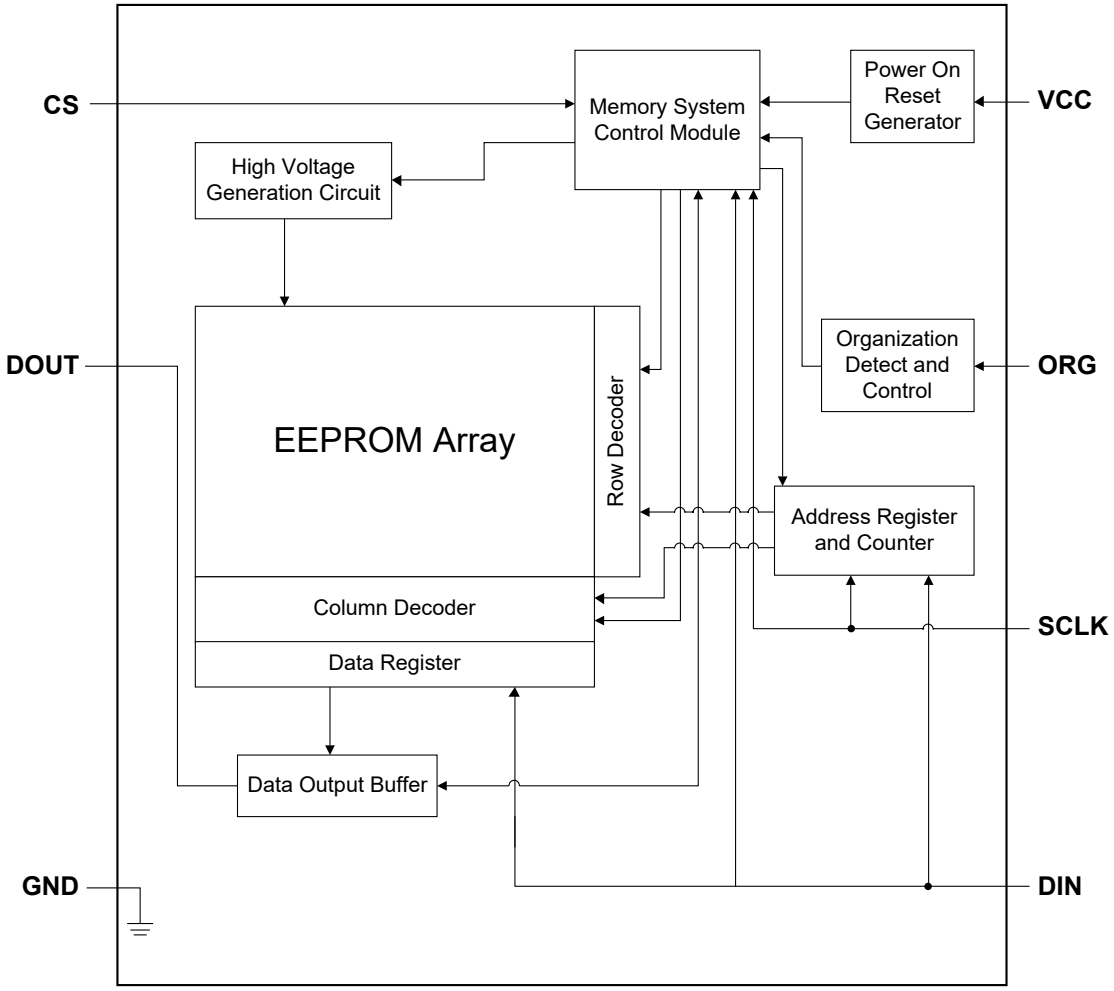


Figure 1. Block Diagram

DC AND AC PARAMETERS

Cycling Performance

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Write Cycle Endurance	N_W	T_A = +25℃, V_{CC} (MIN) < V_{CC} < V_{CC} (MAX)		1×10^6	Write cycle (1)
		T_A = +125℃, V_{CC} (MIN) < V_{CC} < V_{CC} (MAX)		1×10^5	Write cycle (1)

NOTE: 1. The endurance of write cycle is verified via product characterization and qualification test.

Memory Cell Data Retention

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Data Retention (1)	T_A = +55℃	100		Year

NOTE: 1. Data retention performance is verified during production test, whereas the 100-year retention specification is determined based on characterization and qualification assessment results.

AC Measurement Conditions

PARAMETER	CONDITIONS (1)	MIN	MAX	UNITS
Load Capacitance, C_L			100	pF
Input Rise and Fall Times			50	ns
Input Voltage Levels		0.2 × V_{CC}	0.8 × V_{CC}	V
Input Timing Reference Voltages		0.3 × V_{CC}	0.7 × V_{CC}	V
Output Timing Reference Voltages		0.3 × V_{CC}	0.7 × V_{CC}	V

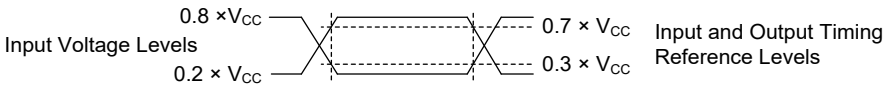


Figure 2. AC Testing Input Output Waveforms

Capacitance

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX (1)	UNITS
Output Capacitance	C_{OUT}	V_{OUT} = 0V		8	pF
Input Capacitance	C_{IN}	V_{IN} = 0V		6	

NOTE: 1. Parameter defined by design specifications. No production-level test is performed for this item.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LI}	V_{IN} = GND or V_{CC}			±2.5	μA
Output Leakage Current	I_{LO}	V_{OUT} = GND or V_{CC}, DOUT in high-Z			±2.5	μA
Operating Supply Current (Read)	I_{CC}	V_{CC} = 5V, CS = V_{IH}, f = 3MHz, DOUT = open			2	mA
		V_{CC} = 1.7V, CS = V_{IH}, f = 1MHz, DOUT = open			1	
Standby Supply Current	I_{CC1}	V_{CC} = 1.7V, CS = GND, SCLK = GND, ORG = GND or V_{CC}, pin 7 = V_{CC}, GND, or high-Z			1	μA
		V_{CC} = 5.5V, CS = GND, SCLK = GND, ORG = GND or V_{CC}, pin 7 = V_{CC}, GND, or high-Z			1	
Input Low Voltage (DIN, SCLK, CS)	V_{IL}		-0.45		0.3 × V_{CC}	V
Input High Voltage (DIN, SCLK, CS)	V_{IH}		0.7 × V_{CC}		V_{CC} + 1	V
Output Low Voltage (DOUT)	V_{OL}	V_{CC} = 5V, I_{OL} = 2.1mA			0.4	V
		V_{CC} = 1.7V, I_{OL} = 100μA			0.2	
Output High Voltage (DOUT)	V_{OH}	V_{CC} = 5V, I_{OH} = -400μA	0.8 × V_{CC}			V
		V_{CC} = 1.7V, I_{OH} = -100μA	V_{CC} - 0.2			

AC ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	ALT.	MIN	TYP	MAX	UNITS
Clock Frequency	V_{CC} ≤ 1.9V	f_C	f_{SK}	D.C.		2	MHz
	V_{CC} > 1.9V	f_C	f_{SK}	D.C.		3	
Chip Select Low to Clock High		t_{SLCH}	-	50			ns
Chip Select Setup Time		t_{SHCH}	t_{CSS}	50			ns
Chip Select Low to Chip Select High		t_{SLSH} (1)	t_{CS}	200			ns
Clock High Time		t_{CHCL} (2)	t_{SKH}	200			ns
Clock Low Time		t_{CLCH} (2)	t_{SKL}	200			ns
Data in Setup Time		t_{DVCH}	t_{DIS}	50			ns
Data in Hold Time		t_{CHDX}	t_{DIH}	50			ns
Clock Setup Time (Relative to CS)		t_{CLSH}	t_{SKS}	50			ns
Chip Select Hold Time		t_{CLSL}	t_{CSH}	0			ns
Chip Select to READY/$\overline{\text{BUSY}}$ Status		t_{SHQV}	t_{SV}			200	ns
Chip Select Low to Output High-Z		t_{SLQZ}	t_{DF}			100	ns
Delay to Output Low		t_{CHQL}	t_{PD0}			200	ns
Delay to Output Valid		t_{CHQV}	t_{PD1}			200	ns
Erase or Write Cycle Time		t_W	t_{WP}			3	ms

NOTES:

1. Chip Select Input (CS) shall remain low for at least t_{SLSH} during adjacent instruction cycles.

2. The total of t_{CH} and t_{CL} shall be no less than the minimum clock cycle, 1 / f_C (MAX).

SYNCHRONOUS TIMING

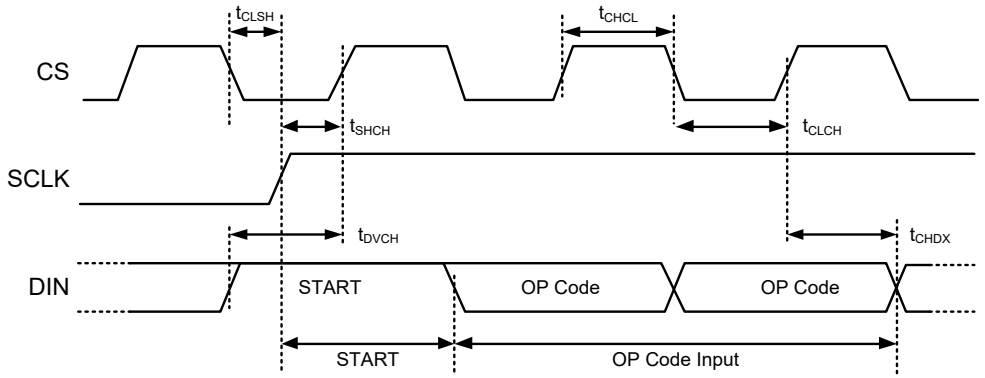


Figure 3. Synchronous Timing (Start and Op-Code Input)

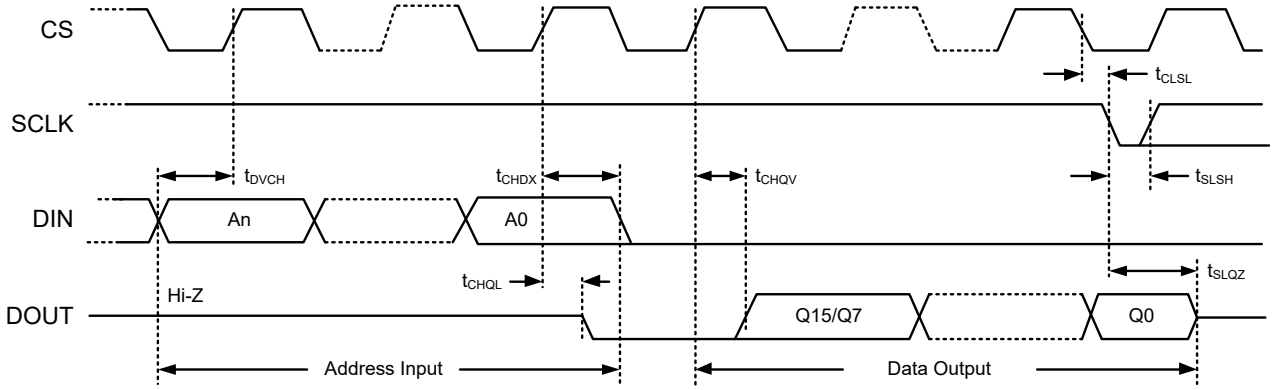


Figure 4. Synchronous Timing (Read)

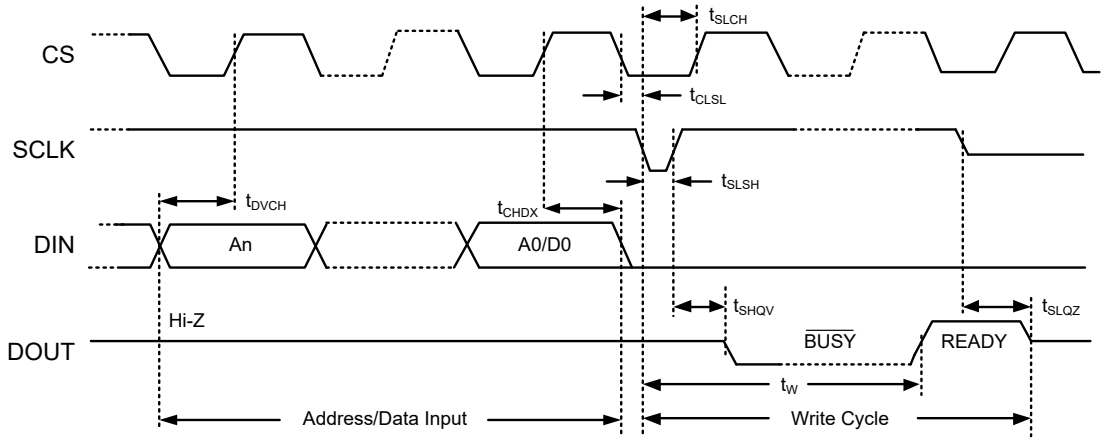


Figure 5. Synchronous Timing (Write)

DETAILED DESCRIPTION

Operating Supply Voltage (V_{CC})

Before selecting the memory chip and sending operational commands, a steady and valid V_{CC} supply within the defined minimum and maximum operating range must be supplied. To ensure stable DC power input, it is recommended to place a decoupling capacitor (typically 10nF to 100nF) near the device's VCC and GND package terminals.

The supply voltage shall stay stable and valid throughout command transmission. For write commands, V_{CC} must remain within specification until the internal write cycle duration (t_W) is fully completed.

Power-Up Conditions

During the power-up phase, V_{CC} ramps upward from the GND level to its nominal operating voltage. In this period, the chip select (CS) pin must not be left floating and shall be held at GND potential. It is thus recommended to pull the CS pin down to GND with an appropriate resistor.

Power-Up and Device Reset

An integrated power-on reset (POR) circuit is adopted to avoid unintended write operations during power ramp-up. As V_{CC} rises continuously at power-up, the device ignores all incoming commands until the supply voltage exceeds the POR threshold, which is set below the minimum rated V_{CC} value.

Once V_{CC} exceeds the POR threshold level, the device completes internal reset and enters the following status:

- Standby power state
- Chip deselected (valid when a pull-down resistor is fitted on the CS line)

Power-Down

As V_{CC} gradually falls from normal operating level during power-down, the device ceases to acknowledge any incoming commands once the supply drops below the POR threshold voltage.

Throughout the power-down process, the device shall remain deselected and be kept in standby mode, with no internal write operation ongoing.

APPLICATION INFORMATION

Memory Organization

The TD93Cx6 memory can be configured to operate in either byte (×8) or word (×16) mode. The ×16 configuration is activated when the organization select (ORG) pin is left unconnected (or tied to VCC); conversely, connecting the ORG pin to GND selects the ×8 configuration. For the TD93Cx6 to achieve minimum power consumption in standby mode, the ORG pin must be set to either GND or VCC (applying any voltage between GND and VCC to the ORG input may result in increased standby current).

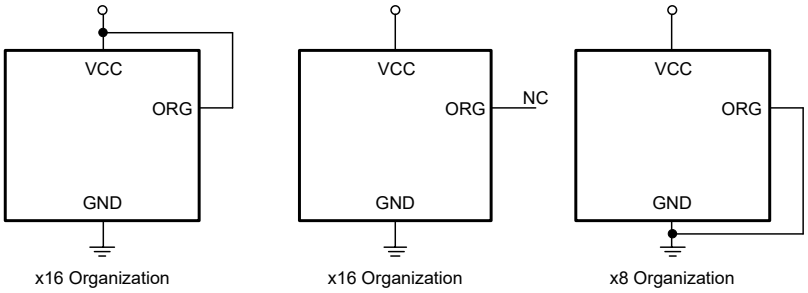


Figure 6. TD93Cx6 ORG Input Connection

Instruction Set

The TD93Cx6 series devices feature a seven-instruction set, detailed in Table 2 to Table 4. As illustrated in Figure 7, each instruction comprises the following components:

- A rising edge on the chip select input (CS), with the serial clock (SCLK) maintained at a low level, precedes every instruction.
- A start bit, defined as the first '1' detected on the serial data input (DIN) during the rising edge of the serial clock (SCLK).
- Two op-code bits, sampled from the serial data input (DIN) during the rising edge of the serial clock (SCLK). (Certain instructions also utilize the first two address bits to define the op-code.)
- Address bits corresponding to the byte or word being accessed. For the TD93C46 variant, the address consists of 6 bits in ×16 mode or 7 bits in ×8 mode (see Table 2). For the TD93C56 and TD93C66 variants, the address is 8 bits in ×16 mode or 9 bits in ×8 mode (see Table 3). For the TD93C76 and TD93C86 variants, the address comprises 10 bits in ×16 mode or 11 bits in ×8 mode (see Table 4).

Fabricated using CMOS technology, the TD93Cx6 devices support operation at speeds ranging from 0Hz (static input signals) up to the maximum ratings specified in the "AC Electrical Characteristics" section.

Table 2. Instruction Set for the TD93C46

Instruction	Description	Start Bit	Op-Code	×8 Origination (ORG = 0)			×16 Origination (ORG = 1)		
				Address (1)	Data	Required Clock Cycles	Address (1)	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
WEN	Write Enable	1	00	11X XXXX		10	11 XXXX		9
WDS	Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

NOTE: 1. X = Don't care bit.

APPLICATION INFORMATION (continued)

Table 3. Instruction Set for the TD93C56 and TD93C66

Instruction	Description	Start Bit	Op-Code	×8 Origination (ORG = 0)			×16 Origination (ORG = 1)		
				Address (1) (2)	Data	Required Clock Cycles	Address (2) (3)	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
WEN	Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
WDS	Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXX XXXX		12	10XX XXXX		11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

NOTES:

1. Address bit A8 is not decoded by the TD93C56.
2. X = Don't care bit.
3. Address bit A7 is not decoded by the TD93C56.

Table 4. Instruction Set for the TD93C76 and TD93C86

Instruction	Description	Start Bit	Op-Code	×8 Origination (ORG = 0)			×16 Origination (ORG = 1)		
				Address (1) (2)	Data	Required Clock Cycles	Address (2) (3)	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0		A9-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
WEN	Write Enable	1	00	11X XXXX XXXX		14	11 XXXX XXXX		13
WDS	Write Disable	1	00	00X XXXX XXXX		14	00 XXXX XXXX		13
ERASE	Erase Byte or Word	1	11	A10-A0		14	A9-A0		13
ERAL	Erase All Memory	1	00	10X XXXX XXXX		14	10 XXXX XXXX		13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

NOTES:

1. Address bit A10 is not decoded by the TD93C76.
2. X = Don't care bit.
3. Address bit A9 is not decoded by the TD93C76.

Read Data from Memory

When executing the memory read command, data is delivered through the serial output terminal DOUT. Once the command is received, internal circuitry decodes its operation code and storage address, then moves corresponding stored data into the output shift register. Transmission starts with a blank zero bit, followed by 8-bit single-byte or 16-bit dual-byte data, where high-order bits are sent ahead of low-order bits. All output signal level changes synchronize with the rising pulse edge of serial clock SCLK. As long as the chip selection signal CS keeps high level, TD93Cx6 series chips will automatically update internal address pointers and output subsequent groups of stored data. Under this uninterrupted reading state, no extra zero filler bit exists between adjacent data groups to ensure continuous data transmission. Once accessing the final storage location, the built-in address counter will reset itself back to the initial 00h address value.

APPLICATION INFORMATION (continued)

Data Erasure and Writing

Write Enable (WEN) and Write Disable (WDS)

The WEN instruction enables the subsequent execution of erase or write operations, while the WDS instruction disables these functions. Upon initial power-up, the TD93Cx6 device initializes with erase and write operations disabled. After a WEN instruction is executed, erase and write capabilities remain enabled until a WDS instruction is issued or the V_{CC} voltage drops below the power-on reset threshold. To prevent accidental corruption of memory contents, it is recommended to issue a WDS instruction after each write cycle. The READ instruction is not affected by either WEN or WDS commands.

Write Operation

When issuing the memory write command, 8-bit or 16-bit data sequences are appended behind operation codes and address signals to constitute the actual data content for storage. All signals fed into the serial input port DIN are captured at the rising edge of serial clock SCLK.

After the last data bit is successfully sampled, the chip selection signal must be set to low level prior to the next SCLK rising edge. Any level shift outside this valid time interval will fail to trigger the built-in programming process, resulting in unsuccessful data writing to designated storage units. Users can judge whether the operation is finished by detecting the status level of READY/$\overline{\text{BUSY}}$ line, which will be elaborated in subsequent chapters.

Once the internal writing process is activated, the whole procedure runs relying on independent internal timing logic, and external clock signals can be suspended or kept transmitting freely in this period. This chip integrates automatic erasing logic before data writing, so users do not need to send independent erase commands in advance before performing data storage operations.

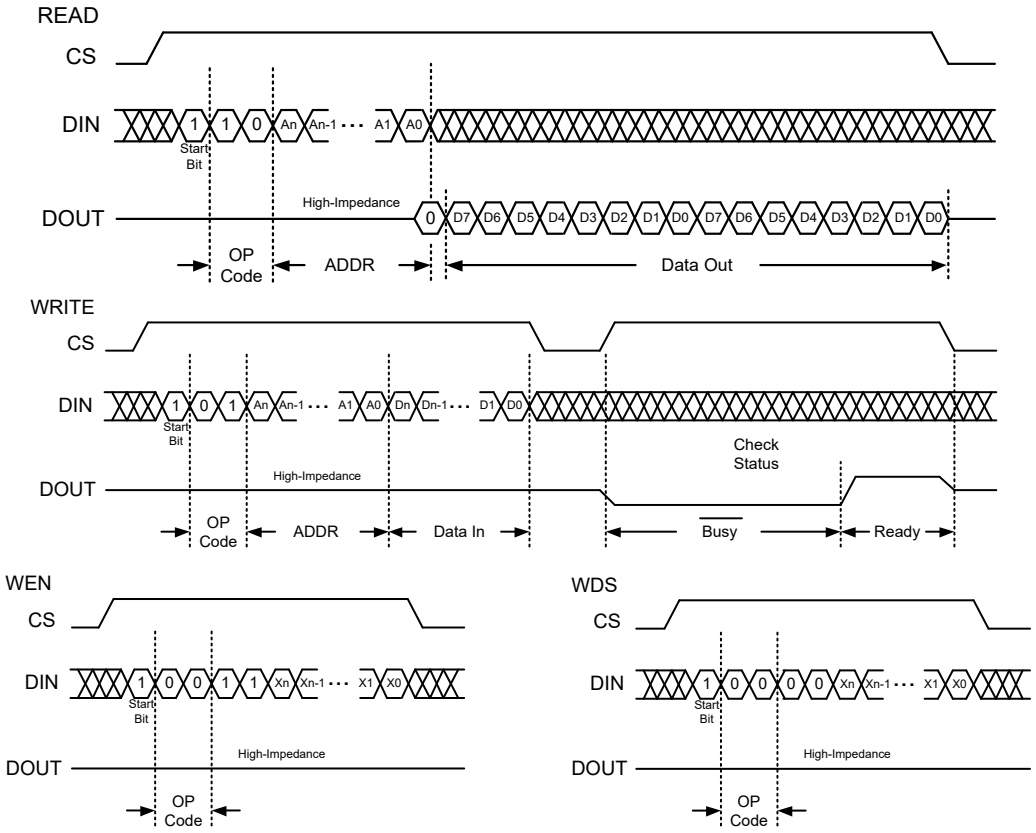


Figure 7. READ, WRITE, WEN, WDS Sequences

APPLICATION INFORMATION (continued)

Write All Operation

Similar to the erase all memory (ERAL) instruction, the write all memory with same data (WRAL) instruction requires a dummy address. Additionally, like the WRITE instruction, WRAL requires an 8-bit data byte or 16-bit data word, which is written to all memory addresses. Cycle completion can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described in the following section.

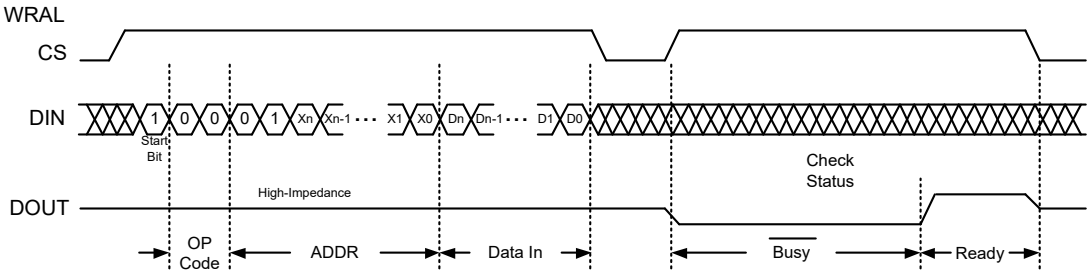


Figure 8. WRAL Sequence

Byte/Word Erasure

The byte and word erase command is used to reset all bits inside the designated storage unit to logic high state. After accurate address recognition is finished, the falling edge of chip selection signal launches the automatic timing erasing process. Users can confirm the end of this operation via detecting the level state of the READY/$\overline{\text{BUSY}}$ line.

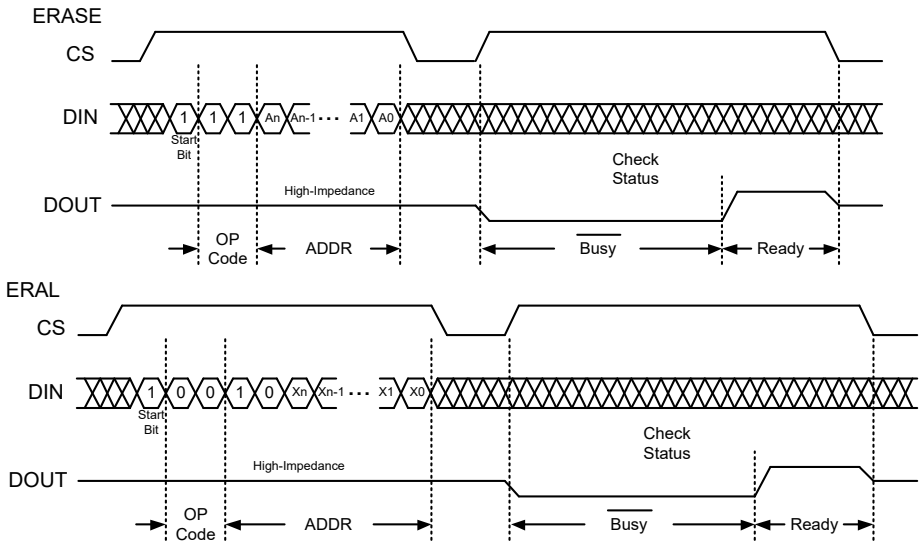


Figure 9. ERASE, ERAL Sequences

Full Memory Erasure

The erase all memory (ERAL) instruction erases the entire memory array (all bits are set to 1). This instruction requires a dummy address in its format and follows the same erase cycle process as the ERASE instruction. Cycle completion can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line.

READY/$\overline{\text{BUSY}}$ Status

When the chip runs data writing or content erasing processes triggered by write, erase, full array write and full array erase commands, it will output low-level busy status via serial data output once the chip selection signal is enabled. This state signal cannot be immediately obtained and needs to wait for the specified t_{SLSH} delay time. While staying in working busy mode, the TD93Cx6 series chip will shield all external bus transmitted signals. After the internal operation finishes, enabling the chip selection pin will make the device output high-level idle prompt, meaning it can respond to new operational commands. The serial output terminal will keep maintaining high logic level until the chip selection signal is disabled or the device identifies new starting signal codes.

APPLICATION INFORMATION (continued)

Clock Pulse Counter

In noisy environments, the number of clock pulses received on the serial clock (SCLK) may exceed that transmitted by the master (microcontroller). This can cause a one-or-more-bit misalignment in the instruction (as shown in Figure 10) and may result in incorrect data being written to an invalid address.

To resolve such abnormal operating conditions, TD93Cx6 integrates an internal pulse counter. This module keeps track of serial clock pulses starting from the start bit till the chip select signal drops to low level. If the actual received pulse quantity fails to conform to the preset standard value, all write, single erase, bulk erase and bulk write commands will be terminated directly without altering any stored data.

Table 2 to Table 4 list the standard clock pulse quantities corresponding to different instructions and various models in TD93Cx6 product series. For instance, TD93C56 and TD93C66 chips need 20 clock pulses under 8-bit operating mode from start bit transmission to CS level pull-down when executing write commands. The specific pulse allocation is described below:

- 1 Start bit
- + 2 Op-code bits
- + 9 Address bits
- + 8 Data bits

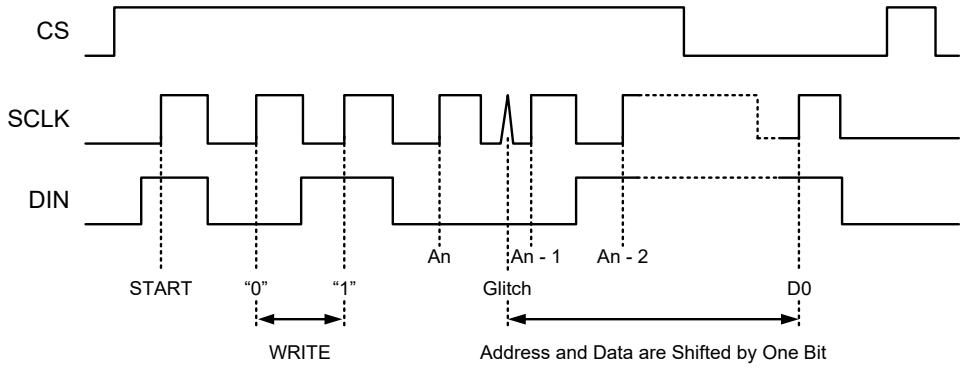


Figure 10. Write Sequence with One Clock Glitch

Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

REVISION HISTORY

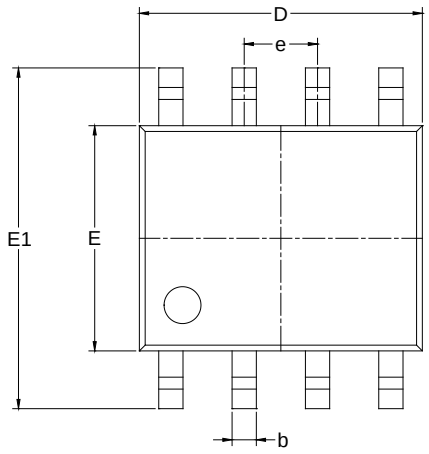
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

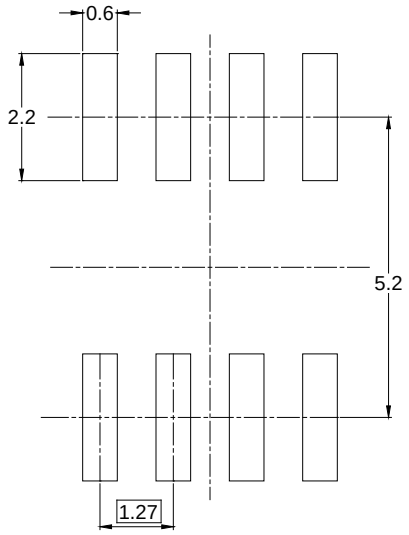
NOVEMBER 2026 – REV.A to REV.A.1	**Page**
Update Operating Ambient Temperature Range	All

Changes from Original to REV.A (OCTOBER 2026)	**Page**
Changed from product preview to production data	All

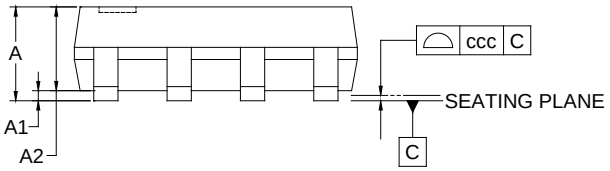
PACKAGE OUTLINE DIMENSIONS

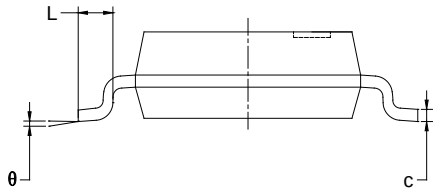
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



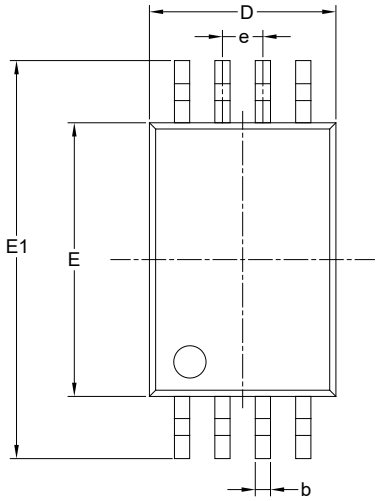


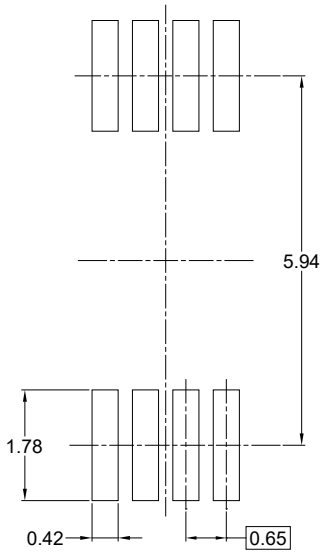
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.350	-	1.550
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Reference JEDEC MS-012.

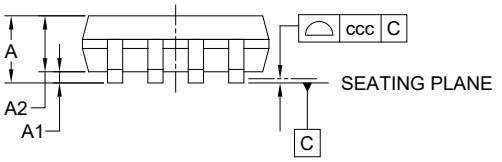
PACKAGE OUTLINE DIMENSIONS

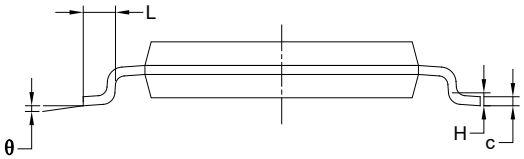
TSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



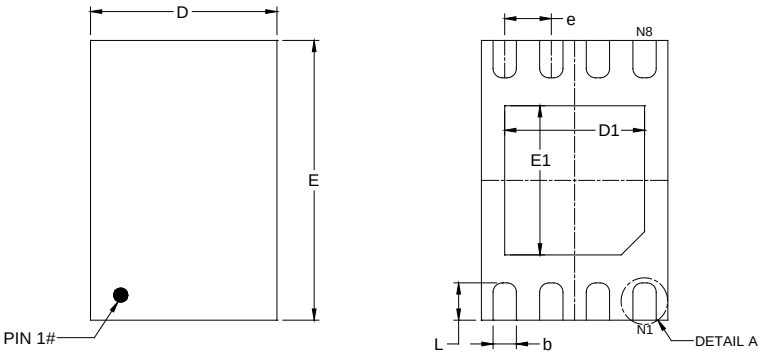


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	-	3.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

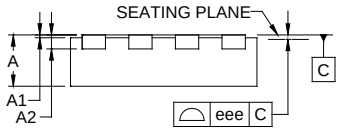
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

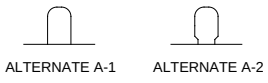
UTDFN-2×3-8AL



TOP VIEW **BOTTOM VIEW**

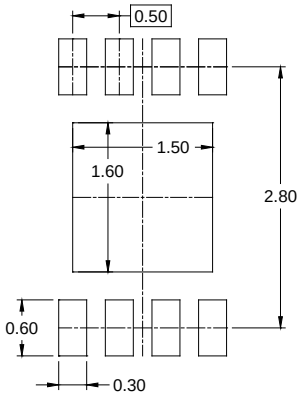


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



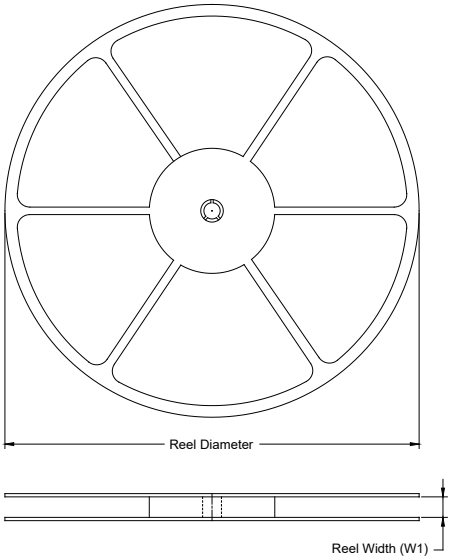
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.150 REF		
b	0.180	-	0.300
D	1.900	-	2.100
D1	1.400	-	1.600
E	2.900	-	3.100
E1	1.500	-	1.700
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

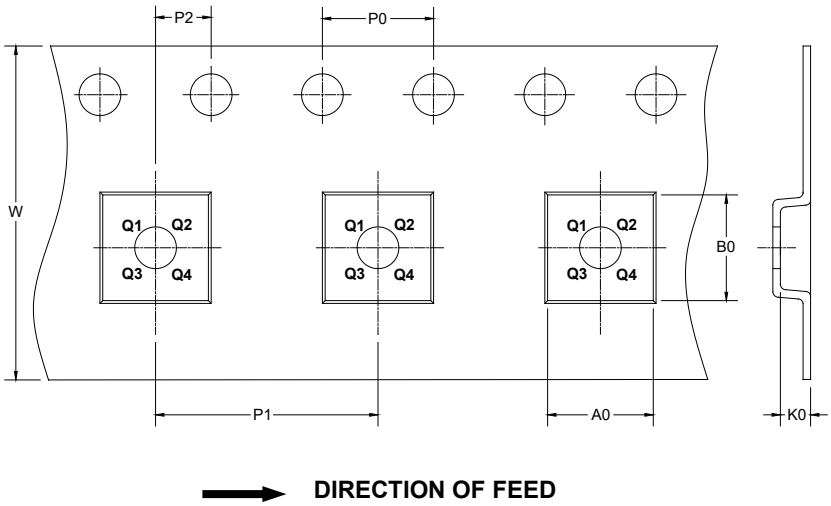
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



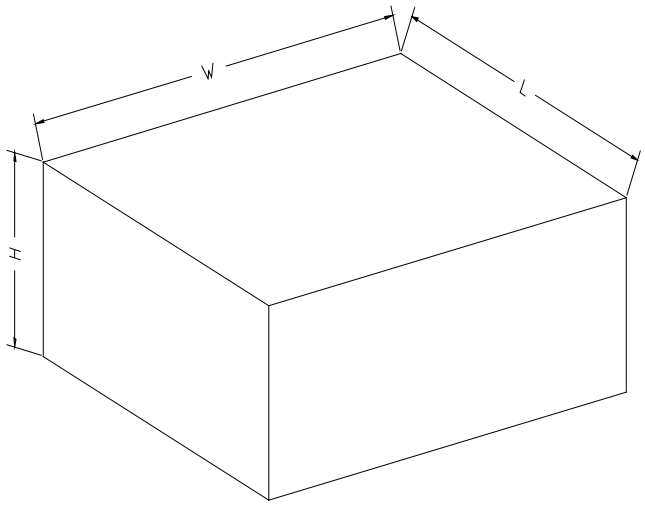
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TSSOP-8	13"	12.4	6.76	3.30	1.80	4.0	8.0	2.0	12.0	Q1
UTDFN-2×3-8AL	7"	9.5	2.30	3.30	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002