SGM51633S2
Dual-Channel, 16-Bit, 3MSPS Simultaneous-Sampling SAR ADC

GENERAL DESCRIPTION

The SGM51633S2 is a 16-bit, 2-channel simultaneous-sampling, high-precision successive approximation (SAR) analog-to-digital converter (ADC).

The SGM51633S2 supports unipolar fully differential input. And the chip is operated with a single 5V power supply.

The SGM51633S2 supports both SPI-compatible and byte-wide parallel interfaces. This flexible digital interface makes it easy to communicate with a diversity of microcontrollers, DSP and FPGA. It provides ADC data averaging function which is configurable by software.

The SGM51633S2 is available in a Green TQFN-5×5-32DL package. It is specified for the extended temperature range of -40℃ to +85℃.

APPLICATIONS

Sine/Cosine Analog Output Encoders
EDFA Gain-Control Loop
I/Q Demodulators
Medical Imaging System
SONAR Receiver
Digital Power Supply

FEATURES

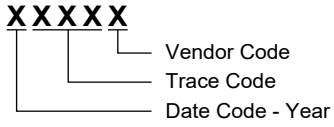
- **High Resolution, High Throughput**
  - **16-Bit, 3MSPS, Low Latency: 333ns**
- **16-Bit NMC DNL**
- **INL: ±1LSB (TYP)**
- **SNR at 2kHz:**
  - **93dBFS (TYP) for Channel A**
  - **91dBFS (TYP) for Channel B**
- **THD at 2kHz:**
  - **-110dB (TYP) for Channel A**
  - **-105dB (TYP) for Channel B**
- **SINAD at 2kHz:**
  - **92.5dBFS (TYP) for Channel A**
  - **90dBFS (TYP) for Channel B**
- **Support Multiple Reference Type**
  - **Internal**
  - **External Buffered**
  - **External**
- **Support Internal REFby2 Buffer for Setting Common Mode Voltage**
- **Support Data Averaging**
- **Enhanced Digital Interface for Transferring Sampling Data**
- **Extended Temperature Range: -40℃ to +85℃**
- **Available in a Green TQFN-5×5-32DL Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51633S2	TQFN-5×5-32DL	-40℃ to +85℃	SGM51633S2YTVJ32G/TR	SGM1XY YTVJ32 XXXXX	Tape and Reel, 3000
			SGM51633S2YTVJ32SG/TR	SGM1XY YTVJ32 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AVDD to GND ..... -0.3V to 6V
DVDD to GND ..... -0.3V to 6V
Digital Input Pins ..... GND - 0.3V to DVDD + 0.3V
Digital Output Pins ..... GND - 0.3V to DVDD + 0.3V
AINA_P, AINB_P to GND, AINA_N, AINB_N to GND
..... -0.3V to AVDD + 0.3V
REFA_N, REFB_N .....GND - 0.1V to GND + 0.1V
REFA_P, REFB_P, REFOUT, REFby2 to GND
.....GND - 0.3V to AVDD + 0.3V
Input or Output Current to Any Pin except Power Supply Pin
..... -10mA to 10mA
Package Thermal Resistance
TQFN-5×5-32DL, θ_{JA} ..... 31.5℃/W
TQFN-5×5-32DL, θ_{JB} ..... 8.3℃/W
TQFN-5×5-32DL, $\theta_{JC\ (TOP)}$ ..... 17.9℃/W
TQFN-5×5-32DL, $\theta_{JC\ (BOT)}$ ..... 1.6℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM .....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range, AVDD
..... 4.5V to 5.5V, 5V (TYP)
Digital Supply Voltage Operating Range, DVDD
..... 1.65V to 5.5V, 3.3V (TYP)
Digital Supply Voltage for SCLK > 20MHz, DVDD
..... 2.35V to 5.5V, 3.3V (TYP)
Operating Temperature Range..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

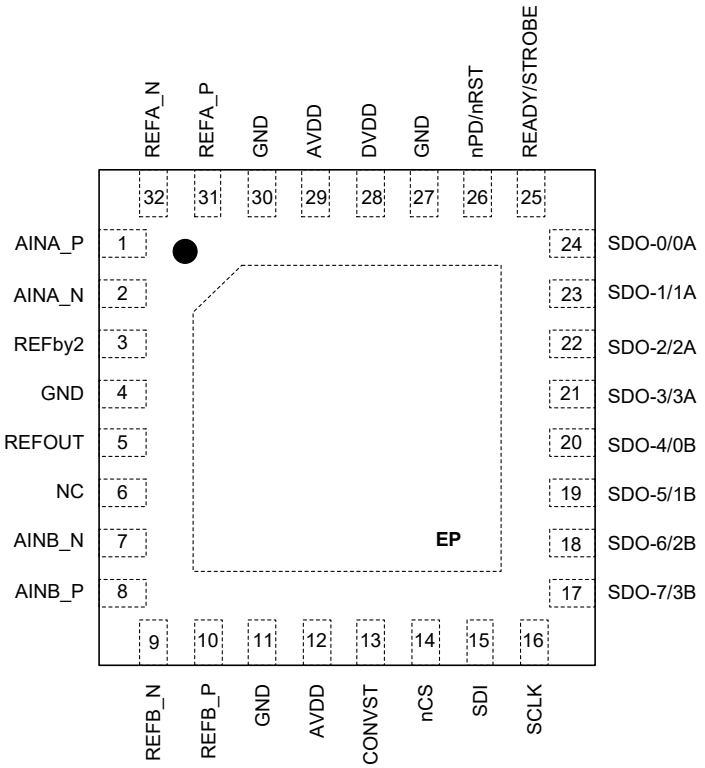
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5×5-32DL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	AINA_P	AI	Analog Input for Channel A Differential Positive Input Pin.
2	AINA_N	AI	Analog Input for Channel A Differential Negative Input Pin.
3	REFby2	AO	REFby2 Buffer Output Pin (0.5 × Reference A). A decoupling capacitor is required between pin 3 and pin 4.
4, 11, 27, 30	GND	P	Ground.
5	REFOUT	AI/O	Internal Reference Output/External Reference Input. A decoupling capacitor is required between pin 4 and pin 5.
6	NC	—	No Connection.
7	AINB_N	AI	Analog Input for Channel B Differential Negative Input Pin.
8	AINB_P	AI	Analog Input for Channel B Differential Positive Input Pin.
9	REFB_N	AO	Negative Output of Reference B with Its Buffer. Negative reference input for ADC_B. Externally connect to the device GND.
10	REFB_P	AO	Positive Output of Reference B with Its Buffer. Positive reference input for ADC_B. A 10μF decoupling capacitor is required between pin 9 and pin 10.
12, 29	AVDD	P	Analog Power Supply Pin. A decoupling capacitor is required between pin 12 and pin 11. And a decoupling capacitor is required between pin 29 and pin 30.
13	CONVST	DI	Conversion Start Input Pin. A conversion (ADC_A and ADC_B) is trigged by the rising edge of CONVST.
14	nCS	DI	Chip Select Input Pin. Active Low. If nCS is pulled low, the chip can be operated. If nCS is pulled high, the SDO-x/y pins are set to Hi-Z.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
15	SDI	DI	Serial Data Input Pin.
16	SCLK	DI	Clock Input Pin for the Serial Interface.
17	SDO-7/3B	DO	SPI Mode: Data Output 3 for Channel B. Parallel Byte Mode: Data Bit7 of the Data Byte.
18	SDO-6/2B	DO	SPI Mode: Data Output 2 for Channel B. Parallel Byte Mode: Data Bit6 of the Data Byte.
19	SDO-5/1B	DO	SPI Mode: Data Output 1 for Channel B. Parallel Byte Mode: Data Bit5 of the Data Byte.
20	SDO-4/0B	DO	SPI Mode: Data Output 0 for Channel B. Parallel Byte Mode: Data Bit4 of the Data Byte.
21	SDO-3/3A	DO	SPI Mode: Data Output 3 for Channel A. Parallel Byte Mode: Data Bit3 of the Data Byte.
22	SDO-2/2A	DO	SPI Mode: Data Output 2 for Channel A. Parallel Byte Mode: Data Bit2 of the Data Byte.
23	SDO-1/1A	DO	SPI Mode: Data Output 1 for Channel A. Parallel Byte Mode: Data Bit1 of the Data Byte.
24	SDO-0/0A	DO	SPI Mode: Data Output 0 for Channel A. Parallel Byte Mode: Data Bit0 of the Data Byte.
25	READY/STROBE	DO	Indicate Data Ready or Strobe Output for Data Capture.
26	nPD/nRST	DI	Asynchronous Reset or Power-Down Input Pin.
28	DVDD	P	Digital Interface Power Supply Pin. A decoupling capacitor is required between pin 27 and pin 28.
31	REFA_P	AO	Positive Output of Reference A with Its Buffer. Positive reference input for ADC_A. A 10μF decoupling capacitor is required between pin 31 and pin 32.
32	REFA_N	AO	Negative Output of Reference A with Its Buffer. Negative reference input for ADC_A. Externally connect to the device GND.
Exposed Pad	EP	—	Exposed Pad. Connect this pin to the printed circuit board (PCB) ground.

NOTE: AI = analog input, DI = digital input, AO = analog output, DO = digital output, AI/O = analog input/output, P = power.

ELECTRICAL CHARACTERISTICS

(AVDD = 4.5V to 5.5V, DVDD = 2.35V to 5.5V, V_{CM} = $V_{REFx\_P/2}$, Internal reference and maximum throughput, T_A = -40℃ to +85℃, typical values are at T_A = +25℃, AVDD = 5V, DVDD = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage (1) (AINx_P - AINx_N)	FSR		-4.096		4.096	V
Absolute Input Voltage (AINx_P or AINx_N to GND)	V_{IN}		0		4.096	V
Common Mode Input Range	V_{CM}		1.848		2.248	V
Analog Input Leakage Current	I_{IN}			±1		μA
Input Capacitance	C_I	Sample mode		22		pF
		Hold mode		1		
Analog Input Bandwidth	BW	-3dB input signal		52		MHz
		-0.1dB input signal		4.2		
Voltage Reference Output						
REFOUT Voltage (2)	V_{REFOUT}		4.081	4.096	4.111	V
V_{REFOUT} Drift (3)	$\Delta V_{REF}/\Delta T$			5.5	15	ppm/℃
V_{REFOUT} Line Regulation	$\Delta V_{REFOUT}/\Delta AVDD$	AVDD variation 4.5V to 5.5V		50		μV/V
REFOUT Output Current Capability	I_{REFOUT}	$\lvert\Delta V_{REF}\rvert$ < 2mV		1.5		μA
REFOUT Capacitor	C_{REFOUT}	For specified performance		1		μF
Internal Reference Buffer						
Reference Buffer Gain	G_{REFBUF}			1		V/V
Reference Buffer Output Offset	$E_{O-REFBUF}$		-1	±0.2	1	mV
Reference Buffer Output Offset Temperature Drift	$\Delta E_{O-REFBUF}/\Delta T$			1		μV/℃
Reference Buffer Output Mismatch	(V_{REFA_P} - V_{REFB_P})		-750	±200	750	μV
Reference Buffer Output Capacitor (3)	C_{REFx_P}	For specified performance, between each pair of REFx_P and REFx_N	7	10	27	μF
REFby2 Output						
REFby2 Output Voltage	V_{REFby2}	EN_REFBY2_OFFSET = 0	2.033	2.046	2.063	V
		EN_REFBY2_OFFSET = 1	2.133	2.146	2.163	
REFby2 Output Current Capability	I_{REFby2}			±3		mA
REFby2 Output Capacitor			1			μF
REFby2 Output Noise		With specified output capacitor		10		μV_{RMS}
Digital Outputs						
High-Level Output Voltage	V_{OH}	I_{OH} = 500μA source	0.8 × DVDD		DVDD	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 500μA sink	0		0.2 × DVDD	V
Digital Inputs						
High-Level Input Voltage	V_{IH}	DVDD > 2.3V	0.7 × DVDD		DVDD +0.3	V
Low-Level Input Voltage	V_{IL}		-0.3		0.3 × DVDD	V
High-Level Input Voltage	V_{IH}	DVDD ≤ 2.3V	0.8 × DVDD		DVDD +0.3	V
Low-Level Input Voltage	V_{IL}		-0.3		0.2 × DVDD	V

NOTES:

1. Ideal input range. It does not consider gain and offset error.
2. Exclude the variation in voltage resulting from solder shift effects.
3. Design and characterization data guarantee the establishment of the minimum and maximum values.

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 4.5V to 5.5V, DVDD = 2.35V to 5.5V, V_{CM} = $V_{REFx\_P/2}$, Internal reference and maximum throughput, T_A = -40℃ to +85℃, typical values are at T_A = +25℃, AVDD = 5V, DVDD = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Analog Supply Voltage	AVDD			4.5	5	5.5	V
Digital Supply Voltage	DVDD			1.65	3.3	5.5	V
Analog Supply Current	I_{AVDD}	f_{SAMPLE} = 3MSPS			60	75	mA
		AVDD = 5V, no conversion			15	21	mA
		Power-down (nPD/nRST low)			1	10	μA
Digital Supply Current (3)	I_{DVDD}	f_{SAMPLE} = 3MSPS, $C_{SDO-x/y}$ = 10pF			3	10	mA
Power Supply Rejection Ratio (4)	PSRR	100mV_{PP} ripple on AVDD of frequency < 100kHz			85		dB
DC Accuracy							
Resolution, No Missing Codes				16			Bits
Differential Nonlinearity	DNL			-0.99	±0.3	1.8	LSB
Integral Nonlinearity	INL			-3	±1	3	LSB
Offset Error	E_O			-7	±1	7	LSB
Cummulative Gain Error for ADC_x and REFBUF_x	G_E			-0.04	±0.01	0.04	%FSR
Gain Drift	$\Delta G_E/\Delta T$				1		ppm/℃
Transition Noise		Mid-code			0.5		LSB
AC Accuracy							
Signal-to-Noise Ratio (4)	SNR	f_{IN} = 2kHz	Channel A	90	93		dBFS
			Channel B	87.5	91		
		f_{IN} = 100kHz, FSR = -3dBFS	Channel A		92		
			Channel B		91		
Signal-to-Noise + Distortion (4) (5)	SINAD	f_{IN} = 2kHz	Channel A	89.5	92.5		dBFS
			Channel B	87	90		
		f_{IN} = 100kHz, FSR = -3dBFS	Channel A		92		
			Channel B		90.5		
Total Harmonic Distortion (4) (5)	THD	f_{IN} = 2kHz	Channel A		-110	-93	dB
			Channel B		-105	-91.5	
		f_{IN} = 100kHz, FSR = -3dBFS	Channel A		-101		
			Channel B		-99		
Spurious-Free Dynamic Range (4)	SFDR	f_{IN} = 2kHz	Channel A	94	113		dBFS
			Channel B	93.5	106		
		f_{IN} = 100kHz, FSR = -3dBFS	Channel A		103		
			Channel B		101		
Common Mode Rejection Ratio (4)	CMRR	f_{IN} = DC to 1MHz, V_{IN} = 100mV_{PP}			55		dB
Channel-to-Channel Isolation (4)	ISOXT	f_{IN_ADCA} = 15kHz at 10%FSR, f_{IN_ADCB} = 25kHz at 100%FSR			-120		dB

NOTES:

4. All specifications are tested with an input signal at 0.5dB below full-scale, unless otherwise noted. All available input ranges are described in full-scale input range (FSR), but not performance guaranteed.

5. Calculated on the first nine harmonics of the input frequency.

TIMING REQUIREMENTS

(AVDD = 4.5V to 5.5V, DVDD = 1.65V to 5.5V, V_{CM} = $V_{REFx\_P/2}$, Internal reference and maximum throughput, T_A = -40℃ to +85℃, typical values at T_A = +25℃, AVDD = 5V, DVDD = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Control and Data Transfer (See Figure 1 and Figure 2)						
Delay Time: CONVST High to nCS Falling for Zero Cycle Latency (Mode_1 Transfer)	$t_{D\_CONVST\_CS}$		t_{DRDY} (1)			ns
Time between Two Adjacent CONVST Rising Edges for Zero Cycle Latency (Mode_1 Transfer)	t_{CYCLE}			t_{DRDY} + t_{READ}		ns
Time between Two Adjacent CONVST Rising Edges for Mode_2 Transfer			333			ns
Sampling Rate	f_{SAMPLE}				3	MSPS
Acquisition Time	t_{ACQ}		140			ns
Delay Time: CONVST High to nCS Falling for Mode_2 Transfer	$t_{D\_CONVST\_CS}$		17		180	ns
Pulse Width: CONVST Low	t_{WL_CONVST}		15			ns
Pulse Width: CONVST High	t_{WH_CONVST}		15			ns
SPI-Compatible and Parallel Byte Protocol (See Figure 3)						
Serial Clock Time Period	t_{CLK}		$1/f_{CLK}$			
SCLK High Time	t_{PH_CLK}		0.45 × t_{CLK}		0.55 × t_{CLK}	ns
SCLK Low Time	t_{PL_CLK}		0.45 × t_{CLK}		0.55 × t_{CLK}	ns
Setup Time: nCS Falling to First SCLK Capture Edge	t_{SU_CSCK}		12			ns
Setup Time: SDI Data Valid to SCLK Capture Edge	t_{SU_CKDI}		2.5			ns
Hold Time: SCLK Capture Edge to Previous Data Valid on SDI	t_{HT_CKDI}		2			ns
Delay Time: Last SCLK Capture Edge to nCS Rising	t_{HT_CKCS}		14			ns
Serial Clock Frequency for SPI Protocols with Single Data Rate	f_{CLK}				60	MHz
Serial Clock Frequency for SPI Protocols with Double Data Rate					22	MHz
Serial Clock Frequency for Parallel Byte Protocol					45	MHz
Clock Re-Timer Protocol with STROBE = SCLK (External Clock) (2) (See Figure 4)						
Serial Clock Frequency with Single Data Rate	f_{CLK}	DVDD = 1.65V to 2.35V			30	MHz
		DVDD = 2.35V to 5.5V			60	
Serial Clock Frequency with Double Data Rate					22	MHz
Asynchronous Reset and Power-Down Timing (See Figure 6)						
Pulse Width (Low) for Reset	t_{WL_RST}		50		500	ns
Minimum Pulse Width (Low) for Power-Down	$t_{WL\_PD\_min}$		1000			ns

NOTES:

1. See the Switching Characteristics section.

2. Other parameters are the same as the SPI-compatible and parallel byte protocols.

SWITCHING CHARACTERISTICS

(AVDD = 4.5V to 5.5V, DVDD = 1.65V to 5.5V, V_{CM} = $V_{REF/2}$, Internal reference and maximum throughput, T_A = -40℃ to +85℃, typical values at T_A = +25℃, AVDD = 5V, DVDD = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Control and Data Transfer (See Figure 1 and Figure 2)						
Data Ready Time for Present Sample: CONVST High to READY High	t_{DRDY}	Zero cycle latency (mode_1 transfer)			315	ns
SPI-Compatible and Parallel Byte Protocol (See Figure 3)						
Delay Time: nCS Falling to Data Valid on SDO Line	t_{DEN_CSDO}				15	ns
Delay Time: nCS Rising Edge to SDO Line Tri-State	t_{DZ_CSDO}				17	ns
Delay Time: SCLK Launch Edge to Next Data Valid on SDO Line	t_{D_CKDO}	SPI-compatible protocols with single data rate			15.8	ns
		SPI-compatible protocols with double data rate			21	
		Parallel byte protocol			21	
Aperture Delay	t_A			8		ns
t_A Mismatch				40		ps
Aperture Jitter	t_{JITTER}			2		ps
Clock Re-Timer Protocol with STROBE = SCLK (External Clock) (1) (See Figure 4)						
Time Offset: STROBE Edge to Next Data Valid on SDO Line	$t_{OFF\_STROBE\_DO}$		-2.5		2.5	ns
Delay Time: nCS Rising to READY Displaying Internal Device State	$t_{D\_CS\_READY}$				13.5	ns
Delay Time: SCLK Rising Edge to STROBE Rising	$t_{D\_CKSTROBE\_r}$				21.5	ns
Delay Time: SCLK Falling Edge to STROBE Falling	$t_{D\_CKSTROBE\_f}$				21.5	ns
STROBE Output High Time	t_{PH_STROBE}		0.45 × t_{STR}		0.55 × t_{STR}	ns
STROBE Output Low Time	t_{PL_STROBE}		0.45 × t_{STR}		0.55 × t_{STR}	ns
Clock Re-Timer Protocol with STROBE = Internal Clock (1) (See Figure 5)						
Delay Time : nCS Falling to 1st STROBE Rising	$t_{D\_CS\_STROBE}$		15		50	ns
Time Offset : STROBE Edge to Next Data Valid on SDO Line	$t_{OFF\_STROBE\_DO}$		-2		4	ns
Delay Time: nCS Rising to READY Displaying Internal Device State	$t_{D\_CS\_READY}$				13.5	ns
INTCLK Period	t_{INTCLK}			15		ns
STROBE Period	t_{STR}	INTCLK (3)		16		ns
		INTCLK/2		30		
		INTCLK/4		60		
STROBE High Period	t_{WH_STR}		0.4 × t_{STR}		0.6 × t_{STR}	ns
STROBE low period	t_{WL_STR}		0.4 × t_{STR}		0.6 × t_{STR}	ns
Asynchronous Reset and Power-Down Timing (See Figure 6)						
Wake-Up Time from Reset	t_{RST_WKUP}				1	μs
Wake-Up Time from Power-Down	t_{PD_WKUP} (2)			18	150	ms
REFOUT Wake-Up Time	t_{WKUP_REFOUT}			15.6	140	ms
Reference Buffer Output Settling Time	$t_{REFx\_P\_SETTLE}$	C_{REFx_P} = 10μF		18	150	ms

NOTES:

1. Other parameters are the same as the SPI-compatible and parallel byte protocols.

2. With C_{REFx_P} = 10μF.

3. In the clock re-timer (CRT) protocols, when STROBE = INTCLK, the DVDD voltage must be greater than 2.35V.

TIMING DIAGRAMS

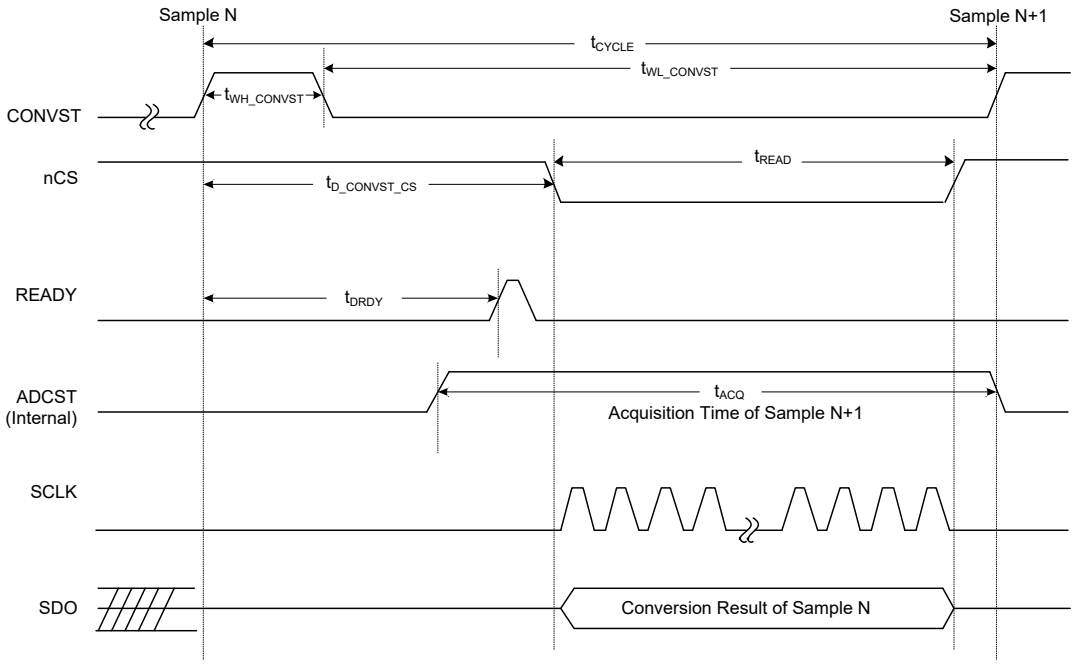
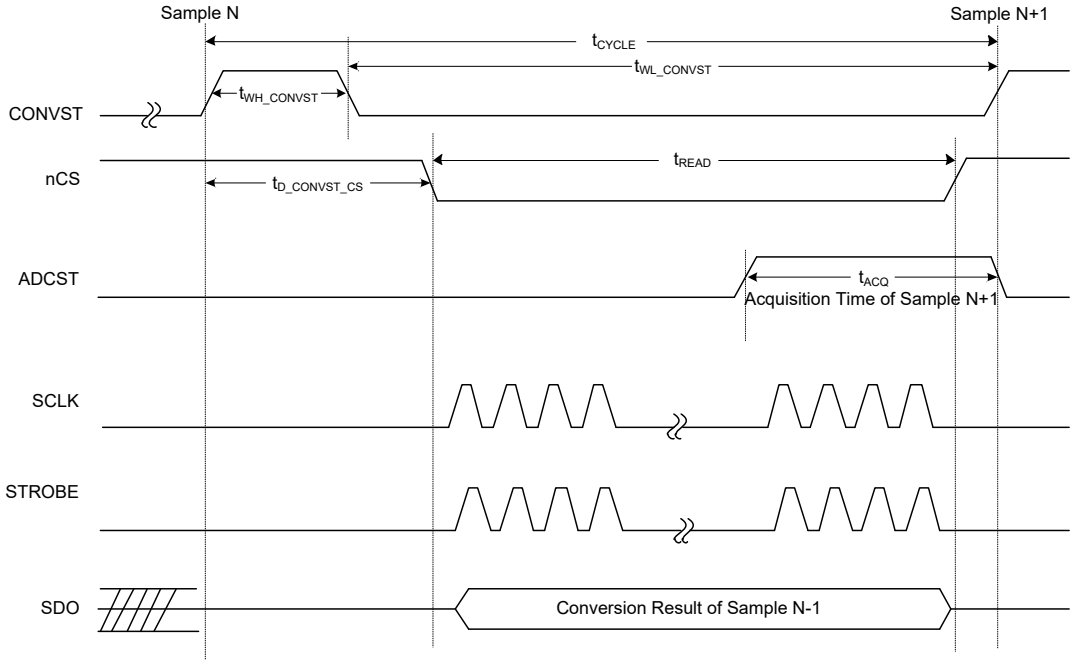


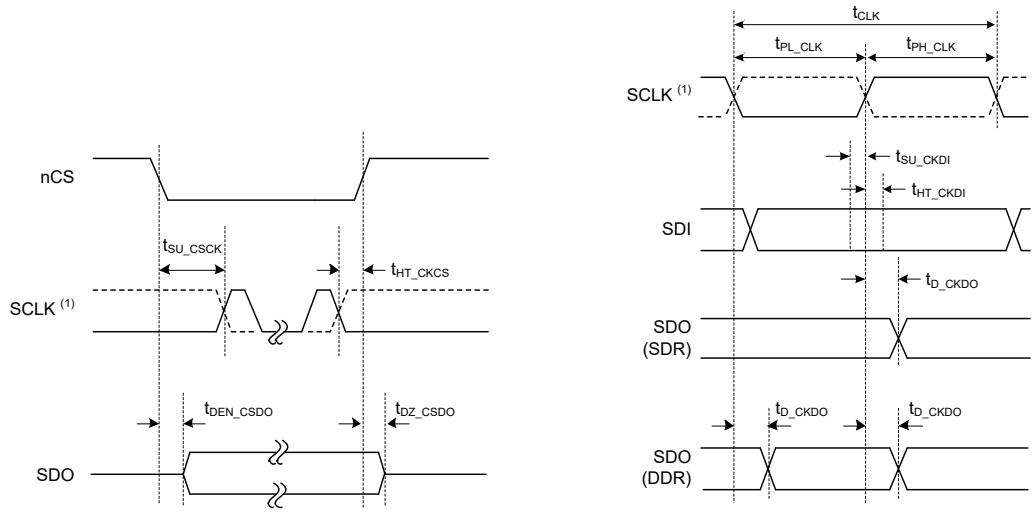
Figure 1. Conversion Control and Data Transfer with Zero Cycle Latency (Mode_1 Transfer)



NOTE: STROBE output is only for clock re-timer protocols. More details please refer to the STROBE section.

Figure 2. Conversion Control and Data Transfer with Wider Read Cycle (Mode_2 Transfer)

TIMING DIAGRAMS (continued)



NOTE:
1. The SCLK polarity, launch edge, and capture edge depend on the selected SPI protocol. DDR is not supported with the parallel byte protocol.

Figure 3. SPI-Compatible and Parallel Byte Protocols Timing

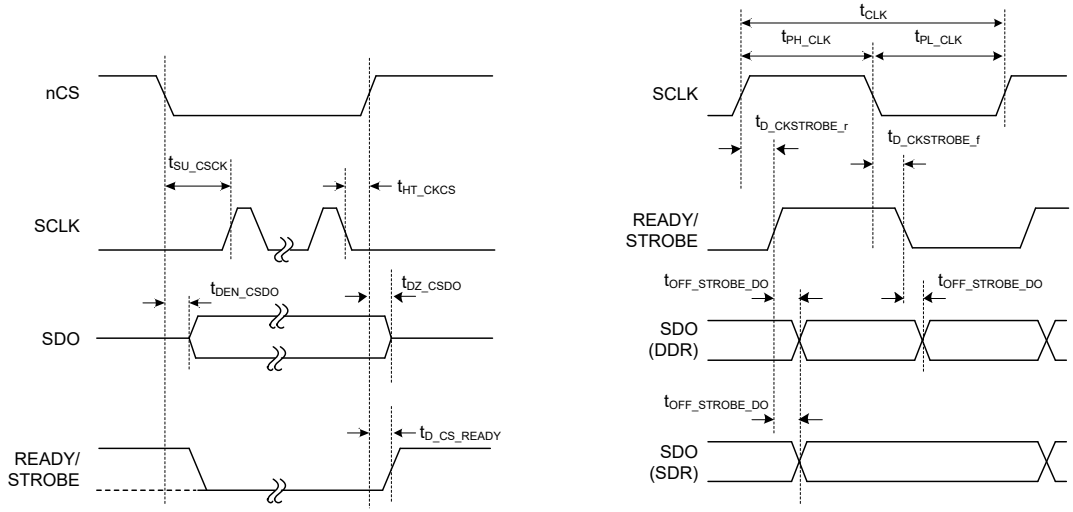


Figure 4. Clock Re-Timer Protocol (External Clock) Timing

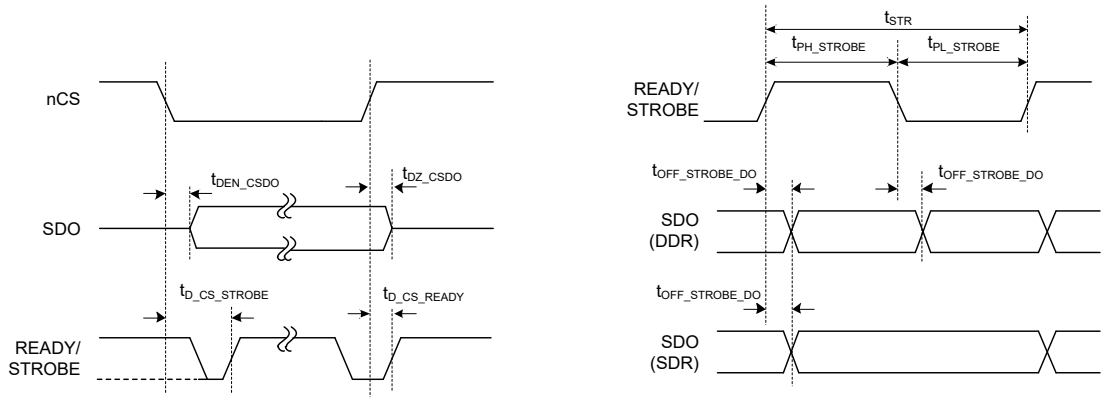


Figure 5. Clock Re-Timer Protocol (Internal Clock) Timing

TIMING DIAGRAMS (continued)

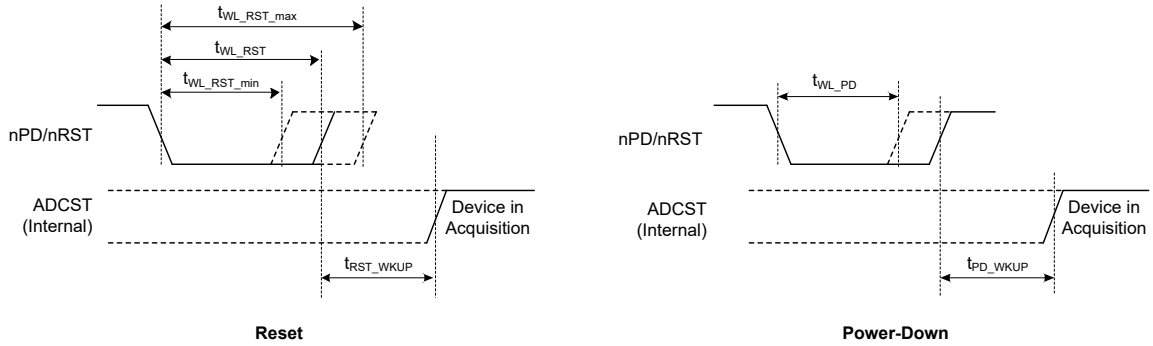
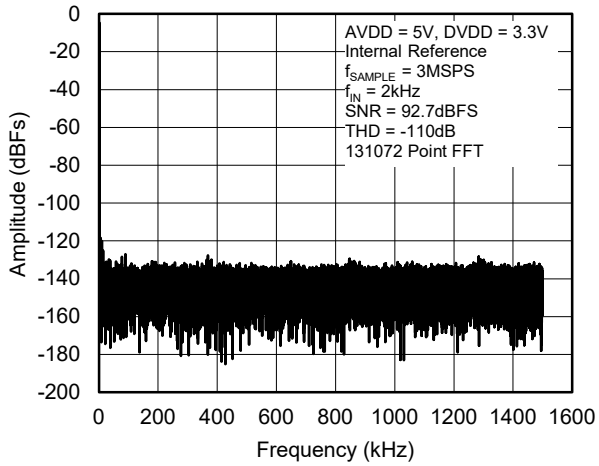


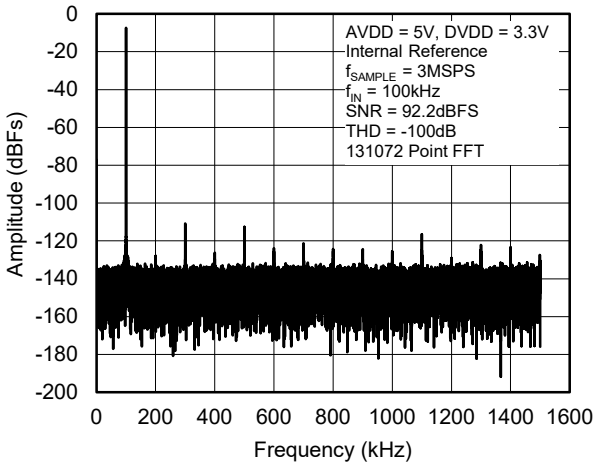
Figure 6. Asynchronous Reset and Power-Down Timing

TYPICAL PERFORMANCE CHARACTERISTICS

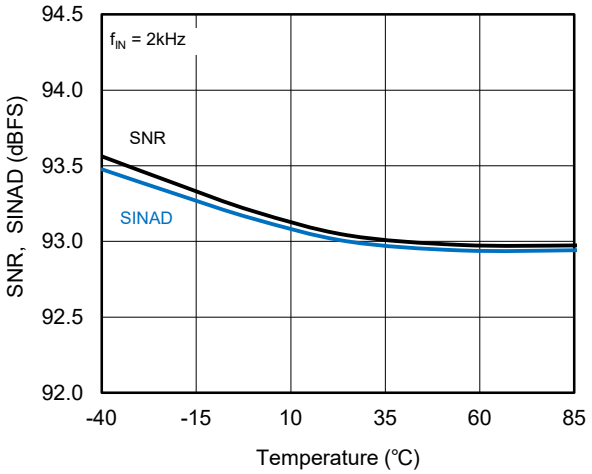
Typical FFT at f_{IN} = 2kHz



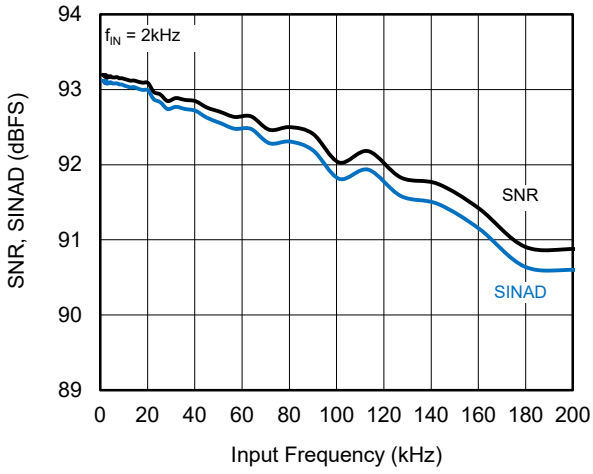
Typical FFT at f_{IN} = 100kHz



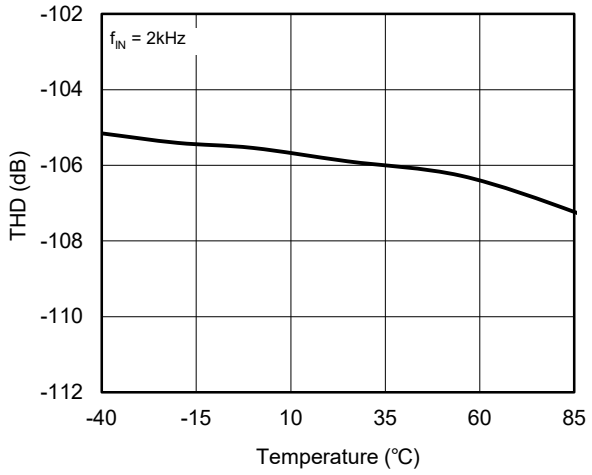
Noise Performance vs. Temperature



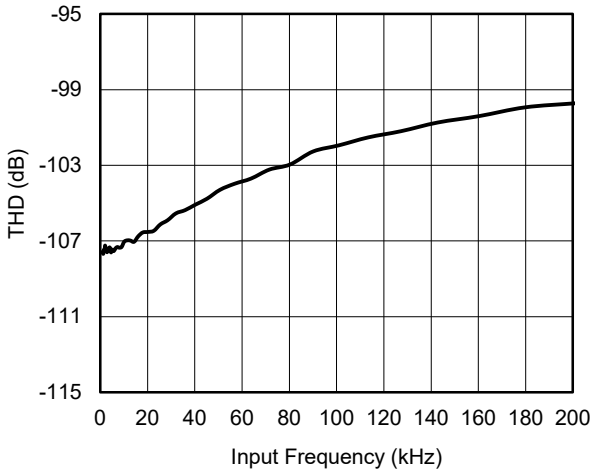
Noise Performance vs. Input Frequency



Distortion Performance vs. Temperature

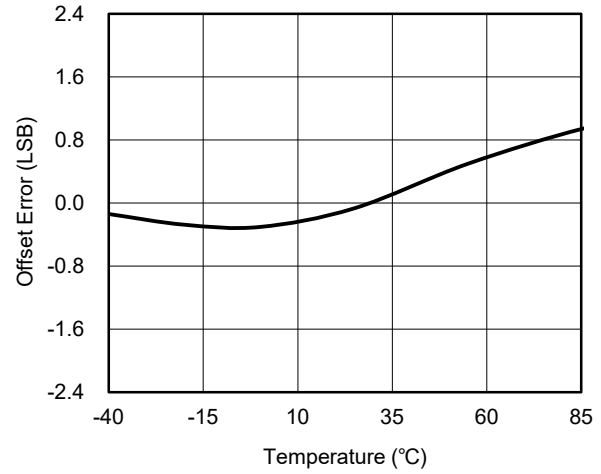


Distortion Performance vs. Input Frequency

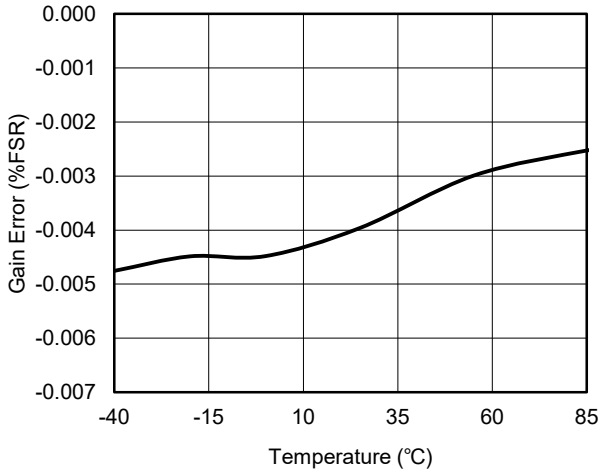


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

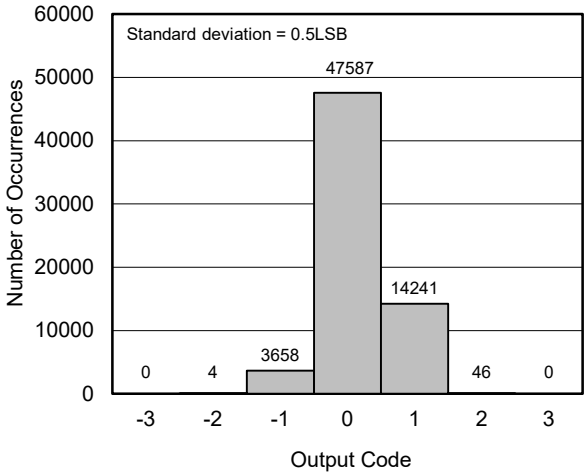
Offset Error vs. Temperature



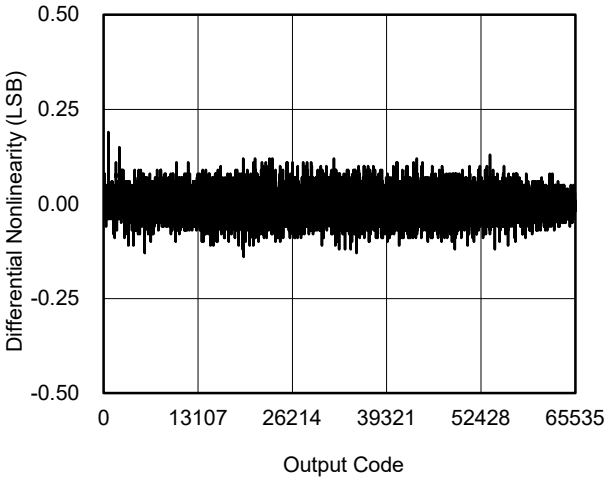
Gain Error vs. Temperature



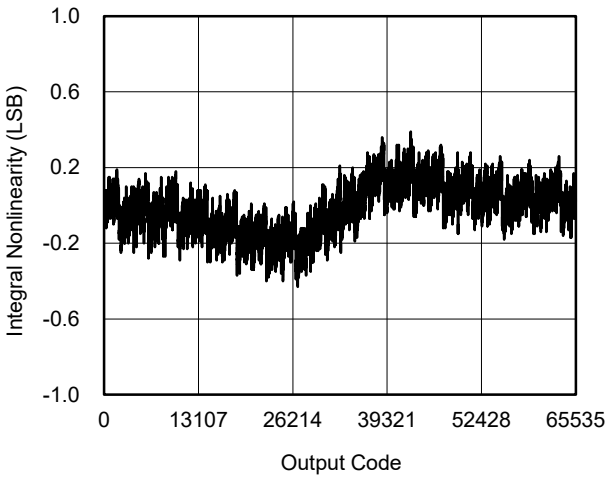
DC Input Histogram



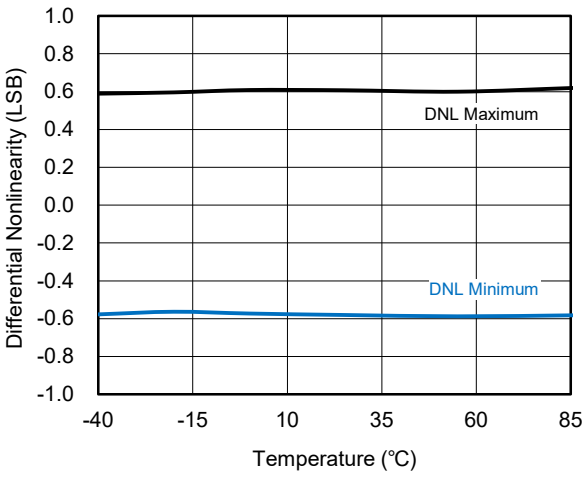
Typical DNL



Typical INL

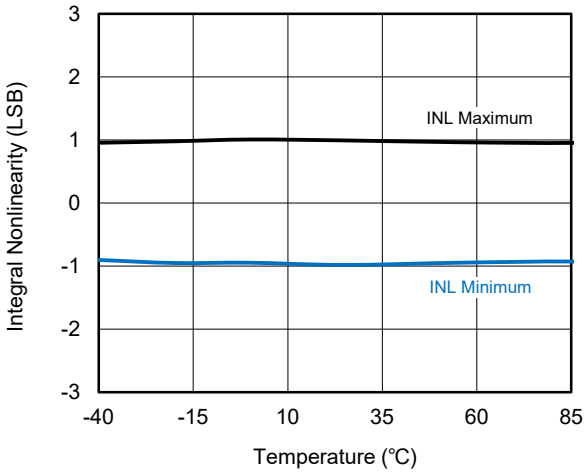


DNL vs. Temperature

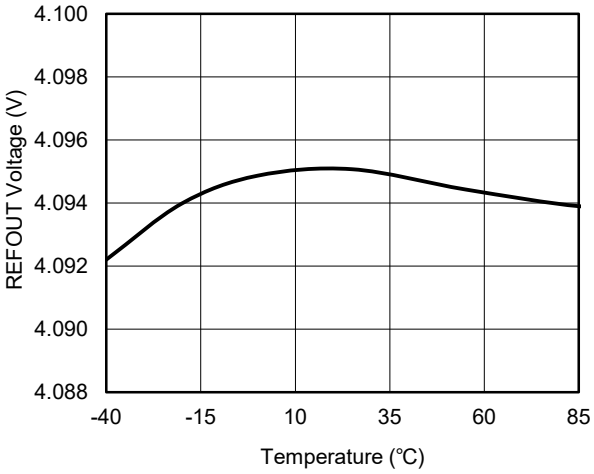


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

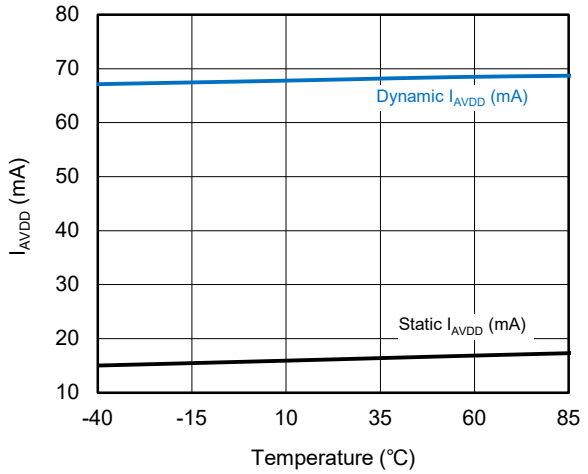
INL vs. Temperature



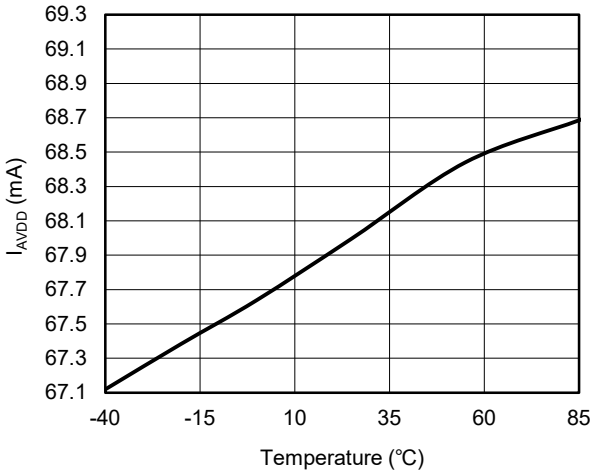
REFOUT Voltage (V_{REFOUT}) vs. Temperature



AVDD Current vs. Temperature



AVDD Current vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

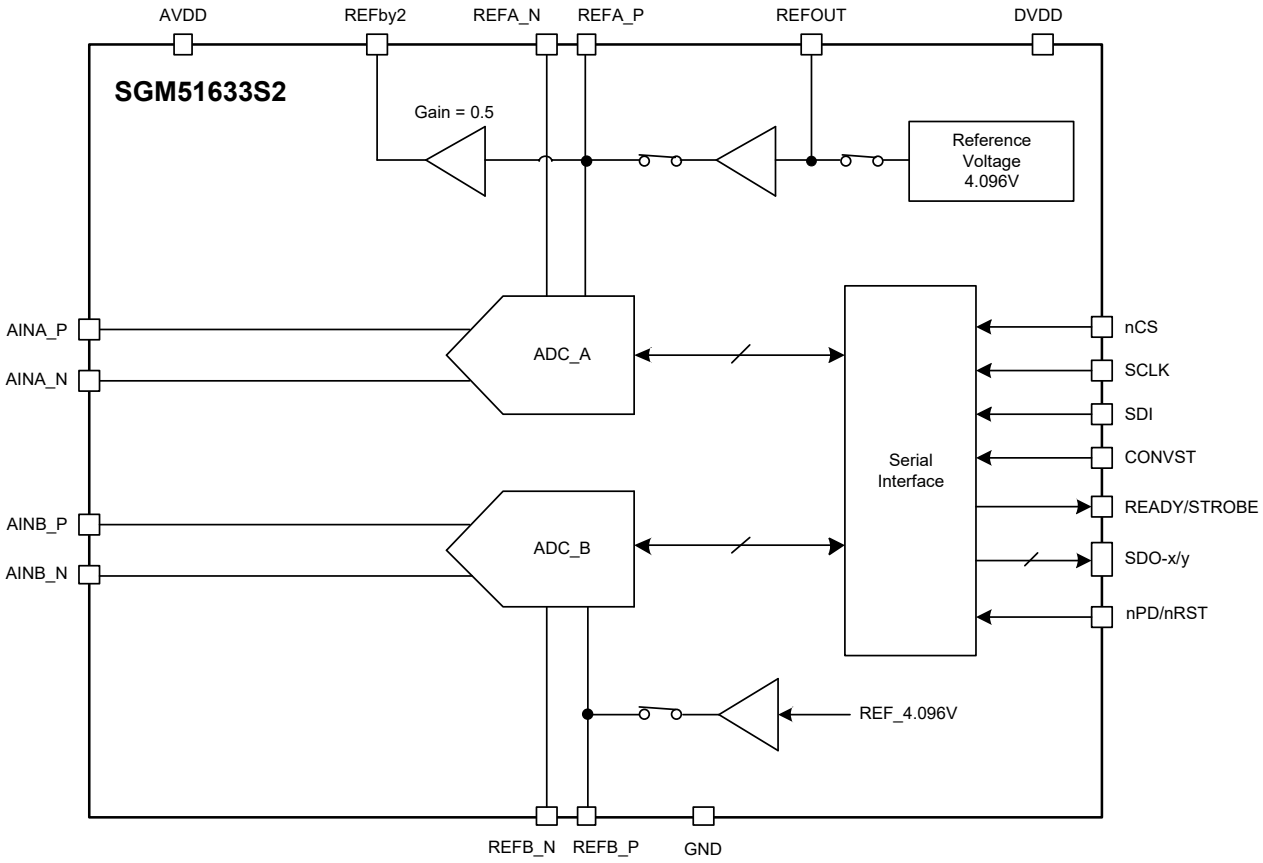


Figure 7. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM51633S2 is a 16-bit simultaneous-sampling, dual SAR ADC. The internal reference and reference buffers are integrated in this part to provide reference voltage for ADCs. 2 × V_{REFx_P} full-scale range of differential input signal is supported by this part.

The flexible digital interfaces provide easy connections with a variety of microcontrollers (MCU), digital signal processors (DSP), and field-programmable gate arrays (FPGAs). The enhanced serial programming interface not only supports higher throughput, but also it is backward-compatible with traditional SPI protocols to give more option for backend processor selections. The specified feature configurable SPI interface simplifies the board layout and firmware design.

In order to reduce the clock rate for the data interface, the parallel mode and wide cycle read mode are supported by this part, also the double data rate mode is supported by this part, which is compatible with legacy SPI. As case of digital isolators is implied, the clock re-timer (CRT) can be used to ensure the signal integrity.

Reference

Internal Reference Voltage

The internal voltage reference, 4.096V nominal output, is integrated in the SGM51633S2. To ensure the high quality of the internal reference, one 1μF decoupling capacitor is required on REFOUT pin to GND, which should be placed as close as possible to the REFOUT pin. See the reference and reference buffer diagram in Figure 8.

Reference Buffers

There is an integrated gain buffer to adjust the reference output voltage, the buffered reference output is connected with REFx_P pin. The reference output voltage is calculated by V_{REFx_P} = G_{REFBUF} × V_{REFOUT}. Decoupling capacitor is required on REFx_P pin to REFx_N, which should be placed as close as possible to the REFx_P pin on the board level layout.

REF by2 Buffer

There is an integrated 1/2 gain buffer to set the reference output voltage on REFby2 pin. This buffered REFby2 output can be used to drive the common mode voltage which is required by the fully differential amplifier (FDA) for input signal conditioning. Decoupling capacitor is required on REFby2 pin to GND, which should be placed as close as possible to the REFx_P pin on the board level layout. The REFby2 output voltage level can be adjusted by EN_REFBY2_OFFSET register to increase 100mV, see details in the Register Maps section. The REF by2 buffer diagram is shown in Figure 9.

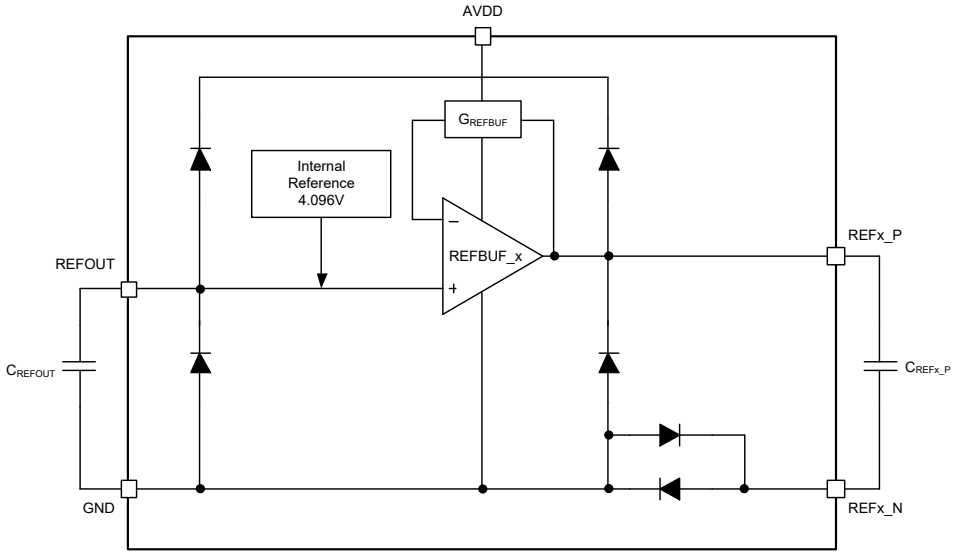


Figure 8. Reference and Reference Buffers Diagram

DETAILED DESCRIPTION (continued)

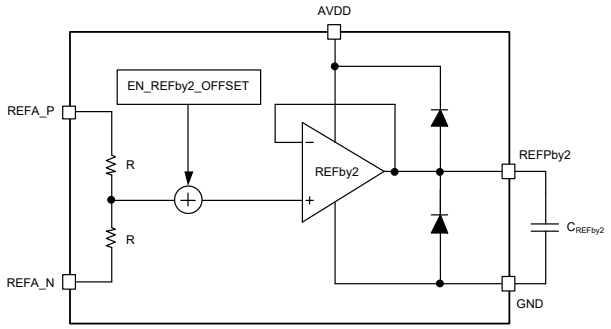


Figure 9. REF by2 Buffer

Data Averaging

The SGM51633S2 features to average two or four samples and provides the averaged value as output data. The data averaging mode can be configured by the DATA_AVG_CFG register.

Averaging of Two Samples

Setting the EN_DATA_AVG[1:0] bits in the DATA_AVG_CFG register to 10 to enable averaging of two samples, by this mode, the device averages two samples and provides the average of two samples as output data. The output data rate reduces to half.

Figure 10 provides the timing diagram for the averaging of two samples.

Averaging of Four Samples

Setting the EN_DATA_AVG[1:0] bits in the DATA_AVG_CFG register to 11 to enable averaging of four samples, by this mode, the device averages four samples and provides the average of four samples as output data. The output data rate reduces to 1/4.

Figure 11 provides the timing diagram for the averaging of four samples.

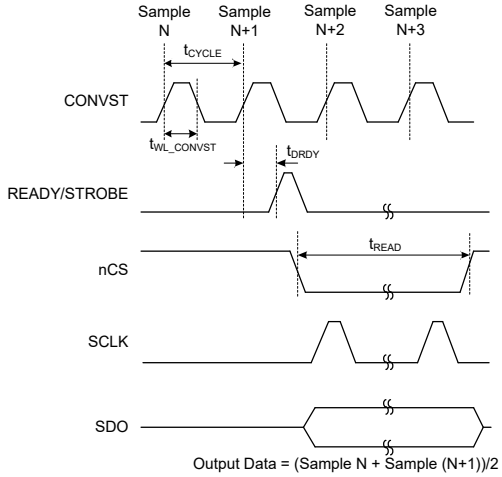


Figure 10. Timing Diagram for Averaging of Two Samples

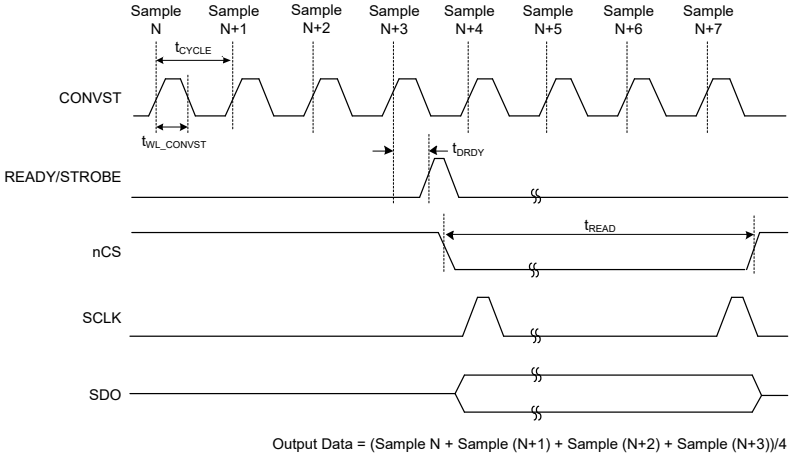


Figure 11. Timing Diagram for Averaging of Four Samples

DETAILED DESCRIPTION (continued)

Device Functional States

The SGM51633S2 supports three functional states as: RST or power-down, ACQ, and CNV. The state machine is controlled by the host controller through nPD/nRST and CONVST signals.

ACQ State

The ACQ state is the state of acquiring the analog input. At power-up, the part enters the ACQ state, and quits the ACQ state at power-down, or by the control signal of reset and ADCST. The part will enter CNV state from ACQ state on the rising edge of CONVST signal. Also the part will enter the RST state on the falling edge of nPD/nRST signal.

CNV State

During the CNV state, the analog input signal is converted to the digital data. On the rising edge of CONVST signal, the part enters the CNV state, and starts to convert the analog input. The minimum time of t_{CYCLE} between two subsequent starts of conversions is required to ensure the conversion is correctly processed.

Reset or Power-Down State

The part entering reset or power-down state is toggled by the low duration of nPD/nRST pulse signal, which is asynchronous signal. nPD/nRST timing is shown in Figure 12. SPI-00-S is the default protocol for configuring registers for the part after reset or power-up.

Reset

After reset, all of the registers are reset to the default value (see details in the Register Maps section), and all the internal processes are killed. The reset timing requirement of t_{WL_RST} is shown in the Timing Requirements table.

Power-Down

The power-down timing requirement of t_{WL_PD} is shown in the Timing Requirements table. When powering up the part from the power-down state by pulling nPD high, there is t_{PD_WKUP} delay between the rising edge of nPD and entering the ACQ state.

Conversion Control and Data Transfer

The SGM51633S2 supports two modes of conversion control and data transfer: one with zero cycle latency (mode_1 transfer) and another with a wide read cycle (mode_2 transfer).

Conversion Control and Data Transfer Frame with Zero Cycle Latency (Mode_1 Transfer)

In the sampling duration from Sample N to Sample N+1 by mode_1 transfer, the SGM51633S2 starts to convert the analog input signal from the rising edge of the CONVST, the duration of CONVST high pulse should meet the minimum t_{WH_CONVST} timing requirement (see details in the Timing Requirements table). The host controller should insert the nCS after reading out the rising edge of READY/STROBE signal, which indicates the converted data is ready for reading out (see the timing diagram in Figure 13). Command for conversion control and reading conversion results are set by SDI pin low (NOP0) or high (NOP1). After all bits on SDO are transferred completely, puling the nCS high, then next conversion can be launched by pulling the CONVST high.

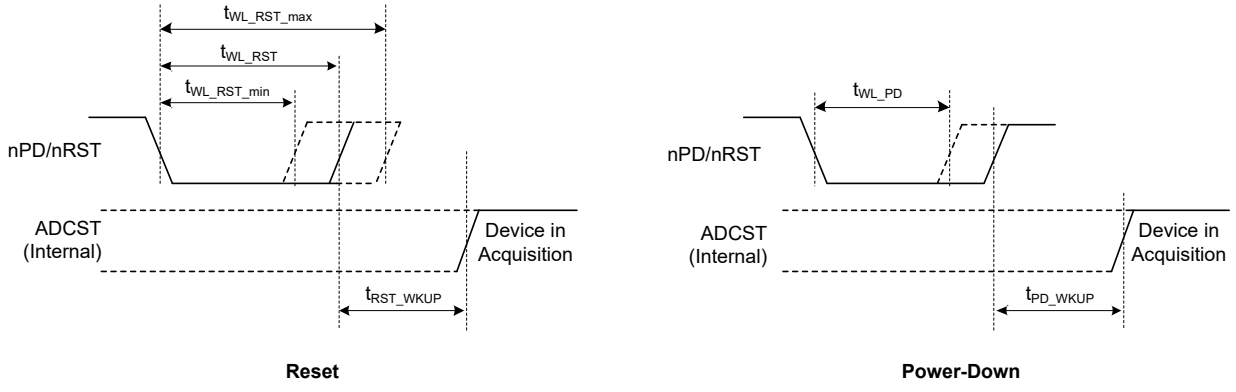
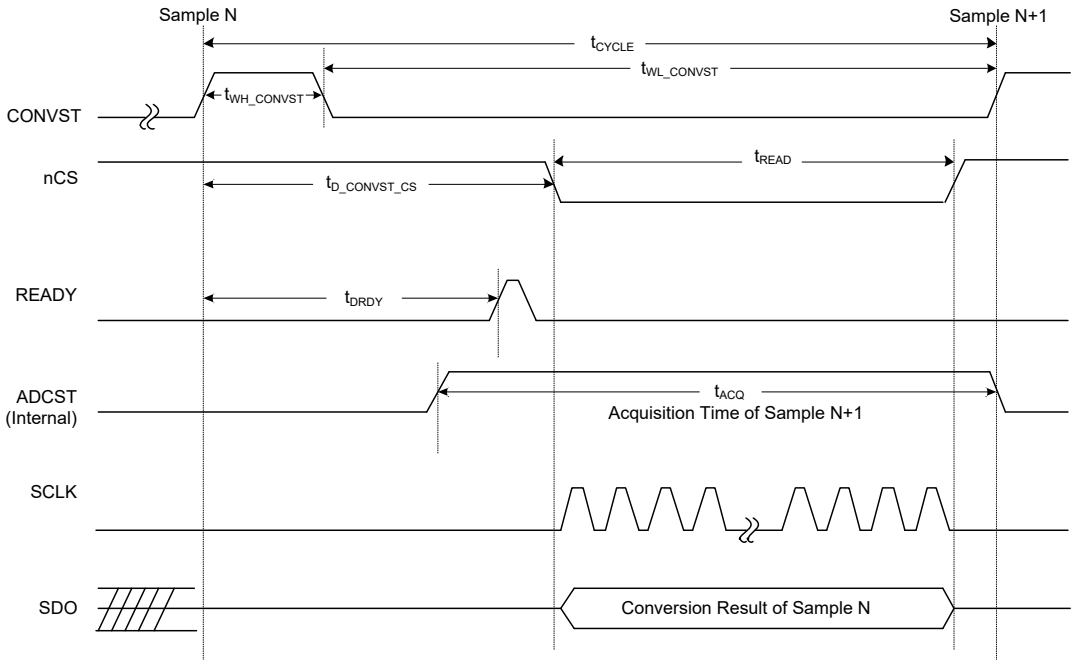


Figure 12. Reset or Power-Down

DETAILED DESCRIPTION (continued)



NOTES:

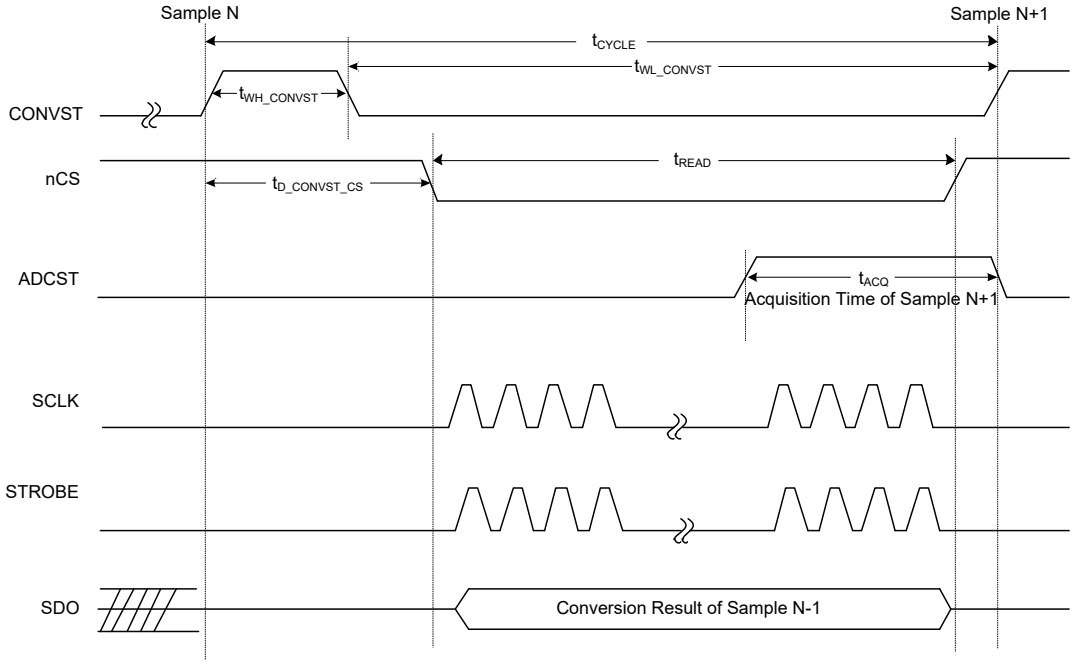
1. The READY output is required for mode_1 transfer.
2. The STROBE output is only required for clock re-timer (CRT) selected.
3. $f_{SAMPLE} = 1/t_{CYCLE}$.

Figure 13. Conversion Control and Data Transfer Frame with Zero Cycle Latency (Mode_1 Transfer)

DETAILED DESCRIPTION (continued)

Conversion Control and Data Transfer Frame with Wide Read Cycle (Mode_2 Transfer)

In the sampling duration from Sample N to Sample N+1 by mode_2 transfer, the SGM51633S2 starts to convert the analog input signal from the rising edge of the CONVST, the duration of CONVST high pulse should meet the minimum t_{WH_CONVST} timing requirement (see details in the Timing Requirements table.). The host controller should insert the nCS after a time of $t_{D\_CONVST\_CS}$, with the minimum value of $t_{D\_CONVST\_CS}$ setting, the host controller can get the maxima reading data time. After the nCS is inserted，the Sample N-1 (the previous sample) data is transferred through SDO line (see the timing diagram in Figure 14). Command for conversion control and reading conversion results are set by SDI pin low (NOP0) or high (NOP1). After all bits on SDO are transferred completely, puling the nCS high, then next conversion can be launched by pulling the CONVST high.



NOTE: STROBE output is only for clock re-timer protocols. More details please refer to the STROBE section.

NOTES:

1. The READY output is not required for mode_1 transfer.
2. The STROBE output is only required for clock re-timer (CRT) selected.
3. $f_{SAMPLE} = 1/t_{CYCLE}$.

Figure 14. Conversion Control and Data Transfer Frame with Wide Read Cycle (Mode_2 Transfer)

DETAILED DESCRIPTION (continued)

READY/STROBE

The READY/STROBE pin is defined for multiple functions. There is a mux to select READY and STROBE as output signals by nCS signal: nCS high (READY output), and nCS low (STROBE output).

READY

The READY signal is toggled to high by the rising edge of nPD/nRST, it will go low after 0.9ms. That indicates the part is well initialized, then the registers can be configured. Follow the t_{PD_WKUP} requirement to perform the conversion control. For mode_1 transfer, the READY signal goes high after the conversion process completes. After the host inserts nCS low, the READY signal goes low (see Figure 13). For mode_2 transfer, the READY signal is not required, and it can be masked by register setting.

STROBE

As the CRT protocols are selected, the synchronous clock for SDO data is sent out through STROBE line, on the other hand, the STROBE signal holds low in non-CRT protocols. In CRT protocols, the data is synchronized with the rising edge of STROBE.

Data Interface

Output Data Word Format

The two's compliment format data (by MSB first) is transferred through the data lines.

Sampled Data Transfer Protocols

In order to reduce the digital interface clock rate, there are three options provided for the host controller in this part. The first option, by mode_2 transfer, the data transfer window is extended. The second option, by DDR (double data rate) mode, the data rate is doubled by using both clock edges to latch the data. The third option, more data lines are used (dual SDO, quad SDO, or parallel mode). All of those options can be combined together to reduce the data clock rate.

Reading Protocols from Device

The SGM51633S2 supports five categories of protocol for the data-read operation, as shown in Table 2.

Table 1. Output Data Word format

Device	Resolution of Device (R)	Width of Output Data Word (N)	Content of Output Data Word
SGM51633S2	16	16	16-bit conversion in two's compliment format (MSB first)

Table 2. Protocol for the Data-Read Operation

Item	Protocols	Descriptions
1	xy-S-SDR	Legacy SPI-compatible protocol.
2	xy-D-SDR	Dual\Quad data line options by single data rate.
	xy-Q-SDR	
3	x1-S-DDR	Single\Dual\Quad data line options by double data rate.
	x1-D-DDR	
	x1-Q-DDR	
4	CRT-S-SDR	CRT (clock re-timer) protocols with different options.
	CRT-D-SDR	
	CRT-Q-SDR	
	CRT-S-DDR	
	CRT-D-DDR	
	CRT-Q-DDR	
5	PB-xy-AB-SDR	Parallel protocols with single data rate.
	PB-xy-AA-SDR	

DETAILED DESCRIPTION (continued)

xy-S-SDR: Legacy SPI-Compatible Protocols

In those transfer protocols, the ADC_A data is on SDO-0A, and ADC_B data is on SDO-0B. See the details of protocol description in Table 3. The 00-S-SDR protocol is the default protocol for reading data from the part after the part is reset.

Figure 15 and Figure 16 show the timing diagrams for the 00-S-SDR, 10-S-SDR and 01-S-SDR, 11-S-SDR protocols, respectively.

Table 3. xy-S-SDR Protocols for Reading from Device

Protocol (1)	SCLK Polarity (CPOL (2))	SCLK Phase (CPHA (2)) (3)	MSB Launch Edge	Bus Width	t_{READ} (4)	Timing Diagram
00-S-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	nCS falling	1	[15.5 × t_{CLK} + k]	Figure 15
01-S-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	1	[15.5 × t_{CLK} + k]	Figure 16
10-S-SDR	High (CPOL = 1)	Falling (CPHA = 0)	nCS falling	1	[15.5 × t_{CLK} + k]	Figure 15
11-S-SDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	1	[15.5 × t_{CLK} + k]	Figure 16

NOTES:

1. The xy-S-SDR protocol can be set in the PROTOCOL_CFG register.
2. The SCLK polarity and phase can be set in the PROTOCOL_CFG register.
3. With SCLK ≥ 30MHz, it recommends data capture on the launch edge for the next bit.
4. t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

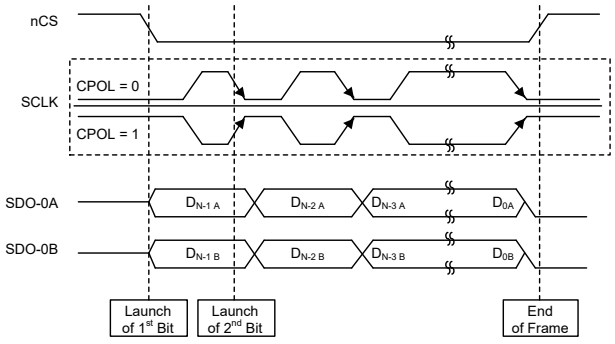


Figure 15. 00-S-SDR and 10-S-SDR Protocols

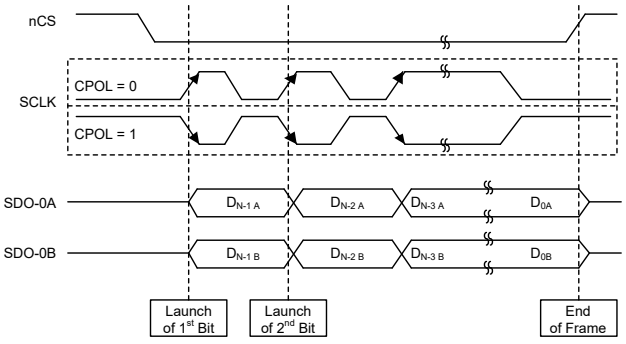


Figure 16. 01-S-SDR and 11-S-SDR Protocols

DETAILED DESCRIPTION (continued)

xy-D-SDR and xy-Q-SDR: SPI-Compatible Protocols with Bus Width Options and Single Data Rate

See the details of protocol description in Table 4. In those data transfer protocols, the SDOs are set to tri-state when they are not enabled by the BUS_WIDTH register. Compared with the single SDO mode, those 2 SDOs and 4 SDOs modes are significantly reduced the data reading time.

Figure 17 and Figure 18 show the timing diagrams for the 00-D-SDR and 10-D-SDR, 01-D-SDR and 11-D-SDR protocols, respectively. Figure 19 and Figure 20 show the timing diagrams for the 00-Q-SDR and 10-Q-SDR, 01-Q-SDR and 11-Q-SDR protocols, respectively.

Table 4. xy-D-SDR and xy-Q-SDR Protocols for Reading from Device

Protocol (1)	SCLK Polarity (CPOL) (2)	SCLK Phase (CPHA) (3)	MSB Launch Edge	Bus Width	t_{READ} (4)	Timing Diagram
00-D-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	nCS falling	2	[7.5 × t_{CLK} + k]	Figure 17
01-D-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	2	[7.5 × t_{CLK} + k]	Figure 18
10-D-SDR	High (CPOL = 1)	Falling (CPHA = 0)	nCS falling	2	[7.5 × t_{CLK} + k]	Figure 17
11-D-SDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	2	[7.5 × t_{CLK} + k]	Figure 18
00-Q-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	nCS falling	4	[3.5 × t_{CLK} + k]	Figure 19
01-Q-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	4	[3.5 × t_{CLK} + k]	Figure 20
10-Q-SDR	High (CPOL = 1)	Falling (CPHA = 0)	nCS falling	4	[3.5 × t_{CLK} + k]	Figure 19
11-Q-SDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	4	[3.5 × t_{CLK} + k]	Figure 20

NOTES:

1. The xy-D-SDR and xy-Q-SDR protocols can be set in the PROTOCOL_CFG register.
2. The SCLK polarity and phase can be set in the PROTOCOL_CFG register.
3. With SCLK ≥ 30MHz, it recommends data capture on the launch edge for the next bit.
4. t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

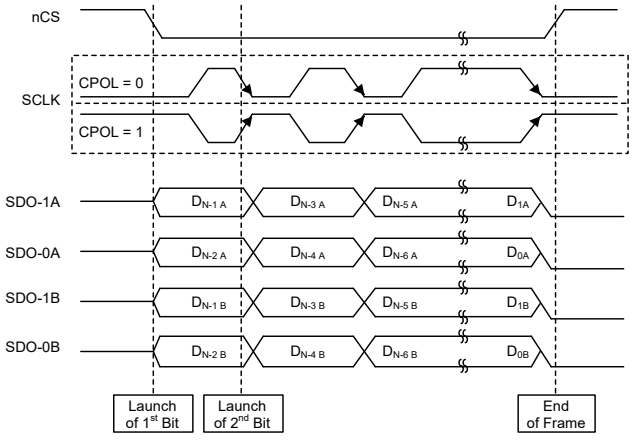


Figure 17. 00-D-SDR and 10-D-SDR Protocols

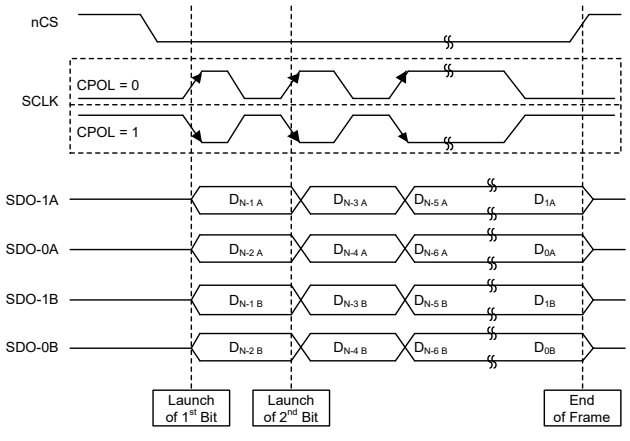


Figure 18. 01-D-SDR and 11-D-SDR Protocols

DETAILED DESCRIPTION (continued)

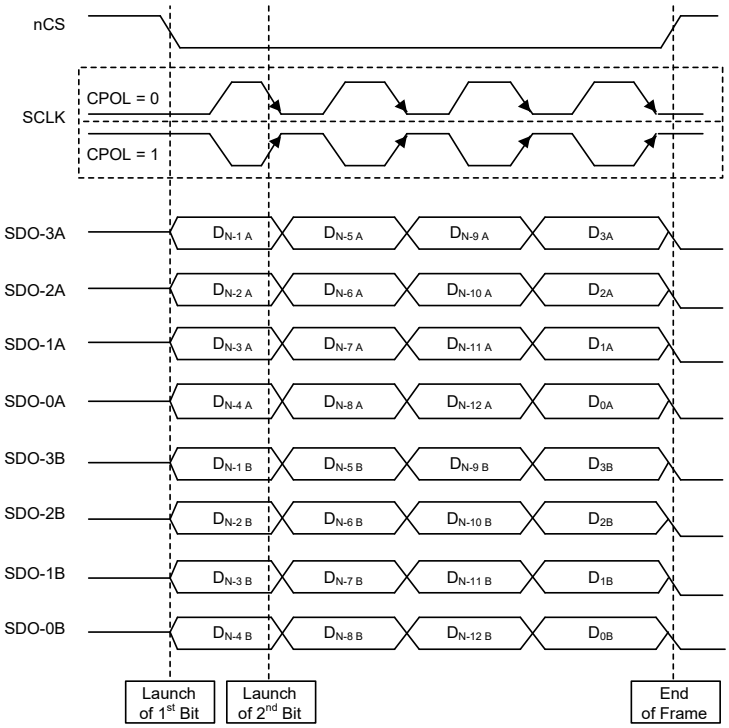


Figure 19. 00-Q-SDR and 10-Q-SDR Protocols

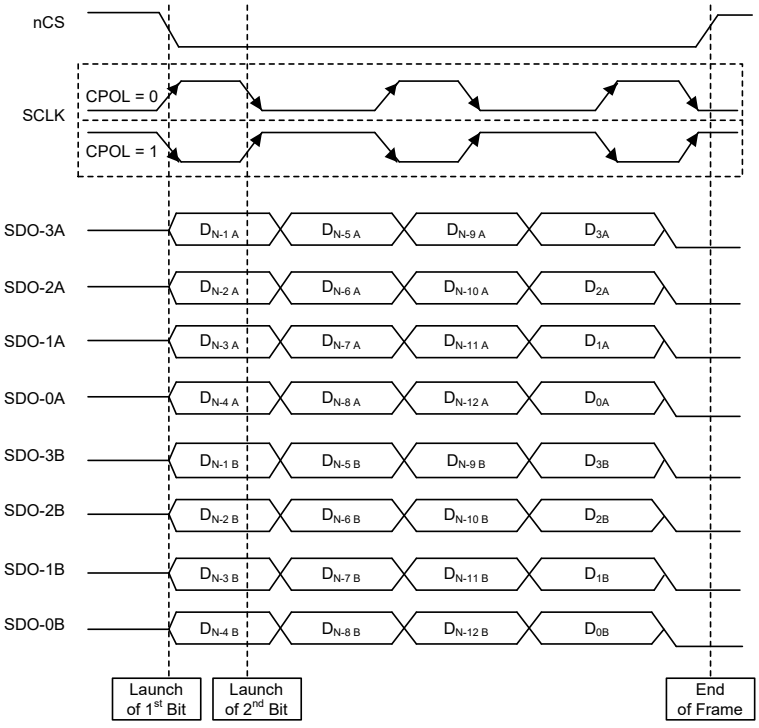


Figure 20. 01-Q-SDR and 11-Q-SDR Protocols

DETAILED DESCRIPTION (continued)

x1-S-DDR, x1-D-DDR, x1-Q-DDR: SPI-Compatible Protocols with Bus Width Options and Double Data Rate

See the details of protocol description in Table 5. In those data transfer protocols, the SDOs are set to tri-state when they are not enabled by the BUS_WIDTH register. Compared with the SDR modes, the DDR modes double the data rate by the same clock rate with SDR mode, meantime the data reading time can be further reduced with increasing the data bus width.

Figure 21, Figure 22, and Figure 23 illustrate timing diagrams for the 01-S-DDR and 11-S-DDR, 01-D-DDR and 11-D-DDR, and 01-Q-DDR and 11-Q-DDR protocols, respectively.

Table 5. x1-S-DDR, x1-D-DDR, and x1-Q-DDR Protocols for Reading from Device

Protocol (1)	SCLK Polarity (CPOL)	SCLK Phase	MSB Launch Edge	Bus Width (2)	t_{READ} (3)	Timing Diagram
01-S-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	1	[9 × t_{CLK} + k]	Figure 21
11-S-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	1	[9 × t_{CLK} + k]	Figure 21
01-D-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	2	[5 × t_{CLK} + k]	Figure 22
11-D-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	2	[5 × t_{CLK} + k]	Figure 22
01-Q-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	4	[3 × t_{CLK} + k]	Figure 23
11-Q-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	4	[3 × t_{CLK} + k]	Figure 23

NOTES:

1. x1-S-DDR, x1-D-DDR, x1-Q-DDR protocols can be set in the PROTOCOL_CFG register.
2. For configuring the bus width, configure the BUS_WIDTH register.
3. t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

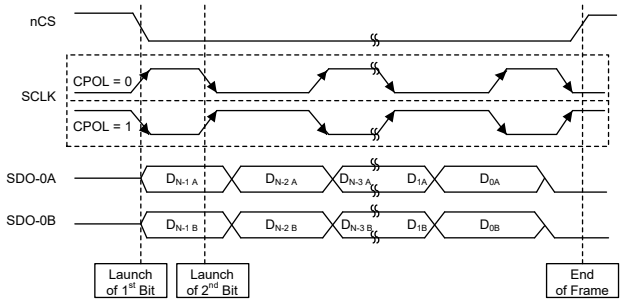


Figure 21. 01-S-DDR and 11-S-DDR Protocols

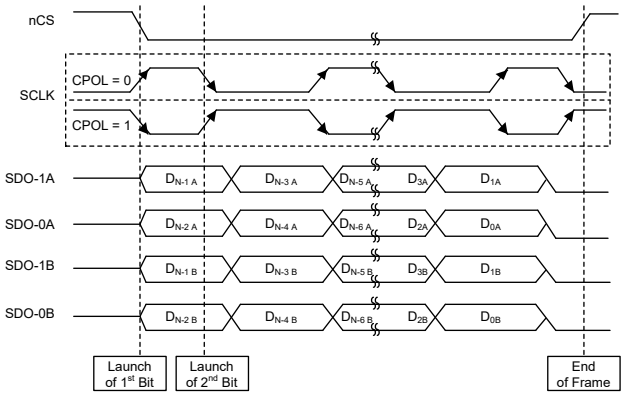


Figure 22. 01-D-DDR and 11-D-DDR Protocols

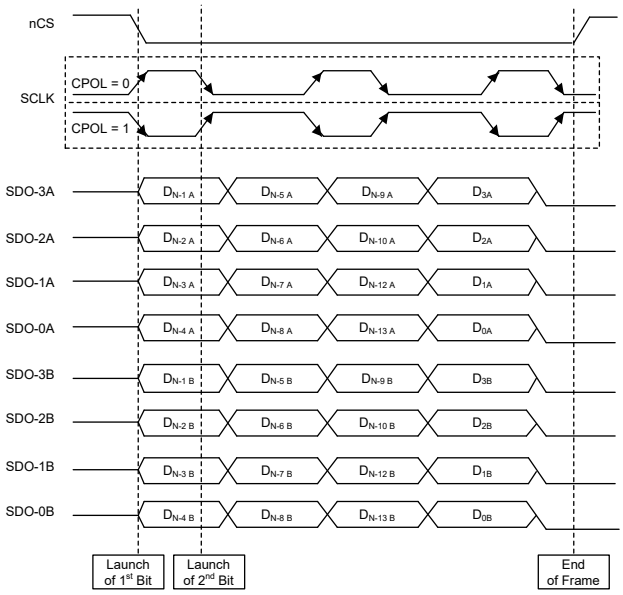


Figure 23. 01-Q-DDR and 11-Q-DDR Protocols

DETAILED DESCRIPTION (continued)

CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, CRT-Q-DDR: Clock Re-Timer (CRT) Protocols

See the details of protocol description in Table 6. In those CRT protocols, the synchronous clock is sent out through the STROBE pin by SGM51633S2. By SDR mode, the SDOs data are synchronized with the rising edge of STROBE signal, by the DDR mode, the SDOs data are synchronized with both edge of STROBE signal. The STROBE signal can be selected from internal clock or external clock by the CRT_CFG register. The SDOs are set to tri-state when they are not enabled by the BUS_WIDTH register. The data reading time can be further reduced with increasing the data bus width.

Figure 24 through Figure 29 illustrate timing diagrams for the CRT-S-SDR, CRT-S-DDR, CRT-D-SDR, CRT-D-DDR, CRT-Q-SDR, and CRT-Q-DDR protocols, respectively.

For reading data, SCLK is only required when the STROBE output is selected as SCLK (external clock). However, SCLK is always required for configuring registers.

Table 6. CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, and CRT-Q-DDR Protocols for Reading from Device

Protocol (1)	SCLK Polarity	Capture Edge	MSB Launch Edge	Bus Width (2)	t_{READ} (3)	Timing Diagram
CRT-S-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	1	[15.5 × t_{STROBE} + m]	Figure 24
CRT-D-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	2	[7.5 × t_{STROBE} + m]	Figure 26
CRT-Q-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	4	[3.5 × t_{STROBE} + m]	Figure 28
CRT-S-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	1	[7.5 × t_{STROBE} + m]	Figure 25
CRT-D-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	2	[3.5× t_{STROBE} + m]	Figure 27
CRT-Q-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	4	[1.5 × t_{STROBE} + m]	Figure 29

NOTES:

1. CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, and CRT-Q-DDR protocols can be set in the PROTOCOL_CFG register.

2. For configuring the bus width, configure the BUS_WIDTH register.

3. t_{READ} is the read time for reading the 16-bit output data word. For an external clock, m = (t_{SU_CSCK} + t_{HT_CKCS}), and for an internal clock, m = $t_{D\_CS\_STROBE}$.

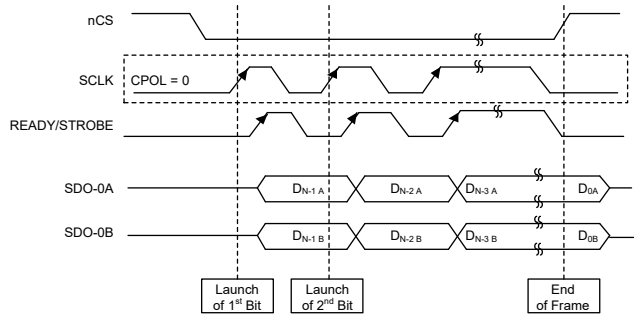


Figure 24. CRT-S-SDR Protocol

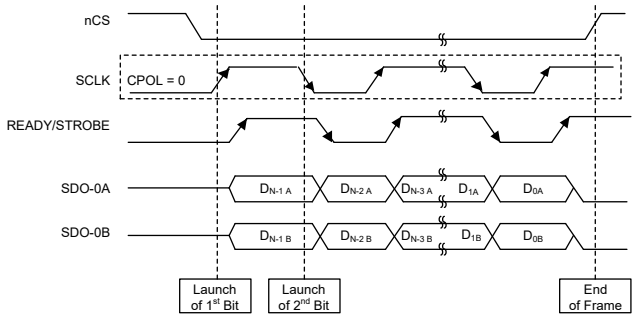


Figure 25. CRT-S-DDR Protocol

DETAILED DESCRIPTION (continued)

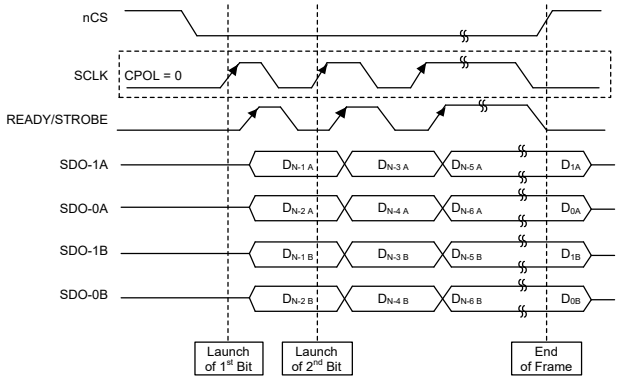


Figure 26. CRT-D-SDR Protocol

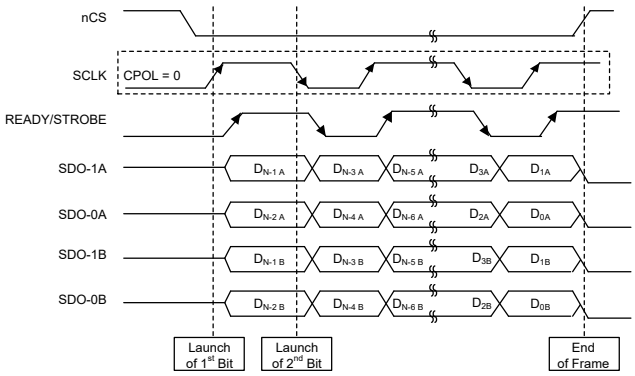


Figure 27. CRT-D-DDR Protocol

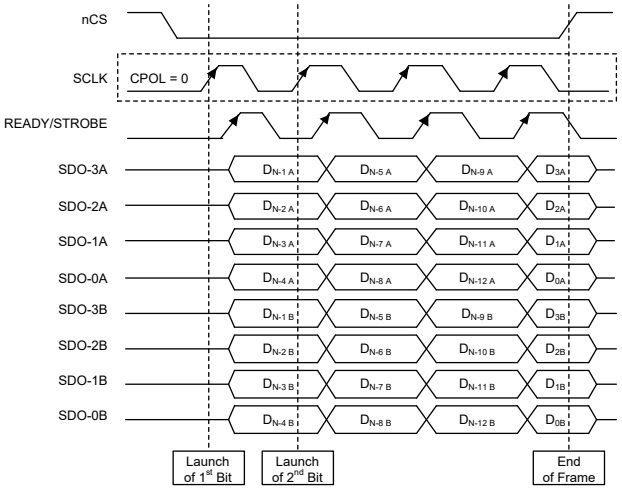


Figure 28. CRT-Q-SDR Protocol

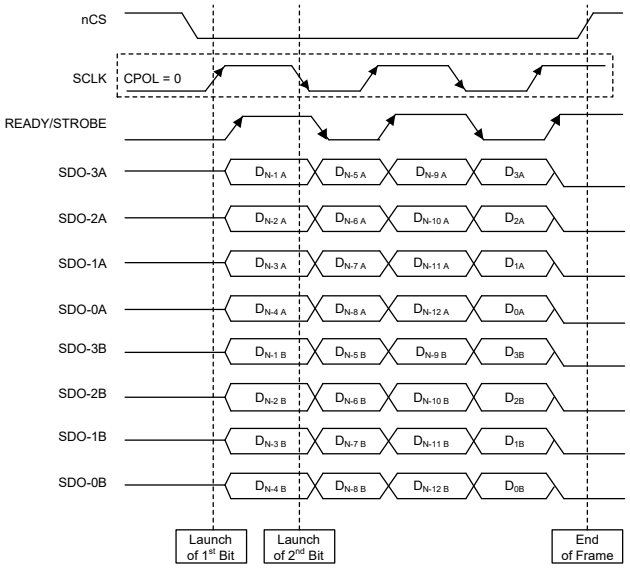


Figure 29. CRT-Q-DDR Protocol

DETAILED DESCRIPTION (continued)

PB-xy-AB-SDR, PB-xy-AA-SDR: Parallel Byte Protocols

See the details of protocol description in Table 7. In those data transfer protocols, the byte format data is sent out through the eight SDO lines from SGM51633S2. The byte data format can be configured by the OUTPUT_DATA_WORD_CFG register.

Figure 30 and Figure 31 illustrate the timing diagrams for the PB-00-AB-SDR and PB-10-AB-SDR, PB-01-AB-SDR and PB-11-AB-SDR protocols, respectively. Figure 32 and Figure 33 illustrate the timing diagrams for the PB-00-AA-SDR and PB-10-AA-SDR, PB-01-AA-SDR and PB-11-AA-SDR protocols, respectively.

Table 7. PB-xy-AB-SDR, PB-xy-AA-SDR Protocols for Reading Data

Protocol (1)	SCLK Polarity (CPOL)	SCLK Phase (CPHA)	MSB Launch Edge	Data Format (2)	t_{READ} (3)	Timing Diagram
PB-00-AB-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	nCS falling	AB	[3.5 × t_{CLK} + k]	Figure 30
PB-01-AB-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	AB	[3.5 × t_{CLK} + k]	Figure 31
PB-10-AB-SDR	High (CPOL = 1)	Falling (CPHA = 1)	nCS falling	AB	[3.5 × t_{CLK} + k]	Figure 30
PB-11-AB-SDR	High (CPOL = 1)	Rising (CPHA = 0)	1st SCLK falling	AB	[3.5 × t_{CLK} + k]	Figure 31
PB-00-AA-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	nCS falling	AA	[3.5 × t_{CLK} + k]	Figure 32
PB-01-AA-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	AA	[3.5 × t_{CLK} + k]	Figure 33
PB-10-AA-SDR	High (CPOL = 1)	Falling (CPHA = 1)	nCS falling	AA	[3.5 × t_{CLK} + k]	Figure 32
PB-11-AA-SDR	High (CPOL = 1)	Rising (CPHA = 0)	1st SCLK falling	AA	[3.5 × t_{CLK} + k]	Figure 33

NOTES:

1. Parallel byte protocols can be set by the PROTOCOL_CFG register.
2. The data format for parallel byte protocols can be set by the OUTPUT_DATA_WORD_CFG register.
3. t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

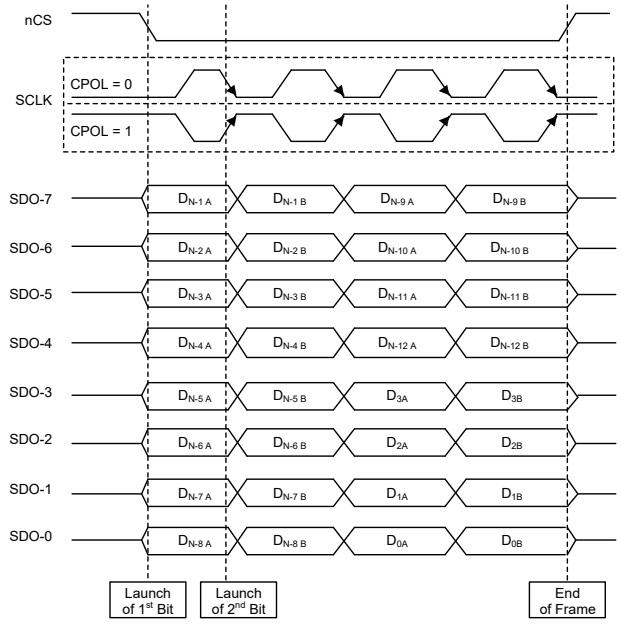


Figure 30. PB-00-AB-SDR and PB-10-AB-SDR Protocols

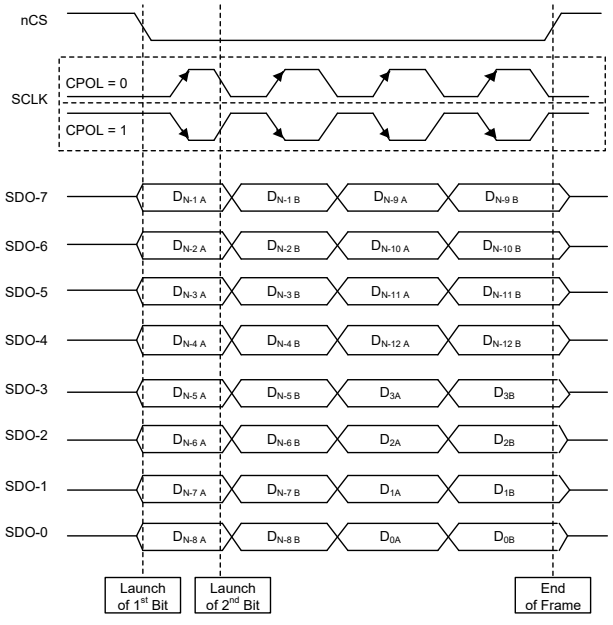


Figure 31. PB-01-AB-SDR and PB-11-AB-SDR Protocols

DETAILED DESCRIPTION (continued)

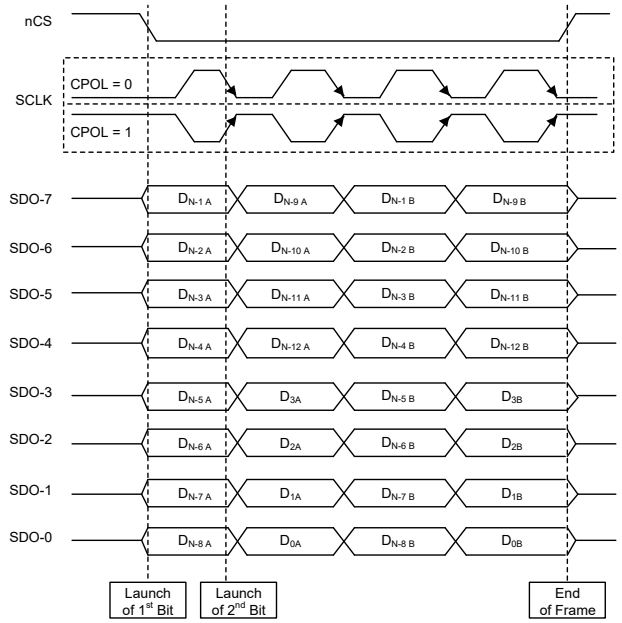


Figure 32. PB-00-AA-SDR and PB-10-AA-SDR Protocols

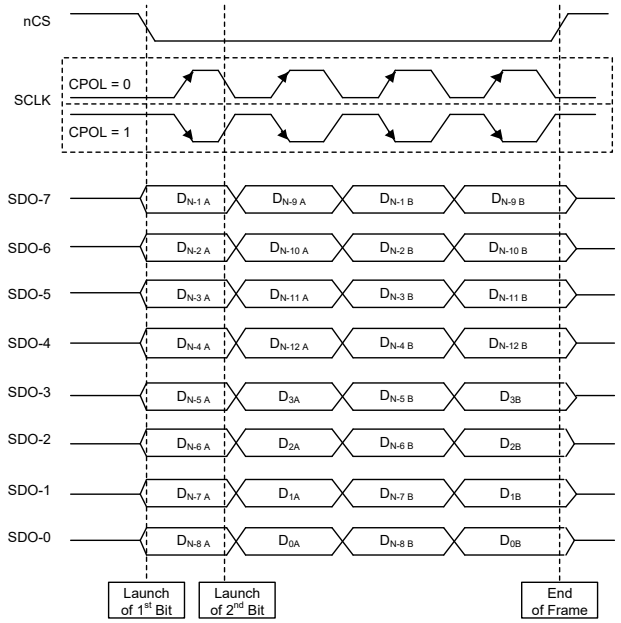


Figure 33. PB-01-AA-SDR and PB-11-AA-SDR Protocols

Device Setup

The SGM51633S2 supports multiple operation modes by the enhanced digital interface configuration. With different application requirement, different optimized hardware connection topology can be selected.

Single Device: All Enhanced-SPI Options

Connection topology in Figure 34 can support all of the enhanced-SPI options.

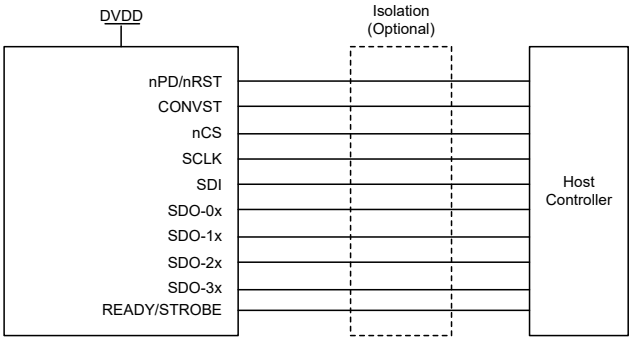


Figure 34. Enhanced-SPI Digital Interface, All Pins

Single Device: Minimum Pins for a Standard SPI Interface

Figure 35 shows the minimum-pin interface for applications using a standard SPI protocol.

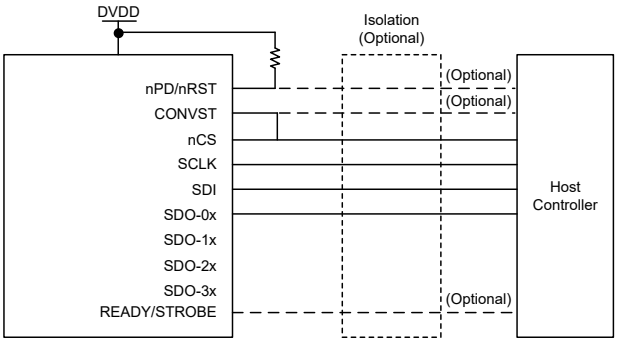


Figure 35. SPI Interface, Minimum Pins

The standard SPI interfaces, including wires of nCS/SCLK/SDI/SDO-0x, builds up the minimum-pin connection system for the compacted application. On the other hand, with employing the optional independent connection of the Isolation/(nPD/nRST)/CONVST/(READY/STROBE), more flexible features can be supported based on the minimum-pin connection system, see details on the corresponding pin description.

DETAILED DESCRIPTION (continued)

Protocols for Configuring the Device by Registers

The SGM51633S2 supports an SPI protocol for writing into the device with all combinations of clock polarity and phase. The SPI-00-S is the default protocol for configuring the device after the part reset. There are different protocols for configuring the part are listed in Table 8.

Figure 36 and Figure 37 show the timing diagrams for the SPI-00-S, SPI-10-S and SPI-01-S, SPI-11-S protocols, respectively, for configuring the device.

Table 8. SPI Protocols for Configuring the Device

Protocol	SCLK Polarity (CPOL) (1)	SCLK Phase (CPHA) (1)	MSB Capture Edge	t_{WRITE} (2)	Timing Diagram
SPI-00-S	Low (CPOL= 0)	Rising (CPHA = 0)	1st SCLK rising	[15.5 × t_{CLK} + k]	Figure 36
SPI-01-S	Low (CPOL= 0)	Falling (CPHA = 1)	1st SCLK falling	[15.5 × t_{CLK} + k]	Figure 37
SPI-10-S	High (CPOL= 1)	Falling (CPHA = 1)	1st SCLK falling	[15.5 × t_{CLK} + k]	Figure 36
SPI-11-S	High (CPOL= 1)	Rising (CPHA = 0)	1st SCLK rising	[15.5 × t_{CLK} + k]	Figure 37

NOTES:

1. Configure the SPI_CPOL and SPI_CPHA bits in the PROTOCOL_CFG register for the desired CPOL and CPHA.

2. t_{WRITE} is the write time for writing the 16-bit data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

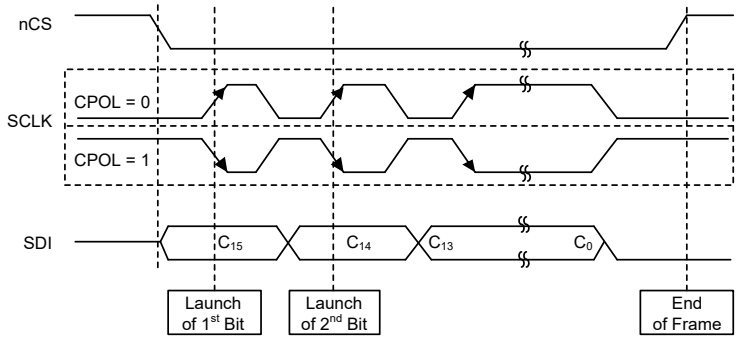


Figure 36. SPI-00-S and SPI-10-S Protocols for Configuring the Device

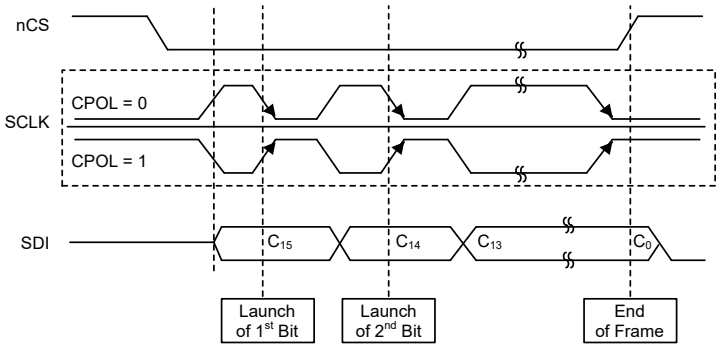


Figure 37. SPI-01-S and SPI-11-S Protocols for Configuring the Device

DETAILED DESCRIPTION (continued)

Reading and Writing Registers Command

The command frame is shown in Figure 38. The host controller provides 16-bit command C[15:0] through SDI pin to write or read the registers in the part. See the details of commands description in Table 9.

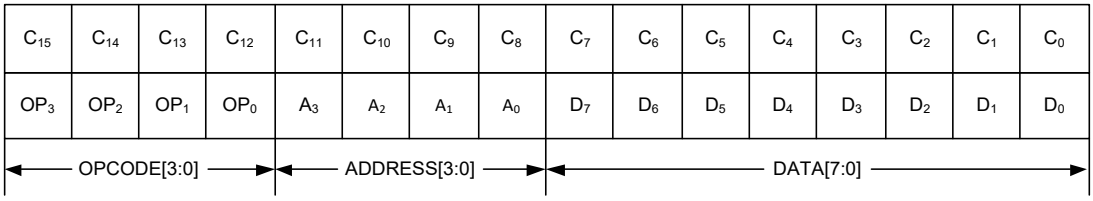


Figure 38. Command Frame C[15:0]

Table 9. Commands for Reading and Writing Registers

OPCODE[3:0]		DESCRIPTION	ADDRESS[3:0]	DATA[7:0]
0000	NOP0	Command for conversion control and reading conversion results.	N/A	N/A
0001	WRITE	Command for writing registers.	4-Bit Register Address	8-bit register data
0010	READ (1)	Command for reading registers.	4-Bit Register Address	00h or FFh
0101	Set Bit	Command for setting the specific bits in a register without changing the other bits.	4-Bit Register Address	Bits with values of 1 in DATA are set and bits with values of 0 in register data are not changed.
0110	Clear Bit	Command for clearing the specific bits in a register without changing the other bits.	4-Bit Register Address	Bits with values of 1 in DATA are cleared and bits with values of 0 in register data are not changed.
1111	NOP1	Command for conversion control and reading conversion results.	N/A	N/A
Remaining Combinations	xxxxxxxxx	xxxxxxxxx	Reserved	These commands are reserved and are treated by device as no operation. Reserved commands, no operation supported.

NOTE:

1. The register data of the READ command is provided by device in the next frame.

REGISTER MAPS

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

Table 10. Register Maps

Address	Register Name	Details	Default
0x00	DEVICE_STATUS	Device Status Register	00h
0x01	POWER_DOWN_CFG	Power-Down Configuration Register	00h
0x02	PROTOCOL_CFG	Protocol Configuration Register	00h
0x03	BUS_WIDTH	Bus Width Configuration Register	00h
0x04	CRT_CFG	Clock Re-Timer Configuration Register	00h
0x05	OUTPUT_DATA_WORD_CFG	Output Data Word Configuration Register	00h
0x06	DATA_AVG_CFG	Data Averaging Configuration Register	00h
0x07	REFBY2_OFFSET	REFby2 Offset Selection Register	00h

REG0x00: DEVICE_STATUS Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	0 0000	R	Reserved. Do not write to these bits. Read returns 0 0000.
D[2]	ZONE2_TRANSFER	0	R/W	The bit is configured when the device operates in mode_2 transfer mode with a wide read cycle. This is a sticky bit. Write 1 to the bit to clear.
D[1]	AVG_ERROR	0	R/W	The bit is configured when the device receives a falling edge of nCS before the current averaging operation is completed. This is a sticky bit. Write 1 to the bit to clear.
D[0]	Reserved	0	R	Reserved. Do not write to this bit. Read returns 0.

REG0x01: POWER_DOWN_CFG Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved.
D[6]	PD_REFBUF_B	0	R/W	Power Down REFBUF_B 0 = REFBUF_B is not powered down (default) 1 = REFBUF_B is powered down
D[5]	PD_REFBY2	0	R/W	Power Down REFby2 Output 0 = REFby2 is not powered down (default) 1 = REFby2 is powered down
D[4]	PD_REFBUF_A	0	R/W	Power Down REFBUF_A 0 = REFBUF_A is not powered down (default) 1 = REFBUF_A is powered down
D[3]	PD_ADCB	0	R/W	Power Down ADC_B 0 = ADC_B is not powered down (default) 1 = ADC_B is powered down
D[2]	Reserved	0	R	Reserved.
D[1]	PD_ADCA	0	R/W	Power Down ADC_A 0 = ADC_A is not powered down (default) 1 = ADC_A is powered down
D[0]	PD_REF	0	R/W	Power Down ADC's Internal Reference 0 = ADC internal reference is not powered down (default) 1 = ADC internal reference is powered down. An external reference unbuffered must be connected to pin 5 (REFOUT pin) or an external reference source for ADC_B must be connected to pin 10 and pin 9 (REFB_P and REFB_N pins). An external reference source for ADC_A must be connected to pin 31 and pin 32 (REFA_P and REFA_N pins)

REGISTER MAPS (continued)

REG0x02: PROTOCOL_CFG Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved. Do not write to this bit. Read returns 0.
D[6:4]	SDO_PROTOCOL[2:0]	000	R/W	Set the Protocol for Reading Data from Device 000 = Legacy, SPI-compatible protocols (xy-S-SDR). SPI-compatible protocols with bus width options and SDR (xy-D-SDR and xy-Q-SDR) protocols (default) 001 = SPI-compatible protocols with bus width options and DDR (x1-S-DDR, x1-D-DDR, x1-Q-DDR) protocols 010 = Clock re-timer (CRT) protocols with SDR (CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR) 011 = CRT protocols with DDR (CRT-S-DDR, CRT-D-DDR, CRT-Q-DDR) 100 = Parallel byte protocol. Writing 1xx enables the parallel byte protocol 101 = Parallel byte protocol. Writing 1xx enables the parallel byte protocol 110 = Parallel byte protocol. Writing 1xx enables the parallel byte protocol 111 = Parallel byte protocol. Writing 1xx enables the parallel byte protocol
D[3:2]	Reserved	00	R	Reserved. Do not write to these bits. Read returns 00.
D[1]	SPI_CPOL	0	R/W	Set the Clock Polarity for Reading Data from Device and Writing Data into the Device 0 = CPOL = 0 (default) 1 = CPOL = 1
D[0]	SPI_CPHA	0	R/W	Set the Clock Phase for Reading Data from Device and Writing Data into the Device 0 = CPHA = 0 (default) 1 = CPHA = 1

REG0x03: BUS_WIDTH Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00 0000	R	Reserved. Do not write to these bits. Read returns 00 0000.
D[1:0]	SDO_WIDTH[1:0]	00	R/W	Set the Number of SDO Lines for Reading Data from Device 00 = One SDO per ADC (default) 01 = One SDO per ADC 10 = Dual SDO per ADC 11 = Quad SDO per ADC If the device is configured for parallel byte protocol, then the SDO_WIDTH[1:0] bits are ignored and the device sends data over all eight SDO lines as per the parallel byte protocol.

REG0x04: CRT_CFG Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00 0000	R	Reserved. Do not write to these bits. Read returns 00 0000.
D[1:0]	CRT_CLK_SELECT[1:0]	00	R/W	Select the Clock Source for the Strobe Output for CRT Protocols 00 = Serial clock (SCLK) is used for STROBE output (default) 01 = INTCLK is used for the STROBE output 10 = INTCLK/2 is used for the STROBE output 11 = INTCLK/4 is used for the STROBE output

REGISTER MAPS (continued)

REG0x05: OUTPUT_DATA_WORD_CFG Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved. Do not write to these bits. Read returns 00.
D[5]	READY_MASK	0	R/W	Mask the READY Output 0 = Do not mask the READY output (default) 1 = Mask the READY output The STROBE output is provided in CRT protocols even if the READY_MASK bit is set to 1. It is recommended to mask the READY output for the Conversion Control and Data Transfer Frame with Wide Read Cycle (Mode_2 Transfer) section.
D[4]	PARALLEL_MODE_DATA_FORMAT	0	R/W	Select the Format for the Output Data Word in the Parallel Byte Protocol 0 = Data format AA: byte from ADC_A followed by byte from ADC_A (PB-xy-AA-zDR protocol) (default) 1 = Data format AB: byte from ADC_A followed by byte from ADC_B (PB-xy-AB-zDR protocol)
D[3:2]	Reserved	00	R	Reserved. Do not write to these bits. Read returns 00.
D[1]	FIXED_PATTERN_DATA	0	R/W	Enable a Fixed Pattern in the Output Data Word 0 = The device provides the conversion results from the register data in the output word (default) 1 = The device provides a fixed pattern (A55AA55Ah) in the output data word
D[0]	DATA_RIGHT_ALIGNED	0	R/W	Enable the Right Alignment in the Output Data Word for Device 0 = The data are left-aligned in the output data word (default) 1 = The data are right-aligned in the output data word

REG0x06: DATA_AVG_CFG Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00 0000	R	Reserved. Do not write to these bits. Read returns 00 0000.
D[1:0]	EN_DATA_AVG[1:0]	00	R/W	Enable Averaging of Conversion Results 00 = No averaging (default) 01 = No averaging 10 = Enable averaging of two conversion results 11 = Enable averaging of four conversion results

REG0x07: REFBY2_OFFSET Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	000 0000	R	Reserved. Do not write to these bits. Read returns 000 0000.
D[0]	EN_REFBY2_OFFSET	0	R/W	Enable the Offset for the REFby2 Output 0 = Disable the offset for the REFby2 output (default) 1 = Enable the offset for the REFby2 output and the REFby2 output increases by 100mV

APPLICATION INFORMATION

ADC Input Driver

The input driver circuit of SGM51633S2 is mainly composed of two parts, a driving amplifier and a charge kickback filter.

In order to buffer the signal source to drive the switched-capacitor inputs of SGM51633S2, the low output impedance amplifier should be selected, and a proper amplifier gain should be set to adjust the condition of the signal source, thereby achieving the optimized dynamic range. Place the RC filter at the input pins of ADC to filter out the charge kickback noise.

Typical Application

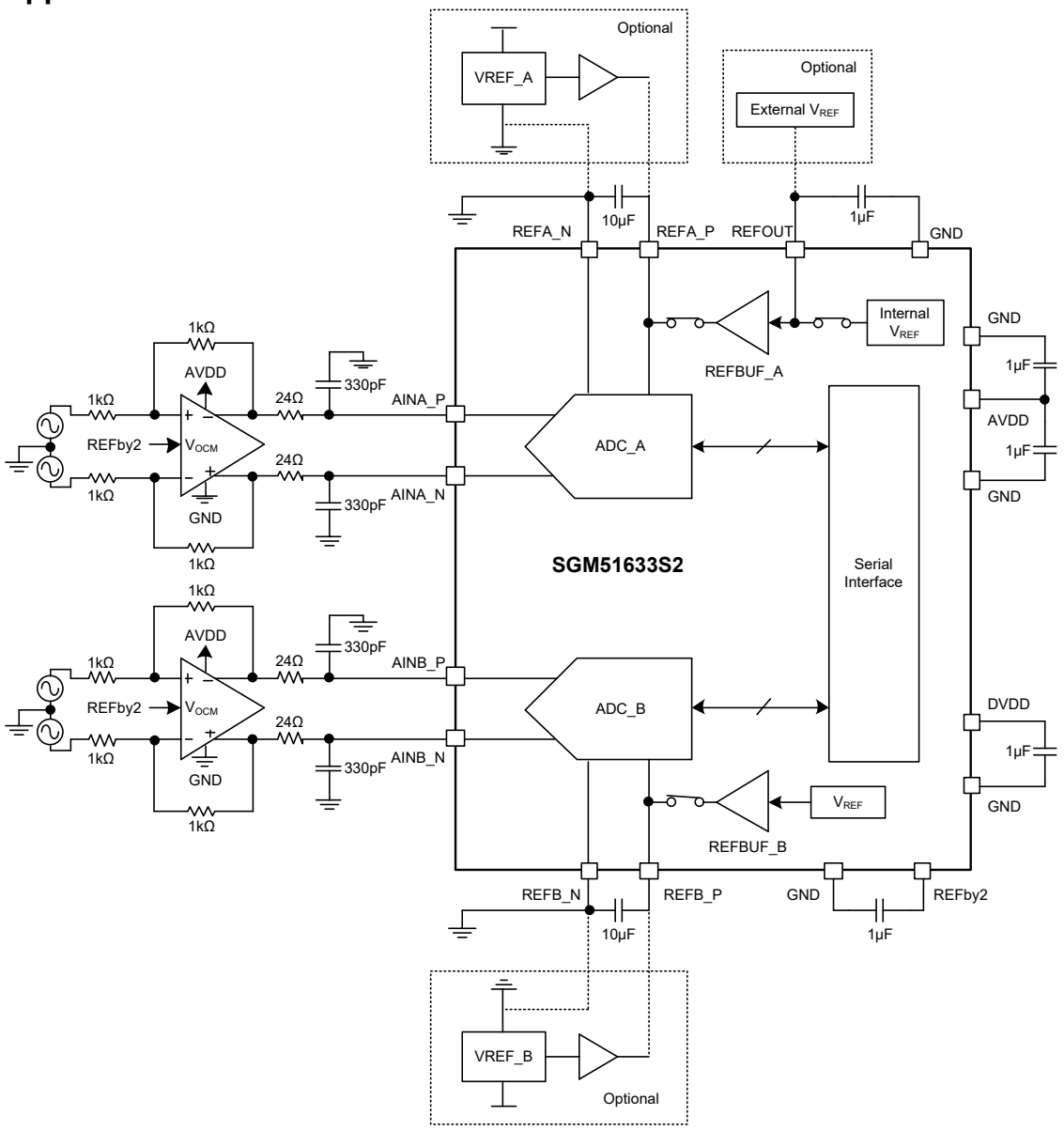


Figure 39. DAQ Circuit for a 100kHz Input Signal

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The high-performance ADC is the power supply noise sensitive component. The analog portions (internal reference, reference buffer, converter cores) are powered by AVDD, while the serial interface is powered by DVDD. It is recommended to place the corresponding decoupling capacitors as shown in Figure 40.

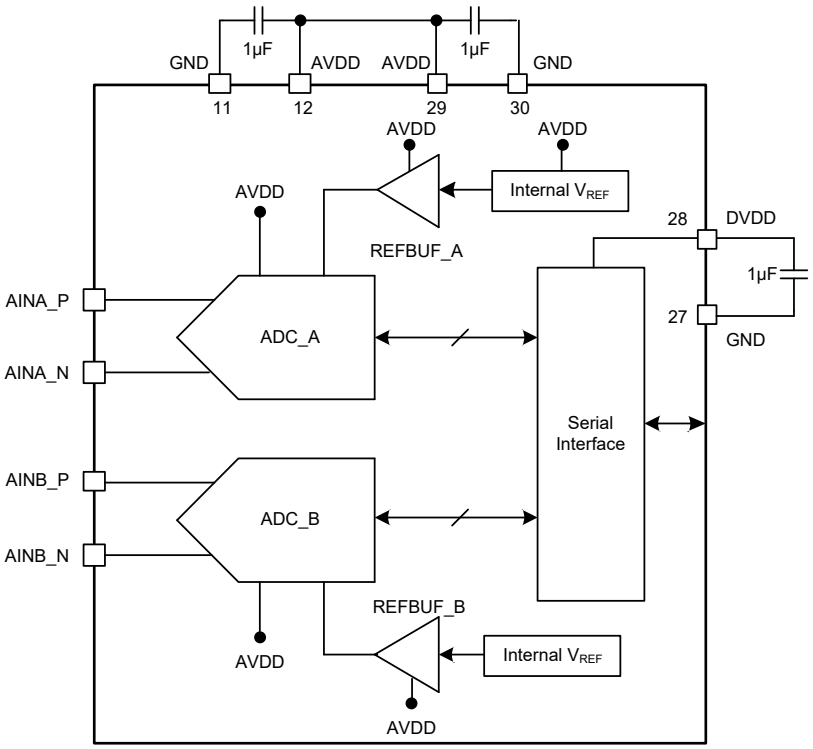


Figure 40. Power Supply Decoupling

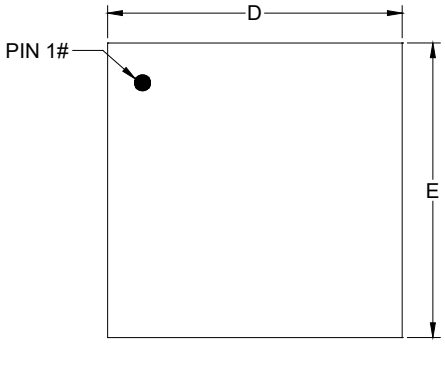
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

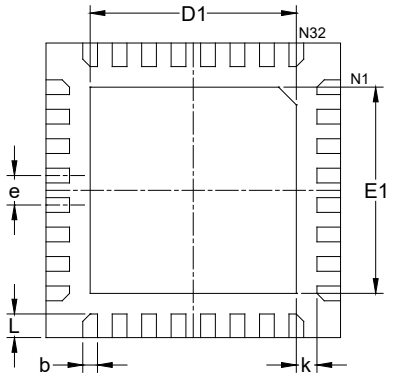
Changes from Original to REV.A (FEBRUARY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

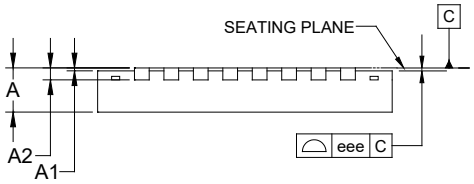
TQFN-5×5-32DL



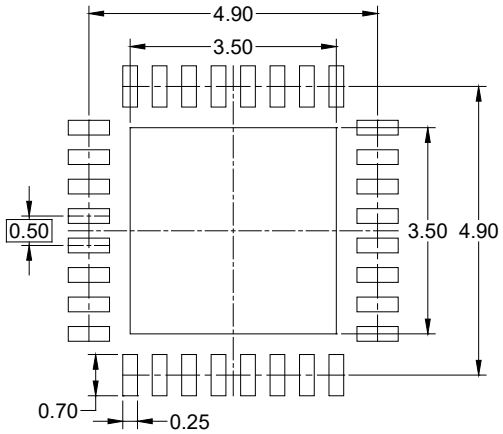
TOP VIEW



BOTTOM VIEW



SIDE VIEW



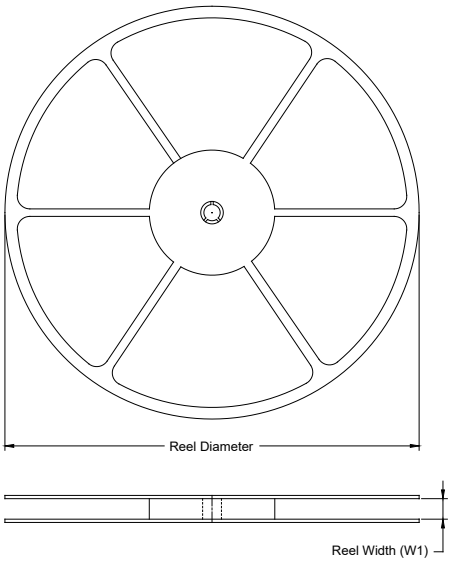
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.100
A2		0.203 REF	
b	0.180	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.400	3.500	3.600
E1	3.400	3.500	3.600
e		0.500 BSC	
k		0.350 REF	
L	0.300	-	0.500
eee		0.080	

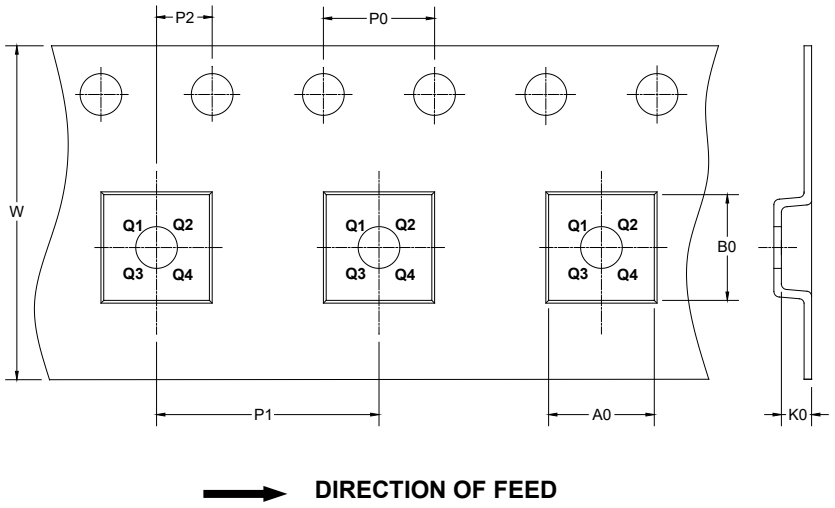
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



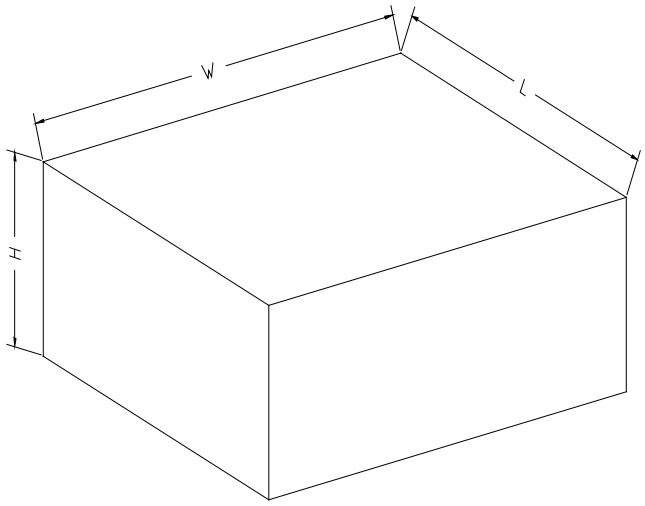
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32DL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002