SGM875xQ

-4V to 48V, 400kHz, Automotive Bidirectional, High-Precision Current Sense Amplifier with Enhanced PWM Rejection

GENERAL DESCRIPTION

The SGM875xQ device is a bidirectional, fixed gain, voltage-output, current-sense amplifier which features enhanced PWM rejection and wide common-mode voltage range from -4V to 48V. The device is powered by a single 2.7V to 5.5V supply, and draws supply current of 0.7mA (TYP). There are four fixed gain options: 20V/V, 50V/V, 100V/V and 200V/V, providing more flexibility to meet the gain requirements in various applications.

The enhanced PWM rejection suppresses large common-mode transients (ΔV/Δt) on the output signal, which is particularly relevant for applications utilizing pulse width modulation (PWM), such as motor drivers. The negative common-mode voltage capability allows the device to operate normally even when the voltage is below ground, which is useful in typical applications like the flyback period of a solenoid.

These characteristics make accurate current measurement without large transients and related recovery disturbances on the output voltage.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM875xQ is available in a Green SC70-6 package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Functional Safety**
  - **Available Documentation in the Design of Functional Safety Systems**
- **Enhanced PWM Rejection**
- **Wide Common-Mode Voltage Range: -4V to 48V**
- **High Signal Bandwidth:**
  - **SGM875AQ/BQ/CQ: 400kHz**
  - **SGM875DQ: 340kHz**
- **Slew Rate: 4V/μs**
- **Gain Error Accuracy:**
  - **SGM875AQ/BQ/CQ: ±0.4% (MAX)**
  - **SGM875DQ: ±0.55% (MAX)**
- **Offset Voltage Accuracy:**
  - **+25℃: ±130μV (MAX)**
  - **Offset Drift: 1μV/℃ (MAX)**
- **Bidirectional Current-Sensing Capability**
- **Available Gains:**
  - **SGM875AQ: 20V/V**
  - **SGM875BQ: 50V/V**
  - **SGM875CQ: 100V/V**
  - **SGM875DQ: 200V/V**
- **Quiescent Current: 0.7mA (TYP)**
- **Available in a Green SC70-6 Package**

APPLICATIONS

Motor Control
Vehicle Body Controllers
Vehicle Zonal Controllers
ADAS Domain Controllers
ADAS Sensor Monitoring

TYPICAL APPLICATION

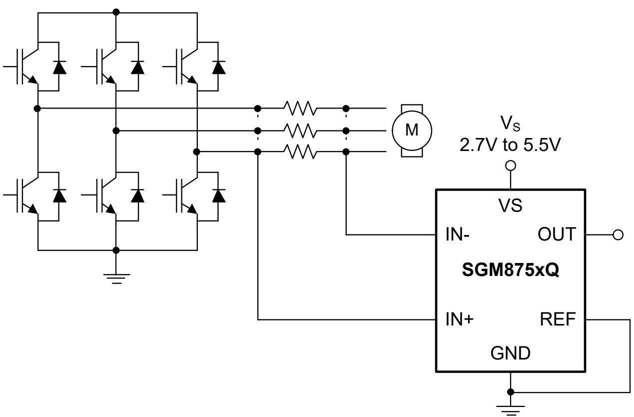


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM875AQ	SC70-6	-40℃ to +125℃	SGM875AQC6G/TR	2E5XX	Tape and Reel, 3000
SGM875BQ	SC70-6	-40℃ to +125℃	SGM875BQC6G/TR	34PXX	Tape and Reel, 3000
SGM875CQ	SC70-6	-40℃ to +125℃	SGM875CQC6G/TR	34QXX	Tape and Reel, 3000
SGM875DQ	SC70-6	-40℃ to +125℃	SGM875DQC6G/TR	34RXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.

YYY X X

Date Code - Week
Date Code - Year
Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S 6V
Analog Inputs, IN+, IN-
Differential V_{IN+} - V_{IN-} .... -36V to 36V
Common Mode [(1)] .... -6V to 50V
Common Mode (Less than 2s) .... -10V to 50V
Reference Voltage, V_{REF} .... GND - 0.3V to V_S + 0.3V
Output Voltage, V_{OUT} [(1)] .... GND - 0.3V to V_S + 0.3V
Package Thermal Resistance
SC70-6, θ_{JA} .... 134.6℃/W
SC70-6, θ_{JB} .... 47℃/W
SC70-6, θ_{JC} .... 104.1℃/W
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility [(2) (3)]
HBM .... ±4000V
CDM .... ±2000V

NOTES:

1. Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5mA.
2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Common-Mode Input Range, V_{CM} ...... -4V to 48V (12V, TYP)
Operating Supply Voltage, V_S .... 2.7V to 5.5V (5V, TYP)
Operating Ambient Temperature Range, T_A . -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

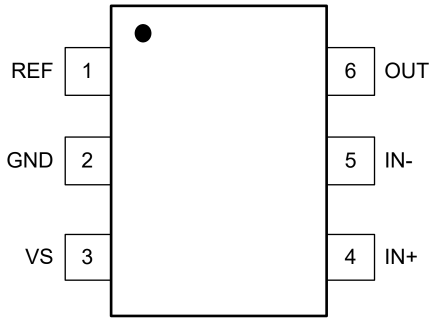
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SC70-6

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	REF	AI	Reference Input.
2	GND	G	Ground.
3	VS	P	2.7V to 5.5V Power Supply. Connect a 0.1μF capacitor from VCC to GND close to the device.
4	IN+	AI	Device Positive Input. For high-side sensing, connect it to the bus-voltage side of the sense resistor; for low-side sensing, connect it to the load side.
5	IN-	AI	Device Negative Input. For high-side sensing, connect it to the load side of the sense resistor; for low-side sensing, connect it to ground side.
6	OUT	AO	Output Voltage.

NOTE: AI = analog input, AO = analog output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{SENSE} = V_{IN+} - V_{IN-}, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.)

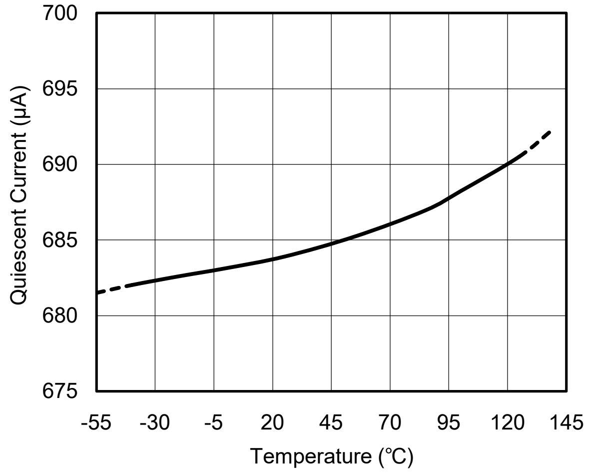
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input							
Common-Mode Rejection Ratio, RTI [1]	CMRR	V_{IN+} = -4V to 48V, V_{SENSE} = 0mV, T_A = -40℃ to +125℃	SGM875AQ	115	135		dB
			SGM875BQ/CQ/DQ	120	145		
		f = 50kHz			100		
Offset Voltage, RTI	V_{OS}	V_{SENSE} = 0mV			±25	±130	μV
Offset Drift, RTI	dV_{OS}/dT	V_{SENSE} = 0mV, T_A = -40℃ to +125℃			0.3	1	μV/℃
Power Supply Rejection Ratio, RTI	PSRR	V_S = 2.7V to 5.5V, V_{IN+} = 12V, V_{SENSE} = 0mV			±1	±15	μV/V
Input Bias Current	I_{IB}	V_{SENSE} = 0mV			10		nA
Input Offset Current	I_{IO}	V_{SENSE} = 0mV			10		nA
Output							
Gain	G	SGM875AQ			20		V/V
		SGM875BQ			50		
		SGM875CQ			100		
		SGM875DQ			200		
Gain Error	E_G	V_{OUT} = 0.5V to V_S - 0.5V, T_A = -40℃ to +125℃	SGM875AQ/BQ/CQ		±0.04	±0.4	%
			SGM875DQ		±0.04	±0.55	
Gain Error Drift		T_A = -40℃ to +125℃	SGM875AQ/BQ/CQ		15	25	ppm/°C
			SGM875DQ		25	40	
Nonlinearity Error		V_{OUT} = 0.5V to V_S - 0.5V			±0.01		%
Reference Voltage Rejection Ratio (Input-Referred)	RVRR	SGM875AQ			45		μV/V
		SGM875BQ			20		
		SGM875CQ/DQ			10		
Maximum Capacitive Load		No sustained oscillation			1		nF
Voltage Output							
Swing to VS	V_{SP}	R_L = 10kΩ to GND, T_A = -40℃ to +125℃			V_S - 0.020	V_S - 0.032	V
Swing to GND	V_{SN}	R_L = 10kΩ to GND, V_{IN+} - V_{IN-} = -10mV, T_A = -40℃ to +125℃			V_{GND} + 0.003	V_{GND} + 0.010	V
Zero-Current Swing to GND	V_{SG}	R_L = open, V_{REF} = 0V, V_{IN+} - V_{IN-} = 0mV, T_A = -40℃ to +125℃	SGM875AQ/BQ		V_{GND} + 0.003	V_{GND} + 0.011	V
			SGM875CQ		V_{GND} + 0.003	V_{GND} + 0.020	
			SGM875DQ		V_{GND} + 0.003	V_{GND} + 0.030	
Frequency Response							
Bandwidth	BW	C_{LOAD} = 10pF	SGM875AQ/BQ/CQ		400		kHz
			SGM875DQ		340		
Slew Rate	SR				4		V/μs
Noise, RTI [1]							
Voltage Noise Density					80		nV/$\sqrt{Hz}$
Power Supply							
Quiescent Current	I_Q	V_{SENSE} = 0mV			0.7	0.9	mA
		V_{SENSE} = 0mV, T_A = -40℃ to +125℃				1	

NOTE: 1. RTI = referred-to-input.

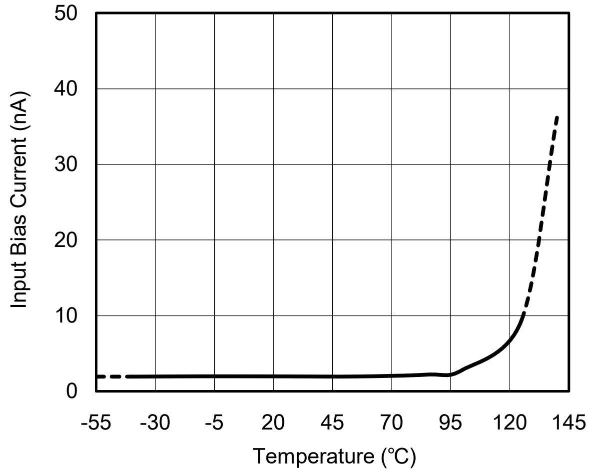
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

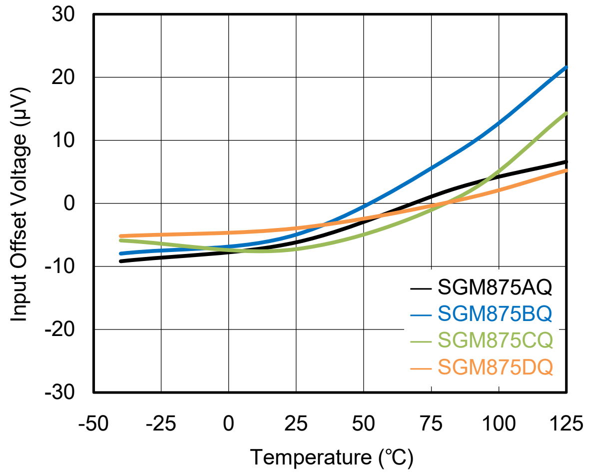
Quiescent Current vs. Temperature



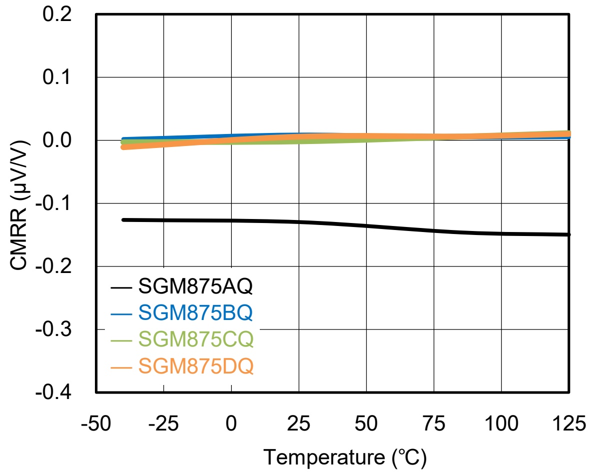
Input Bias Current vs. Temperature



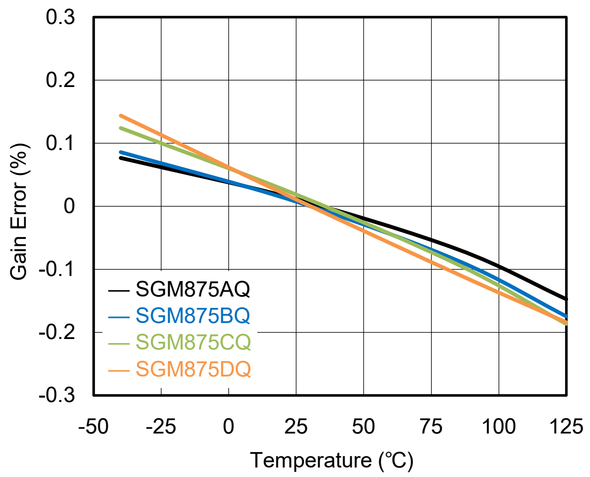
Input Offset Voltage vs. Temperature



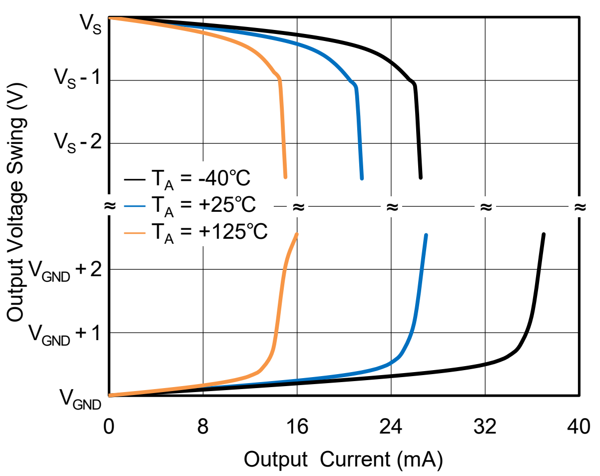
Common-Mode Rejection Ratio vs. Temperature



Gain Error vs. Temperature



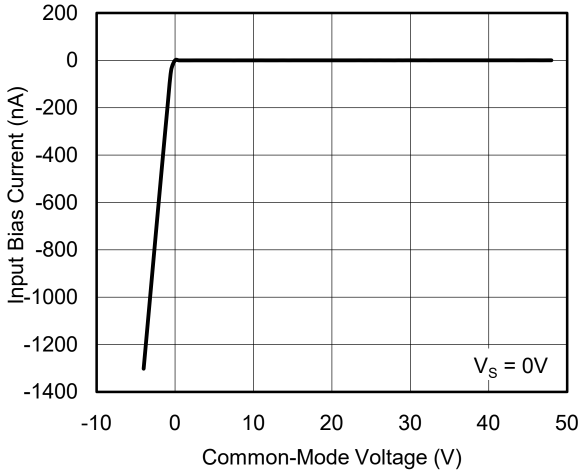
Output Voltage Swing vs. Output Current



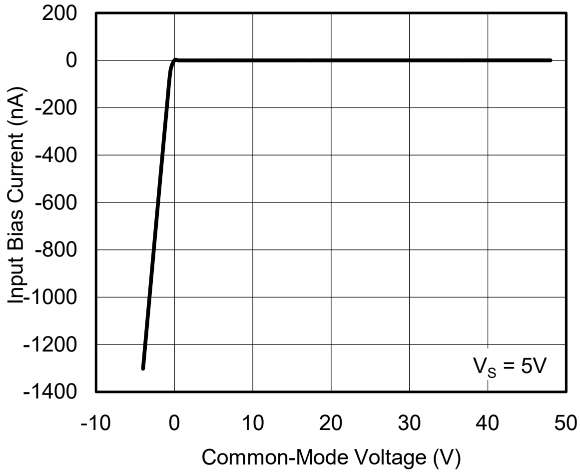
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

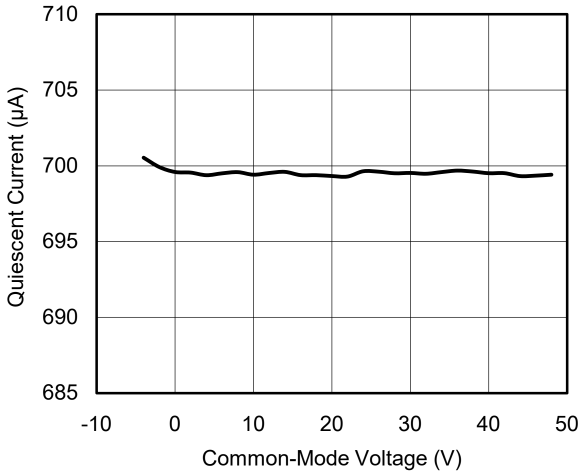
Input Bias Current vs. Common-Mode Voltage



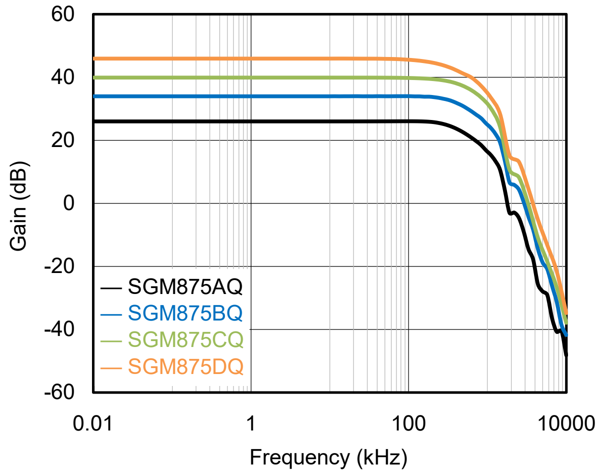
Input Bias Current vs. Common-Mode Voltage



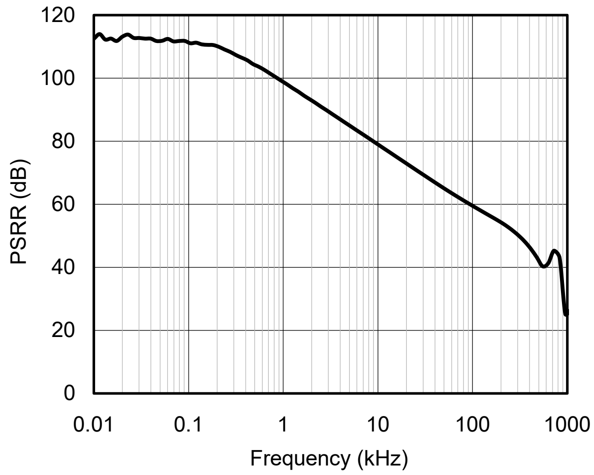
Quiescent Current vs. Common-Mode Voltage



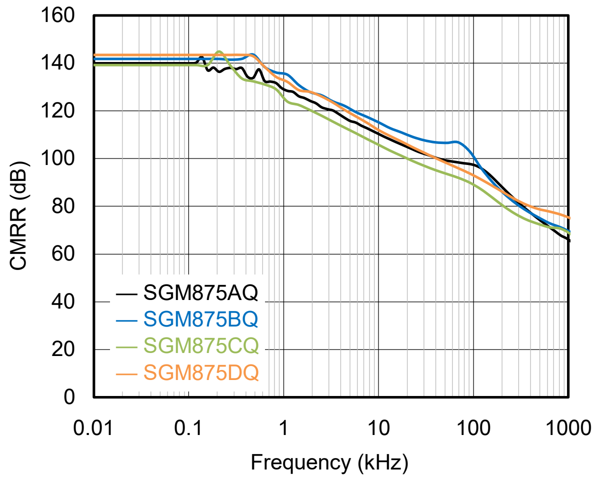
Gain vs. Frequency



Power-Supply Rejection Ratio vs. Frequency



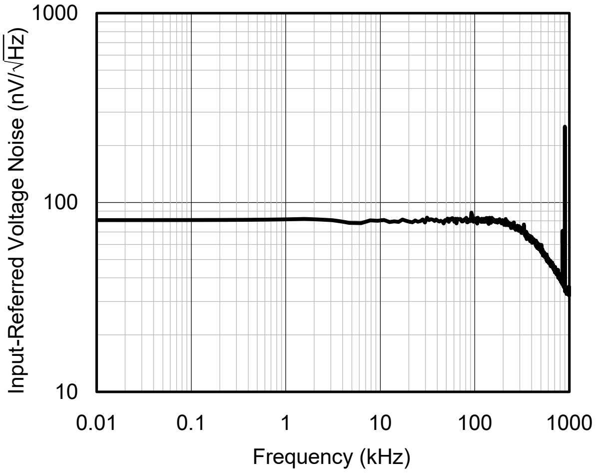
Common-Mode Rejection Ratio vs. Frequency



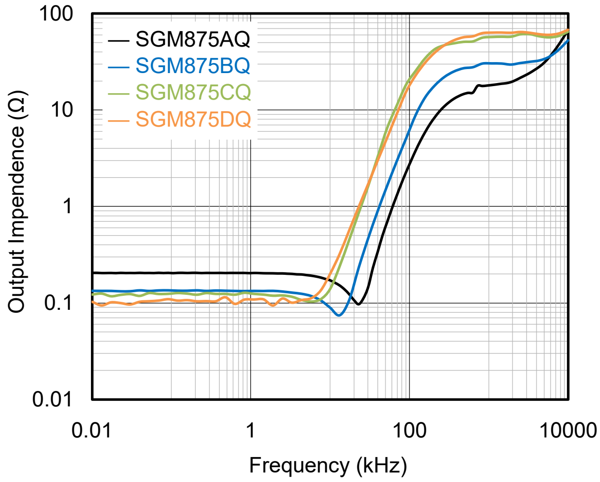
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

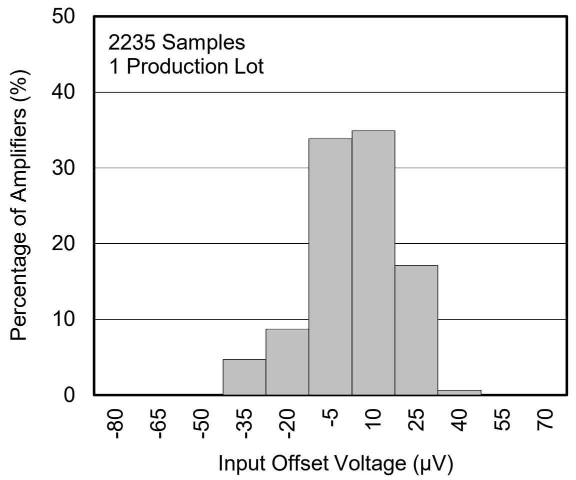
Input-Referred Voltage Noise vs. Frequency (SGM875AQ)



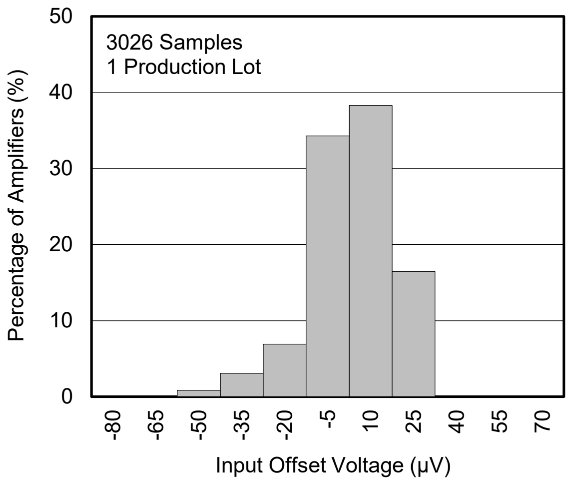
Output Impedance vs. Frequency



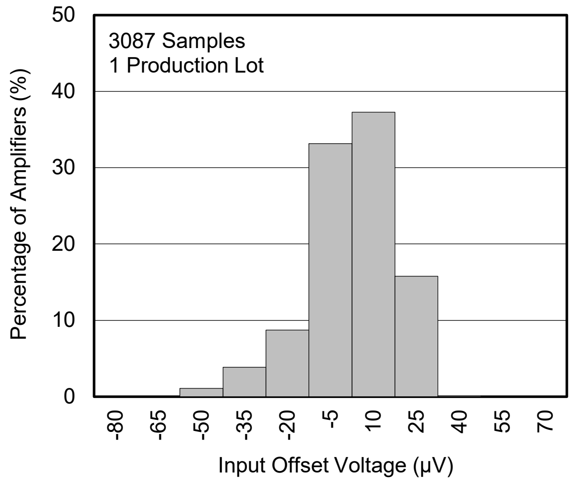
Input Offset Voltage Production Distribution (SGM875AQ)



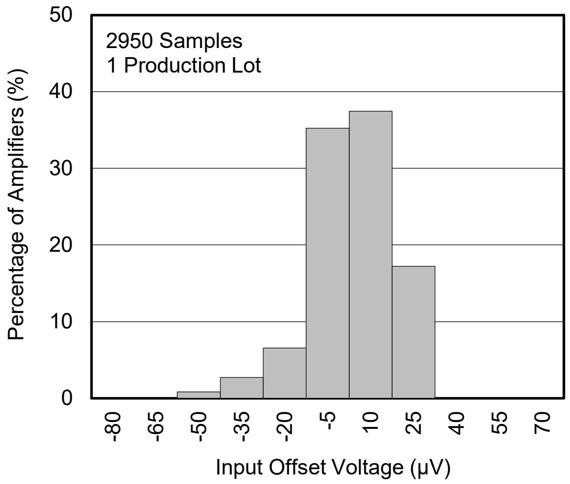
Input Offset Voltage Production Distribution (SGM875BQ)



Input Offset Voltage Production Distribution (SGM875CQ)



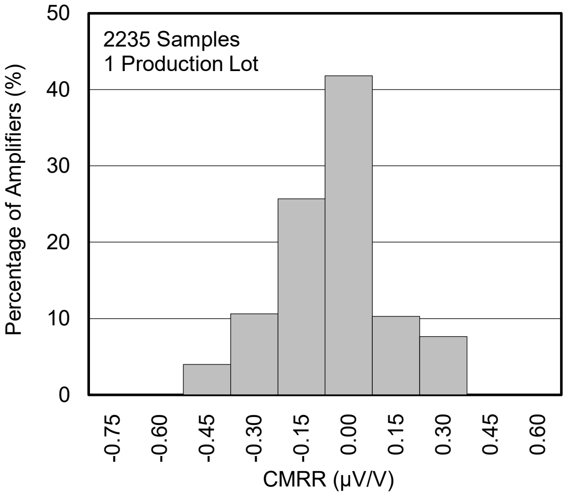
Input Offset Voltage Production Distribution (SGM875DQ)



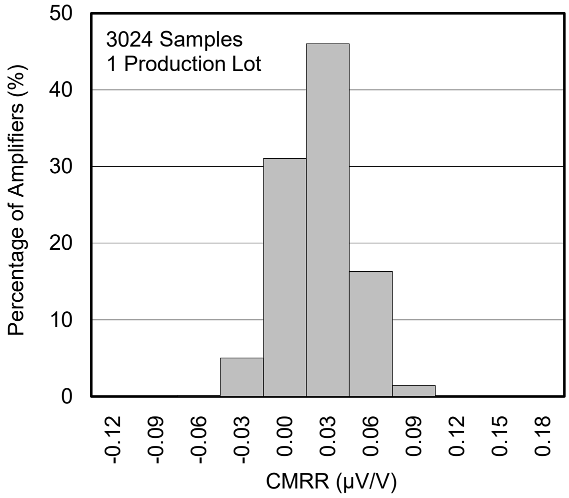
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

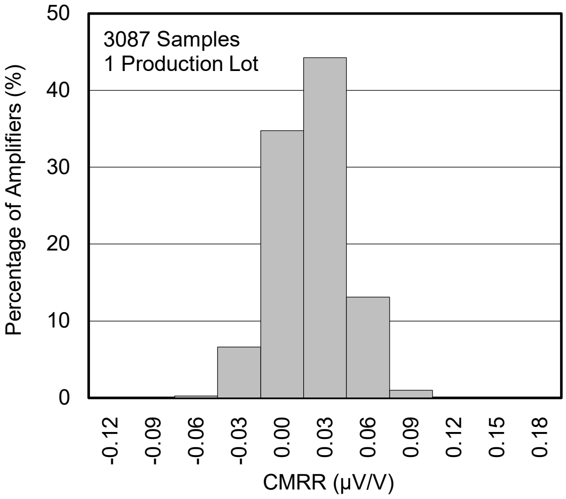
Common-Mode Rejection Production Distribution (SGM875AQ)



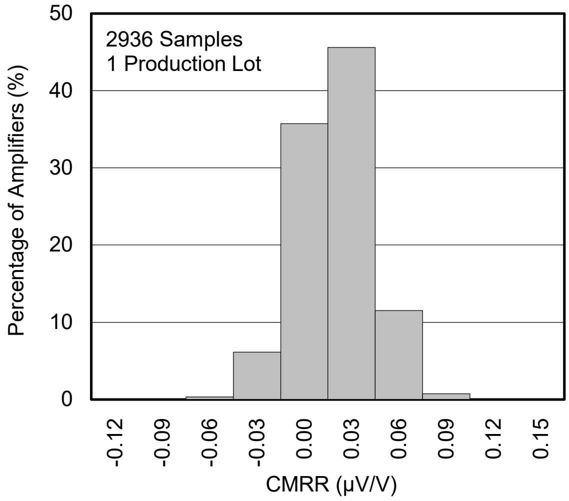
Common-Mode Rejection Production Distribution (SGM875BQ)



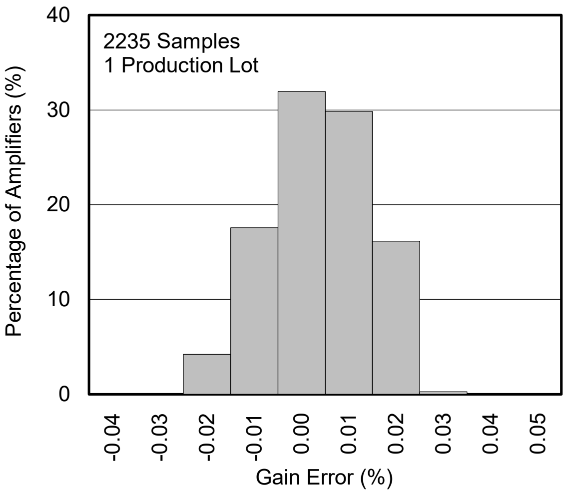
Common-Mode Rejection Production Distribution (SGM875CQ)



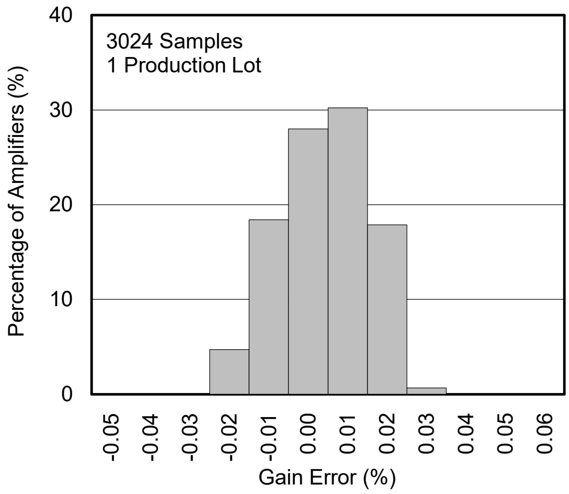
Common-Mode Rejection Production Distribution (SGM875DQ)



Gain Error Production Distribution (SGM875AQ)



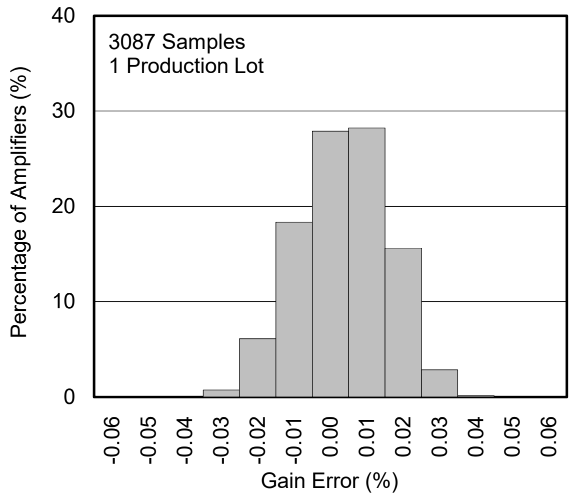
Gain Error Production Distribution (SGM875BQ)



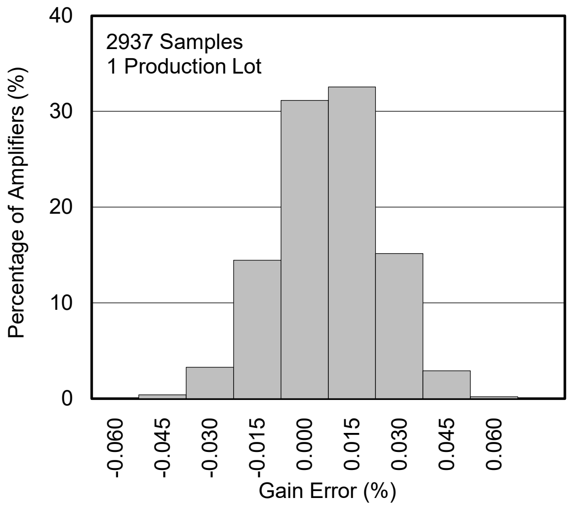
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

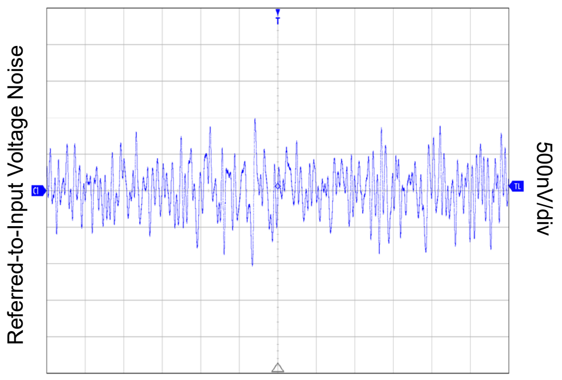
Gain Error Production Distribution (SGM875CQ)



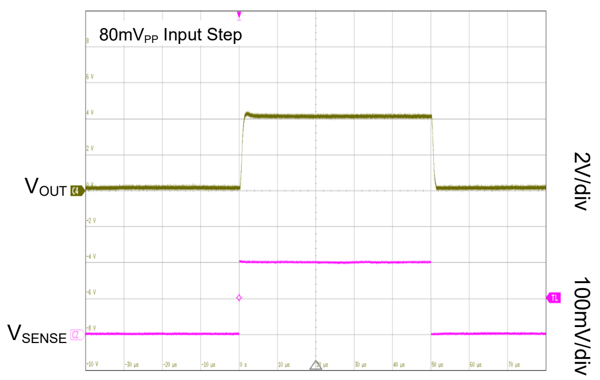
Gain Error Production Distribution (SGM875DQ)



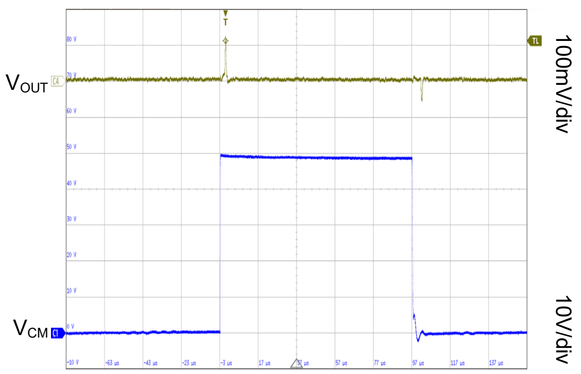
0.1Hz to 10Hz Referred-to-Input Voltage Noise



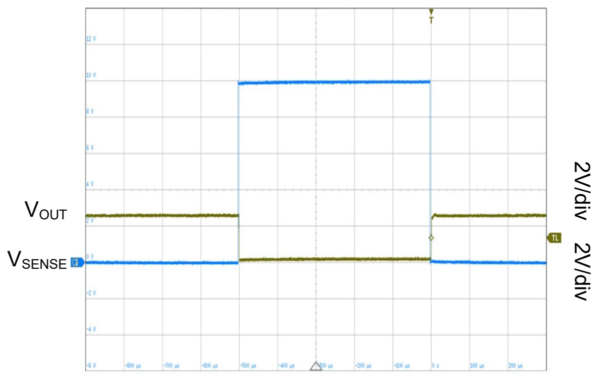
Step Response (SGM875AQ)



Common-Mode Voltage Transient Response



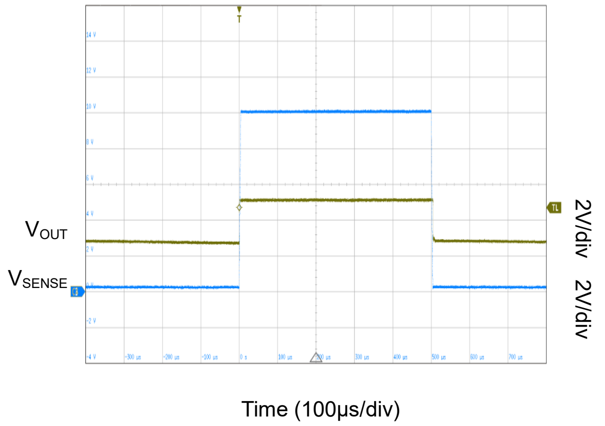
Inverting Differential Input Overload



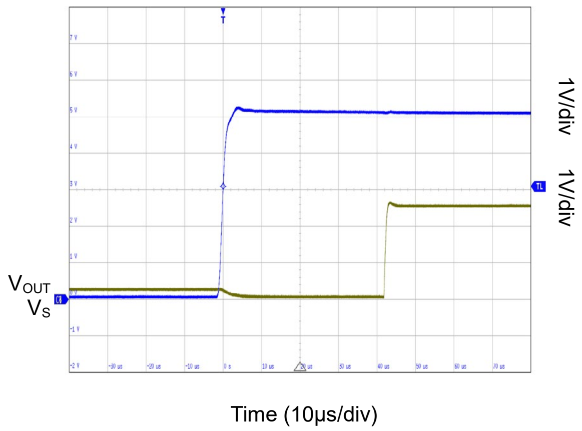
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 5V, V_{REF} = V_S/2 and V_{IN+} = 12V, unless otherwise noted.

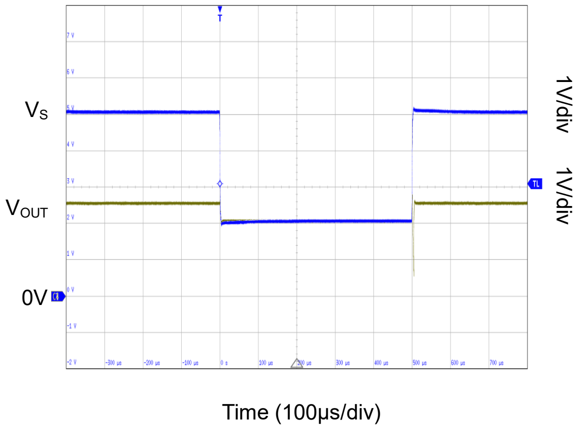
Non-Inverting Differential Input Overload



Startup Response



Brownout Recovery



FUNCTIONAL BLOCK DIAGRAM

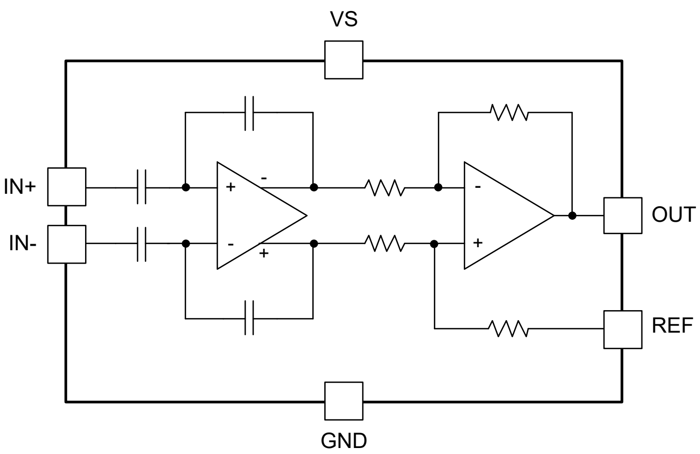


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGM875xQ is a current-sense amplifier supporting up to 48V common-mode voltage (V_{CM}), compatible with both high-side and low-side shunt resistor sampling schemes. Its proprietary internal topology enables precise voltage measurement across current shunts when the bus common-mode voltage far exceeds the supply rail of the chip. The component can accurately sample current on bus rails with potentials as high as 48V while operating from a minimal 2.7V supply input.

Feature Description

High Bandwidth and Slew Rate

The SGM875xQ delivers a maximum small-signal bandwidth of 400kHz for SGM875AQ/BQ/CQ, and 340kHz for SGM875DQ alongside a 4V/μs large-signal slew rate. This fast response capability allows real-time tracking of rapidly fluctuating load currents and rapid output voltage transitions, making it suitable for applications requiring ultra-fast signal capture. Low-side motor control is one major use case: rapid current tracking enables precise motor regulation across full operating ranges. The chip also serves fast fault detection circuits; paired with external comparators and reference voltages, it can instantly flag over-current and under-current fault conditions.

Bidirectional Current Monitoring

This amplifier tracks load current passing through the shunt resistor in both flow directions, implemented via adjustable voltage biasing on the REF pin. A positive differential voltage ($V_{IN+} > V_{IN-}$) pushes the output voltage above the reference potential set at REF; a negative differential input pulls V_{OUT} below V_{REF}. The mathematical formula to calculate output voltage is shown as Equation 1.

$$V_{OUT} = (I_{LOAD} \times R_{SENSE} \times G) + V_{REF} \quad (1)$$

where:

- I_{LOAD} = monitored load current;
- R_{SENSE} = shunt sampling resistor resistance;
- G = fixed voltage gain of the selected SGM875xQ variant;
- V_{REF} = external voltage applied to the REF terminal.

Wide Input Common-Mode Voltage Range

The SGM875xQ supports input common-mode potentials spanning from -4V to 48V. Its unique internal circuit design decouples the common-mode operating limit from the chip supply rail (V_S), as long as V_S stays within the 2.7V to 5.5V operating window. The ability to process input voltages both above and below V_S enables flexible deployment in high-side and low-side current measurement topologies, illustrated in Figure 3.

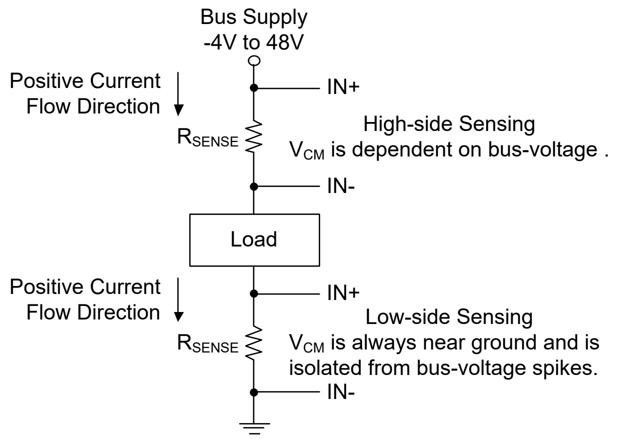


Figure 3. High-side and Low-side Sensing Connections

Precise Low-side Current Sensing

When configured for low-side current measurement, the SGM875xQ maintains tight input offset voltage tolerances below ±130μV across all device variants. Low offset delivers two critical system benefits. Firstly, expanded dynamic measurement range: minimal offset error preserves reading precision for small low-magnitude currents. Secondly, lower-value shunt resistors can be deployed without sacrificing accuracy, reducing power dissipation across the sampling resistor and boosting overall system power efficiency. Gain error constitutes the dominant measurement error source when the shunt differential voltage far exceeds the offset voltage of the chip, with maximum gain error limited to ±0.4% for SGM875AQ/BQ/CQ, and ±0.55% for SGM875DQ.

Rail-to-Rail Output Swing

The output stage of SGM875xQ delivers linear signal operation with output potentials positioned extremely close to both the positive supply rail and circuit ground. The output only drops 32mV below V_S at maximum positive swing, and sits merely 10mV above GND for ground-proximity swing limits.

DETAILED DESCRIPTION (continued)

Unlike standard operational amplifiers, current-sense amplifiers operate in closed-loop feedback architecture, so ground swing limits under unidirectional sampling (REF tied to GND, zero-load current) are constrained by the inherent offset voltage of the chip. Under zero-current conditions, the maximum output voltage near ground is capped at 11mV for SGM875AQ, 20mV for. SGM875BQ, and 30mV for SGM875CQ/DQ.

Device Functional Modes

Normal Mode

The SGM875xQ enters standard linear measurement mode when all criteria below are satisfied.

- Supply voltage V_S falls between 2.7V and 5.5V.
- Input common-mode voltage V_{CM} remains within -4V to 48V.
- G × maximum differential input voltage + V_{REF} < V_S - positive rail swing margin.
- G × minimum differential input voltage + V_{REF} > ground swing margin (refer to Rail-to-Rail Output Swing section).
- In normal operation, the output terminal produces an amplified replica of the differential voltage across IN+/IN-, offset by the external reference voltage at the REF pin.

Unidirectional Mode

Single-direction current monitoring is achieved by hard-wiring the REF pin to ground potential, as shown in Figure 4. With zero-load current, OUT sits close to GND; current flowing from bus rail to load generates a positive differential shunt voltage, raising the output voltage proportionally.

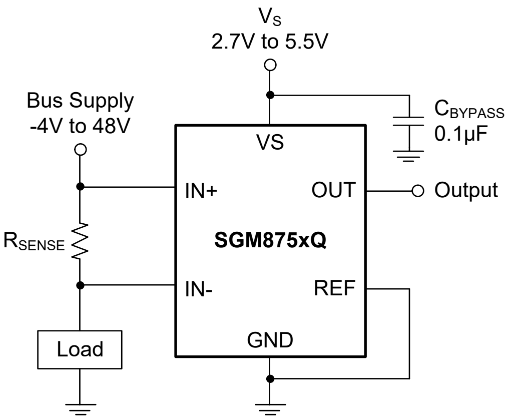


Figure 4. Unidirectional Application

The output linear operating range is constrained by how closely VOUT can approach ground with zero input signal. For systems requiring precise low-current readings, engineers can bias the REF pin to a voltage above 50mV to shift the output into the optimal linear region of the device. A buffered reference voltage supply is recommended for the REF pin to minimize CMRR degradation.

An alternative biasing scheme connects the REF pin directly to VS, which clamps the output 32mV below the supply rail with zero differential input signal. In this configuration, output voltage only responds to reverse-direction load currents that create negative IN+/IN- differential potentials, with V_{OUT} falling as reverse current magnitude rises. The voltage fed to REF must never exceed the VS supply rail.

Bidirectional Mode

This chip supports dual-direction current sampling for circuits with bidirectional current flow (such as battery charge/discharge loops and forward/reverse motor control). Figure 5 shows the standard bidirectional circuit topology.

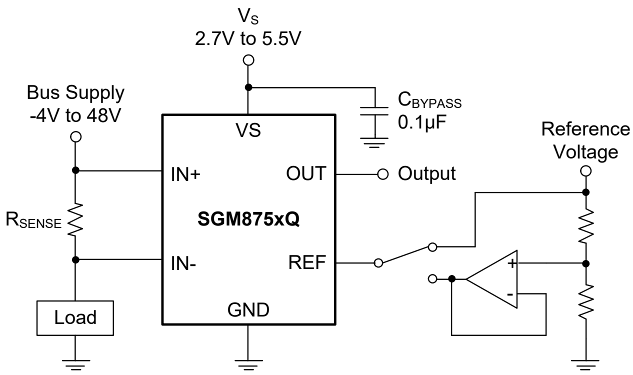


Figure 5. Bidirectional Application

Dual-range measurement is realized by feeding a fixed voltage to the REF pin, which sets the zero-current output baseline. Positive load currents generate V_{IN+} > V_{IN-} differential voltages and push V_{OUT} higher than V_{REF}; reverse currents create negative differential potentials and pull V_{OUT} below the reference level. V_{REF} can be programmed to any potential between 0V and V_S. For symmetric bidirectional current ranges, V_{REF} is typically set to $V_S/2$ to allocate equal linear swing range for forward and reverse currents. Asymmetric reference biasing is used when forward and reverse current operating ranges are mismatched.

DETAILED DESCRIPTION (continued)

Input Differential Overload

If the product of differential input voltage and device gain, summed with V_{REF}, exceeds the output swing boundaries of the chip, the output saturates at the nearest supply rail and stops delivering accurate current readings. To avoid this state during regular operation, designers can either reduce the shunt resistor resistance or select a lower-gain amplifier variant. If overload only occurs during transient fault events, the output automatically recovers valid readings approximately 5μs after the fault condition clears.

Shutdown Mode

No dedicated hardware shutdown pin is integrated on the SGM875xQ. System-level power gating can be implemented by switching the VS supply rail via logic transistors or gate outputs to cut the quiescent current draw of the chip. Designers must evaluate leakage current flowing through the sampling shunt when the amplifier is fully powered down. Figure 6 presents a typical power gating circuit.

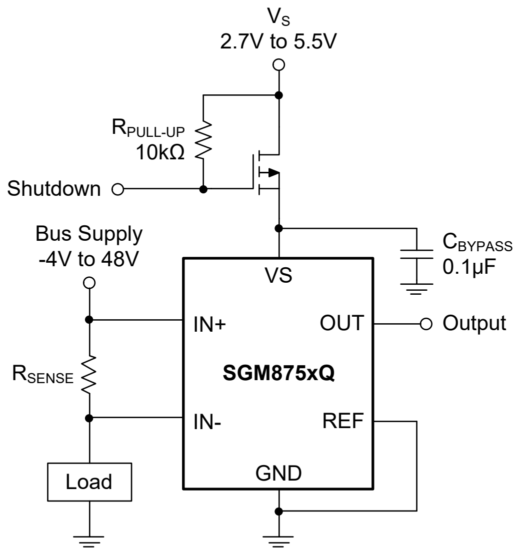


Figure 6. Basic Circuit to Shut Down the SGM875xQ with a Grounded Reference

As shown in Figure 2, by adding a capacitive coupled input bias stage at the input pins, when the amplifier is in a powered down state, the current at the input pins end is as low as the nA level. Especially when the common-mode voltage is greater than 0V, the current is approximately 10nA.

APPLICATION INFORMATION

The SGM875xQ amplifies the tiny voltage drop generated across a series sampling shunt resistor when load current passes through the component. Adjustable biasing on the REF pin unlocks multiple circuit topologies for unidirectional and bidirectional sampling.

Basic Connections

Figure 7 displays the minimal peripheral circuit wiring for the amplifier. Traces linking the IN+ and IN- pins to the shunt resistor must be routed as short, matched-length Kelvin connections to eliminate series parasitic resistance measurement errors.

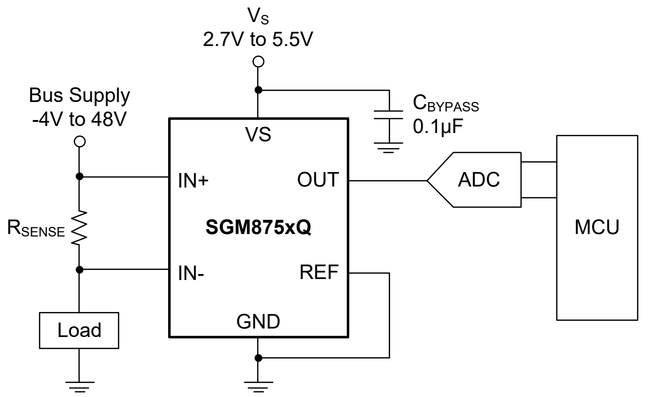


Figure 7. Basic Connections for the SGM875xQ

A minimum-value 0.1μF decoupling capacitor must be mounted directly adjacent to the VS and GND pins for stable power delivery. Additional bulk decoupling capacitance can be added for noisy or high-impedance supply rails to suppress supply-borne interference.

R_{SENSE} and Device Gain Selection

Engineers should maximize shunt resistance as much as possible to boost differential input signal magnitude and reduce the relative contribution of offset voltage to total measurement error. However, practical hardware constraints limit maximum R_{SENSE} values. Input bias current mismatch error increases with larger shunt resistance, degrading CMRR performance; resistances above several ohms are discouraged for high-precision sampling systems. Maximum allowable power dissipation across the shunt resistor sets an upper resistance bound, calculated via Equation 2.

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^{2}} \tag{2}$$

where:

- PD_{MAX} = maximum permitted power loss on the sampling resistor;
- I_{MAX} = peak load current magnitude.

Output swing limits defined by V_S and device rail proximity performance impose further gain/resistance tradeoffs. Equation 3 calculates the combined maximum gain and shunt resistance to avoid positive rail saturation.

$$I_{MAX} \times R_{SENSE} \times G < V_{SP} - V_{REF} \tag{3}$$

where:

- I_{MAX} is the maximum current that flows through R_{SENSE};
- G is the gain of the current sense-amplifier;
- V_{SP} is the positive output swing specified in the data sheet;
- V_{REF} is the externally applied voltage on the REF pin.

If the resistance value calculated from power dissipation constraints creates saturated output signals at peak load current, switch to a lower-gain SGM875xQ model. Equation 4 quantifies ground swing limitations to define minimum usable shunt resistance values.

$$I_{MIN} \times R_{SENSE} \times G > V_{SN} - V_{REF} \tag{4}$$

where:

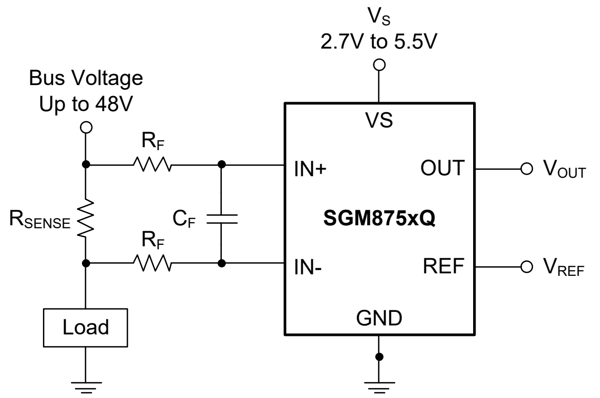
- I_{MIN} is the minimum current that flows through R_{SENSE};
- G is the gain of the current sense amplifier;
- V_{SN} is the negative output swing of the device (see Rail-to-Rail Output Swing section);
- V_{REF} is the externally applied voltage on the REF pin.

In addition to adjusting the offset and gain, the voltage applied to the REF pin can be slightly increased to avoid negative swing limitations.

APPLICATION INFORMATION (continued)

Signal Filtering

If the downstream receiving circuit presents high input impedance, the optimal noise filtering position is an RC low-pass network wired between the OUT pin and system ground. Output-side filtering attenuates high-frequency interference originating from common-mode voltage transients, differential shunt signal noise, and supply rail fluctuations. If input-side filtering is mandatory or differential signal-only noise suppression is required, install RC filter networks on the IN+ and IN- pins as illustrated in Figure 8.



$$f_{-3dB} = \frac{1}{2\pi \times (R_F + R_F) \times C_F}$$

Figure 8. Filter at Input Pins

External series filter resistors introduce additional measurement errors, so their resistance value must be restricted below 10Ω to limit accuracy degradation. Internal input bias networks create minor input bias current mismatch; adding external series resistors generates differential voltage errors across the filter resistors, which offset the true shunt voltage drop captured by the amplifier inputs. Equation 5 quantifies the signal attenuation factor caused by external filter resistors.

$$\text{Gain Error Factor} = \frac{R_{DIFF}}{R_{SENSE} + 2 \times R_F + R_{DIFF}} \quad (5)$$

where:

- R_{DIFF} is the differential input impedance about 110kΩ;
- R_F is the added value of the series filter resistance.

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 6.

$$\text{Gain Error}(\%) = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

Table 1 simplifies the attenuation factor formula for each model to calculate added gain error from external filter resistors via Equation 6. For example, fitting 10Ω series filter resistors to SGM875xQ produces an attenuation factor of 0.9998, translating to an extra 0.018% total gain error originating solely from the filter resistors. Table 1 illustrates the gain error introduced by R_F where R_{SENSE} has been neglected.

Table 1. Gain Error Introduced by the External Filter Resistance at Input Pins

External Filter Resistance R_F (Ω)	Gain Error (%)
4.7	0.009
10	0.018
22	0.04

Typical Application

Dual-direction current monitoring represents a primary target application for the SGM875xQ, including battery charge/discharge monitoring and bidirectional motor current tracking. Figure 9 shows the complete bidirectional sampling circuit. Setting the REF pin to a stable voltage near $V_S/2$ allocates equal linear output swing for forward and reverse current flow; tying REF directly to GND reconfigures the circuit for single-direction measurement.

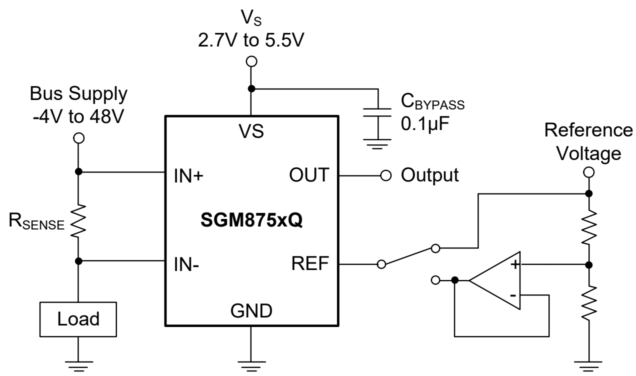


Figure 9. Measuring Bidirectional Current

APPLICATION INFORMATION (continued)

Design Requirements

The design requirements for the circuit shown in Figure 9 are listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Power-Supply Voltage	V_S	5V
Bus Supply Rail	V_{CM}	12V
R_{SENSE} Power Loss		< 450mW
Maximum Sense Current	I_{MAX}	±20A
Current Sensing Error		Less than 1% at maximum current, T_J = +25℃
Small-Signal Bandwidth		> 100kHz

Detailed Design Procedure

First, calculate maximum allowable shunt resistance via power loss constraints by applying Equation 2: PD_{MAX} = 450mW, I_{MAX} = 20A yields R_{SENSE_MAX} = 1.125mΩ. Select the closest standard industry resistor value of 1mΩ to meet thermal power limits.

Select matching amplifier gain for bidirectional symmetric ±20A current range. Since this design targets bidirectional current measurement, the REF pin needs an input voltage within the 0V to V_S range. The bidirectional currents monitored are symmetric around 0A (that is, ±20A); therefore, the ideal voltage to apply to V_{REF} is $V_S/2$ or 2.5V. Using Equation 3, and given that I_{MAX} = 20A, R_{SENSE} = 1mΩ, and V_{REF} = 2.5V, positive swing limit calculation returns maximum allowable gain of 122.5V/V. Likewise, using Equation 4 for negative swing constraints yields a maximum gain of 124.75V/V. The 100V/V gain of SGM875CQ is selected to maximize output swing headroom without rail saturation. If calculated maximum allowable gain falls below 100V/V, reduce shunt resistance to expand linear signal range.

Two error components, gain error and offset error, will be analyzed to assess accuracy under peak current conditions. The SGM875CQ features a maximum gain error of 0.4%. Under the conditions of V_{CM} = 12V and V_S = 5V, offset-originated error is a fixed value with an upper limit of 130μV. Given total offset error = 130μV, R_{SENSE} = 1mΩ and I_{SENSE} = 20A, Equation 7 produces an offset-voltage-related percentage error contribution of 0.65%.

$$\text{Total Offset Error}(\%) = \frac{\text{Total Offset Error(V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \quad (7)$$

Statistically accurate total error is computed via root-sum-square (R_{SS}) summation of uncorrelated gain and offset error components (Equation 8), delivering a total measurement error of 0.76% at peak current, which satisfies the < 1% design target.

$$\text{Total Error}(\%) = \sqrt{\text{Total Gain Error}(\%)^2 + \text{Total Offset Error}(\%)^2} \quad (8)$$

Equation 8 gives an overall current-sensing error of 0.76% at full-scale current, which meets the example design specification requiring error below 1%.

SGM875CQ provides 400kHz small-signal bandwidth, exceeding the 100kHz minimum specification.

Application Curve

Figure 10 plots the typical output voltage transfer curve for a bidirectional sampling circuit with V_{REF} set to 2.5V; output rises above 2.5V for forward load currents and falls below 2.5V for reverse current flow.

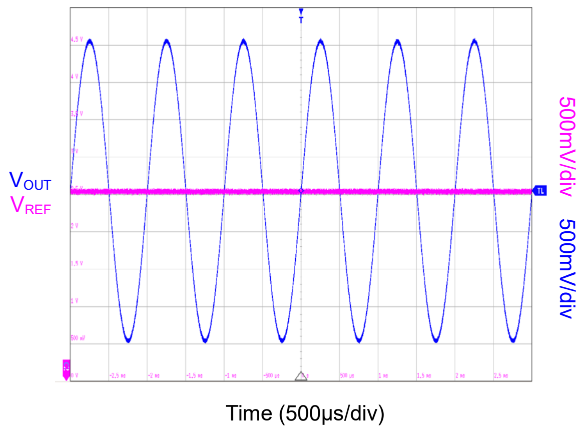


Figure 10. Bidirectional Application Output Response

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The front-end input topology of SGM875xQ enables accurate current sampling at bus voltages far exceeding the VS supply rail (e.g., 12V bus with 5V amplifier supply). However, the linear voltage operating window of OUT pin remains strictly bounded by the VS and GND supply potentials. The IN+ and IN- input pins also tolerate the full ±36V differential voltage range even when the VS supply rail is unpowered.

Common-Mode Transients Greater than 48V

Automotive wiring harnesses frequently generate voltage transients exceeding native 48V common-mode operating limit of the chip, which can be mitigated with minimal external protection components. Zener diodes or TVS transorbs are mandatory for fast transient clamping (alternative surge suppression devices introduce excessive response delay). The standard protection circuit adds low-value series resistors (< 10Ω) to form a current-limiting impedance for the clamping diodes, shown in Figure 11. Larger series resistors are usable but introduce measurable gain error as outlined in the signal filtering section. Low-power Zener diodes in SOD-523/SOT-523 miniature package deliver compact board-area protection for short-duration transients.

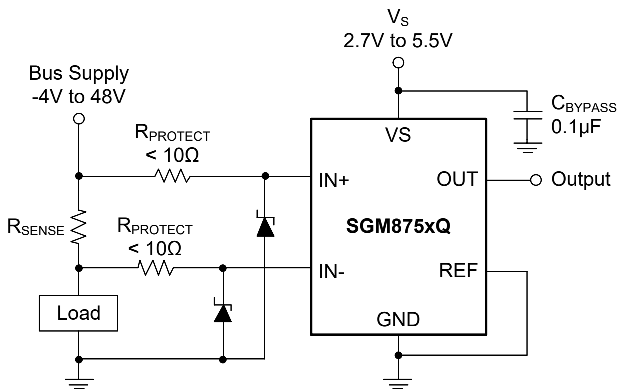


Figure 11. Transient Protection Using Dual Zener Diodes

For high-energy surge environments requiring stronger clamping capability, replace dual Zener diodes with a single unidirectional transorb paired with back-to-back signal diodes between IN+ and IN- pins, as shown in Figure 12. Dual series diodes integrated within single SOT/SOD miniature package minimize PCB footprint. With all protection peripherals populated, the total circuit footprint remains smaller than a standard SOIC-8 package and marginally larger than MSOP-8 footprint dimensions. Reference design documents covering high-transient shunt monitoring circuits contain additional protection topology details.

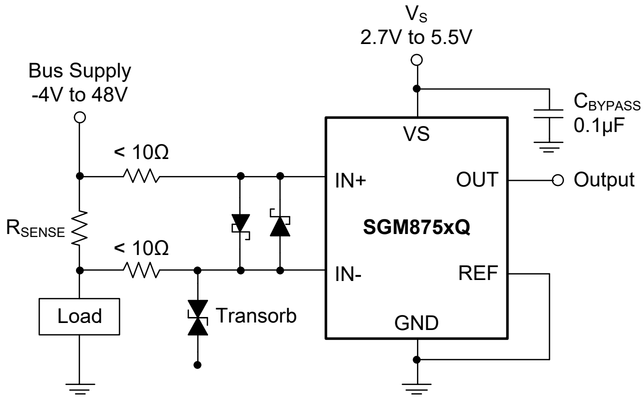


Figure 12. Transient Protection Using a Single Transorb and Input Clamps

Layout Guidelines

Implement Kelvin 4-wire routing between the shunt resistor and IN+/IN- pins to eliminate parasitic trace resistance from measurement readings; mismatched high-current trace resistance introduces severe full-scale errors due to the milliohm-scale shunt resistance values used in high-current systems.

Mount the 0.1μF decoupling capacitor between VS and GND in direct physical proximity to power and ground pins of the amplifier. Add supplementary bulk decoupling capacitance for noisy, high-impedance power delivery rails.

Route traces connecting the shunt resistor to the amplifier input pins with identical length and matched impedance to eliminate differential signal mismatch errors.

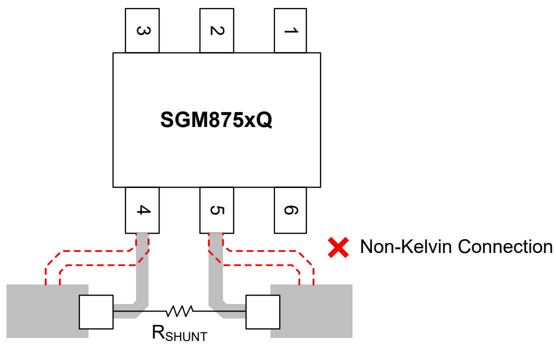


Figure 13. Shunt Connections to the SGM875xQ

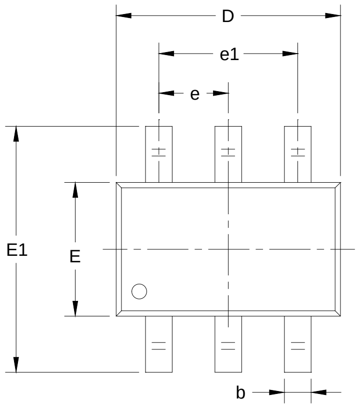
REVISION HISTORY

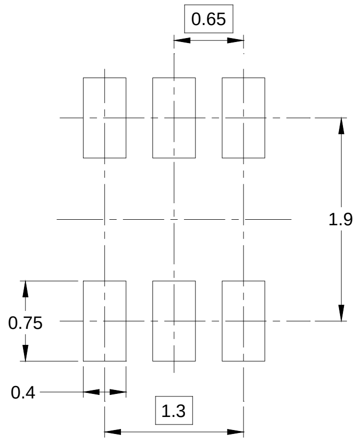
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (SEPTEMBER 2026)	Page
Changed from product preview to production data	All

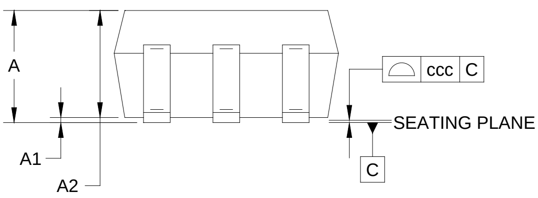
PACKAGE OUTLINE DIMENSIONS

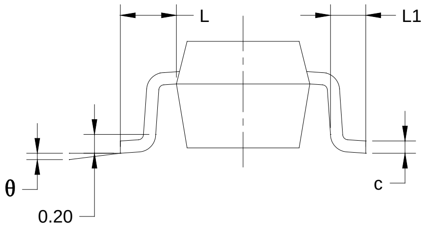
SC70-6





RECOMMENDED LAND PATTERN (Unit: mm)



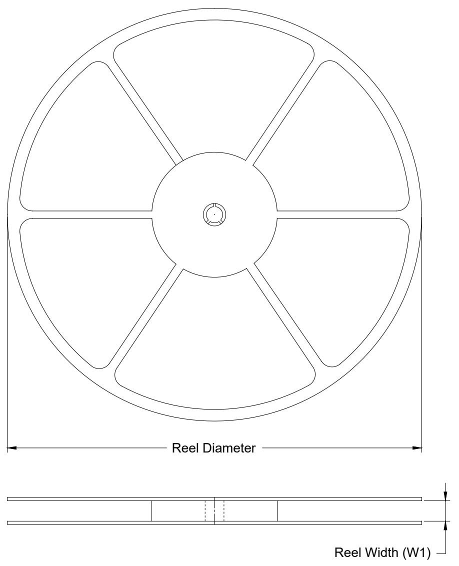


Symbol	Dimensions In Millimeters		
	MIN	**NOM**	**MAX**
A	0.800	-	1.100
A1	0.000	-	0.100
A2	0.800	-	1.000
b	0.150	-	0.350
c	0.080	-	0.220
D	2.000	-	2.200
E	1.150	-	1.350
E1	2.150	-	2.450
e	0.600	0.650	0.700
e1	1.200	1.300	1.400
L	0.525 REF		
L1	0.260	-	0.460
ccc	0.100		
θ	0°	-	8°

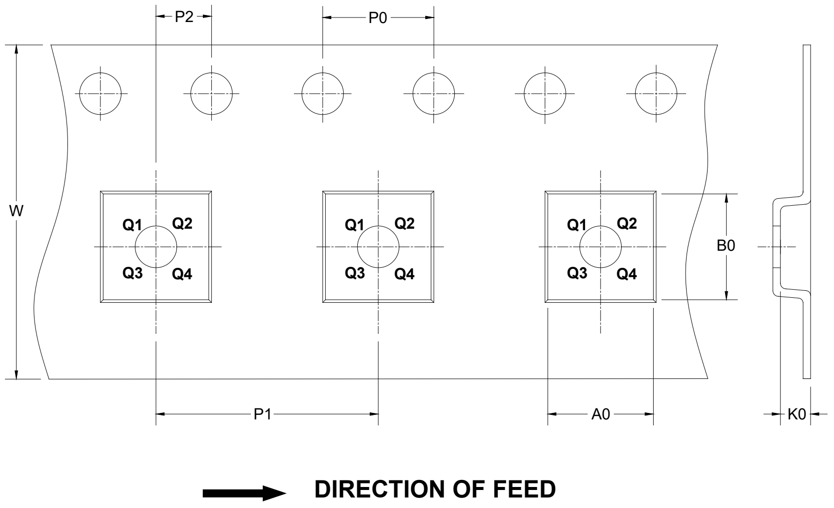
NOTES:
1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.2mm per side.
3. Reference JEDEC MO-203.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



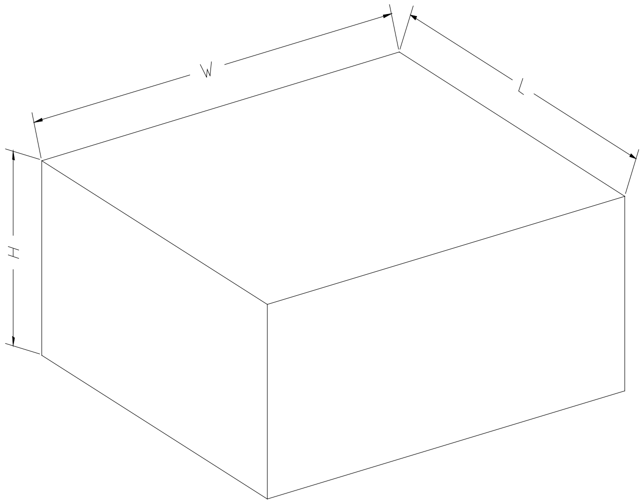
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-6	7"	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002