SGM8258-1/SGM8258-2/SGM8258-4
10MHz, High Voltage, High Precision, Low Noise, RRIO, Operational Amplifiers

GENERAL DESCRIPTION

The SGM8258-1/2/4 are a family of single, dual and quad operational amplifiers, which are optimized for low noise, high precision and high voltage operation. These devices can operate from 4.5V to 36V single supply or ±2.25V to ±18V dual supplies. They provide rail-to-rail input and output operation.

The SGM8258-1/2/4 offer a low offset voltage of ±12μV (SGM8258-4 MAX) and a low bias current. The combination of characteristics makes them good choices for temperature measurements, pressure and position sensors, strain gauge amplifiers and medical instrumentation, or any other 4.5V to 36V applications requiring precision, long-term stability and low drifting.

The SGM8258-1 is available in Green SOT-23-5 and SOIC-8 packages. The SGM8258-2 is available in Green SOIC-8 and MSOP-8 packages. The SGM8258-4 is available in Green SOIC-14 and TSSOP-14 packages. They are rated over the -40℃ to +125℃ temperature range.

FEATURES

- **Low Offset Voltage:**
  - **SGM8258-1/2: ±2μV (TYP), ±10μV (MAX)**
  - **SGM8258-4: ±2μV (TYP), ±12μV (MAX)**
- **0.1Hz to 10Hz Noise: 0.2μV_{P-P}**
- **Input Voltage Noise Density: 10.5nV/$\sqrt{Hz}$ at 1kHz**
- **Open-Loop Voltage Gain: 155dB (TYP)**
- **CMRR:**
  - **145dB (TYP)**
  - **57dB (TYP) at 1MHz**
- **PSRR: 146dB (TYP)**
- **Gain-Bandwidth Product: 10MHz**
- **Overload Recovery Time: 0.5μs**
- **Rail-to-Rail Input and Output**
- **Supply Voltage Range: 4.5V to 36V**
- **Low Quiescent Current: 1.5mA/Amplifier (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8258-1 Available in Green SOT-23-5 and SOIC-8 Packages
  SGM8258-2 Available in Green SOIC-8 and MSOP-8 Packages
  SGM8258-4 Available in Green SOIC-14 and TSSOP-14 Packages

APPLICATIONS

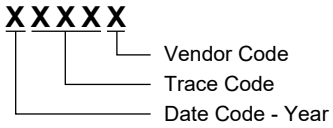
Industrial Equipment
Telecom Equipment
Medical Instrumentation

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8258-1	SOT-23-5	-40℃ to +125℃	SGM8258-1XN5G/TR	2AV XXXXX	Tape and Reel, 3000
	SOIC-8	-40℃ to +125℃	SGM8258-1XS8G/TR	SGM 82581XS8 XXXXX	Tape and Reel, 4000
SGM8258-2	SOIC-8	-40℃ to +125℃	SGM8258-2XS8G/TR	SGM 82582XS8 XXXXX	Tape and Reel, 4000
	MSOP-8	-40℃ to +125℃	SGM8258-2XMS8G/TR	SGM2TC XMS8 XXXXX	Tape and Reel, 4000
SGM8258-4	SOIC-14	-40℃ to +125℃	SGM8258-4XS14G/TR	SGM82584XS14 XXXXX	Tape and Reel, 2500
	TSSOP-14	-40℃ to +125℃	SGM8258-4XTS14G/TR	SGM82584 XTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Voltage Range ..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Common Mode Voltage Range
..... $(-V_S)$ - 0.1V to $(+V_S)$ + 0.1V
Differential Input Voltage Range ..... $-V_S$ to $+V_S$
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 148.7℃/W
SOT-23-5, θ_{JB} ..... 28.2℃/W
SOIC-8, θ_{JA} (SGM8258-1) ..... 136.8℃/W
SOIC-8, θ_{JB} (SGM8258-1) ..... 78.3℃/W
SOIC-8, θ_{JA} (SGM8258-2) ..... 116.3℃/W
SOIC-8, θ_{JB} (SGM8258-2) ..... 65.3℃/W
MSOP-8, θ_{JA} ..... 135.2℃/W
MSOP-8, θ_{JB} ..... 77.2℃/W
SOIC-14, θ_{JA} ..... 76.4℃/W
SOIC-14, θ_{JB} ..... 32.7℃/W
TSSOP-14, θ_{JA} ..... 91.3℃/W
TSSOP-14, θ_{JB} ..... 54.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±6000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Voltage Range ..... 4.5V to 36V
Operating Temperature Range ..... -40℃ to +125℃

NOTE: The power-on time of $+V_S$ should be greater than 35μs from 0V to 36V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

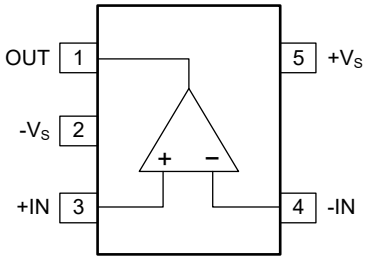
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

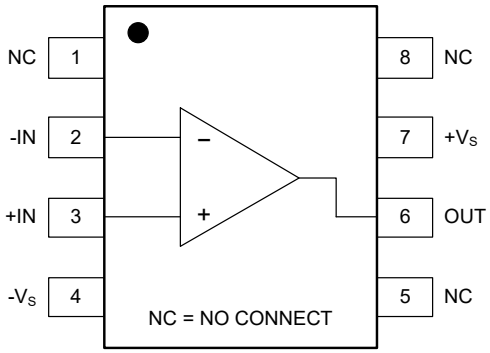
PIN CONFIGURATIONS

SGM8258-1 (TOP VIEW)



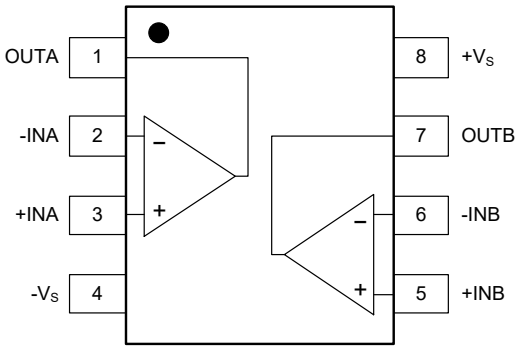
SOT-23-5

SGM8258-1 (TOP VIEW)



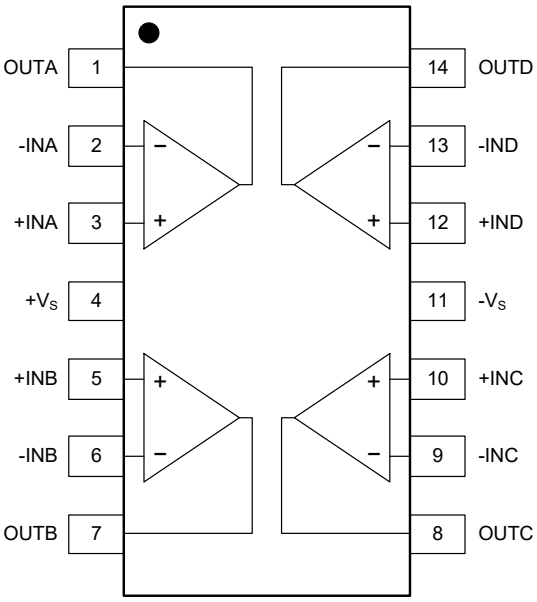
SOIC-8

SGM8258-2 (TOP VIEW)



SOIC-8/MSOP-8

SGM8258-4 (TOP VIEW)



SOIC-14/TSSOP-14

PIN DESCRIPTION

Table 1. SGM8258-1 Pin Description

PIN		NAME	TYPE	FUNCTION
SOT-23-5	SOIC-8			
1	6	OUT	O	Output.
2	4	$-V_S$	—	Negative Power Supply.
3	3	+IN	I	Non-Inverting Input.
4	2	-IN	I	Inverting Input.
5	7	$+V_S$	—	Positive Power Supply.
—	1, 5, 8	NC	—	No Internal Connection.

NOTE: I = input, O = output.

Table 2. SGM8258-2 Pin Description

PIN	NAME	TYPE	FUNCTION
SOIC-8/MSOP-8			
1	OUTA	O	Output of Amplifier A.
2	-INA	I	Inverting Input of Amplifier A.
3	+INA	I	Non-Inverting Input of Amplifier A.
4	$-V_S$	—	Negative Power Supply.
5	+INB	I	Non-Inverting Input of Amplifier B.
6	-INB	I	Inverting Input of Amplifier B.
7	OUTB	O	Output of Amplifier B.
8	$+V_S$	—	Positive Power Supply.

NOTE: I = input, O = output.

Table 3. SGM8258-4 Pin Description

PIN	NAME	TYPE	FUNCTION
SOIC-14/TSSOP-14			
1	OUTA	O	Output of Amplifier A.
2	-INA	I	Inverting Input of Amplifier A.
3	+INA	I	Non-Inverting Input of Amplifier A.
4	$+V_S$	—	Positive Power Supply.
5	+INB	I	Non-Inverting Input of Amplifier B.
6	-INB	I	Inverting Input of Amplifier B.
7	OUTB	O	Output of Amplifier B.
8	OUTC	O	Output of Amplifier C.
9	-INC	I	Inverting Input of Amplifier C.
10	+INC	I	Non-Inverting Input of Amplifier C.
11	$-V_S$	—	Negative Power Supply.
12	+IND	I	Non-Inverting Input of Amplifier D.
13	-IND	I	Inverting Input of Amplifier D.
14	OUTD	O	Output of Amplifier D.

NOTE: I = input, O = output.

ELECTRICAL CHARACTERISTICS

(V_S = ±2.25V to V_S = ±18V, V_{CM} = 0V and R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}	SGM8258-1/2	+25℃		±2	±10	μV
			Full			±12	
		SGM8258-4	+25℃		±2	±12	
			Full			±15	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		9		nV/℃
Input Bias Current	I_B		+25℃		±150	±400	pA
			+85℃			±900	pA
			Full			±15	nA
Input Offset Current	I_{OS}		+25℃		±250	±1400	pA
			+85℃			±1500	pA
			Full			±5.5	nA
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio (1)	CMRR	V_S = 5V, V_{CM} = $(-V_S)$ - 0.1V to $(+V_S)$ + 0.1V	+25℃	108	125		dB
			Full	104			
		V_S = 5V, V_{CM} = $(-V_S)$ - 0.1V to $(+V_S)$ - 3V	+25℃	110	136		
			Full	106			
		V_S = 36V, V_{CM} = $(-V_S)$ - 0.1V to $(+V_S)$ + 0.1V	+25℃	118	145		
			Full	115			
		V_S = 36V, V_{CM} = $(-V_S)$ - 0.1V to $(+V_S)$ - 3V	+25℃	126	158		
			Full	120			
Open-Loop Voltage Gain	A_{OL}	V_S = ±2.5V, V_{OUT} = ±2V	+25℃	122	145		dB
			Full	118			
		V_S = ±18V, V_{OUT} = ±17.5V	+25℃	118	155		
			Full	115			
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±2.5V	+25℃		10	20	mV
			Full			27	
		V_S = ±18V	+25℃		80	110	
			Full			150	
Output Short-Circuit Current	I_{SC}	V_S = ±2.5V	+25℃	±30	±40		mA
		V_S = ±18V	+25℃	±35	±55		

NOTE: 1. PSRR and CMRR are affected by the matching between external gain-setting resistor ratios.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±2.25V to V_S = ±18V, V_{CM} = 0V and R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

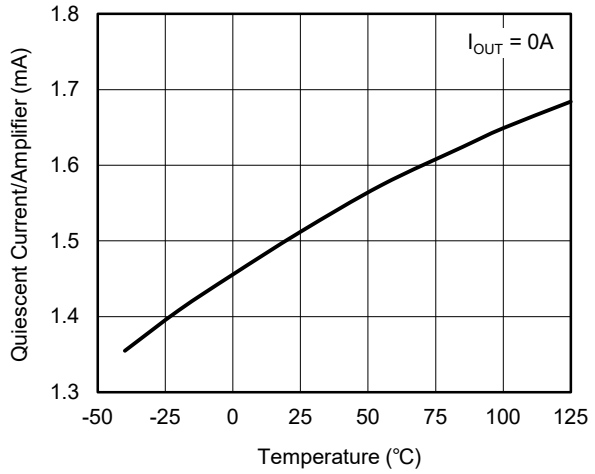
PARAMETER		SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Power Supply								
Operating Voltage Range		V_S		Full	4.5		36	V
Power Supply Rejection Ratio (1)		PSRR	V_S = 4.5V to 36V	+25℃	126	146		dB
				Full	120			
Quiescent Current/Amplifier		I_Q	I_{OUT} = 0A	+25℃		1.5	2	mA
				Full			2.5	
Dynamic Performance								
Gain-Bandwidth Product		GBP	V_{OUT} = 100mV_{P-P}, C_L = 10pF, G = +1	+25℃		10		MHz
			V_{OUT} = 100mV_{P-P}, C_L = 10pF, G = +1000	+25℃		15		
Slew Rate		SR	V_S = ±18V, V_{OUT} = 10V_{P-P}	+25℃		18		V/μs
Phase Margin		φ_O	C_L = 10pF	+25℃		55		°
Common Mode Rejection Ratio		CMRR	f = 1MHz	+25℃		57		dB
Settling Time	To 0.1%	t_S	V_{IN} = 1V Step	+25℃		12		μs
	To 1%	t_S		+25℃		1.1		μs
Overload Recovery Time		ORT	V_{IN} × G > V_S	+25℃		0.5		μs
Total Harmonic Distortion + Noise		THD+N	V_{IN} = 2V_{P-P}, G = +1, f = 1kHz	+25℃		0.0003		%
Noise								
Input Voltage Noise			f = 0.1Hz to 10Hz	+25℃		0.2		μV_{P-P}
Input Voltage Noise Density		e_n	f = 0.1kHz	+25℃		10.5		nV/√Hz
			f = 1kHz	+25℃		10.5		
			f = 10kHz	+25℃		10.5		

NOTE: 1. PSRR and CMRR are affected by the matching between external gain-setting resistor ratios.

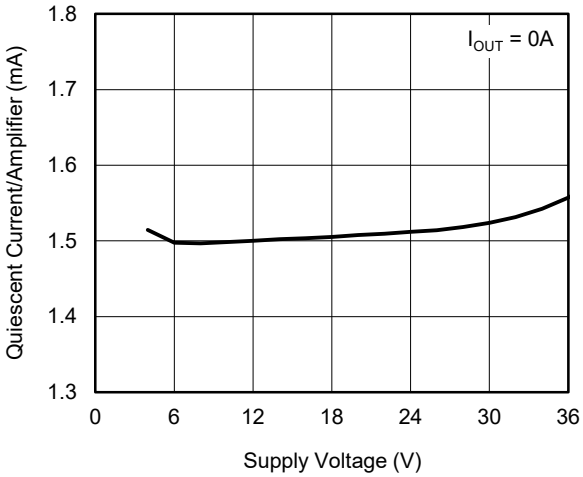
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±18V, unless otherwise noted.

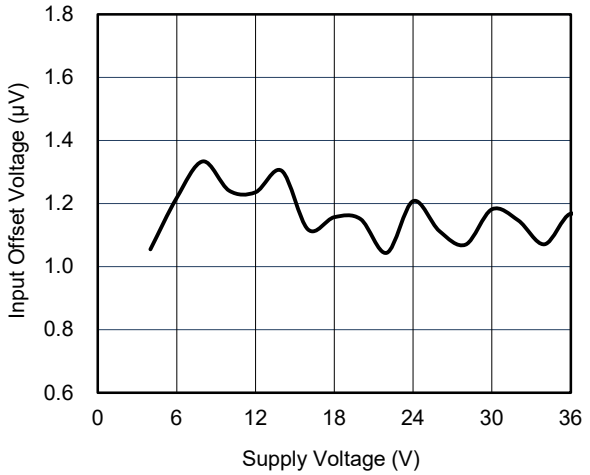
Quiescent Current vs. Temperature



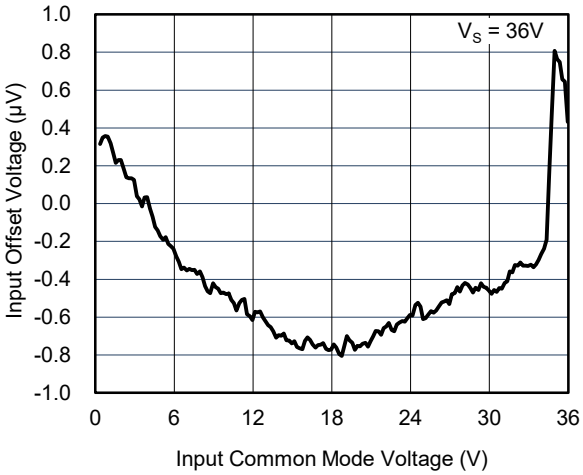
Quiescent Current vs. Supply Voltage



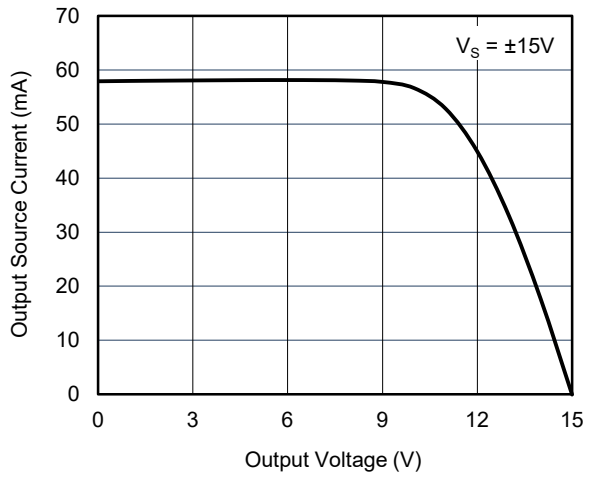
Input Offset Voltage vs. Supply Voltage



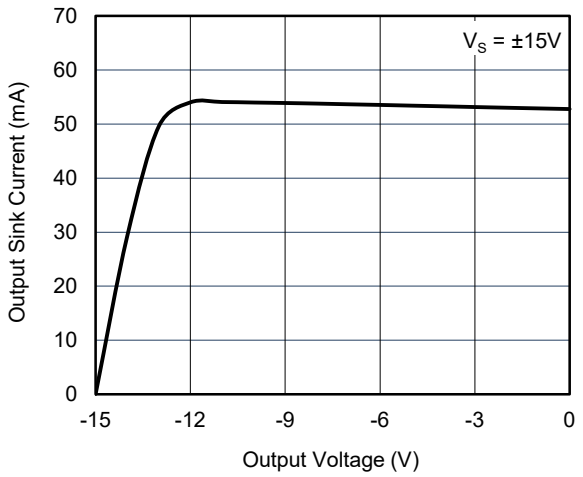
Input Offset Voltage vs. Input Common Mode Voltage



Output Source Current vs. Output Voltage



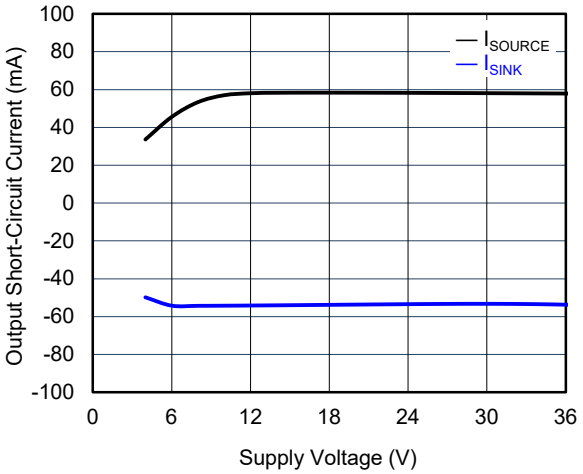
Output Sink Current vs. Output Voltage



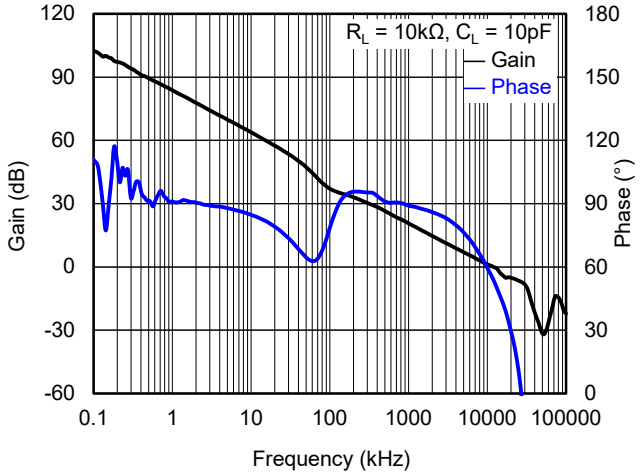
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, unless otherwise noted.

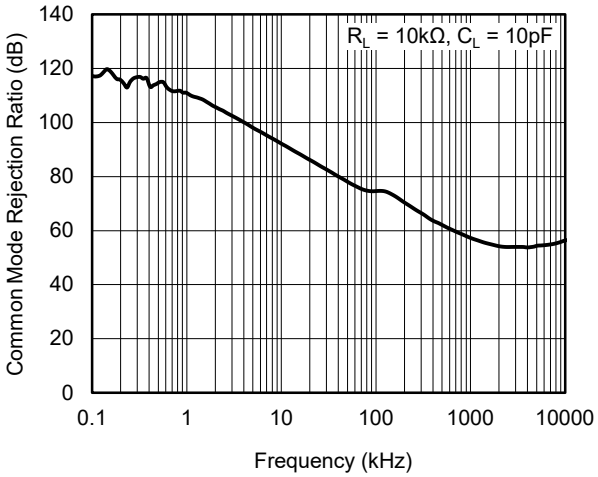
Output Short-Circuit Current vs. Supply Voltage



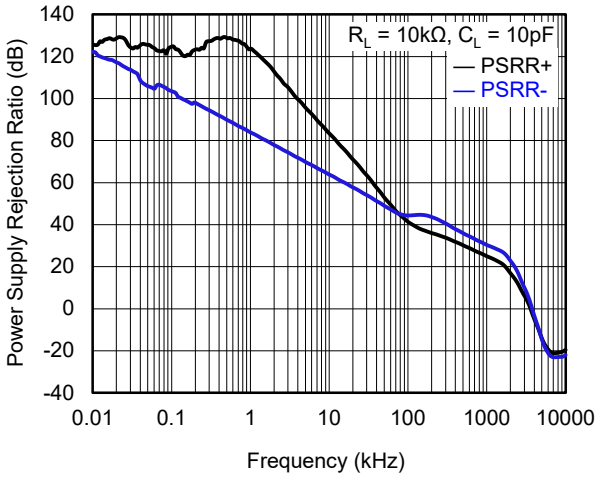
Open-Loop Gain and Phase vs. Frequency



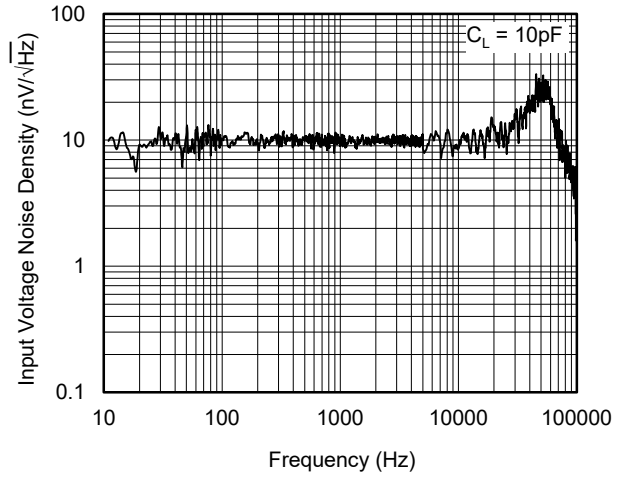
CMRR vs. Frequency



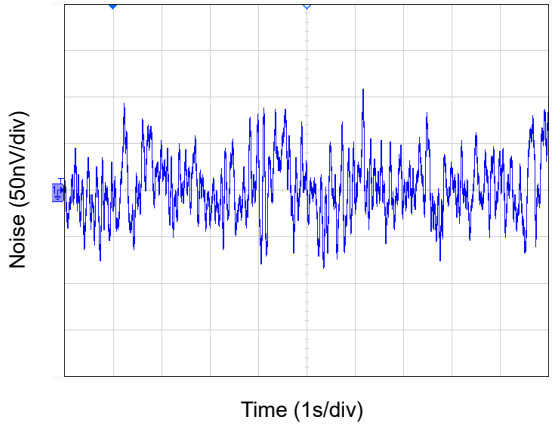
PSRR vs. Frequency



Input Voltage Noise Density vs. Frequency



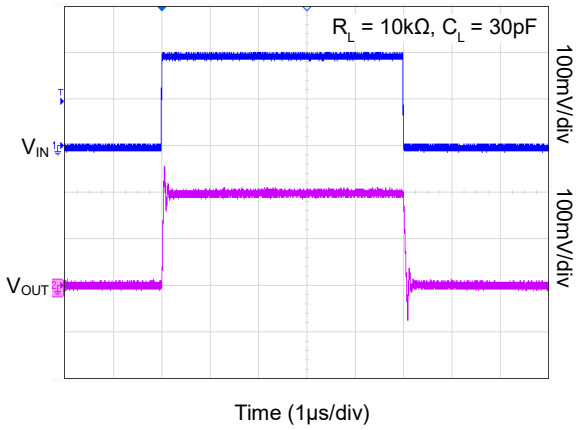
0.1Hz to 10Hz Input Voltage Noise



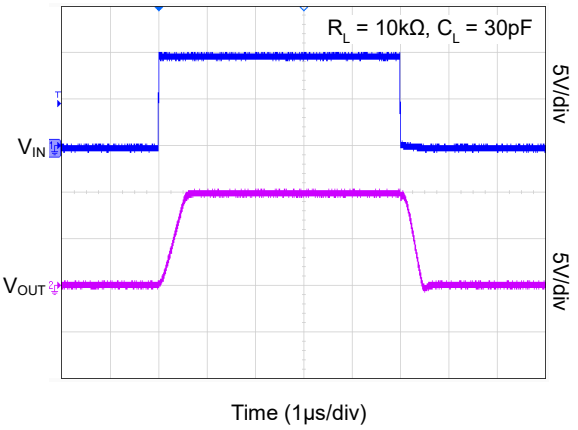
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, unless otherwise noted.

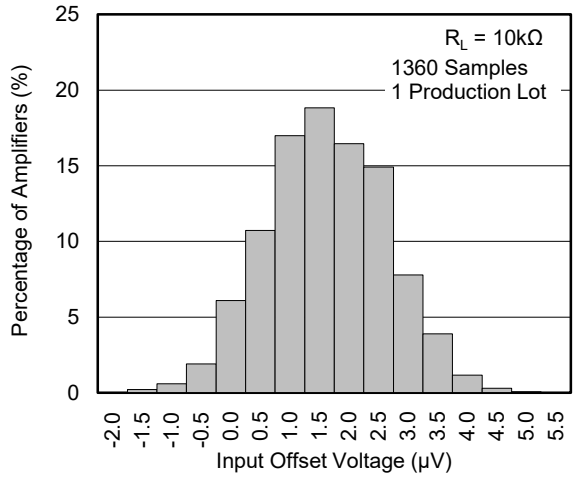
Small-Signal Step Response



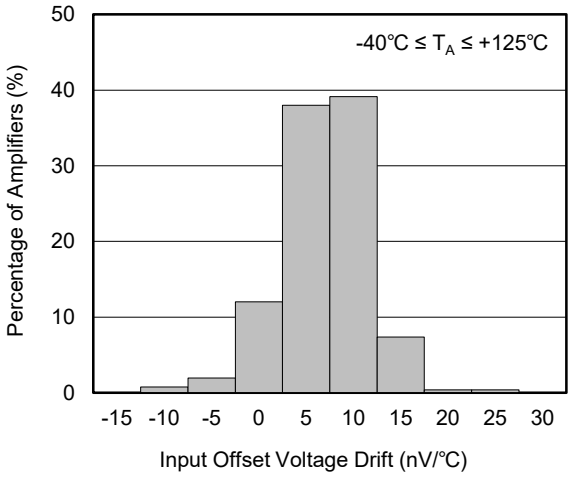
Large-Signal Step Response



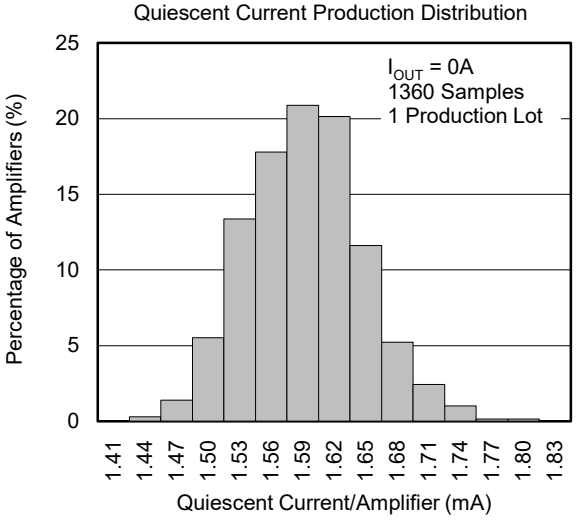
Input Offset Voltage Production Distribution



Input Offset Voltage Drift Distribution



Quiescent Current Production Distribution



APPLICATION INFORMATION

Rail-to-Rail Input

When SGM8258-1/2/4 work at the power supply between 4.5V and 36V, the input common mode voltage range is from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage so that it does not exceed the rails.

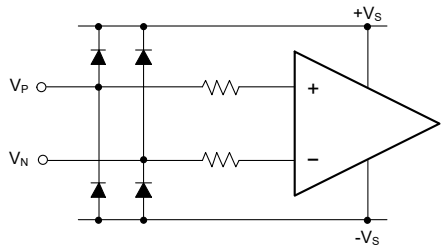


Figure 1. Input Equivalent Circuit

Rail-to-Rail Output

The SGM8258-1/2/4 support rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 36V, $-V_S$ = GND, 10kΩ load resistor is tied from OUT pin to ground, the typical output swing range is from 0V to 35.92V.

Driving Capacitive Loads

The SGM8258-1/2/4 are unity-gain stable with heavy capacitive load. If greater capacitive load must be driven in application, the circuit in Figure 2 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

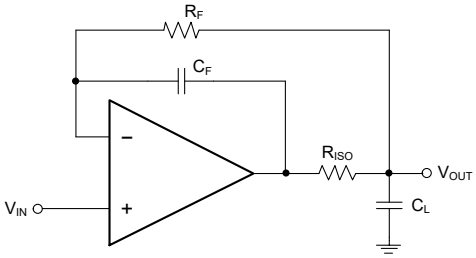


Figure 2. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design. Besides of input signal noise, the power supply is one of important source of noise to the amplifier through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 3. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

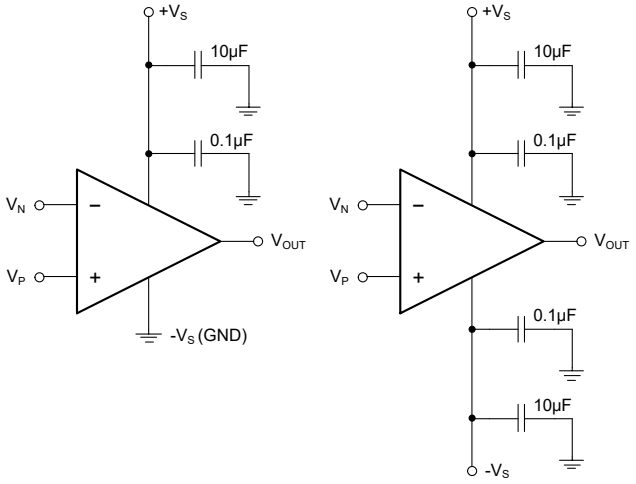


Figure 3. Amplifier Power Supply Bypassing

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in the same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

APPLICATION INFORMATION (continued)

Typical Application Circuits

Difference Amplifier

The circuit in Figure 4 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

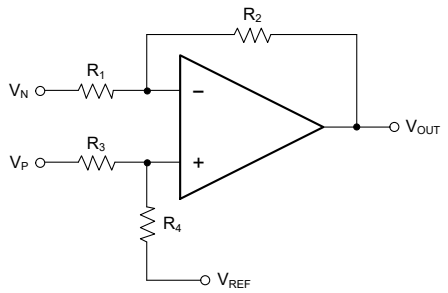


Figure 4. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 5 is a design example of high input impedance difference amplifier. The added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 4.

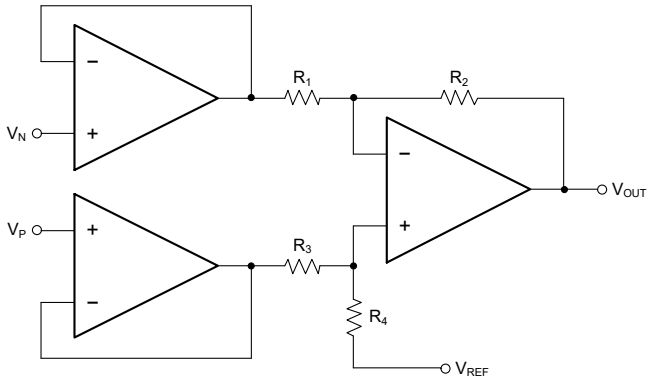


Figure 5. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 6 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/(2\pi R_2 C)$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, and the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

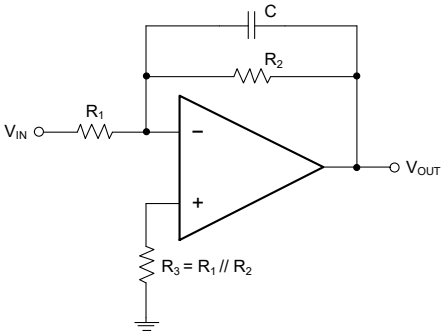


Figure 6. Active Low-Pass Filter

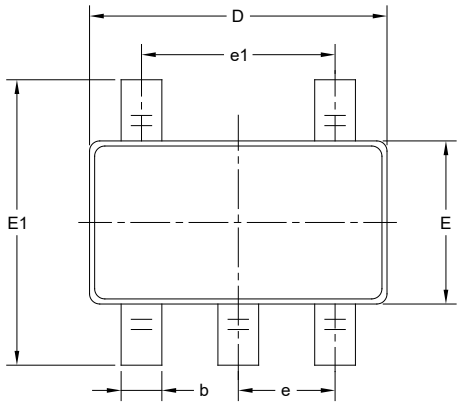
REVISION HISTORY

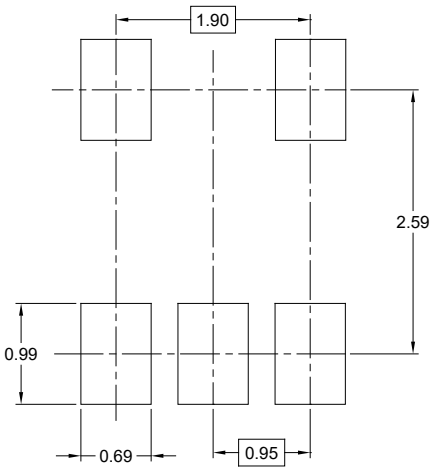
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

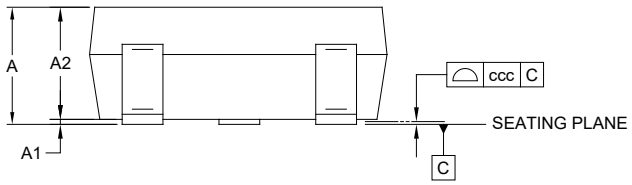
PACKAGE OUTLINE DIMENSIONS

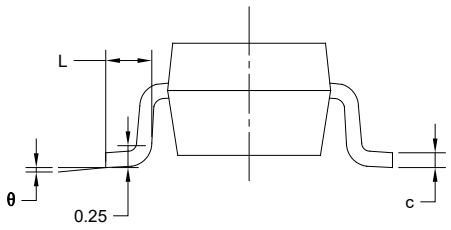
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



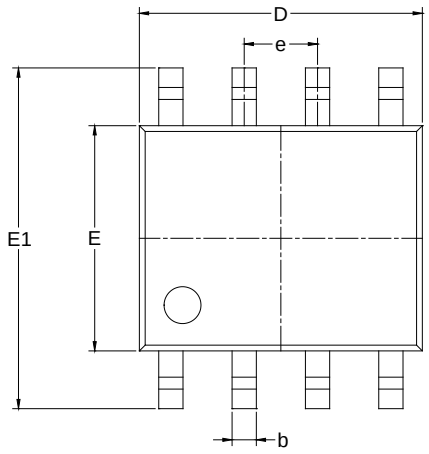


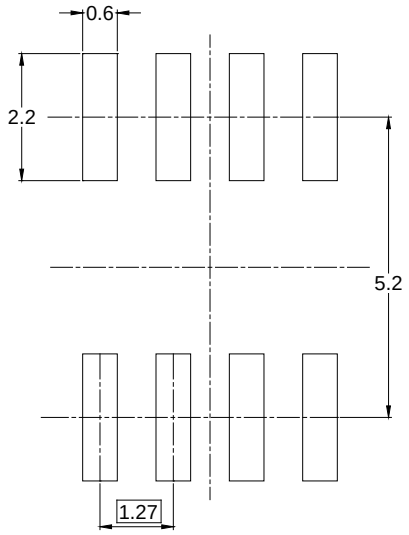
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

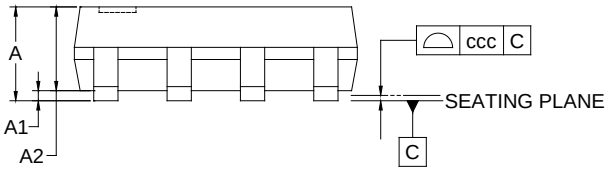
PACKAGE OUTLINE DIMENSIONS

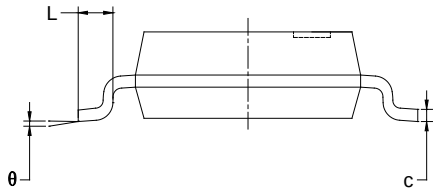
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



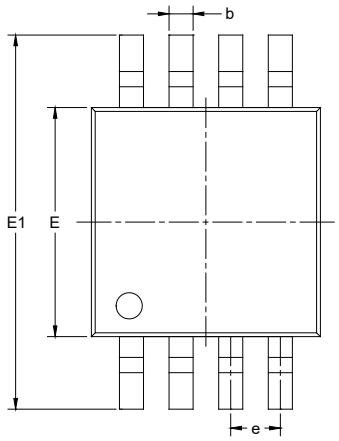


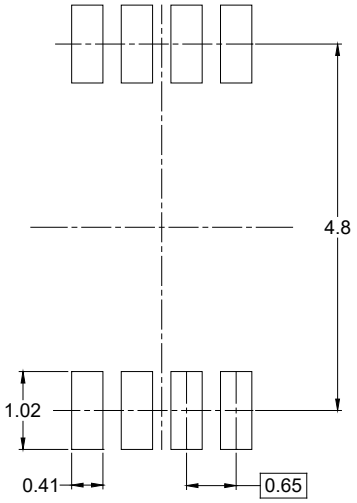
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.350	-	1.550
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Reference JEDEC MS-012.

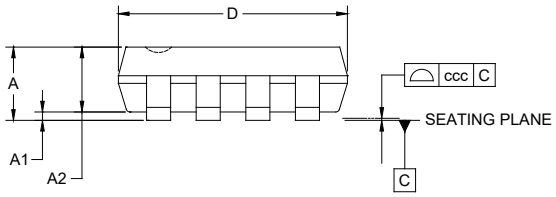
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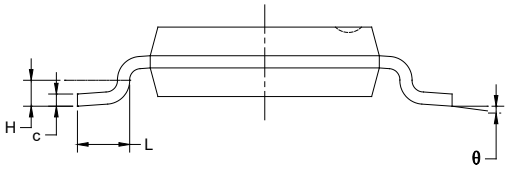
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



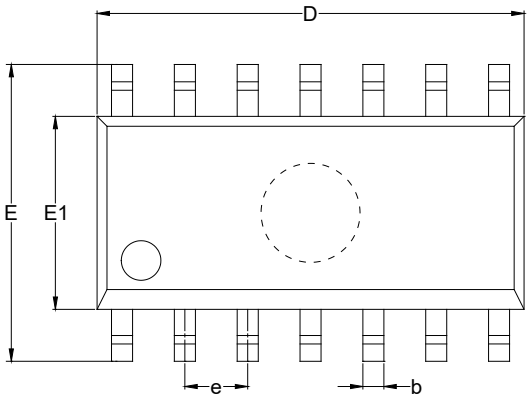


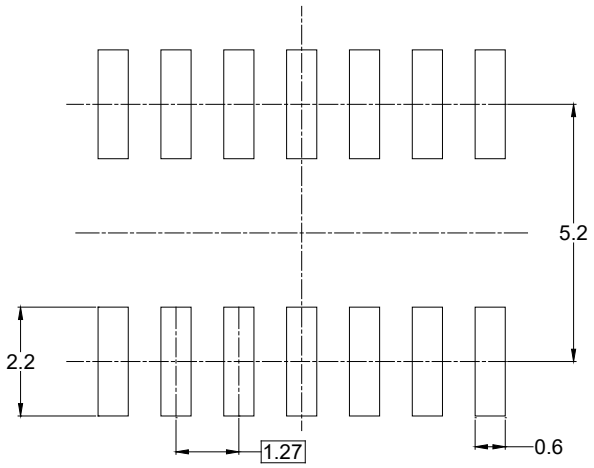
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.220	-	0.380
c	0.080	-	0.230
D	2.800	-	3.200
E	2.800	-	3.200
E1	4.650	-	5.150
e	0.650 BSC		
L	0.400	-	0.800
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

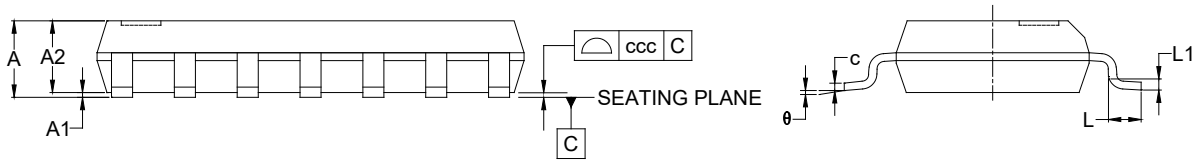
PACKAGE OUTLINE DIMENSIONS

SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)

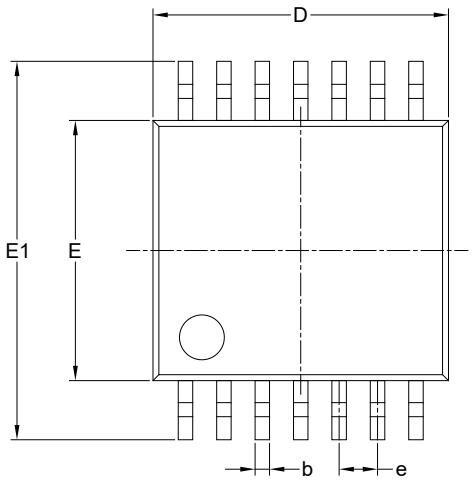


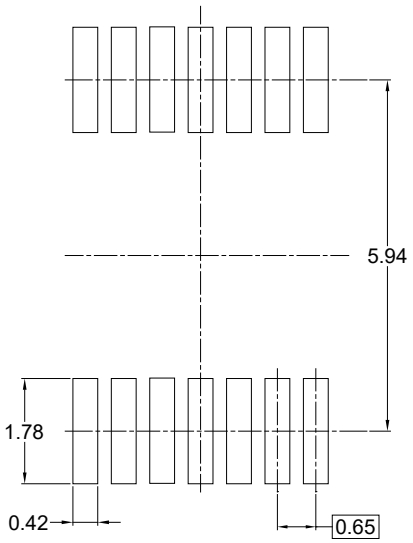
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.100	-	0.250
D	8.450	-	8.850
E	5.800	-	6.200
E1	3.800	-	4.000
e	1.270 BSC		
L	0.400	-	1.270
L1	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

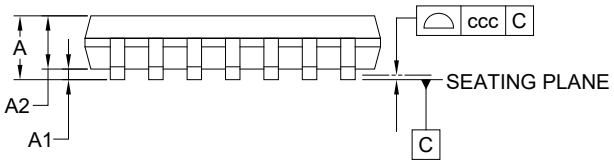
PACKAGE OUTLINE DIMENSIONS

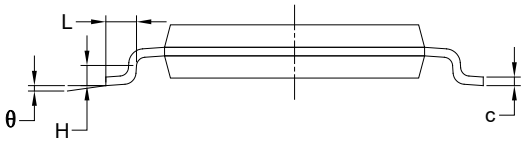
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



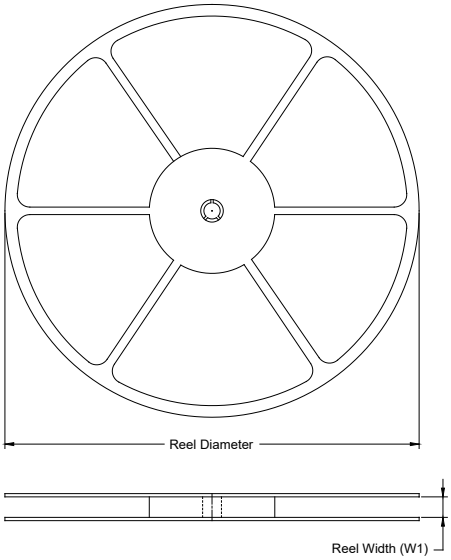


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

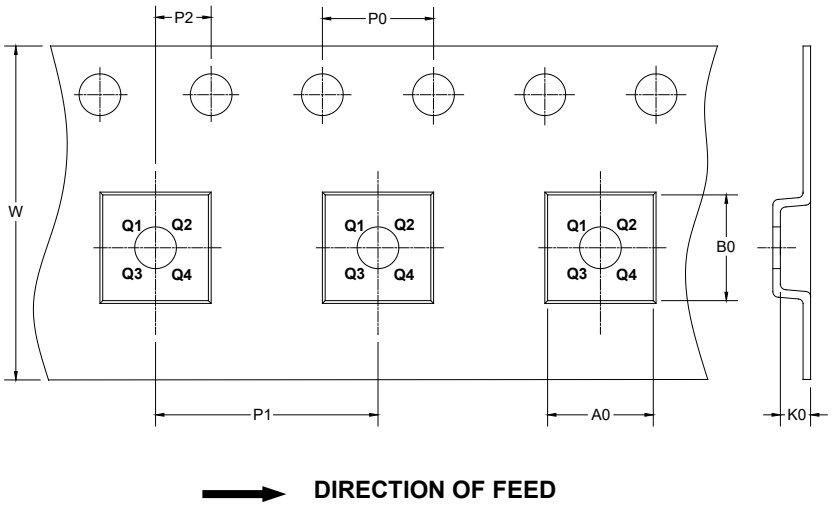
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



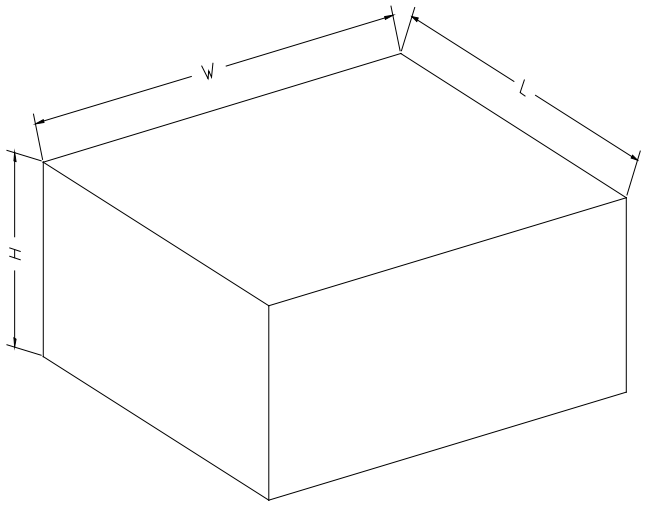
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-14	13″	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002