SGM257050
60V, 2A with Integrated Reverse Input Polarity Protection Industrial eFuse

GENERAL DESCRIPTION

The SGM257050 device is a compact and feature-rich high-voltage eFuse family, which offers comprehensive protection features. With a broad supply input range of 4.2V to 60V, it is suitable for controlling many commonly used DC bus voltages. The device has the ability to handle and protect loads from negative -60V up to positive +60V supply voltages. Reverse current blocking is allowed by the integrated back-to-back MOSFETs, so if the systems require output voltage hold-up during power failures and brownout conditions, the device is an ideal choice. It offers source, device, and load protection with numerous adjustable features, including over-current protection, output slew rate control, and over-voltage and under-voltage thresholds. The SGM257050 incorporates strong internal protection control blocks and a high voltage rating, making it easier to design systems with effective surge protection.

The nSHDN pin allows external control, which can activate or deactivate the internal MOSFETs, and switch the device into a low power shutdown mode. For system-status monitoring and downstream-loads controlling, the device offers fault indicators and a precise analog current monitor. Additionally, the MODE pin enables configuration among three different current-limiting fault responses: auto-retry, latch-off, or circuit breaker modes.

The SGM257050 is available in Green TSSOP-16B (Exposed Pad) and TQFN-4×5-24AL packages.

SIMPLIFIED SCHEMATIC

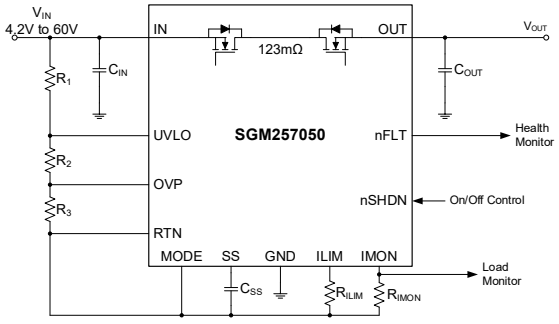


Figure 1. Simplified Schematic

FEATURES

- **Recommend Operating Voltage 4.2V to 60V, DC Maximum 60V, Absolute Maximum 62V**
- **Up to -60V Integrated Reverse Input Polarity Protection**
  - **Zero Additional Components Required**
- **Integrated Back-to-Back MOSFETs Total On-Resistance (R_{ON}): 123mΩ**
- **Adjustable Current Limit (±5.5% Accuracy at 1A): 0.1A to 2.24A**
- **Functional Safety Capable**
  - **Documentation Available to Aid in the Design of Functional Safety System**
- **Load Protection during Surge (IEC 61000-4-5) with Minimum External Components**
- **IMON Output**
  - **±16.5% Accuracy with I_{OUT} = 0.1A to 0.5A**
  - **±7% Accuracy with I_{OUT} = 0.5A to 1A**
  - **±5% Accuracy with I_{OUT} = 1A to 2A**
- **Low Quiescent Current, 255μA in Operating, 14μA in Shutdown**
- **Adjustable UVLO, OVLO, Output Slew Rate Control for Inrush Current Control**
- **Reverse Current Blocking**
- **Fixed 37.5V Over-Voltage Clamp (SGM257050C Only)**
- **Selectable Options for Current-Limiting Fault Response**
  - **Auto-Retry**
  - **Latch-Off**
  - **Circuit Breaker Modes**
- **Available in Green TSSOP-16B (Exposed Pad) and TQFN-4×5-24AL Packages**

APPLICATIONS

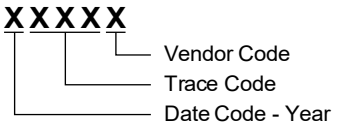
Programmable Logic Controller
Distributed Control System (DCS)
Control and Automation
Redundant Supply ORing
Industrial Surge Protection

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM257050A	TSSOP-16B (Exposed Pad)	-40℃ to +125℃	SGM257050AXPTS16G/TR	SGM39P XPTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×5-24AL	-40℃ to +125℃	SGM257050AXTQY24G/TR	SGM3BN XTQY24 XXXXX	Tape and Reel, 3000
SGM257050B	TQFN-4×5-24AL	-40℃ to +125℃	SGM257050BXTQY24G/TR	SGM3BO XTQY24 XXXXX	Tape and Reel, 3000
SGM257050C	TSSOP-16B (Exposed Pad)	-40℃ to +125℃	SGM257050CXPTS16G/TR	SGM39Q XPTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×5-24AL	-40℃ to +125℃	SGM257050CXTQY24G/TR	SGM3BP XTQY24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

SELECTABLE MODEL

Model	Over-Voltage Protection	Over Load Fault Response with MODE = Open
SGM257050A	Over-Voltage Cut-Off, Adjustable	Circuit Breaker with Auto-Retry
SGM257050B	Over-Voltage Cut-Off, Adjustable	Circuit Breaker with Latch
SGM257050C	Over-Voltage Clamp, Fixed (37.5V)	Circuit Breaker with Auto-Retry

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- IN, IN to OUT ..... -60V to 62V
- IN, IN to OUT (10ms Transient, T_A = +25℃)..... -70V to 70V
- IN, OUT, nFLT, UVLO, nSHDN to RTN ..... -0.3V to 62V
- OVP, SS, ILIM, IMON, MODE to RTN ..... -0.3V to 5V
- RTN ..... -60V to 0.3V

Sink Current, I_{nFLT}, I_{SS}, I_{nSHDN} 10mA

Source Current, I_{SS}, I_{ILIM}, I_{IMON} ..... Internally Limited

Package Thermal Resistance
- TSSOP-16B (Exposed Pad), θ_{JA} ..... 29.6℃/W
- TSSOP-16B (Exposed Pad), θ_{JB} ..... 10.6℃/W
- TSSOP-16B (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 27.6℃/W
- TSSOP-16B (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.4℃/W
- TQFN-4×5-24AL, θ_{JA} ..... 30℃/W
- TQFN-4×5-24AL, θ_{JB} ..... 9℃/W
- TQFN-4×5-24AL, $\theta_{JC\ (TOP)}$ ..... 19.4℃/W
- TQFN-4×5-24AL, $\theta_{JC\ (BOT)}$ ..... 1℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±3000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
- IN ..... -55V to 60V
- UVLO, OUT, nFLT, nSHDN ..... 0V to 60V
- OVP, SS, ILIM, IMON ..... 0V to 4V

Resistance
- ILIM ..... 5.36kΩ to 120kΩ
- IMON ..... 1kΩ (MIN)

External Capacitance
- IN, OUT ..... 1μF (MIN)
- SS ..... 10nF (MIN)

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

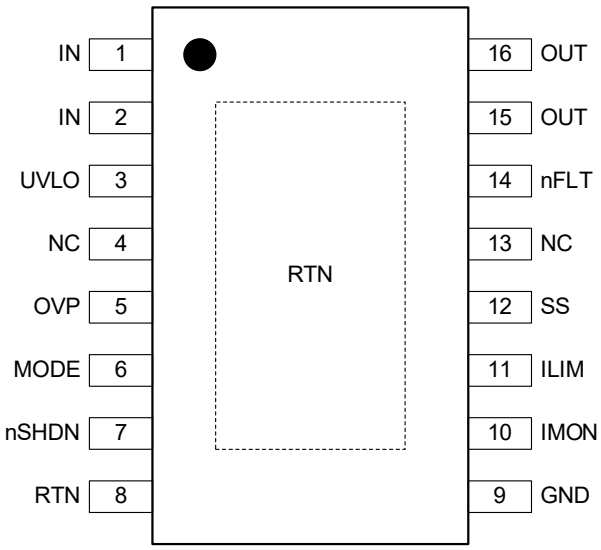
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

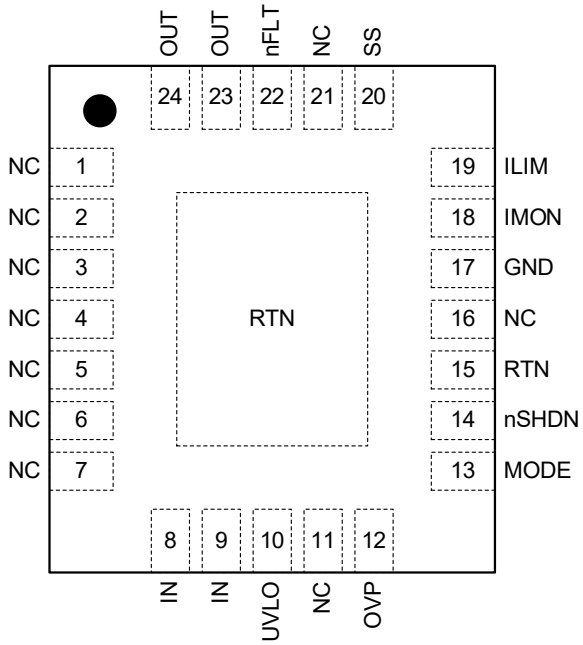
PIN CONFIGURATIONS

SGM257050A/C (TOP VIEW)



TSSOP-16B (Exposed Pad)

SGM257050A/B/C (TOP VIEW)



TQFN-4×5-24AL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TSSOP	TQFN			
1, 2	8, 9	IN	P	Power Input and Supply Voltage.
3	10	UVLO	I	This input sets the programmable under-voltage lockout threshold. When an under-voltage condition occurs, the internal MOSFET is turned off and nFLT is asserted to signal a power failure. To use the internal default threshold, connect the UVLO pin to the RTN pin.
4, 13	1, 2, 3, 4, 5, 6, 7, 11, 16, 21	NC	-	No Connection.
5	12	OVP	I	This input configures the programmable over-voltage protection threshold (SGM257050A/B only). During an over-voltage event, the internal MOSFET is turned off and nFLT is asserted to indicate the fault. To use the internal default threshold, connect the OVP pin to the RTN pin externally. For over-voltage clamp response (SGM257050C only), also connect the OVP pin to the RTN pin externally.
6	13	MODE	I	Mode Selection Pin for Overload Fault Response.
7	14	nSHDN	I	Shutdown Pin. Pulling the nSHDN pin low switches the device into low power shutdown mode. Toggle this pin to reset the device latched off upon a fault condition.
8	15	RTN	-	Device Internal Control Circuits Reference.
9	17	GND	G	Connect to System Ground.
10	18	IMON	O	Analog Current Monitor Output. This pin sources a current that is proportionally reduced to the current flowing through the MOSFET. To convert this current into a proportional voltage, connect a resistor between this pin and RTN. If unused, leave it floating.
11	19	ILIM	I/O	A resistor from this pin to RTN sets the overload and short-circuit current limit.
12	20	SS	I/O	Soft-Start Pin. Connect a capacitor between this pin and GND to set the output voltage slew rate.
14	22	nFLT	O	Fault Event Indicator. It is an open-drain output. If unused, leave the pin floating.
15, 16	23, 24	OUT	P	Power Output of the Device.
Exposed Pad	Exposed Pad	RTN	-	Connect it to RTN for Heat Sinking. Cannot be used as the only electrical connection to RTN.

NOTE: G = ground, P = power, I = input, O = output, I/O = input/output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 120kΩ, IMON = nFLT = open, C_{OUT} = 1μF, C_{SS} = open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Operating Input Voltage	V_{IN}		4.2		60	V
Internal POR Threshold, Rising	V_{PORR}		3.8	3.97	4.14	V
Internal POR Hysteresis	V_{POR_HYS}		232	257	282	mV
Supply Current	I_{Q_ON}	Enabled: V_{nSHDN} = 2V	160	255	350	μA
	I_{Q_OFF}	V_{nSHDN} = 0V	6	14	23	μA
Reverse Input Supply Current	I_{VINR}	V_{IN} = -60V, V_{OUT} = 0V			45	μA
Over-Voltage Clamp	V_{OVC}	V_{IN} > 42V, SGM257050C only	35.5	37.5	39.5	V
Under-Voltage Lockout (UVLO) Input						
Factory Set V_{IN} Under-Voltage Trip Level	V_{IN_UVLO}	V_{IN} rising, V_{UVLO} = 0V	14.25	14.9	15.45	V
		V_{IN} falling, V_{UVLO} = 0V	13.15	13.8	14.35	
Internal UVLO Select Threshold	V_{SEL_UVLO}		180	200	220	mV
UVLO Threshold Voltage, Rising	V_{UVLOR}		1.165	1.19	1.217	V
UVLO Threshold Voltage, Falling	V_{UVLOF}		1.074	1.1	1.126	V
UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to 60V	-150	0	150	nA
Low I_Q Shutdown (nSHDN) Input						
Output Voltage	V_{nSHDN}	I_{nSHDN} = 0.1μA	3.05	3.45	3.85	V
nSHDN Threshold Rising	V_{nSHDNR}	V_{IN} = 4.2V to 60V	1.2			V
nSHDN Threshold Voltage for Low I_Q Shutdown, Falling	V_{nSHDNF}	V_{IN} = 4.2V to 60V			0.6	V
Leakage Current	I_{nSHDN}	V_{nSHDN} = 0V	-6			μA
Over-Voltage Protection (OVP) Input - SGM257050A/B Only						
Factory Set V_{IN} Over-Voltage Trip Level	V_{IN_OVP}	V_{IN} rising, V_{OVP} = 0V	31	32.6	34	V
		V_{IN} falling, V_{OVP} = 0V	28.5	30.3	31.5	
Internal OVP Select Threshold	V_{SEL_OVP}		180	200	220	mV
Over-Voltage Threshold Voltage, Rising	V_{OVPR}		1.165	1.19	1.217	V
Over-Voltage Threshold Voltage, Falling	V_{OVPF}		1.074	1.1	1.126	V
OVP Input Leakage Current	I_{OVP}	V_{OVP} = 0V to 4V	-100	0	100	nA
Output Ramp Control (SS)						
SS Charging Current	I_{SS}	V_{SS} = 0V	3.48	4.84	6.2	μA
SS Discharging Resistance	R_{SS}	V_{nSHDN} = 0V, with I_{SS} = 10mA sinking		14.5		Ω
SS to OUT Gain	$GAIN_{SS}$	V_{OUT}/V_{SS}	23.8	24.6	25.4	V/V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 120kΩ, IMON = nFLT = open, C_{OUT} = 1μF, C_{SS} = open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Programming (ILIM)						
ILIM Bias Voltage	V_{ILIM}			1		V
Overload Current Limit	I_{OL}	R_{ILIM} = 120kΩ, V_{IN} - V_{OUT} = 1V	0.085	0.1	0.115	A
		R_{ILIM} = 12kΩ, V_{IN} - V_{OUT} = 1V	0.945	1	1.055	
		R_{ILIM} = 8kΩ, V_{IN} - V_{OUT} = 1V	1.418	1.5	1.583	
		R_{ILIM} = 5.36kΩ, V_{IN} - V_{OUT} = 1V	2.117	2.24	2.363	
	$I_{OL_R\text{-}OPEN}$	R_{ILIM} = open, open resistor current limit		0.055		
	$I_{OL_R\text{-}SHORT}$	R_{ILIM} = short, shorted resistor current limit		0.095		
Circuit Breaker Detection Threshold	I_{CB}	R_{ILIM} = 120kΩ, MODE = open	0.085	0.1	0.115	A
		R_{ILIM} = 5.36kΩ, MODE = open	2.117	2.24	2.363	
Short-Circuit Current Limit	I_{SCL}	R_{ILIM} = 120kΩ, V_{IN} - V_{OUT} = 5V	0.085	0.1	0.115	A
		R_{ILIM} = 8kΩ, V_{IN} - V_{OUT} = 5V	1.418	1.5	1.583	
		R_{ILIM} = 5.36kΩ, V_{IN} - V_{OUT} = 5V	2.107	2.23	2.353	
Fast-Trip Comparator Threshold	$I_{FASTTRIP}$			1.87 × I_{OL} + 0.015		A
Current Monitor Output (IMON)						
Gain Factor I_{IMON}:I_{OUT}	$GAIN_{IMON}$	I_{OUT} = 0.1A to 0.5A	65.36	78.28	91.2	μA/A
		I_{OUT} = 0.5A to 1A	72.8	78.28	83.76	
		I_{OUT} = 1A to 2A	74.37	78.28	82.19	
Pass FET Output (OUT)						
IN to OUT Total On-Resistance	R_{ON}	I_{OUT} = 0.1A to 2A, T_J = +25℃	105	123	141	mΩ
		I_{OUT} = 0.1A to 2A, T_J = +85℃			195	
		I_{OUT} = 0.1A to 2A, T_J = -40℃ to +125℃	55	123	225	
OUT Leakage Current in Off-State	I_{LKG_OUT}	V_{IN} = 60V, V_{nSHDN} = 0V, V_{OUT} = 0V, sourcing			0.9	μA
		V_{IN} = 0V, V_{nSHDN} = 0V, V_{OUT} = 24V, sinking			13	
		V_{IN} = -60V, V_{nSHDN} = 0V, V_{OUT} = 0V, sinking			14	
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Falling	V_{REVTH}		-22	-14	-6	mV
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Rising	V_{FWDTH}		74	96	118	mV
Fault Flag (nFLT): Active Low						
nFLT Pull-Down Resistance	R_{nFLT}	V_{UVLO} = 0.5V, I_{nFLT} = 10mA sinking	50	90	140	Ω
nFLT Input Leakage Current	I_{nFLT}	V_{nFLT} = 0V to 60V	-200	15	200	nA
Thermal Shutdown (TSD)						
TSD Threshold, Rising	T_{TSD}			154		℃
TSD Hysteresis	T_{TSD_HYS}			14		℃
Mode						
Thermal Fault Mode Selection	MODE_SEL	MODE = 402kΩ to RTN	Current Limiting with Latch			
		MODE = open	Circuit Breaker Mode with Auto-Retry			
		MODE = open (SGM257050B only)	Circuit Breaker Mode with Latch			
		MODE = short to RTN	Current Limiting with Auto-Retry			

TIMING REQUIREMENTS

(V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 120kΩ, IMON = nFLT = open, C_{OUT} = 1μF, C_{SS} = open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Input (UVLO)						
UVLO Turn-On Delay	$t_{UVLO_ON_DLY}$	UVLO↑ (100mV above V_{UVLOR}) to V_{OUT} = 100mV, C_{SS} = open		180		μs
		UVLO↑ (100mV above V_{UVLOR}) to V_{OUT} = 100mV, C_{SS} ≥ 10nF		180 + 14.5 × C_{SS}		
UVLO Turn-Off Delay	$t_{UVLO_OFF_DLY}$	UVLO↓ (100mV below V_{UVLOF}) to nFLT↓		5		μs
Shutdown Control Input (nSHDN)						
Shutdown Exit Delay	$t_{SD_ON_DLY}$	nSHDN↑ to V_{OUT} = 100mV, C_{SS} ≥ 10nF		230 + 14.5 × C_{SS}		μs
		nSHDN↑ to V_{OUT} = 100mV, C_{SS} = open		230		
Shutdown Entry Delay	$t_{SD_OFF_DLY}$	nSHDN↓ (below V_{nSHDNF}) to nFLT↓		0.5		μs
Over-Voltage Protection Input (OVP)						
OVP Exit Delay	$t_{OVP_ON_DLY}$	OVP↓ (20mV below V_{OVPF}) to V_{OUT} = 100mV, SGM257050A/B only		160		μs
OVP Disable Delay	$t_{OVP_OFF_DLY}$	OVP↑ (20mV above V_{OVPR}) to nFLT↓, SGM257050A/B only		4		μs
Current Limit						
Fast-Trip Comparator Delay	$t_{FASTTRIP_DLY}$	I_{OUT} > $I_{FASTTRIP}$		250		ns
Reverse Protection Comparator						
Reverse Protection Comparator Delay	t_{REV_DLY}	(V_{IN} - V_{OUT})↓ (100mV overdrive below V_{REVTH}) to internal FET turn OFF		1.5		μs
		(V_{IN} - V_{OUT})↓ (100mV overdrive below V_{REVTH}) to nFLT↓		45		
	t_{FWD_DLY}	(V_{IN} - V_{OUT})↑ (100mV overdrive above V_{FWDTH}) to nFLT↑		70		
Thermal Shutdown						
Retry Delay in TSD	t_{RETRY}			505		ms
Output Ramp Control (SS)						
Output Ramp Time	t_{SS}	nSHDN↑ to V_{OUT} = 23.9V, with C_{SS} = 47nF		10		ms
		nSHDN↑ to V_{OUT} = 23.9V, with C_{SS} = open		1.1		
Fault Flag (nFLT)						
nFLT Assertion Delay in Circuit Breaker Mode	t_{CB_DLY}	MODE = open, delay from I_{OUT} > I_{OL} to nFLT↓		4		ms
Retry Delay in Circuit Breaker Mode	$t_{CB_RETRY_DLY}$	MODE = open		505		ms
PGOOD Delay (De-Glitch) Time	t_{PGOODF}	Falling edge		860		μs
	t_{PGOODR}	Rising edge		1800		

PARAMETER MEASUREMENT INFORMATION

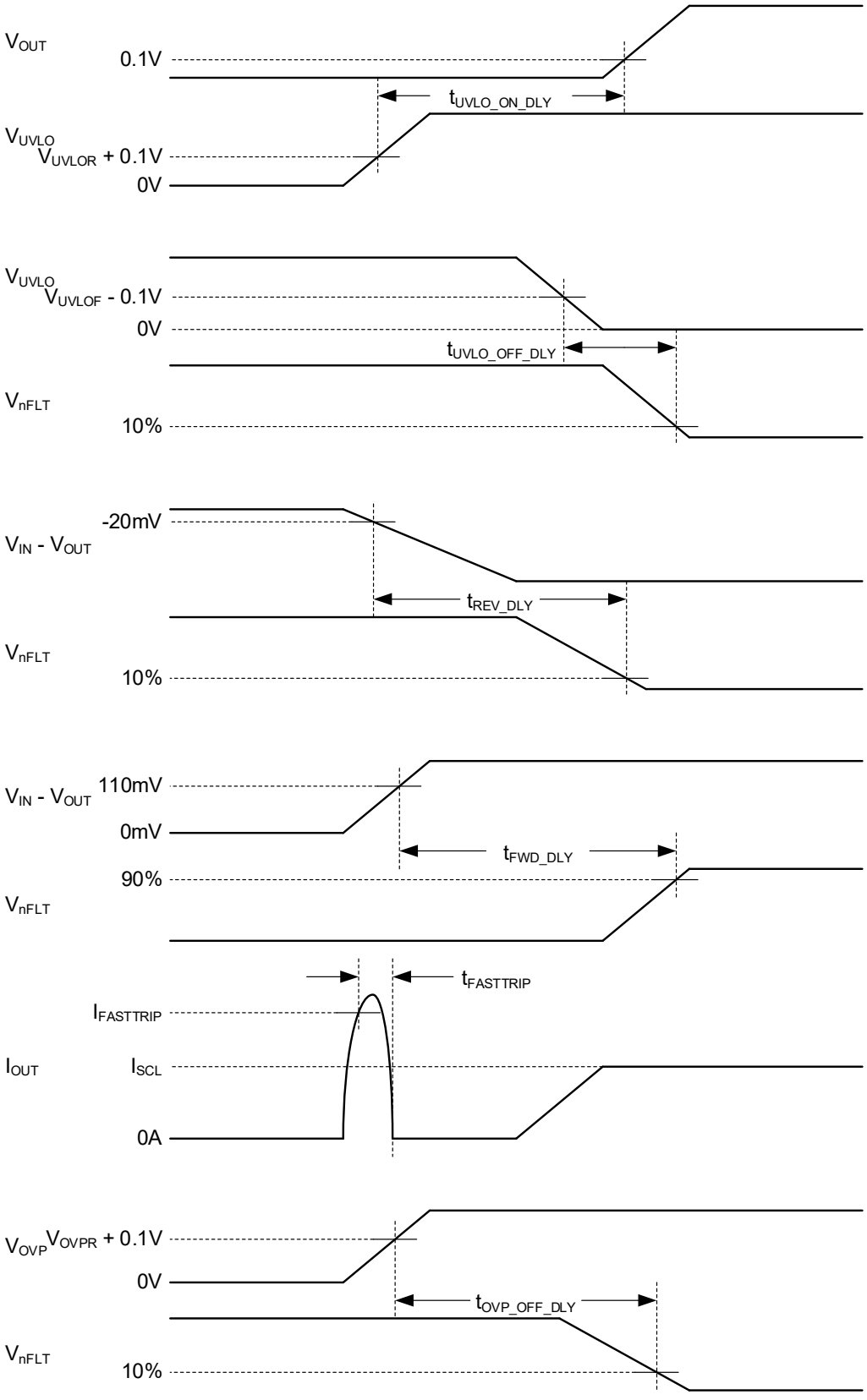
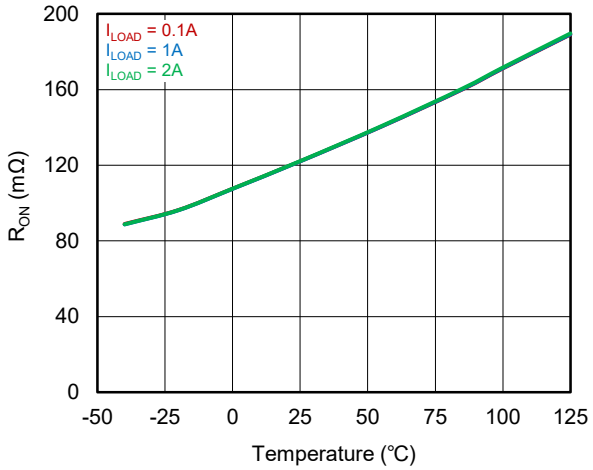


Figure 2. Timing Waveforms

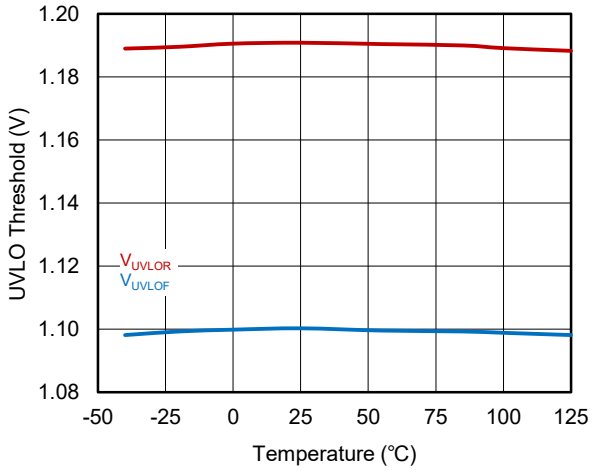
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 24V, unless otherwise noted.

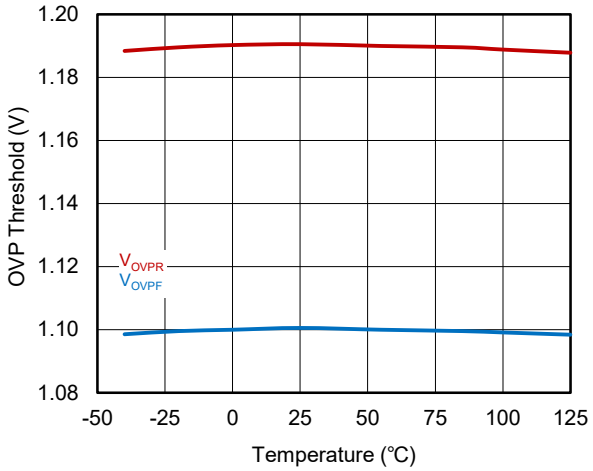
R_{ON} vs. Temperature (Across Load Current)



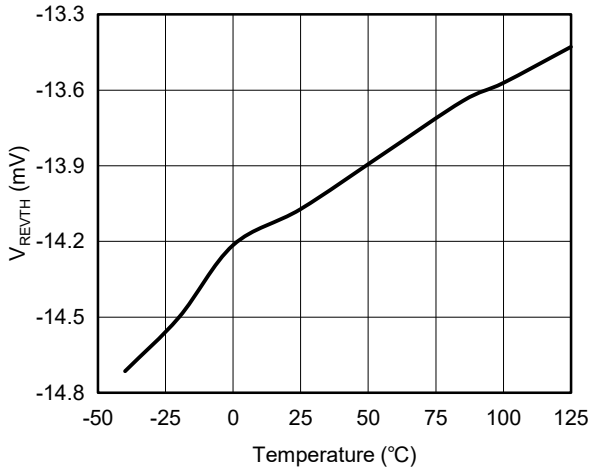
UVLO Threshold vs. Temperature



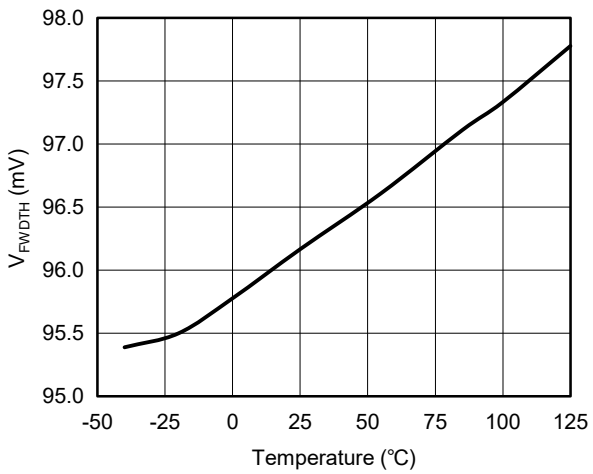
OVP Threshold vs. Temperature



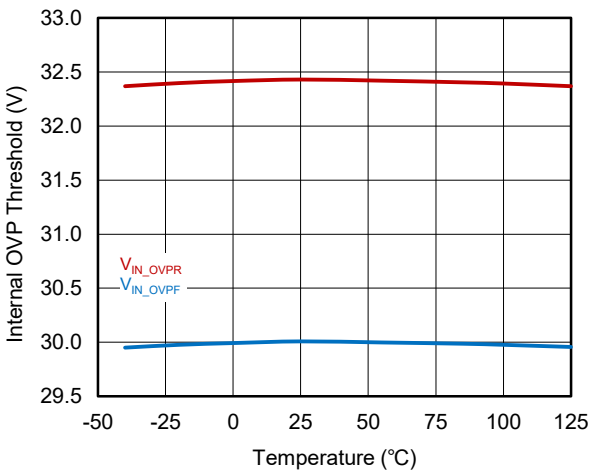
V_{REVTH} vs. Temperature



V_{FWDTH} vs. Temperature



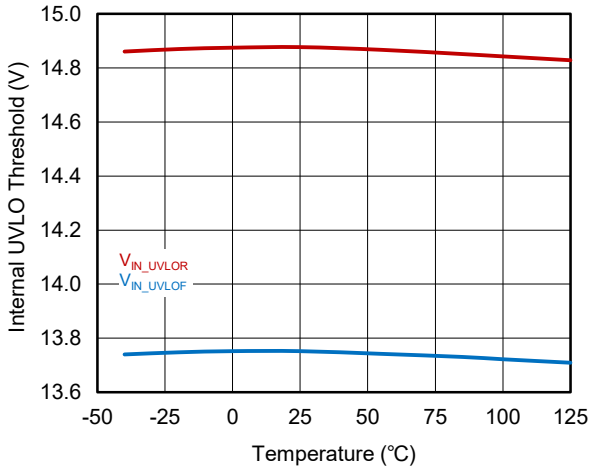
Internal OVP Threshold vs. Temperature



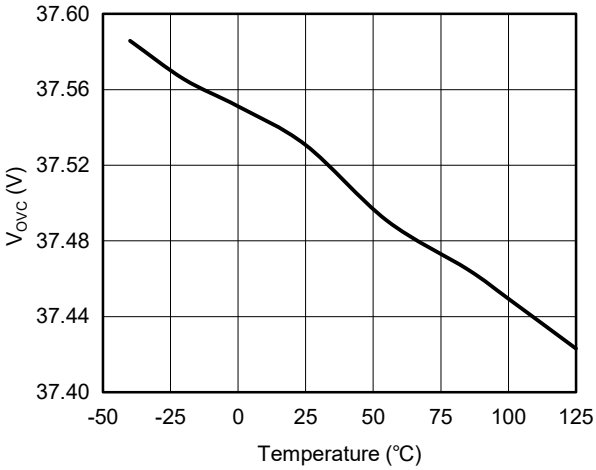
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, unless otherwise noted.

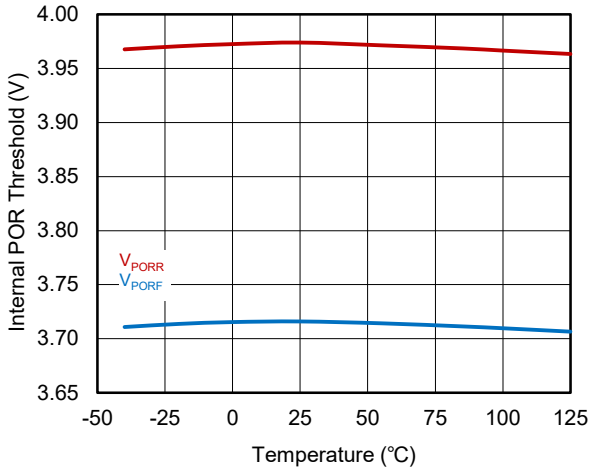
Internal UVLO Threshold vs. Temperature



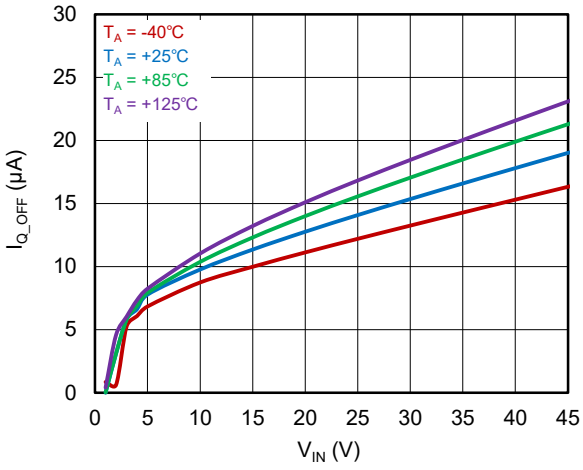
V_{OVC} vs. Temperature



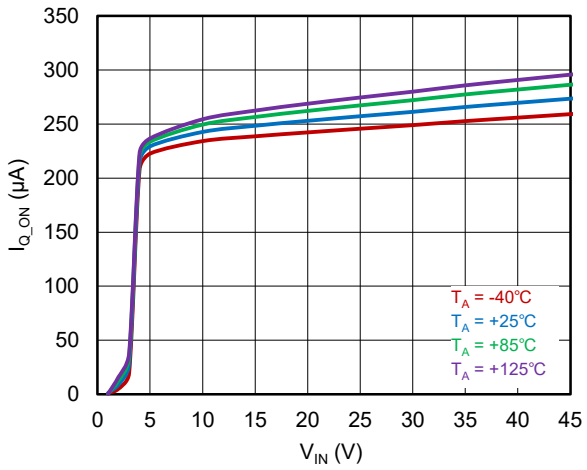
Internal POR Threshold vs. Temperature



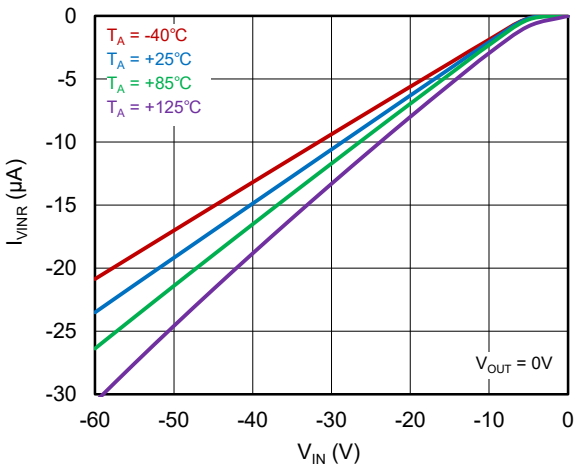
I_{Q_OFF} vs V_{IN} (Shutdown)



I_{Q_ON} vs. V_{IN} (Normal Operation)



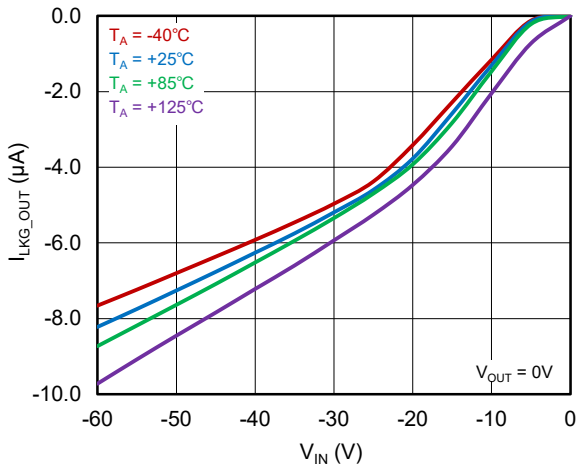
I_{VINR} vs. V_{IN} (Reverse Voltage)



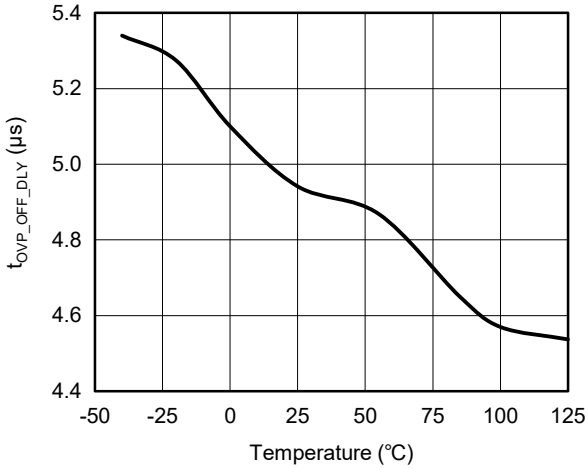
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, unless otherwise noted.

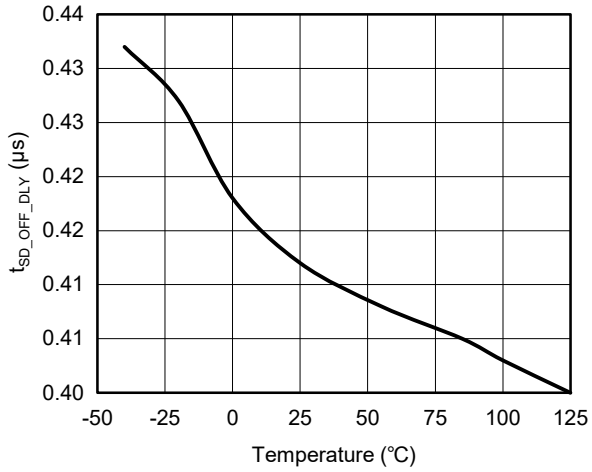
I_{LKG_OUT} vs. V_{IN} (Reverse Voltage)



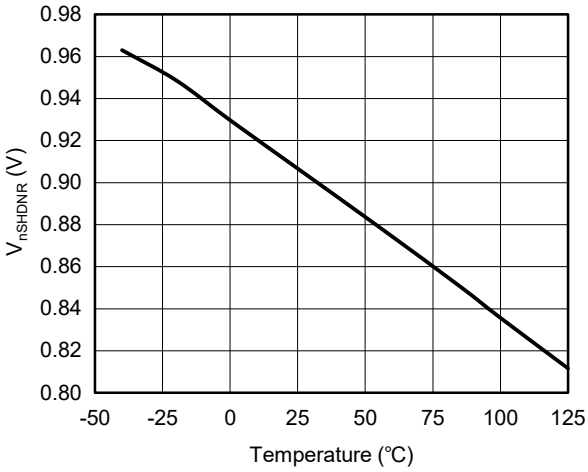
$t_{OVP_OFF_DLY}$ vs. Temperature



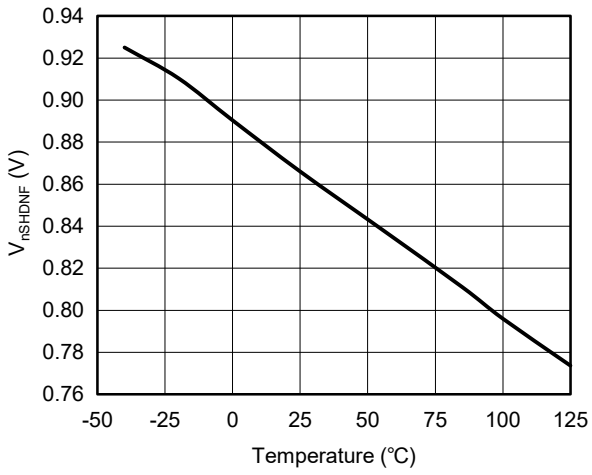
$t_{SD_OFF_DLY}$ vs. Temperature



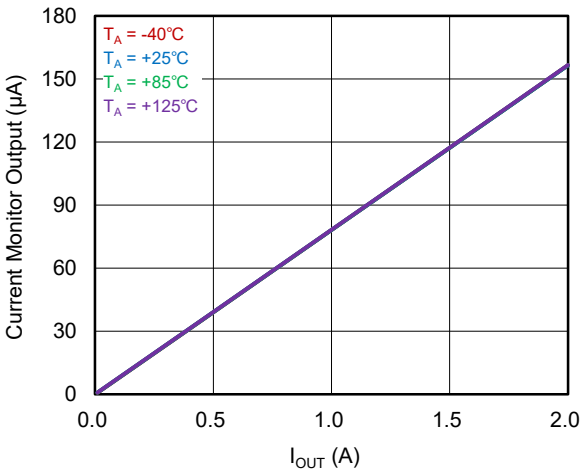
V_{nSHDNR} vs. Temperature



V_{nSHDNF} vs. Temperature



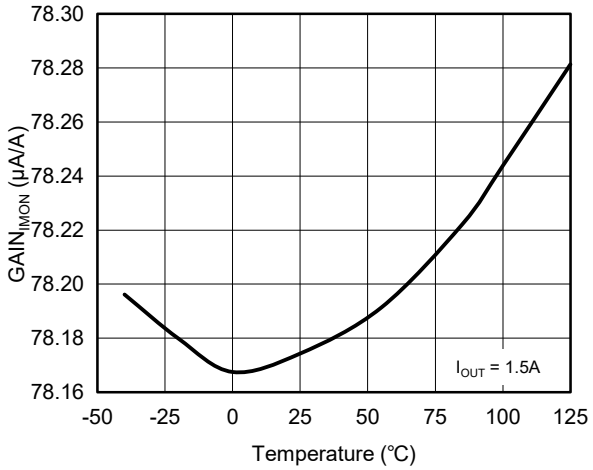
Current Monitor Output vs. I_{OUT}



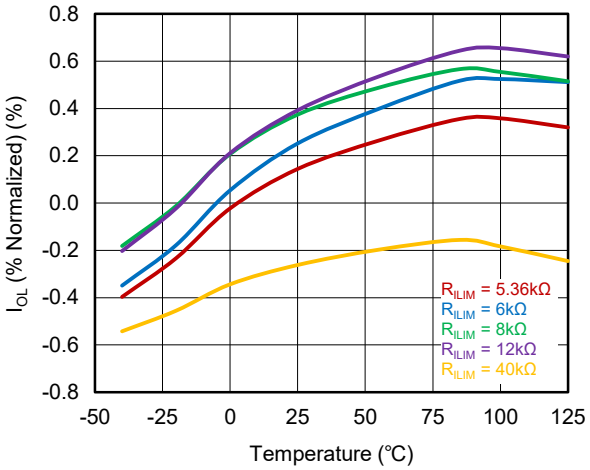
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, unless otherwise noted.

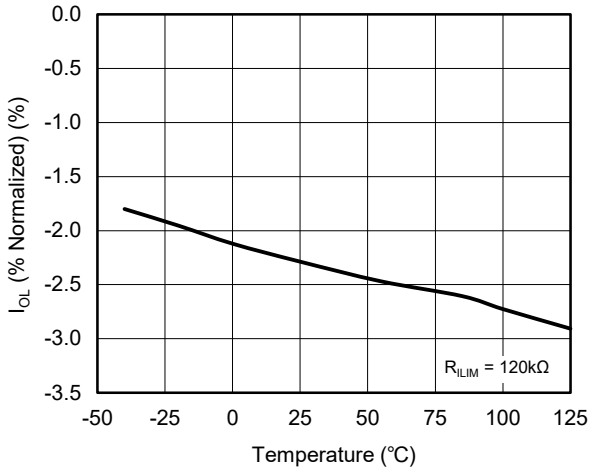
$GAIN_{IMON}$ vs. Temperature



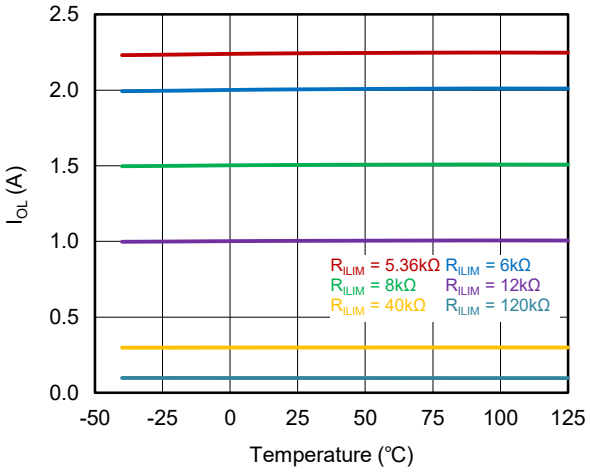
I_{OL} (% Normalized) vs. Temperature



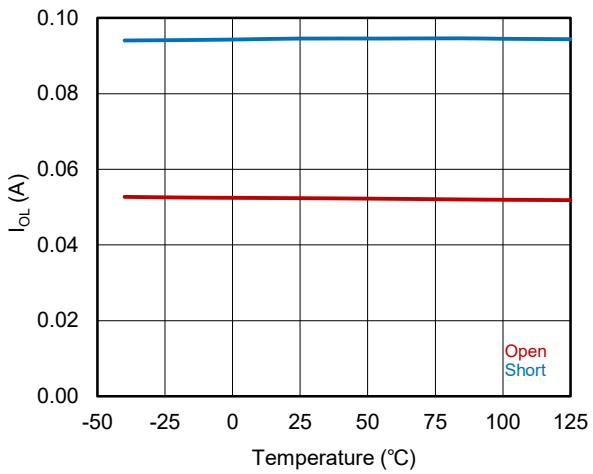
I_{OL} (% Normalized) vs. Temperature



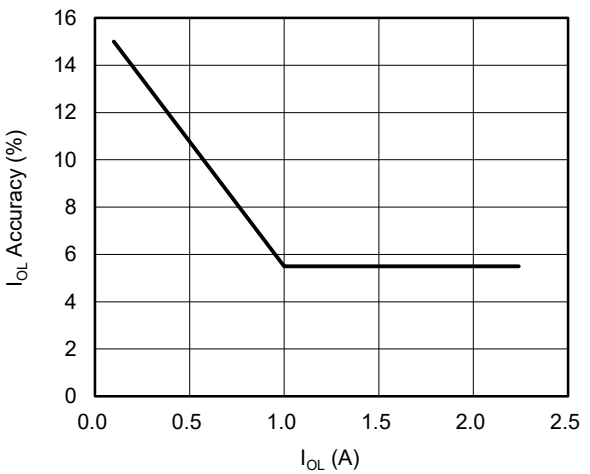
I_{OL} vs. Temperature



I_{OL} vs. Temperature (R_{ILIM} = Open and Short)

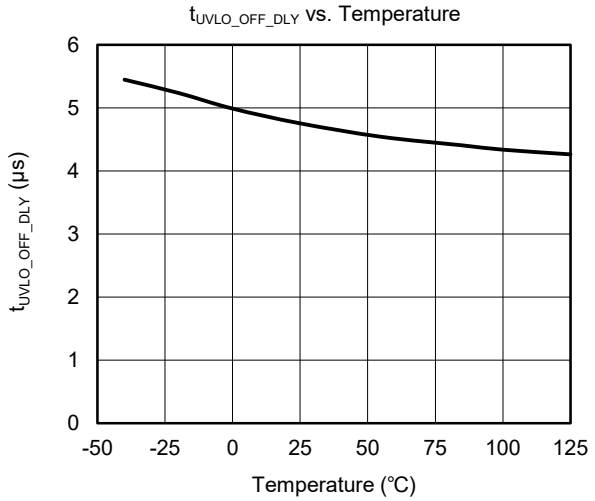


I_{OL} Accuracy vs. I_{OL}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

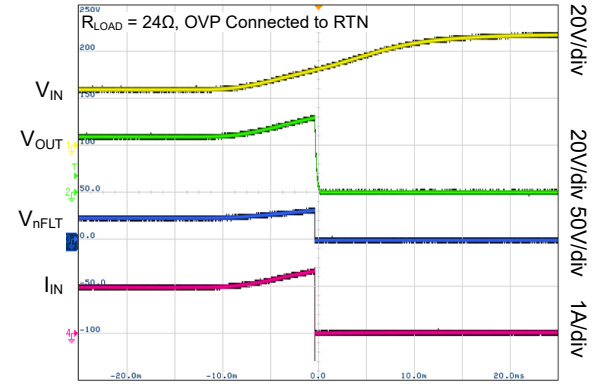
T_A = +25℃, V_{IN} = 24V, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

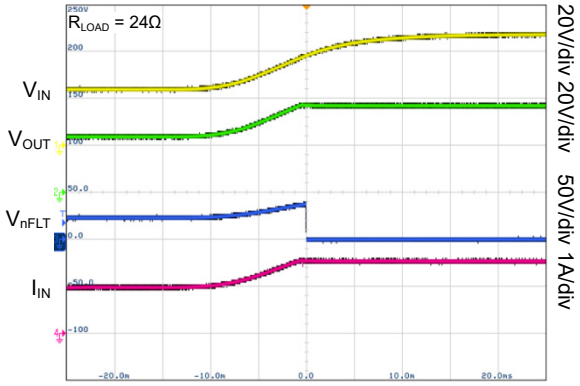
T_A = +25℃, R_{ILIM} = 8kΩ, R_{nFLT} = 50kΩ, V_{IN} = 24V, unless otherwise noted.

OVP Over-Voltage Cut-Off Response



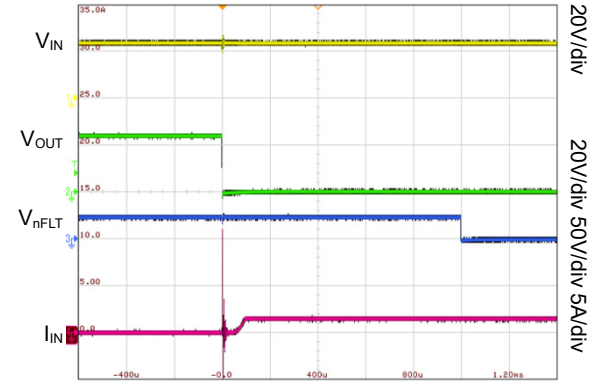
Time (5ms/div)

OV Clamp Response (SGM257050C Only)



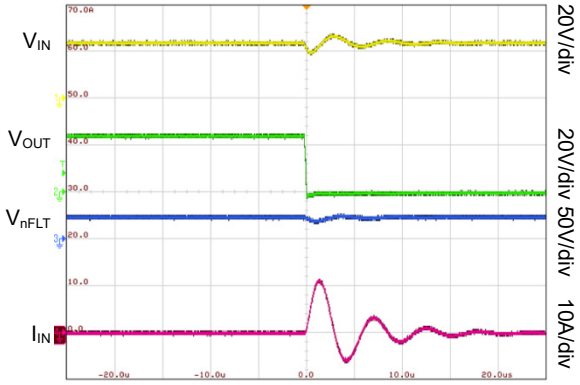
Time (5ms/div)

Hot-Short: Fast-Trip Response and Current Regulation



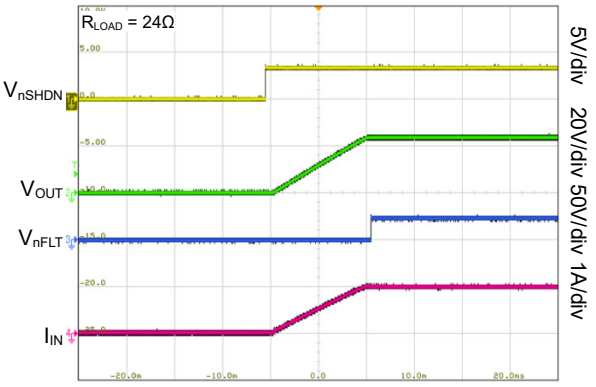
Time (200μs/div)

Hot-Short: Fast-Trip Response (Zoomed)



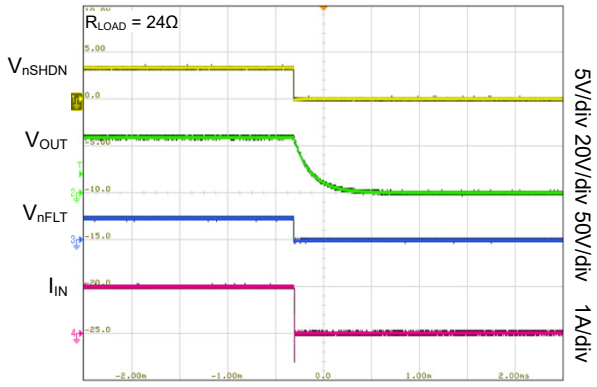
Time (50μs/div)

Turn-On Control with nSHDN



Time (5ms/div)

Turn-Off Control with nSHDN

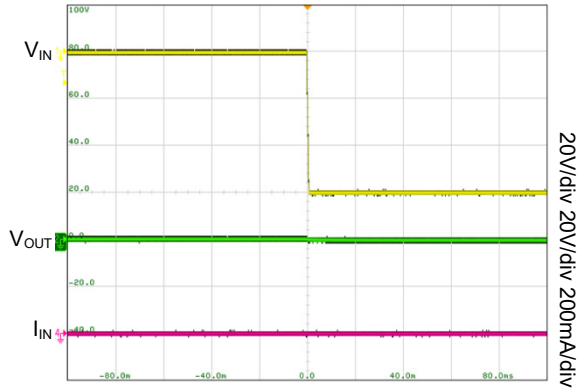


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

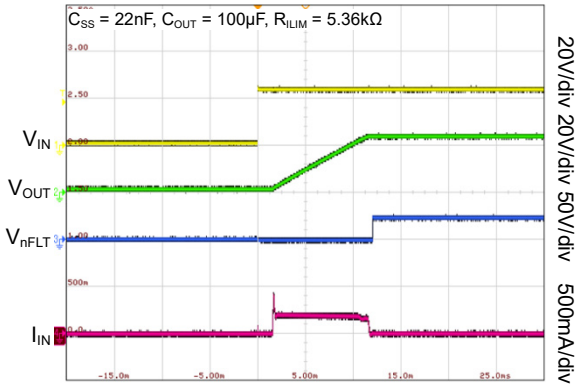
T_A = +25℃, R_{ILIM} = 8kΩ, R_{nFLT} = 50kΩ, V_{IN} = 24V, unless otherwise noted.

Reverse Input Supply Protection at -60V



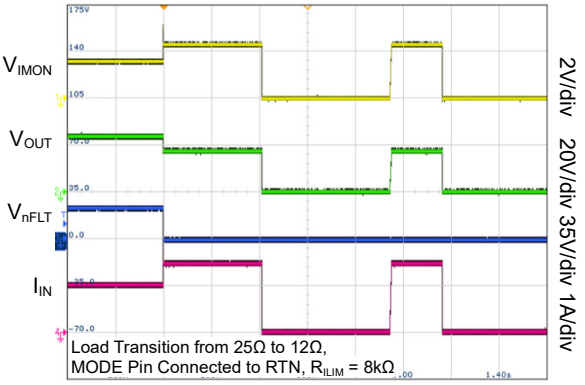
Time (20ms/div)

Hot Plug-In and Inrush Current Control at 24V Input



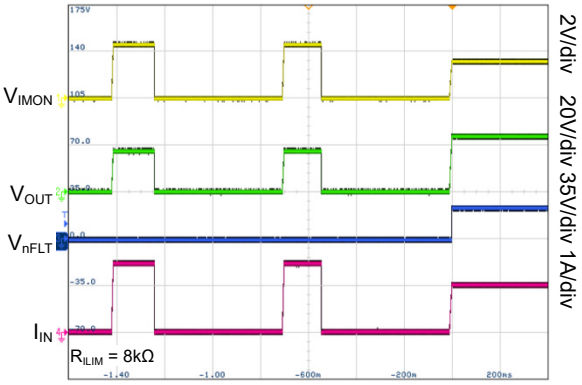
Time (5ms/div)

Auto-Retry MODE Fault Behavior



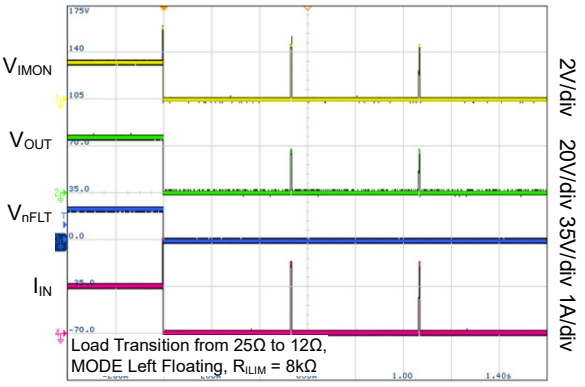
Time (200ms/div)

Response during Coming Out of Overload Fault



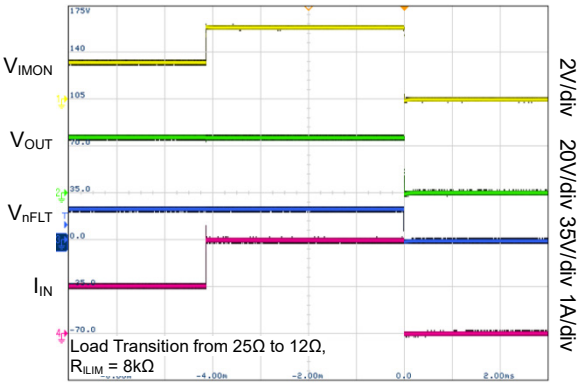
Time (200ms/div)

Circuit Breaker Functionality



Time (200ms/div)

Zoomed at the Instance of Load Step

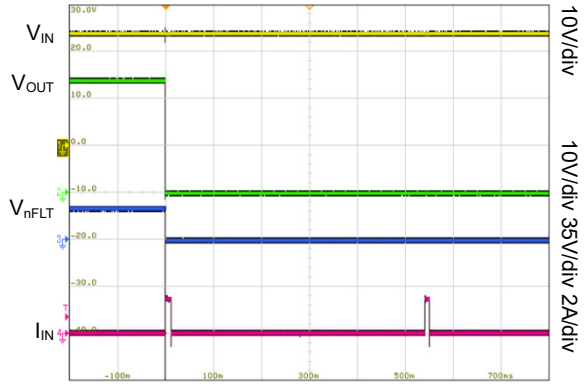


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

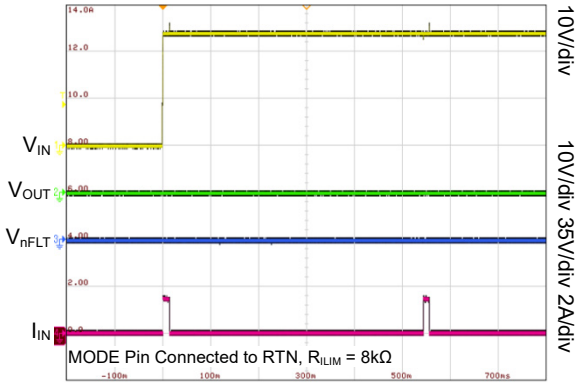
T_A = +25℃, R_{ILIM} = 8kΩ, R_{nFLT} = 50kΩ, V_{IN} = 24V, unless otherwise noted.

Output Hot-Short Functionality at 24V Input



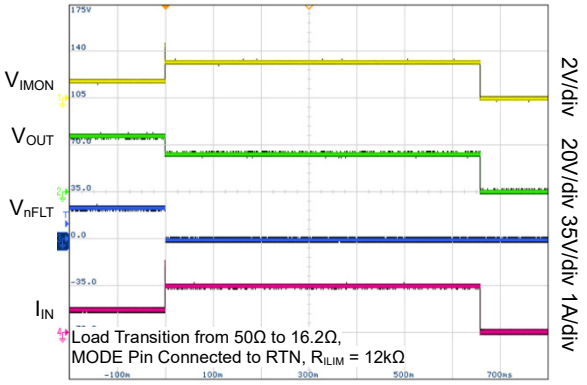
Time (100ms/div)

Start-Up with Short on Output



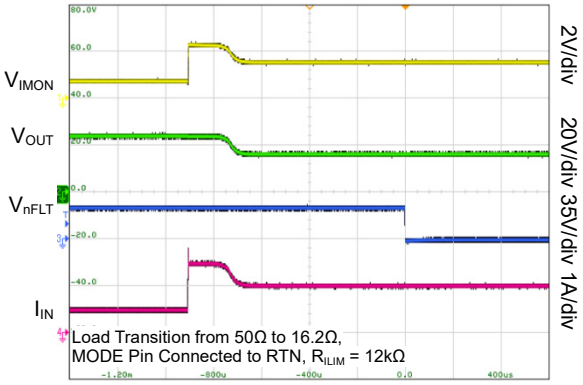
Time (100ms/div)

Look Ahead Overload Current Fault Indication



Time (100ms/div)

Overload Current Fault Response (Zoomed)



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

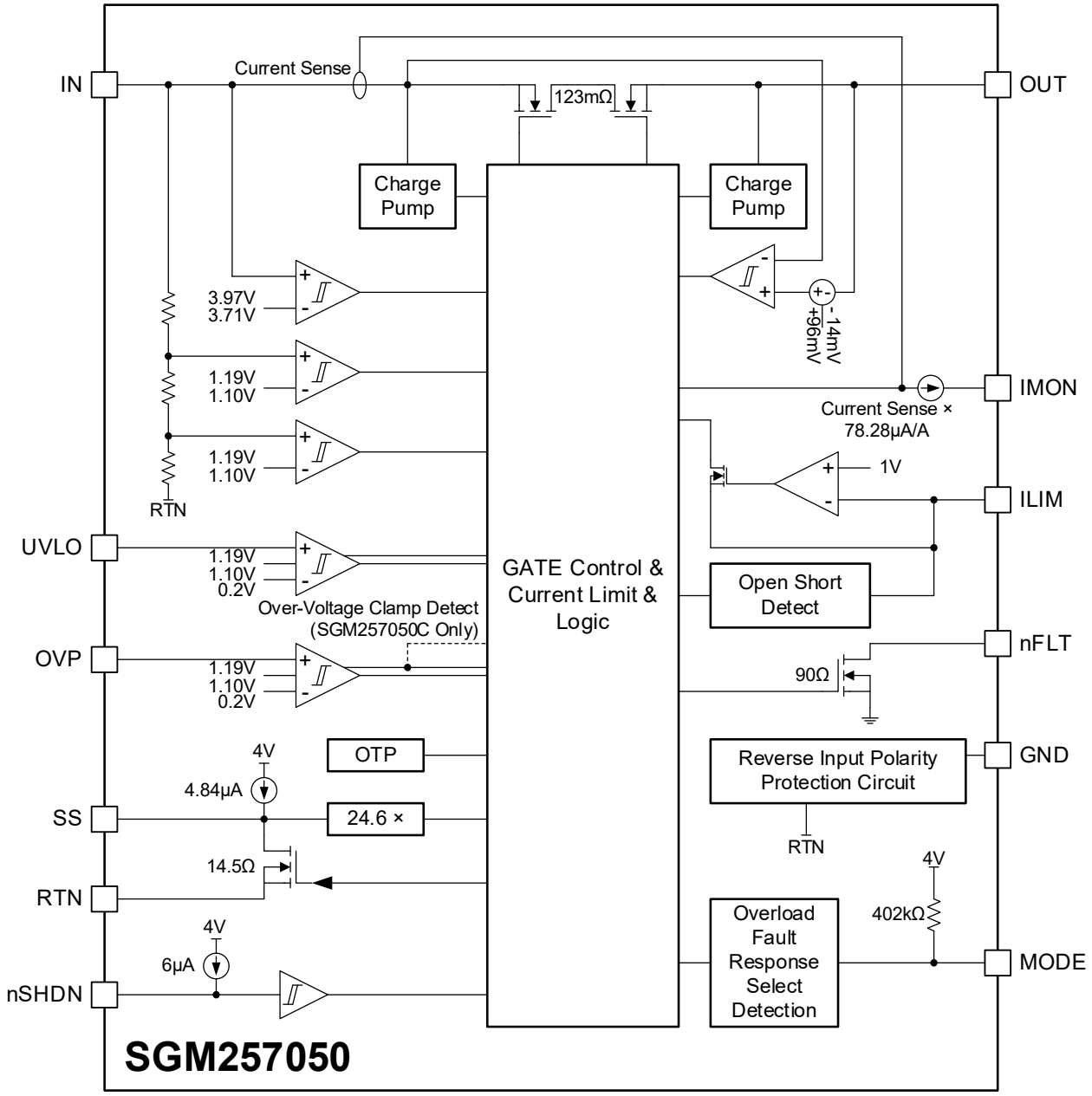


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM257050 is a high-voltage industrial eFuse featuring an integrated back-to-back MOSFET design and comprehensive protection functions. This device supports inrush current control and programmable output voltage slew rate control. With an ability to withstand up to ±60V at the input without damage, it is well-suited for hot-swap power applications. Additionally, it integrates multiple protection features such as under-voltage, over-voltage, and over-current protection to ensure robust safeguarding of peripheral equipment. The accurate over-current limit (±5.5% at 1A) threshold reduces the system over-design. Under output short-circuit conditions, the fast-trip short-circuit protection responds within 250ns (TYP) to shut down the device and disconnect the fault current.

Under-Voltage Lockout (UVLO)

The SGM257050 provides programmable under-voltage lockout (UVLO) protection. When the voltage of UVLO drops below the falling threshold V_{UVLOF}, the internal MOSFET is turned-off and nFLT pin is asserted. The UVLO hysteresis is 90mV (TYP). The UVLO threshold can be set through connecting a resistor network from IN to UVLO pin and to RTN.

The device has a default 14.9V UVLO rising threshold (TYP) with 1.1V hysteresis which is selected by pulling UVLO pin to RTN. If the UVLO protection is not used, the UVLO pin must be connected to IN and must not be floating.

The device provides an internal Power-On Reset (POR) function. When the voltage at the IN pin falls below the POR threshold (V_{PORF}), the internal circuitry is disabled. The POR threshold features 257mV of hysteresis.

Over-Voltage Protection (OVP)

The SGM257050 series of device provide robust input over-voltage protection. The SGM257050A and SGM257050B offer programmable over-voltage cut off protection. When the voltage on OVP pin exceeds the rising threshold V_{OVPR}, the internal MOSFET is turned off. The OVP threshold can be set by connecting a resistor network from IN to OVP pin and to RTN. The SGM257050A and SGM257050B also provide a default 32.6V Input over-voltage cut off V_{IN_OVP} threshold with 2.3V hysteresis which can be enabled by pulling OVP pin to RTN.

The SGM257050C provides 37.5V over-voltage clamp protection. When the input voltage exceeds 37.5V, the device clamps the output to the V_{OVC} threshold. Under this condition, the power dissipation of the chip is P_D = (V_{IN} - V_{OVC}) × I_{OUT} If the device continues to operate in the over-voltage clamp state, it may trigger thermal protection due to excessive heat.

Reverse Input Supply Protection

To prevent damage to system components caused by reverse input voltage due to incorrect wiring, Schottky diodes or other protective components are typically connected in series at the input (as shown in Figure 4). However, this approach introduces additional components, leading to increased size and power consumption. The SGM257050 series integrates reverse polarity protection, obviating the need for an external diode and allowing the input to withstand reverse voltages of up to -60V without damage, thereby safeguarding downstream components. The implementation of the reverse polarity protection feature is illustrated in Reverse Input Supply Protection at -60V.

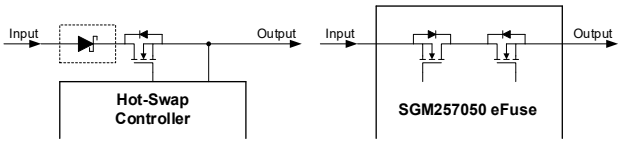


Figure 4. Reverse Input Supply Protection Circuits

Hot Plug-In and Inrush Current Control

The SGM257050 is designed to provide hot plug-in power management by controlling the inrush current as well as the output slew rate. This design helps eliminate the voltage drop and avoid undesired power reset. The output ramp rate at power-on is set by the capacitor from the SS pin to RTN. If SS pin is left open, the device will start up with the fastest output slew rate (t_{SS}). The inrush current can be calculated using Equation 1.

$$I_{SS} = \frac{C_{SS}}{Gain_{SS}} \times \frac{dV_{OUT}}{dt} \quad (1)$$

where:

C_{SS} is the external soft-start capacitor, in nF.

I_{SS} = 4.84μA (TYP).

$Gain_{SS}$ = SS to V_{OUT} gain = 24.6V/V (TYP).

The total rising time t_{SS} of V_{OUT} for 0V to V_{IN} can be calculated using Equation 2.

$$t_{SS} = 8.4 \times 10^3 \times V_{IN} \times C_{SS} \quad (2)$$

DETAILED DESCRIPTION (continued)

Overload and Short-Circuit Protection

The device monitors the load current continuously to provide overload protection.

Overload Protection

Available overload protection fault response options are as follows:

- Active current limiting (auto-retry/latch-off modes).
- Overload timeout electronic circuit breaker (auto-retry/latch-off modes).

Refer to Table 1 for configurations to select a specific overload fault response.

Table 1. Overload Fault Response Configuration Table

MODE Pin Configuration	Overload Protection Type	Device
Open	Auto-retry electronic circuit breaker	SGM257050A/C
	Latch-off electronic circuit breaker	SGM257050B
Shorted to RTN	Auto-retry active current limiting	SGM257050A/B/C
A 402kΩ resistor between the MODE pin and the RTN pin	Latch-off active current limiting	SGM257050A/B/C

Active Current Limiting

When the active current limit mode is selected, the device will regulate the output current to the user-programmed current limit I_{OL} during an overload event. The over-current limit threshold can be set by an external R_{ILIM} resistor, referring to Equation 3.

$$I_{OL} = \frac{12}{R_{ILIM}} \quad (3)$$

where:

I_{OL} is the overload current limit, in A.

R_{ILIM} is the current limit resistor, in kΩ.

Electronic Circuit Breaker with Overload Timeout, MODE = Open

In this mode, the device enters circuit breaker operation. During an overload event, it permits over-current conditions provided the current remains below the $I_{FASTTRIP}$ threshold. The circuit breaker threshold (I_{CB}) can be programmed via the R_{ILIM} resistor, referring to Equation 4.

$$I_{CB} = \frac{12}{R_{ILIM}} \quad (4)$$

where:

I_{CB} is circuit breaker current threshold, in A.

R_{ILIM} is the current limit resistor, in kΩ.

Short-Circuit Protection

When the output short-circuit occurs, the current from IN to OUT rises very rapidly. Due to limited bandwidth, the current limit amplifier is unable to respond quickly to this fault. To solve this, the SGM257050 integrates with a fast-trip comparator which can shut down the internal MOSFETs within 250ns (TYP). The fast-trip comparator works and cuts off the short-circuit current when I_{OUT}, the current flowing through the device, exceeds the fast-trip threshold $I_{FASTTRIP}$. The internal fast-trip threshold is configured as 1.87 times the over-current limit value ($I_{FASTTRIP}$ = 1.87 × I_{OL} + 0.015). The internal MOSFETs would remain off-state for only a few ms, following by soft-restart in a current limit manner where current through the device is regulated to I_{OL} under the regulation of current limit amplifier. Then, the device behaves the same as the overload condition.

Start-Up with Short-Circuit on Output

For power-up with output short-circuit to GND, the current flowing across the device is limited to I_{OL}. This capability facilitates rapid fault isolation and thereby maintains the DC bus stability.

FAULT Response

The SGM257050 features an open-drain fault indicator (nFLT) pin. This pin is pulled low to signal a fault condition when any of the following events occur: input under-voltage, over-voltage, overload, reverse current, thermal shutdown, nSHDN pin being pulled low or during the start-up sequence before the MOSFET is fully turned on. To avoid false reporting, this pin is designed with an internal de-glitch without additional external circuits. When unused, the nFLT pin may either be left floating or connected to GND.

Look Ahead Overload Current Fault Indicator

When the device operates in active current limit mode and an overload event persists beyond the t_{PGOODF} duration, the fault indicator (nFLT) is asserted to warn of a potential thermal shutdown event.

DETAILED DESCRIPTION (continued)

Current Monitoring

The SGM257050 has a current monitoring function at the IMON pin. The sourcing current of this pin is proportional to the current of internal MOSFETs. Connecting resistor R_{IMON} between this pin and RTN transforms the sensed current into the IMON voltage. The maximum voltage on the IMON pin is internally limited to 4V. With this limitation, the maximum value of R_{IMON} can be determined using Equation 5.

$$V_{IMON} = \left[I_{OUT} \times GAIN_{IMON}\right] \times R_{IMON} \quad (5)$$

where:

$GAIN_{IMON}$ is the gain factor associated with I_{IMON}:I_{OUT} = 78.28μA/A (TYP).

I_{OUT} is the load current.

This pin should not incorporate any bypass capacitor so as to prevent lag within current-monitoring data.

When a reverse polarity input fault occurs, it is recommended to connect a 100kΩ resistor between the IMON and ADC input pins to protect peripheral circuitry.

IN, OUT, RTN, and GND Pins

The SGM257050 features two pins each for IN and OUT. The two input pins must be jointly linked to the input power supply, with ceramic capacitors placed near the device to suppress transient interference. Similarly, the output pins must be connected together to the load. The output voltage is calculated as shown in Equation 6.

$$V_{OUT} = V_{IN} - (R_{ON} \times I_{OUT}) \quad (6)$$

where:

R_{ON} is the total on-resistance of the internal FETs.

The GND pin of the device must be directly connected to the system ground. The RTN pin serves as the reference point for all internal control circuits. When configuring the external circuitry of the SGM257050, note that components including R_{ILIM}, C_{SS}, R_{IMON}, R_{MODE}, and the resistors connected to UVLO and OVP must be referenced to RTN. To handle input reverse polarity faults, the device incorporates an internal protection circuit between RTN and GND. Connecting RTN directly to GND will disable the input reverse polarity protection function.

Thermal Shutdown

The device features over-temperature protection. When the junction temperature exceeds the thermal shutdown threshold T_{TSD}, the internal FETs are immediately turned off. Once thermal shutdown is triggered, the device will time 505ms after the junction temperature cools to T_{TSD} - 14℃, and then either latch-off or attempt an auto-retry based on the configured fault response mode. During the thermal shutdown process, the nFLT pin is pulled low to signal the fault condition.

Low Current Shutdown Control (nSHDN)

The device can be shut down through pulling the nSHDN pin below the 0.6V (MAX) threshold with a micro-controller. In shutdown mode, the quiescent current of the device is reduced to 14μA (TYP). The controller or any other device should have at least 6μA sinking current capability to pull down the nSHDN pin. To enable the device, nSHDN should be pulled up to at least 1.2V where the device starts up with soft-start mode.

Device Functional Modes

During over-current and short-circuit events, the SGM257050A, SGM257050B, SGM257050C exhibits distinct responses, as detailed in Table 2.

DETAILED DESCRIPTION (continued)

Table 2. Device Operational Differences under Different MODE Configurations

MODE Pin Configuration	MODE Connected to RTN (Current Limit with Auto-Retry)	A 402kΩ Resistor Connected between MODE and RTN Pins (Current Limit with Latch-Off)	MODE Pin = Open (Circuit Breaker with Auto-Retry - SGM257050A/C, Circuit Breaker with Latch - SGM257050B Only)
Start-up	Inrush current controlled by SS		
	Inrush capped at I_{OL} level set by R_{ILIM}	Inrush capped at I_{OL} level set by R_{ILIM}	Inrush capped at I_{OL} level set by R_{ILIM}
			Fault timer runs when current is limited to I_{OL}
			Fault timer expires at t_{CB_DLY}, turning off FETs
	If $T_J > T_{TSD}$, device turns off	If $T_J > T_{TSD}$, device turns off	Device shuts off if $T_J > T_{TSD}$ prior to timer expiry
Over-current response	Current is capped at I_{OL} level as set by R_{ILIM}	Current is capped at I_{OL} level as set by R_{ILIM}	Current passes through the device if $I_{LOAD} < I_{FASTTRIP}$
	Power dissipation increases as V_{IN} - V_{OUT} increases	Power dissipation increases as V_{IN} - V_{OUT} increases	Fault timer triggers when the current exceeds I_{OL}
			Fault timer expires at t_{CB_DLY}, turning off FETs
	Device shuts off upon $T_J > T_{TSD}$	Device shuts off upon $T_J > T_{TSD}$	Device shuts off if $T_J > T_{TSD}$ prior to timer expiry
	Device attempts restart 505ms after $T_J < [T_{TSD}$ - 14℃]	Device remains off	SGM257050A and SGM257050C attempt restart 505ms after $T_J < [T_{TSD}$ - 14℃]. SGM257050B remains off
Short-circuit response	Fast turnoff when $I_{LOAD} > I_{FASTTRIP}$		
	Quick restart enabled, current capped at I_{OL}, follows standard start-up		

APPLICATION INFORMATION

Typical Application

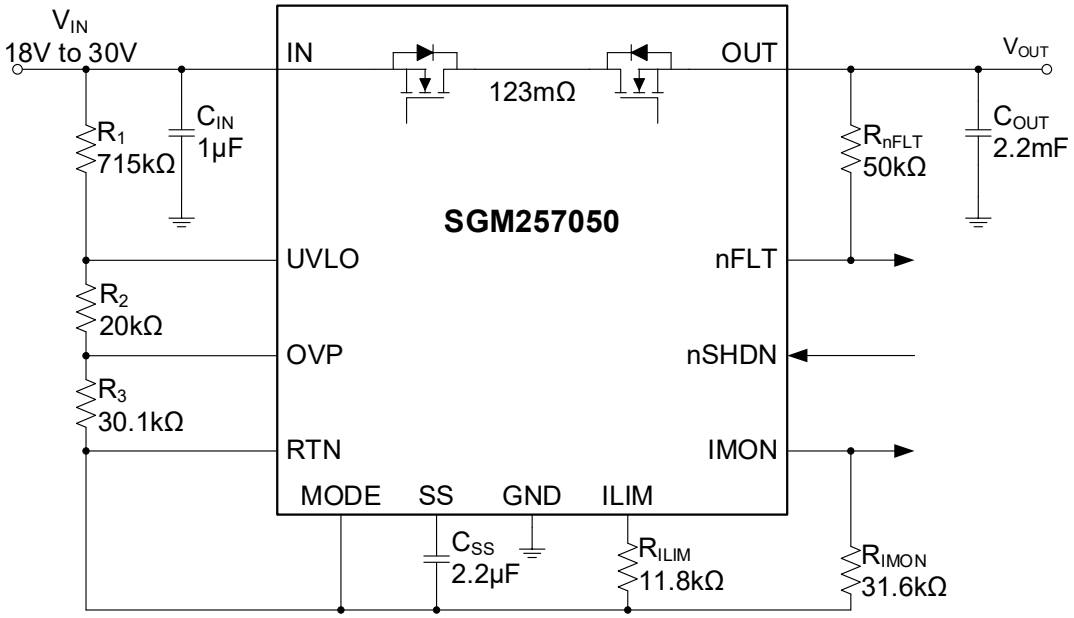


Figure 5. SGM257050 Typical Application

Design Requirements

The Design Requirements for SGM257050 are shown in Table 3.

Table 3. Design Requirements

Example Value		Design Parameter
Typical Input Voltage	V_{IN}	24V
Under-Voltage Lockout Set Point	V_{UV}	18V
Over-Voltage Cut-Off Set Point	V_{OV}	30V
Load During Start-Up	R_{L_SU}	48Ω
Overload Current Limit	I_{OL}	1A
Load Capacitance	C_{OUT}	2200μF
Maximum Ambient Temperature	T_A	+25℃

Detailed Design Procedure

Programming the Current-Limit Threshold - R_{ILIM} Selection

The current limit level is set by the ILIM pin resistor R_{ILIM} which can be calculated using Equation 7.

$$R_{ILIM} = \frac{12}{I_{OL}} = 12k\Omega \quad (7)$$

where:

I_{OL} = 1A.

Choose the closest standard 1% resistor value: R_{ILIM} = 11.8kΩ.

Under-Voltage Lockout and Over-Voltage Set Point

The UVLO and OVLO threshold value are set through a resistor network of R_1, R_2 and R_3 connected between IN, UVLO, OVP and RTN pin. These resistors are selected based on Equation 8 and 9.

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \quad (8)$$

$$V_{UVLOR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \quad (9)$$

To reduce the current drawn from the power supply, resistors with higher value for R_1, R_2 and R_3 are recommended.

However, using higher value resistors may introduce more calculation errors affected by the leakage current into the device pins. Therefore, the current through the resistor $V_{IN}/(R_1 + R_2 + R_3)$ should be 20 times greater than the leakage current into the UVLO and OVP pins.

Form the electrical specifications, V_{OVPR} = 1.19V and V_{UVLOR} = 1.19V. For this design, V_{OV} is 30V and V_{UV} is 18V. First, choose R_3 = 30.1kΩ first, and use Equation 8 to solve (R_1 + R_2) = 728.7kΩ. Combine this with Equation 9 to solve R_2 = 20.05kΩ and R_1 = 708.6kΩ.

APPLICATION INFORMATION (continued)

Choose the closest standard 1% resistor values: R_1 = 715kΩ, R_2 = 20kΩ and R_3 = 30.1kΩ.

The UVLO and OVP pins can also be directly connected to the RTN pin, selecting the internal fixed over-voltage threshold V_{OV} = 32.6V and under-voltage threshold V_{UV} = 14.9V.

Programming Current Monitoring Resistor - R_{IMON}

A resistor on the IMON pin sets a voltage proportional to the load current, which can be read by an external ADC to monitor system operation. The resistor R_{IMON} should be designed based on the maximum input voltage of the ADC, and its value is determined by Equation 10:

$$R_{IMON} = \frac{V_{IMON_MAX}}{I_{OL} \times 78.28 \times 10^{-6}} \quad (10)$$

With an input current limit of 1A and a maximum ADC input voltage of 2.5V, R_{IMON} is determined by Equation 11.

$$R_{IMON} = \frac{2.5}{1 \times 78.28 \times 10^{-6}} = 31.9k\Omega \quad (11)$$

To prevent exceeding the maximum input voltage range of the ADC, select the closest standard 1% resistor value: R_{IMON} = 31.6kΩ.

If detecting the $I_{FASTTRIP}$ current is required, R_{IMON} can be reduced by a factor of 1.8 as shown in Equation 5.

Setting Output Voltage Ramp Time - t_{SS}

The chip junction temperature must be maintained below the thermal shutdown threshold (T_{TSD}) to ensure proper operation during both start-up and steady state. Since dynamic power consumption can be an order of magnitude higher than steady-state levels, the output start-up time and inrush current limiting must be considered in the design to prevent thermal shutdown events.

The soft-start capacitor (C_{SS}) must be calculated based on the following two scenarios:

Case 1: Start-Up without Load - Only Output Capacitance C_{OUT} Draws Current during Start-Up

During a capacitive load start-up, the output voltage increases with a constant slope, and the inrush current remains at a fixed value. As the voltage differential across the internal FET gradually decreases, its power dissipation is reduced accordingly. Figure 6 illustrates the output voltage, inrush current, and device power dissipation curves during start-up with an output capacitor. The average chip power dissipation during the start-up process equals the time-averaged value of the instantaneous power.

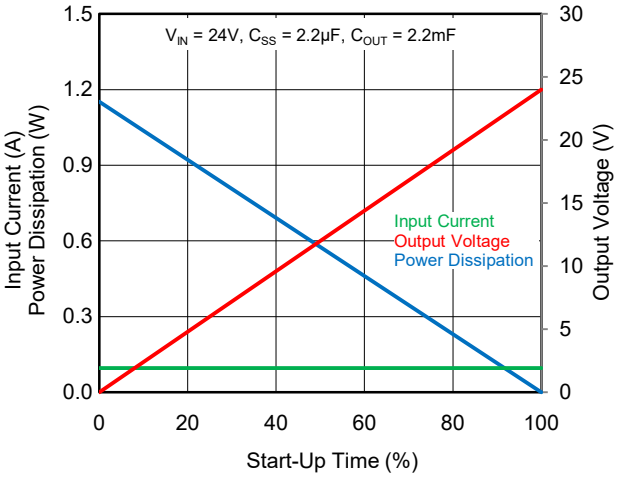


Figure 6. P_{D_INRUSH} due to Inrush Current

The inrush current is determined as shown in Equation 12.

$$I = C \times \frac{dV}{dt} \geq I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}} \quad (12)$$

Average power dissipated during start-up is given by Equation 13.

$$P_{D_INRUSH} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (13)$$

Equation 13 states that during the start-up phase, the inrush current solely charges the output capacitor.

APPLICATION INFORMATION (continued)

Case 2: Start-Up with Load - Output Capacitance C_{OUT} and Load Draws Current during Start-Up

During start-up, the presence of additional loads will introduce extra power loss. Taking a resistive load R_{L_SU} as an example, Figure 9 shows its output voltage, inrush current, and the chip's instantaneous power dissipation. The Figure 7 illustrates the relationship between the power loss of the internal FET and the start-up time. The additional power loss during start-up can be calculated using Equation 14.

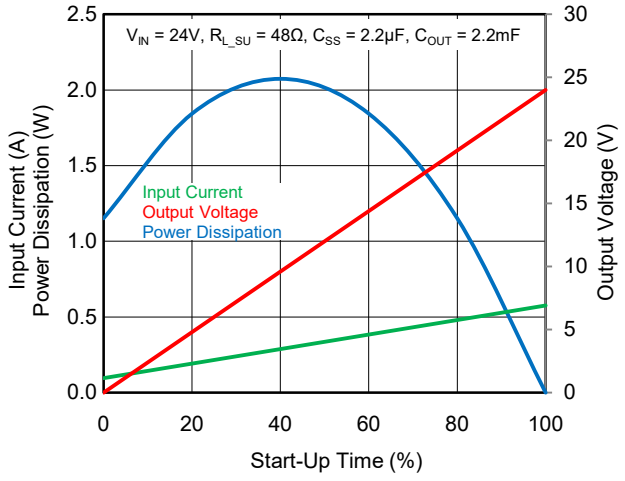


Figure 7. P_{D_INRUSH} due to Inrush and Load Current

$$P_{D_LOAD} = \frac{1}{6} \times \frac{V_{IN}^2}{R_{L_SU}} \quad (14)$$

The total power dissipation during start-up is given by Equation 15.

$$P_{D_STARTUP} = P_{D_INRUSH} + P_{D_LOAD} \quad (15)$$

The total current during the start-up phase is given by Equation 16.

$$I_{STARTUP} = I_{INRUSH} + I_{L_t} \quad (16)$$

With the inrush current set to I_{INRUSH} = 0.1A for this case, t_{SS} is calculated using Equation 17.

$$t_{SS} = 2.2ms \times \frac{24}{0.1} = 0.528s \quad (17)$$

Based on the calculated start-up time, the C_{SS} capacitor value can be determined using Equation 18.

$$C_{SS} = \frac{t_{SS}}{8 \times 10^3 \times V_{IN}} = 2.75\mu F \quad (18)$$

where:

t_{SS} = 0.528s.

V_{IN} = 24V.

Choose the closest standard value: 2.2μF/16V capacitor.

The inrush power dissipation is calculated, using Equation 19.

$$P_{D_INRUSH} = 0.5 \times V_{IN} \times I_{INRUSH} = 1.2W \quad (19)$$

where:

V_{IN} = 24V.

I_{INRUSH} = 0.1A.

Considering the start-up with 48Ω load, the additional power dissipation, is calculated using Equation 20.

$$P_{D_LOAD} = \frac{1}{6} \times \frac{V_{IN}^2}{R_{L_SU}} = 2W \quad (20)$$

where:

V_{IN} = 24V.

R_{L_SU} = 48Ω.

The total device power dissipation during start-up is given by Equation 21.

$$P_{D_STARTUP} = P_{D_INRUSH} + P_{D_LOAD} = 3.2W \quad (21)$$

Based on the relationship between thermal shutdown power and time, at a maximum ambient temperature (T_A) of +25℃, the maximum allowable duration for a power dissipation of 3.2W is 3000ms. Considering variations in load, component tolerances, input voltage, and circuit layout, it is recommended to reserve at least a 30% margin.

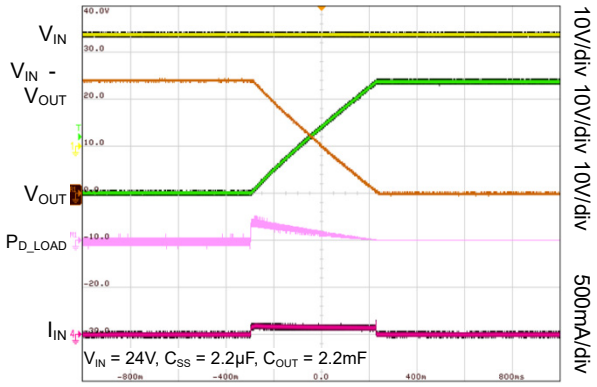
In the above case, a 2.2μF soft-start capacitor sets the start-up time to approximately 528ms, which meets the start-up requirement for a 48Ω load. To further reduce power dissipation, a larger soft-start capacitor (C_{SS}) value can be selected.

APPLICATION INFORMATION (continued)

Support Component Selections - R_{nFLT} and C_{IN}

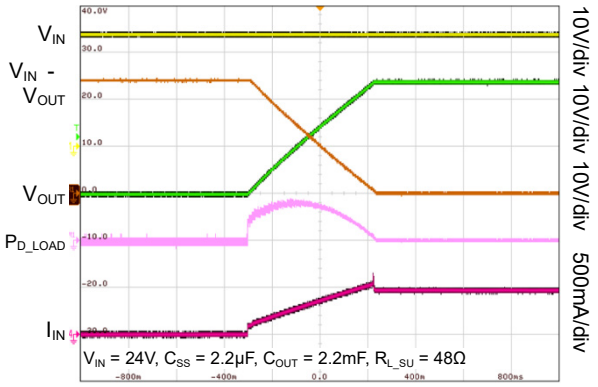
The nFLT pin is an open-drain output and requires an external pull-up resistor, R_{nFLT}. The maximum sink current for this pin must not exceed 10mA. It is recommended to use a resistor value between 10kΩ and 100kΩ for R_{nFLT}. C_{IN} is the input bypass capacitor, which serves to suppress noise from the power supply. A 1μF capacitor is recommended for C_{IN}.

Application Curves



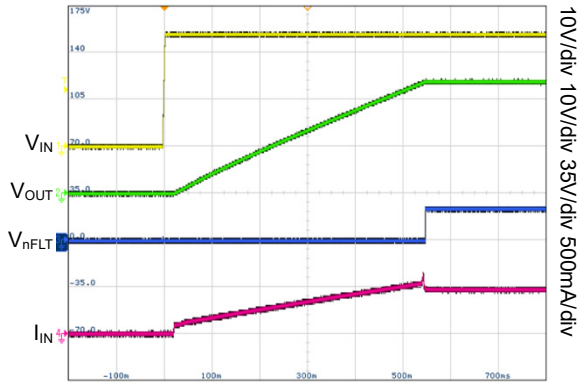
Time (200ms/div)

Figure 8. Start-Up without Load



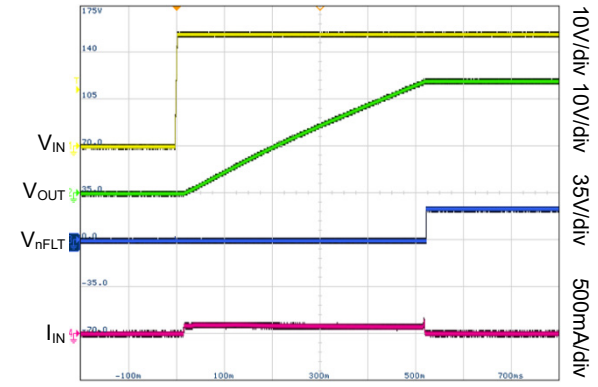
Time (200ms/div)

Figure 9. Start-Up with Load



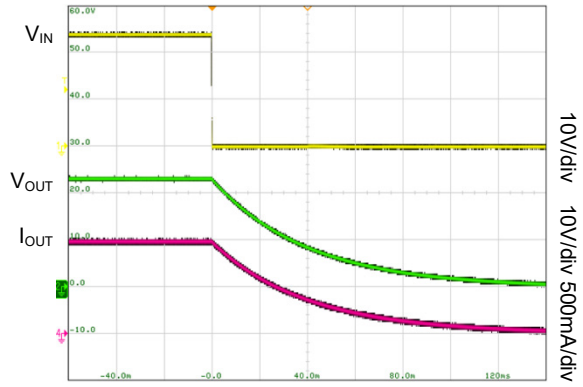
Time (100ms/div)

Figure 10. Start-Up with V_{IN} - 48Ω Load



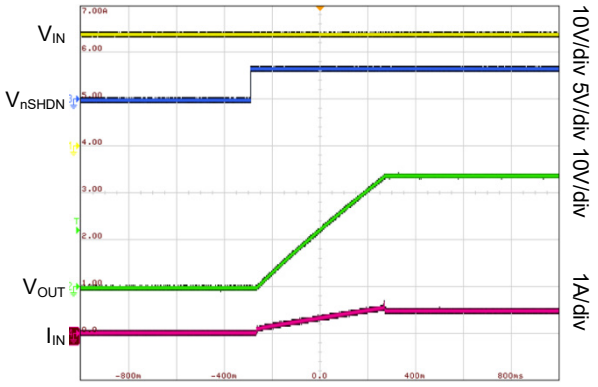
Time (100ms/div)

Figure 11. Start-Up with V_{IN} - No Load



Time (20ms/div)

Figure 12. Power Fail with 24Ω Load - Supports 1A Load for 10ms Power Fail



Time (200ms/div)

Figure 13. Start-Up with Shutdown Pin - 48Ω Load

APPLICATION INFORMATION (continued)

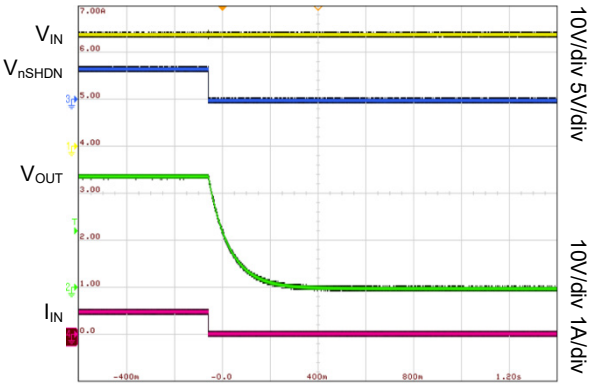


Figure 14. Power Down with Shutdown Pin - 48Ω Load

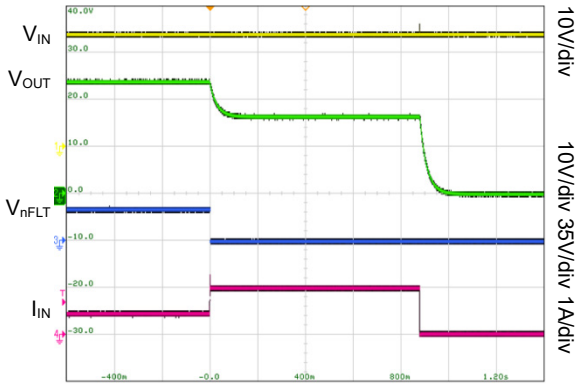


Figure 15. Over Load Response - Load Stepped from 100Ω to 18Ω Load

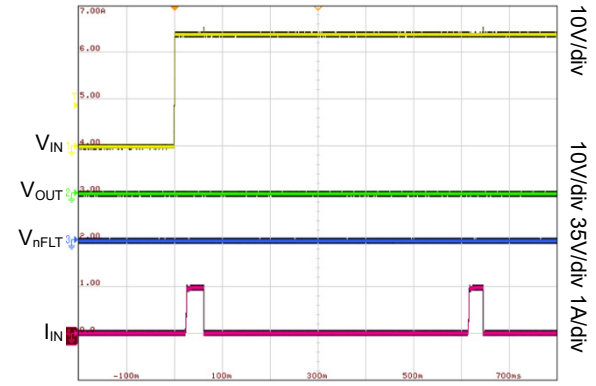


Figure 16. Turn-On with Short-Circuit on Output



Figure 17. Reverse Polarity Protection

APPLICATION INFORMATION (continued)

System Examples

Active ORing Operation

A common system power redundancy configuration is shown in Figure 18.

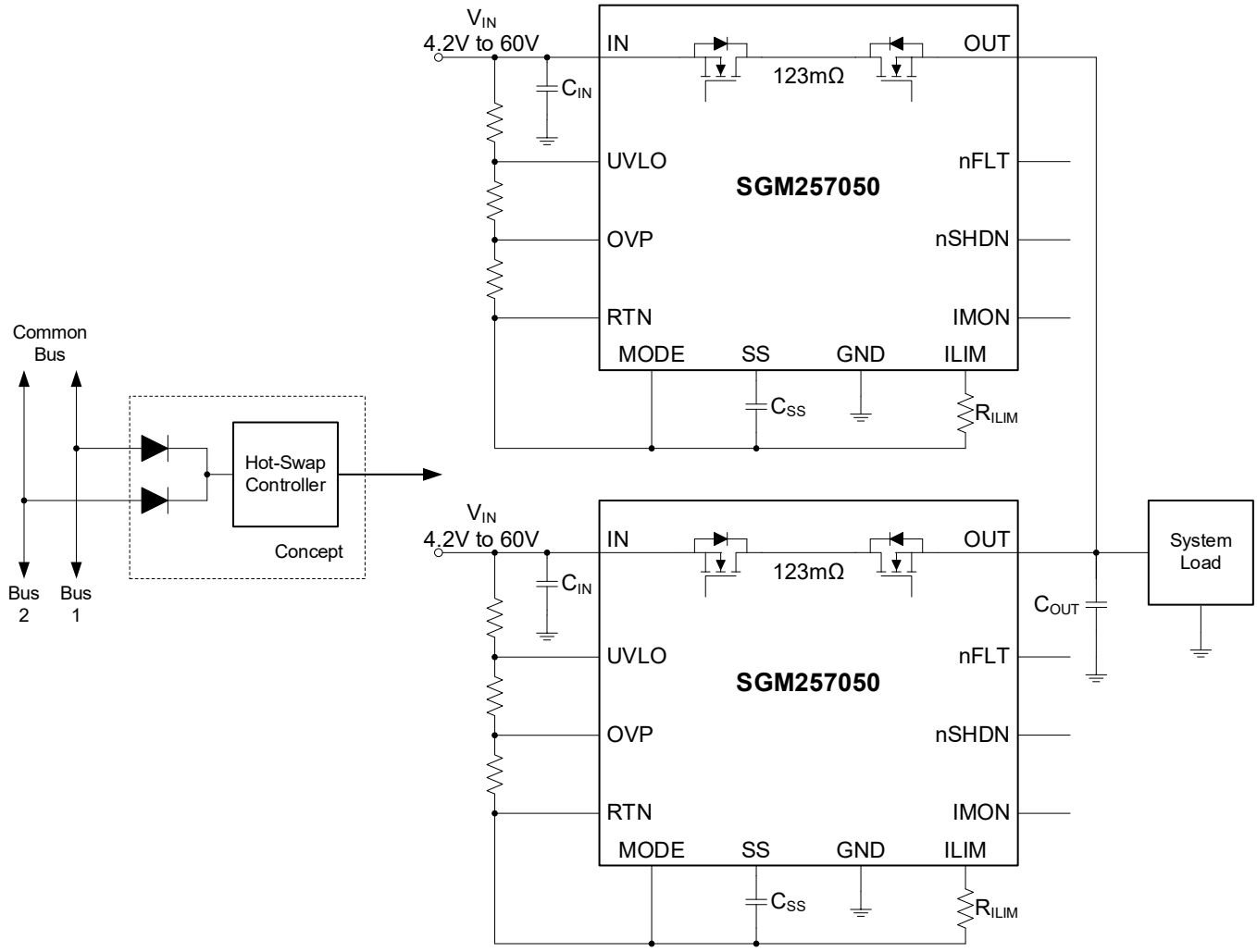


Figure 18. Active ORing Application Schematic

Such applications traditionally use Schottky ORing diodes to connect parallel power supplies. However, this approach introduces issues such as a high forward voltage drop, significant power loss, and severe heat generation. As an alternative, the SGM257050, which integrates back-to-back N-channel FETs, offers a simple and highly effective solution to this problem.

The SGM257050 utilizes a fast reverse-voltage comparator to control its internal FET. To prevent false triggering, this control incorporates a defined hysteresis in turn-on and turn-off operations, as illustrated in Figure 19.

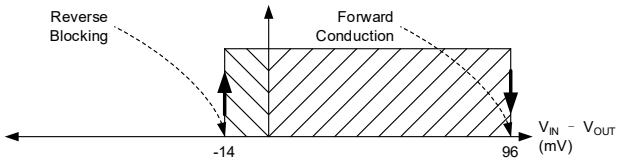
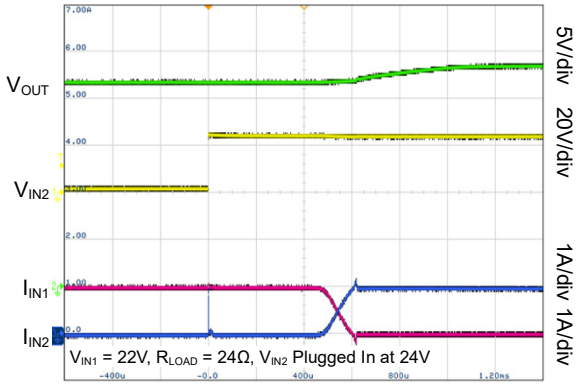


Figure 19. Active ORing Thresholds

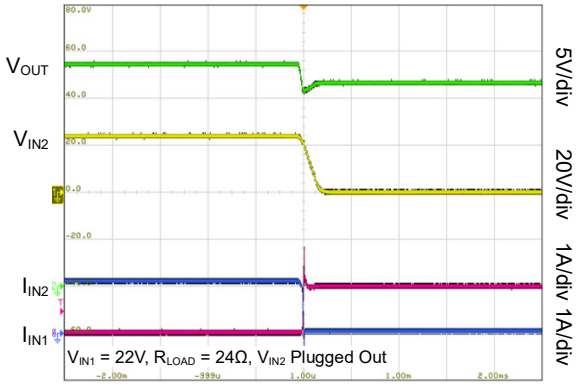
APPLICATION INFORMATION (continued)

When the voltage difference (V_{IN} - V_{OUT}) falls below -114mV, the internal FET is quickly turned off within 1.5μs. Conversely, when the forward voltage (V_{IN} - V_{OUT}) exceeds +196mV, the FET is enabled within 70μs. Figure 20 and Figure 21 show the typical switch-over waveforms of the SGM257050 in an active ORing application.



Time (200μs/div)

Figure 20. Active ORing between Two Supplies V_{OUT} Change Over to V_{IN2}



Time (500μs/div)

Figure 21. Active ORing between Two Supplies V_{OUT} Change Over to V_{IN1}

Field Supply Protection in PLC, DCS I/O Modules

In PLC or Distributed Control Systems (DCS), I/O modules often interface with external field-side power supplies to meet the power demands of sensors, actuators, and other field devices. Power supply faults or wiring errors can lead to system failure or device damage. The SGM257050, when placed at the front end, provides effective protection for downstream equipment. It integrates under-voltage (UVLO), over-voltage (OVP), and reverse-polarity protection, preventing permanent damage by ensuring the back-end components remain within their specified voltage limits.

The field power supply typically powers multiple I/O modules, and its available current far exceeds the capacity of a single module. The SGM257050 integrates over-current protection, which effectively limits the module current to ensure it does not exceed the design specifications of an individual module. The device also features fast short-circuit protection. In the event of a load fault causing a sudden current surge, the chip can rapidly disconnect the faulty load, preventing bus voltage droop and ensuring normal operation of other modules. Its high-precision (±5.5% at 1A) current limiting capability supports the connection of multiple I/O modules to a common field power supply. Additionally, the load current monitoring (IMON) and fault indicator (nFLT) functions enable real-time status monitoring of the load.

The SGM257050 also provides reverse-current protection in case of output wiring errors, functioning as an ideal diode. Reverse current flow could potentially damage the field power supply and cause overheating or permanent failure of I/O modules.

If the field supply input is reversely connected, downstream loads may suffer permanent damage due to the applied reverse voltage. The SGM257050 features integrated input reverse polarity protection, capable of withstanding voltages down to -60V and effectively preventing reverse voltage from appearing at the output.

APPLICATION INFORMATION (continued)

Simple 24V Power Supply Path Protection

The protection schematic for a 24V power supply using the SGM257050 requires only three external components, referring to Figure 22. The necessary components include: a current-limit set resistor R_{ILIM}, and C_{IN} and C_{OUT} capacitors.

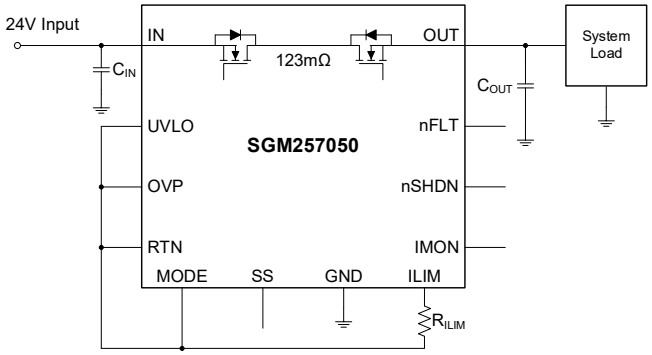


Figure 22. SGM257050 Configured for a Simple 24V Supply Path Protection

The protection features enabled in this configuration include:

- Input Reverse Polarity Protection.
- Under-Voltage Lockout (UVLO) with a 14.9V Threshold.
- Over-Voltage Protection (OVP) with a 32.6V Shutdown Threshold.
- Active Inrush Current Control with Slew Rate Management (24V/1.3ms).
- Reverse Current Blocking.
- Auto-Retry Function and Accurate Current Limiting.

Do's and Don'ts

Don't connect RTN to GND. Connecting RTN to GND will cause the input reverse polarity protection to fail.

All external components for the SGM257050 - including R_{ILIM}, C_{SS}, R_{IMON}, R_{MODE}, and the UVLO and OVP resistor dividers - must be connected to the RTN pin.

To optimize thermal performance, the PowerPAD must be connected to the RTN plane.

Power Supply Recommendations

The SGM257050 electronic fuse is recommended for a working power supply voltage range of 4.2V to 60V, with the V_{IN} (input voltage) supported up to 60V. For power supplies a few inches away, a 1μF or larger bypass ceramic capacitor should be placed at the input end.

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input with a negative voltage spike occurring at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the OUT pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

The value of the input capacitance can be calculated from the Equation 22:

$$V_{SPIKE_ABSOLUTE} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (22)$$

where:

V_{IN} is the rating of the input voltage.

I_{LOAD} is the load current.

L_{IN} is the effective inductance viewed from the source.

C_{IN} is the capacitance of the input.

For applications such as USB-C interfaces, the power cord may be plugged into the output of the device. In this case, the voltage stress from OUT to IN may exceed the absolute maximum rating, so it is recommended to add a TVS diode from OUT to IN to clamp the voltage for safety.

APPLICATION INFORMATION (continued)

The circuit implementation featuring optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in Figure 23.

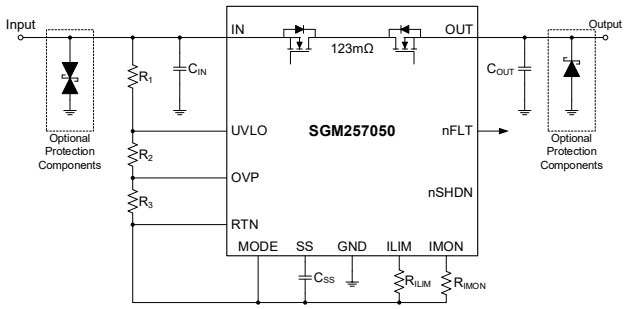


Figure 23. Circuit Implementation with Optional Protection Components

Layout Guidelines

- In any application, it is recommended to connect a decoupling capacitor of 1μF or greater between IN and GND. This decoupling capacitor should be as close as possible to IN and GND pins.
- The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.
- RTN serves as the chip's reference ground and must be implemented as a copper plane or a dedicated copper island.
- All external components - including R_{ILIM}, C_{SS}, R_{IMON}, R_{MODE}, and the OVP and UVLO resistors - must be placed close to their respective chip pins and connected to the RTN plane. All associated traces must be made as short as possible.
- The traces for the R_{ILIM} and R_{IMON} components must be kept as short as possible to minimize parasitic effects that could degrade accuracy. Furthermore, these critical traces must be routed away from any switching signals to prevent noise coupling.
- Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.
- Thermal Design Requirement: To ensure reliable operation at rated power, the PowerPAD must be soldered directly to the RTN copper plane. For high-current applications, the PCB bottom layer or other internal planes should be utilized to enhance thermal dissipation.

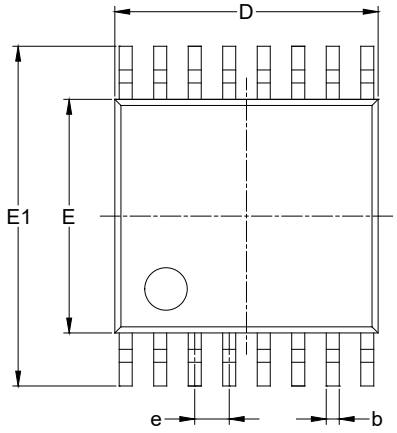
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

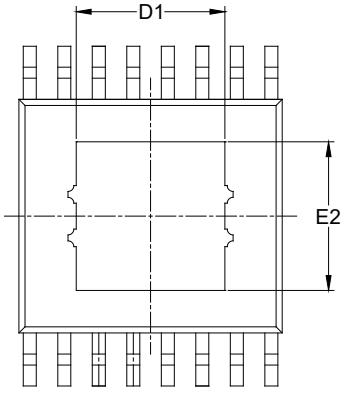
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

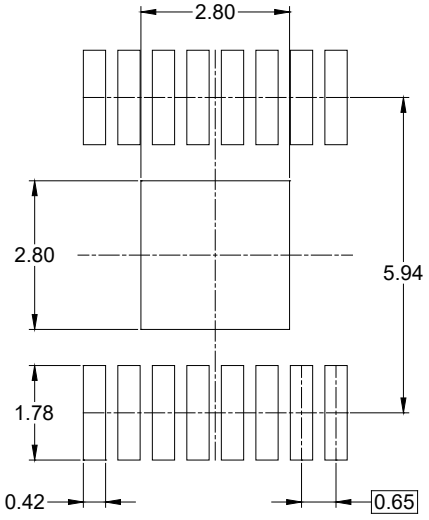
TSSOP-16B (Exposed Pad)



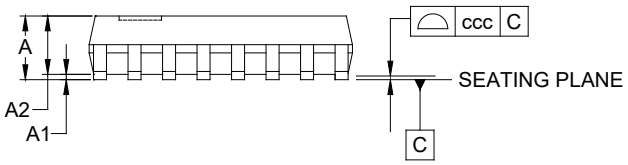
TOP VIEW

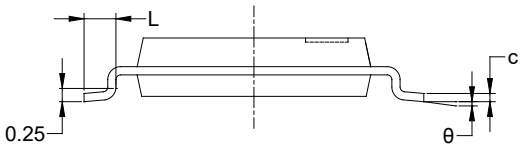


BOTTOM VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



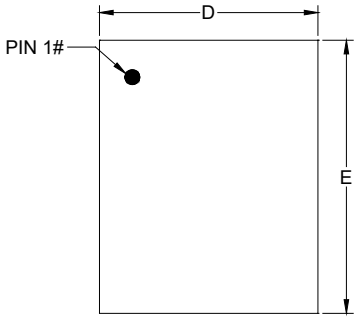


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
D1	2.600	-	3.000
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.600	-	3.000
e	0.650 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

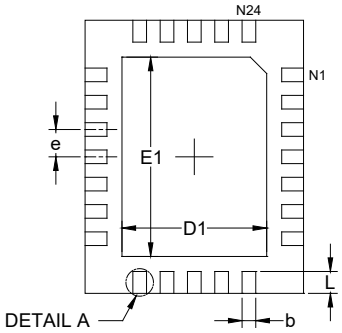
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions, or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

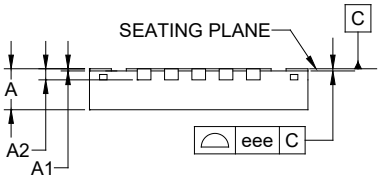
TQFN-4×5-24AL



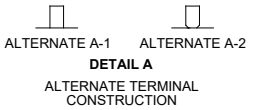
TOP VIEW



BOTTOM VIEW

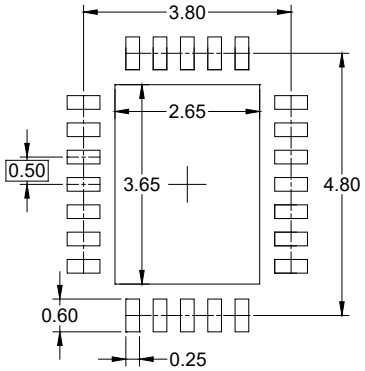


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



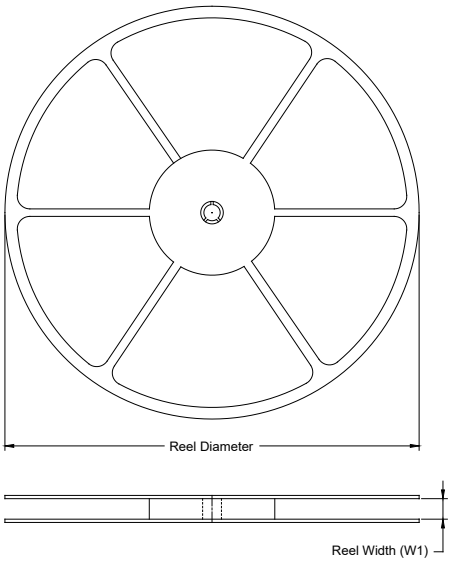
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.900	-	4.100
E	4.900	-	5.100
D1	2.550	-	2.750
E1	3.550	-	3.750
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

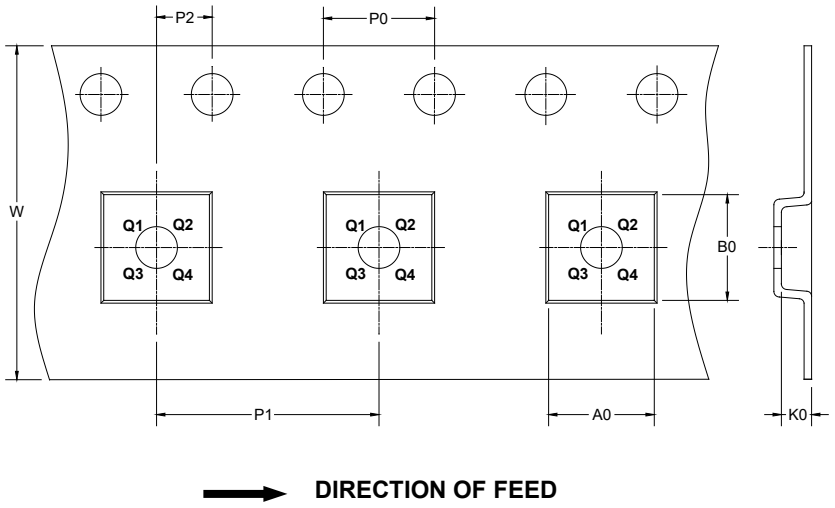
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



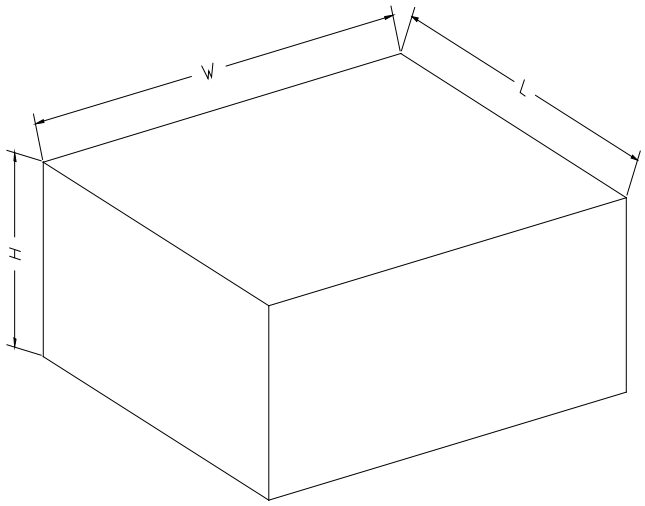
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16B (Exposed Pad)	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-4×5-24AL	13"	12.4	4.30	5.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002