SGM62115
Single Inductor Buck-Boost Converter with 1A Switches and Adjustable Soft-Start

GENERAL DESCRIPTION

The SGM62115 is a fully integrated synchronous Buck-Boost converter capable to operate with 2.15V to 5.5V input range, making it ideal for battery-powered applications including 1-cell Li-ion and 2-cell or 3-cell Alkaline/NiMH battery systems. The device supports up to 0.5A output current in Boost mode with input voltage above 2.5V, and up to 1A in Buck mode.

The SGM62115 employs peak current mode control with a fixed switching frequency of 2.5MHz to regulate the output voltage. Additionally, the device supports configurable light-load operation via the MODE pin, allowing selection between forced PWM (FPWM) and automatic PFM modes. PFM mode provides higher light-load efficiency, while FPWM maintains a constant switching frequency across the entire load range. The SGM62115 is offered in both adjustable output and fixed 3.3V output versions.

The SGM62115 integrates multiple protection features to enhance device robustness. These include programmable average input current limiting combined with soft-start to reduce startup inrush current, cycle-by-cycle over-current protection, and thermal shutdown protection. In addition, the device provides true load-disconnect when the EN pin is pulled low.

The device is available in Green TQFN-2.5×2.5-12L and WLCSP-1.33×1.62-12B packages.

FEATURES

- **Input Voltage Range: 2.15V to 5.5V**
- **Adjustable Output Voltage Range from 2.5V to 5.5V**
- **Up to 90% Efficiency in Boost Mode and up to 95% in Buck Mode**
- **0.5A Continuous Output Current at V_{IN} ≥ 2.5V and V_{OUT} = 3.3V**
- **Real Buck or Boost with Seamless Transition between Buck and Boost Mode**
- **Low Quiescent Current: 32μA (TYP)**
- **Adjustable and Fixed (3.3V) Output Voltage Options**
- **2.5MHz Typical Switching Frequency**
- **Adjustable Average Input Current Limit**
- **Adjustable Soft-Start Time**
- **Automatic Power Save Mode or Forced PWM Mode**
- **Load Disconnect during Shutdown**
- **Over-Temperature Protection**
- **Available in Green WLCSP-1.33×1.62-12B and TQFN-2.5×2.5-12L Packages**

APPLICATIONS

Cellular and Smart Phones
Tablet PCs
PC and Smart Phone Accessories
Battery Powered Applications
Smart Grid/Smart Meter

TYPICAL APPLICATION

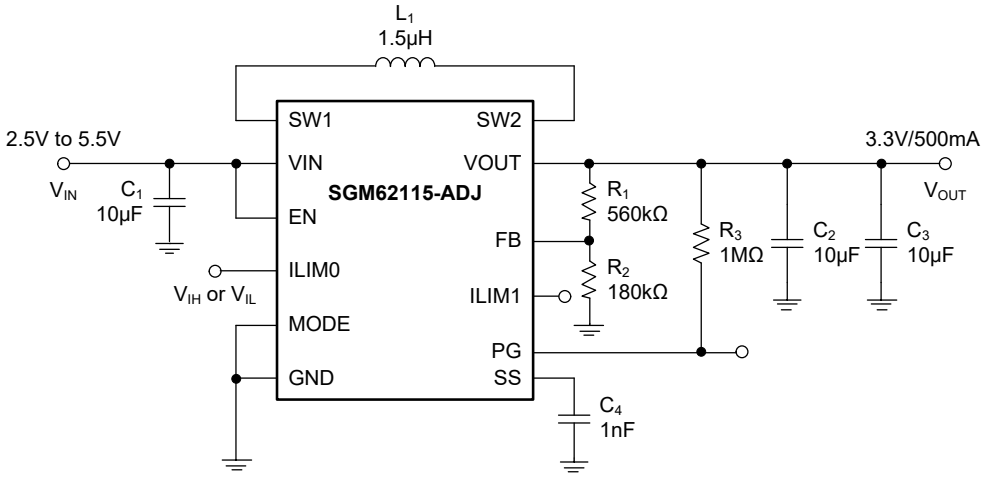


Figure 1. Typical Application Circuit

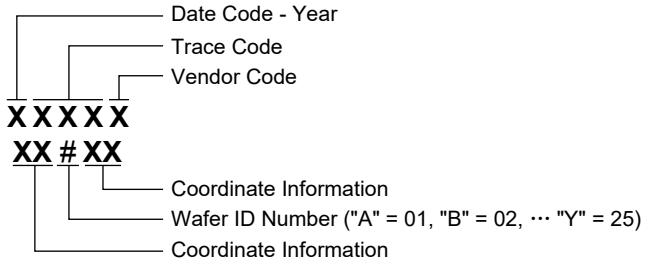
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM62115-3.3	WLCSP-1.33×1.62-12B	-40℃ to +85℃	SGM62115-3.3YG/TR	099YG XXXXX XX#XX	Tape and Reel, 5000
	TQFN-2.5×2.5-12L	-40℃ to +85℃	SGM62115-3.3YTSI12G/TR	MDJ XXXXX	Tape and Reel, 3000
SGM62115-ADJ	WLCSP-1.33×1.62-12B	-40℃ to +85℃	SGM62115-ADJYG/TR	SWUYG XXXXX XX#XX	Tape and Reel, 5000
	TQFN-2.5×2.5-12L	-40℃ to +85℃	SGM62115-ADJYTSI12G/TR	MCK XXXXX	Tape and Reel, 3000

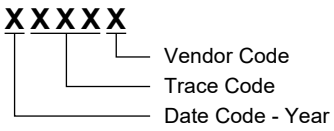
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

WLCSP-1.33×1.62-12B



TQFN-2.5×2.5-12L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage (1)
- VIN, VOUT ..... -0.3V to 6V
- EN, FB, MODE, ILIM0, ILIM1, SS, PG ..... -0.3V to 6V
- SW1, SW2..... -0.3V to 6V
- SW1, SW2 (10ns Transient)..... -0.3V to 9.5V

Package Thermal Resistance
- WLCSP-1.33×1.62-12B, θ_{JA}..... 94.5℃/W
- WLCSP-1.33×1.62-12B, θ_{JB}..... 20.3℃/W
- WLCSP-1.33×1.62-12B, θ_{JC}..... 29.9℃/W
- TQFN-2.5×2.5-12L, θ_{JA}..... 26.8℃/W
- TQFN-2.5×2.5-12L, θ_{JB}..... 59.8℃/W
- TQFN-2.5×2.5-12L, θ_{JC}..... 30.1℃/W

Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (2) (3)
HBM.....±4000V
CDM .....±750V

NOTES:

1. All voltage values are with respect to network ground pin.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN}.....2.15V to 5.5V
Output Current, I_{OUT} 0.5A
Inductance, L (1).....1.5μH
Output Capacitance, C_{OUT} (2)..... 10μF (MIN)
Operating Ambient Temperature .....-40℃ to +85℃
Operating Junction Temperature..... -40℃ to +125℃

NOTES:

1. Effective inductance under operating conditions. The listed nominal value corresponds to a typical inductor selected to satisfy the required inductance.

2. Due to the DC bias characteristic of ceramic capacitors, the effective capacitance is lower than the nominal value under applied voltage. For this reason, the capacitance is specified to account for the DC bias effect when selecting the nominal capacitor. The provided nominal value corresponds to a typical capacitor chosen to meet the minimum required capacitance.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

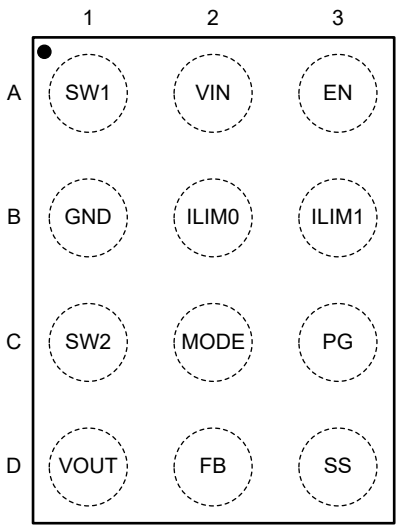
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

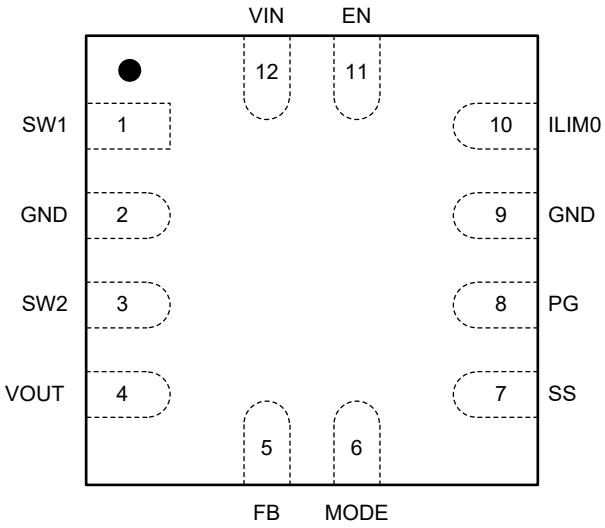
PIN CONFIGURATIONS

(TOP VIEW)



WLCSP-1.33×1.62-12B

(TOP VIEW)



TQFN-2.5×2.5-12L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
WLCSP	TQFN			
A1	1	SW1	P	The SW1 pin is the high-current switching node of the synchronous Buck-Boost power stage, connecting the internal power MOSFETs and the external inductor.
B1	2, 9	GND	GND	Ground for Power Stage and Control Stage. For the TQFN package, pin-2 can be used as PGND, and pin-9 can be used as AGND.
C1	3	SW2	P	The SW2 pin is the high-current switching node of the synchronous Buck-Boost power stage, connecting the internal power MOSFETs and the external inductor.
D1	4	VOUT	P	Buck-Boost Converter Power Output. It supplies power to the load and should be bypassed with low-ESR ceramic capacitors (effective value: 10μF) close to the VOUT and GND.
A2	12	VIN	P	Supply Voltage for Power Stage and Control Stage. A 10μF input capacitor should be placed close to VIN and GND for noise filtering and stability.
B2	10	ILIM0	DI	Programmable Input Inrush Current-Limit Pin. It works together with I_{LIM1}. Do not leave it floating.
C2	6	MODE	DI	Mode Selection Pin. The MODE pin configures the light-load operating mode. Pulling the MODE pin high enables forced PWM mode, while pulling it low enables automatic PFM mode. Do not leave it floating.
D2	5	FB	AI	Voltage Feedback Pin. The FB pin is used to set the output voltage via an external resistor divider, with a typical FB leakage current of 0.01μA and a typical internal reference voltage of 0.8V. If users use the fixed 3.3V version, this pin should be connected to VOUT.
A3	11	EN	DI	Pull high to enable the IC. Do not leave it floating.
B3	—	ILIM1	DI	Programmable Input Inrush Current-Limit Pin. It works together with I_{LIM0}. Do not leave it floating. For the TQFN package, this pin is not available and is internally tied to V_{IH}.
C3	8	PG	DO	The PG pin of the device is an open-drain output. An external pull-up resistor is required for proper operation.
D3	7	SS	AI	The soft-start time can be programmed by connecting an external capacitor. Leaving this pin floating will apply the default soft-start time.

NOTE: AO = analog output, AI = analog input, DI = digital input, DO = digital output, P = power, GND = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply								
Input Voltage Range		V_{IN}			2.15		5.5	V
Minimum Input Voltage to Turn on in Full Load		V_{IN_MIN}	I_{OUT} = 500mA			2.7		V
Output Current		I_{OUT}	ILIM0 = V_{IH}, ILIM1 = V_{IH}			500		mA
V_{IN} Quiescent Current		I_Q	I_{OUT} = 0mA, EN = V_{IN} = 3.6V, V_{OUT} = 3.3V			32	50	μA
V_{OUT} Quiescent Current							10	μA
Shutdown Current		I_{SD}	EN = 0V			0.01	1	μA
Under-Voltage Lockout Threshold		V_{UVLO_TH}	V_{IN} Rising		1.8	1.9	2.0	V
		V_{UVLO_TL}	V_{IN} falling		1.7	1.8	1.9	V
Under-Voltage Lockout Hysteresis		V_{UVLO_HYS}				100		mV
Thermal Shutdown		T_{SD}	Temperature rising			140		℃
Thermal Shutdown Hysteresis		T_{SD_HYS}				20		℃
Logic Signals EN, MODE, ILIM0, ILIM1								
High-Level Input Voltage		V_{IH}	V_{IN} = 2.15V to 5.5V		1.2			V
Low-Level Voltage Input Voltage		V_{IL}	V_{IN} = 2.15V to 5.5V				0.3	V
Input Leakage Current		I_{LKG}	MODE, EN, ILIM0, ILIM1 = GND or V_{IN}			0.01	0.2	μA
Power-Good								
Low-Level Voltage		V_{OL}	I_{SINK} = 100μA				0.3	V
PG Sinking Current		I_{PG}	V_{PG} = 0.3V, V_{IN} = 3.6V		0.1			mA
Input Leakage Current		I_{LKG}	V_{PG} = 3.6V			0.01	0.2	μA
Output								
Output Voltage Range		V_{OUT}			2.5		5.5	V
Feedback Regulation Voltage		V_{FB}				0.8		V
SGM62115-3.3 Output Voltage Accuracy		V_{OUT}	FPWM mode		3.265	3.3	3.335	V
			PFM mode		3.265	3.3	3.399	
Feedback Voltage Accuracy		V_{FB}	PWM mode		-1.4		1.4	%
			PFM mode, f_{SW} = 2.5MHz, L = 1.5μH, C_{OUT} = 10μF		-1		3	
Minimum Output Current to Enter PFM Mode		$I_{PWM-PFM}$	V_{IN} = 3V, V_{OUT} = 3.3V			150		mA
Feedback Input Bias Current		I_{FB}	V_{FB} = 0.8V			10	200	nA
FET On-Resistance	Input High-side	R_{DSON}	I_{SW} = 500mA			90		mΩ
	Output High-side		I_{SW} = 500mA			55		
	Input Low-side		I_{SW} = 500mA			50		
	Output Low-side		I_{SW} = 500mA			85		
Input Current-Limit Boost Mode		I_{IN_MAX}	ILIM0 = V_{IH}, ILIM1 = V_{IH}	V_{IN} = 2.7V to 3V, V_{OUT} = 3V	570		1440	mA
				V_{IN} = 2.7V to 3.3V, V_{OUT} = 3.3V	650		1460	
				V_{IN} = 2.7V to 4.5V, V_{OUT} = 4.5V	730		1590	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Programmable Inrush Current Limit	I_{SS_IN}	ILIM0 = V_{IL}, ILIM1 = V_{IL}, V_{IN} = 3V, V_{OUT} = 3.3V, T_J = -40℃ to +85℃		0.44 × I_{IN_MAX}		mA
		ILIM0 = V_{IH}, ILIM1 = V_{IL}, V_{IN} = 3V, V_{OUT} = 3.3V, T_J = -40℃ to +85℃		0.52 × I_{IN_MAX}		
		ILIM0 = V_{IL}, ILIM1 = V_{IH}, V_{IN} = 3V, V_{OUT} = 3.3V, T_J = -40℃ to +85℃		0.68 × I_{IN_MAX}		
		ILIM0 = V_{IH}, ILIM1 = V_{IH}, V_{IN} = 3V, V_{OUT} = 3.3V, T_J = -40℃ to +85℃		I_{IN_MAX}		
Soft-Start Current	I_{SS}	SGM62115-3.3		1		μA
		SGM62115-ADJ		3		
Line Regulation		V_{IN} = 2.5V to 5.5V, I_{OUT} = 500mA, PWM mode		0.963		mV/V
Load Regulation		V_{IN} = 3.6V, I_{OUT} = 0mA to 500mA, PWM mode		4		mV/A

SWITCHING CHARACTERISTICS

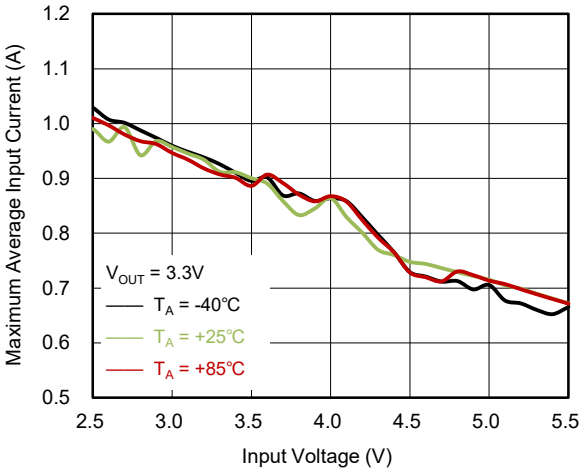
(V_{IN} = 3.6V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output						
Switching Frequency	f_{SW}			2.5		MHz
Soft-Start Time	t_{SS}	V_{OUT} = EN = low to high, SS = floating, Buck mode V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 500mA		150		μs
		V_{OUT} = EN = low to high, SS = floating, Boost mode V_{IN} = 2.5V, V_{OUT} = 3.3V, I_{OUT} = 500mA		150		
Startup Delay	t_D	Time from when EN = high to when device starts switching		192		μs

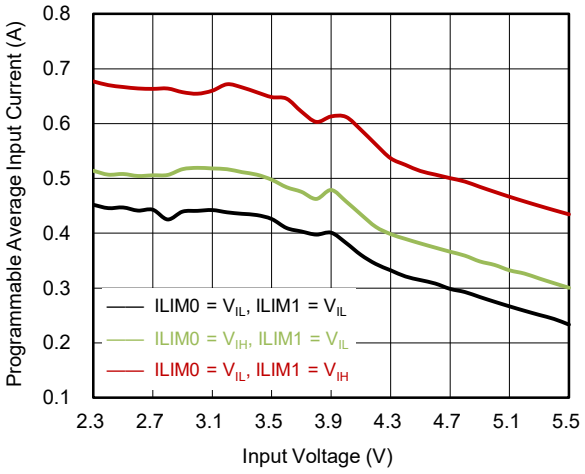
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, C_{IN} = 10μF, L = 1.5μH and C_{OUT} = 2 × 10μF, unless otherwise noted.

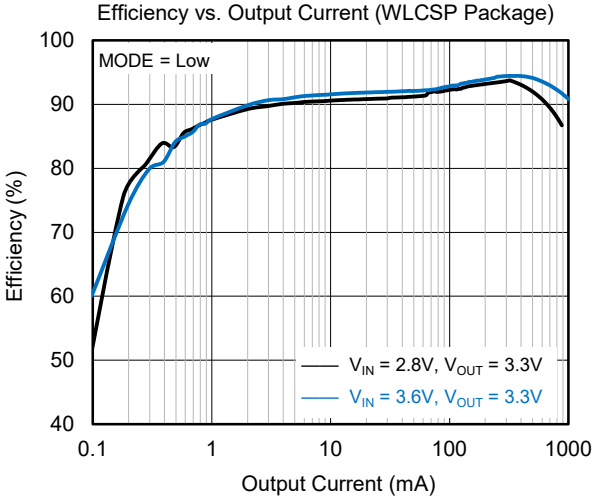
Maximum Average Input Current vs. Input Voltage



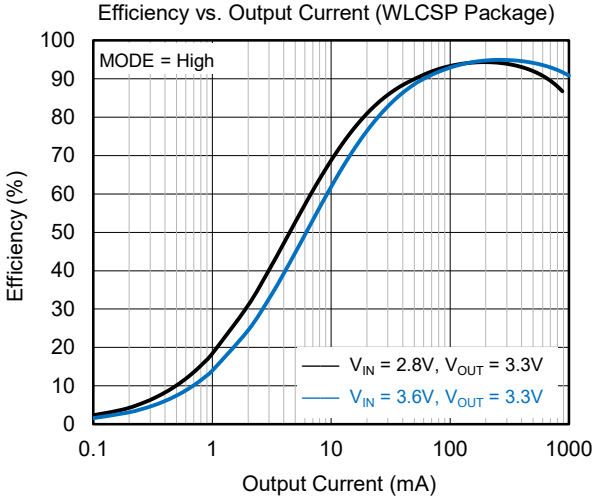
Programmable Average Input Current vs. Input Voltage



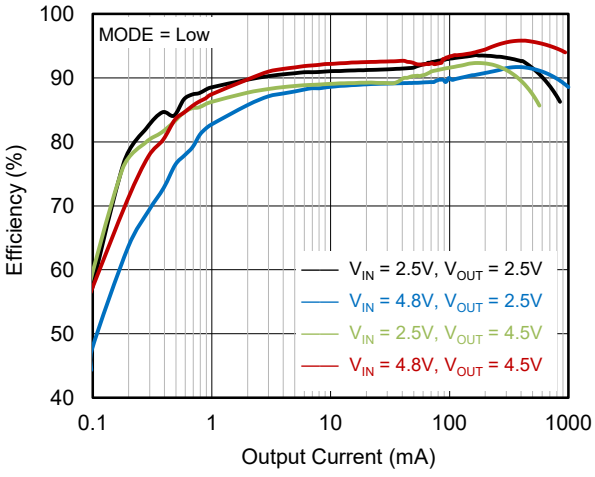
Efficiency vs. Output Current (WLCSP Package)



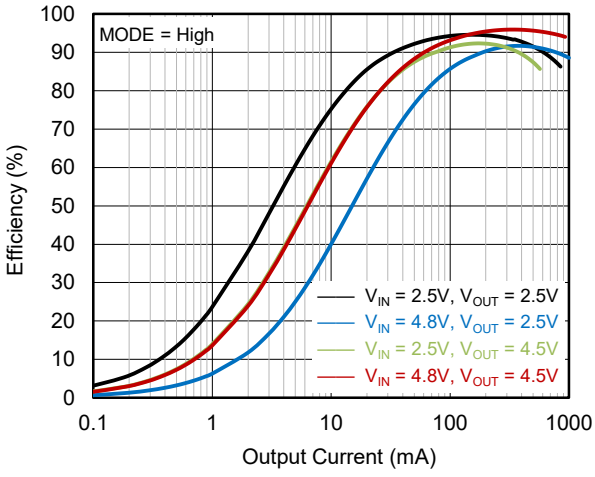
Efficiency vs. Output Current (WLCSP Package)



Efficiency vs. Output Current (TQFN Package)



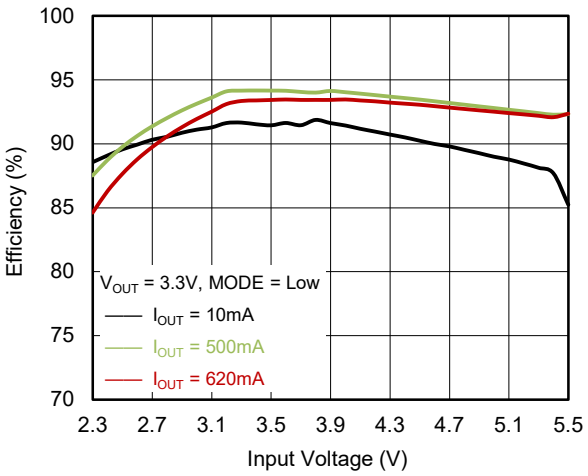
Efficiency vs. Output Current (TQFN Package)



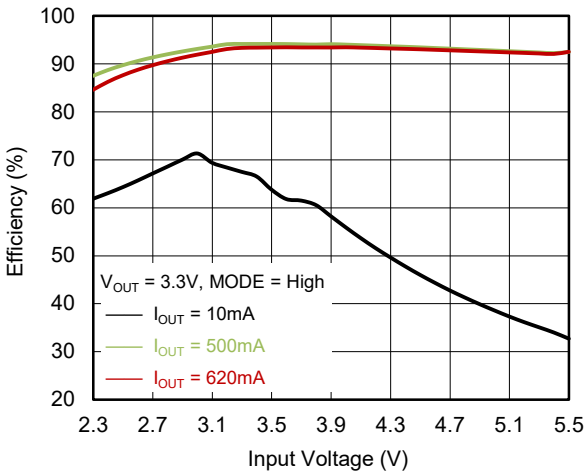
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{IN} = 10μF, L = 1.5μH and C_{OUT} = 2 × 10μF, unless otherwise noted.

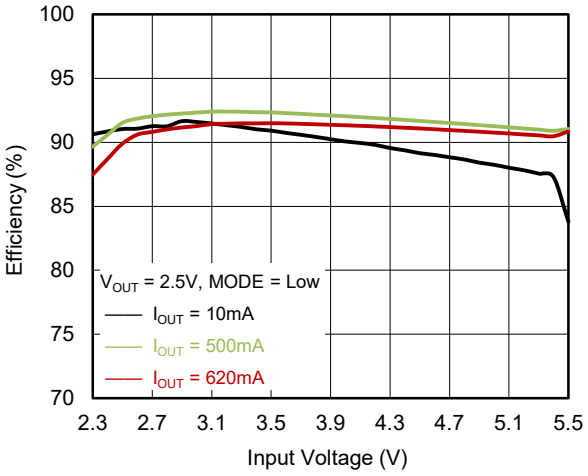
Efficiency vs. Input Voltage (WLCSP Package)



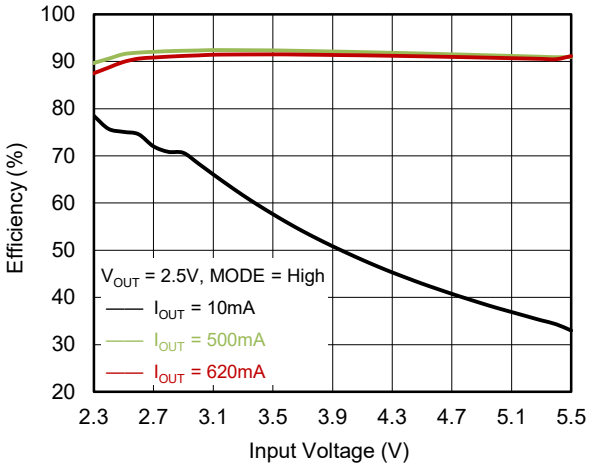
Efficiency vs. Input Voltage (WLCSP Package)



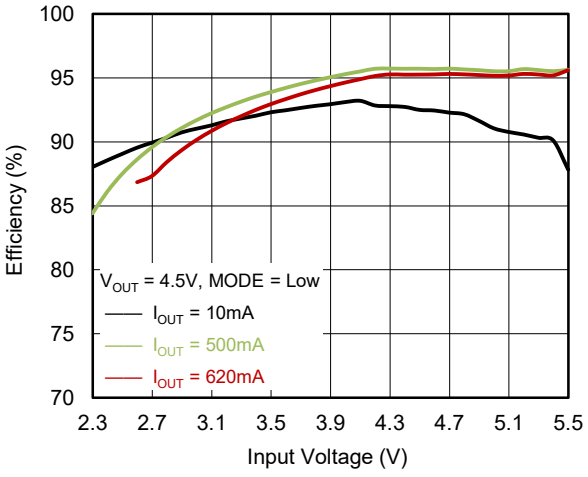
Efficiency vs. Input Voltage (TQFN Package)



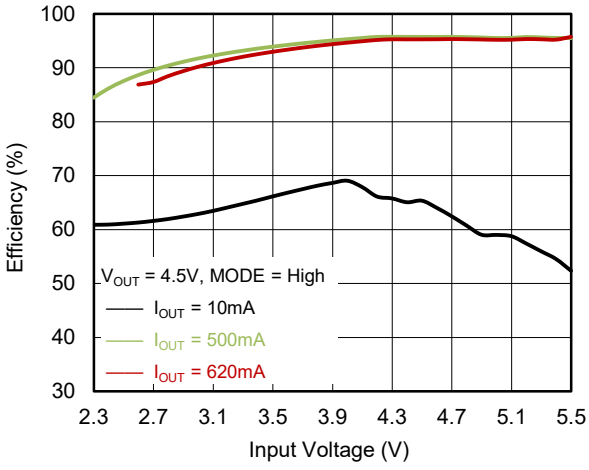
Efficiency vs. Input Voltage (TQFN Package)



Efficiency vs. Input Voltage (TQFN Package)



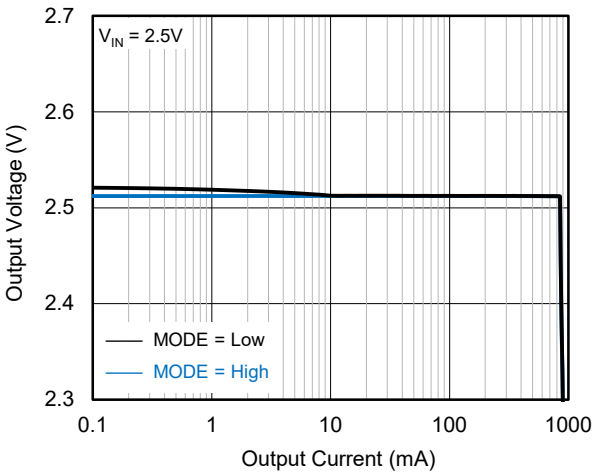
Efficiency vs. Input Voltage (TQFN Package)



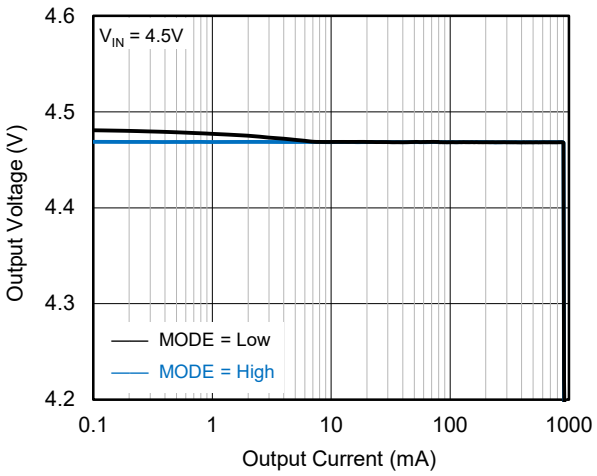
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{IN} = 10μF, L = 1.5μH and C_{OUT} = 2 × 10μF, unless otherwise noted.

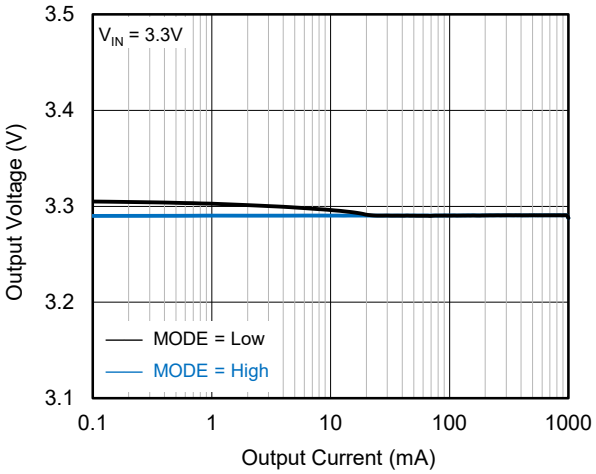
Output Voltage vs. Output Current (TQFN Package)



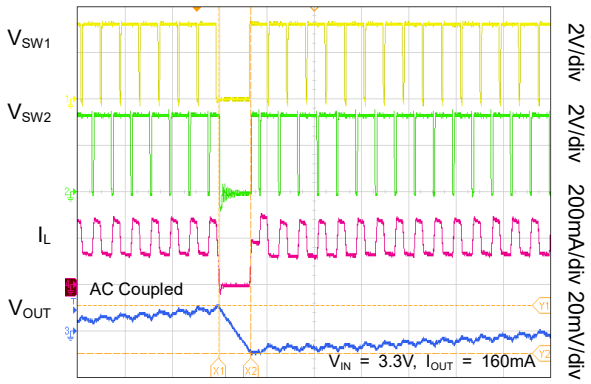
Output Voltage vs. Output Current (TQFN Package)



Output Voltage vs. Output Current (WLCSP Package)

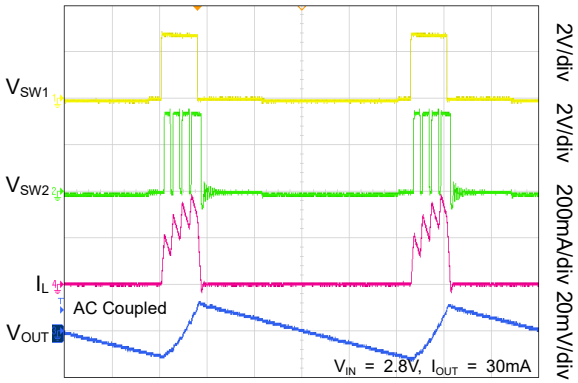


Output Voltage Ripple in Buck-Boost Mode



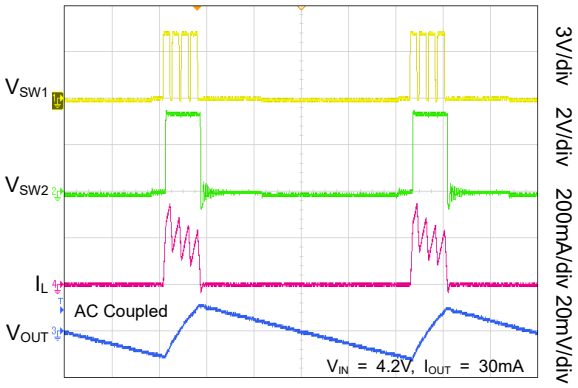
Time (2μs/div)

Output Voltage Ripple in Boost Mode



Time (2μs/div)

Output Voltage Ripple in Buck Mode

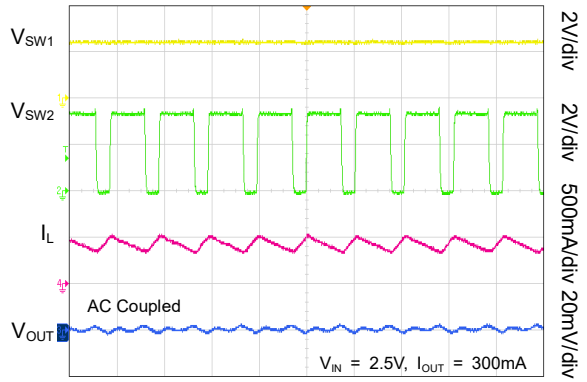


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

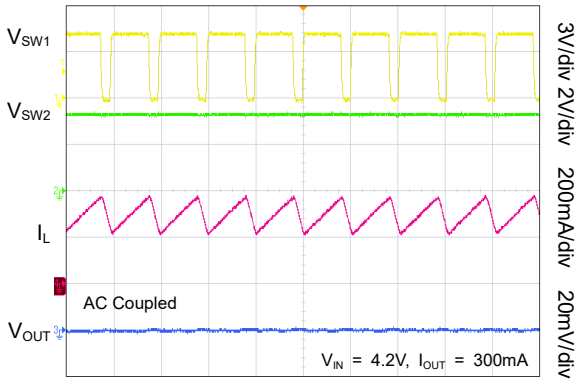
T_A = +25℃, C_{IN} = 10μF, L = 1.5μH and C_{OUT} = 2 × 10μF, unless otherwise noted.

Switching Waveform in Boost Mode and PWM



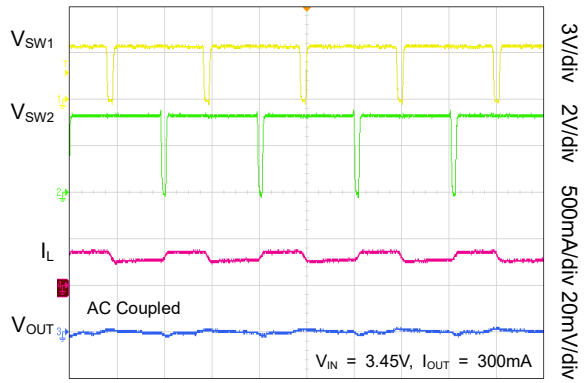
Time (400ns/div)

Switching Waveform in Buck Mode and PWM



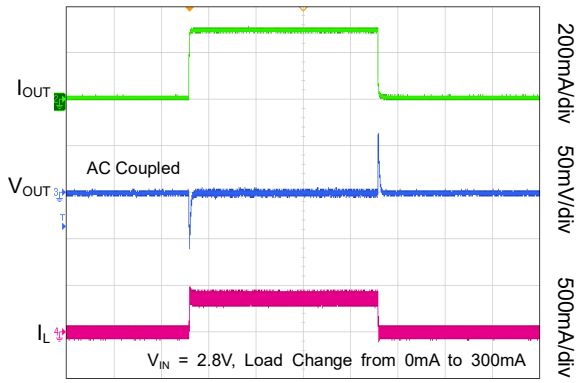
Time (400ns/div)

Switching Waveform in Buck-Boost Mode and PWM



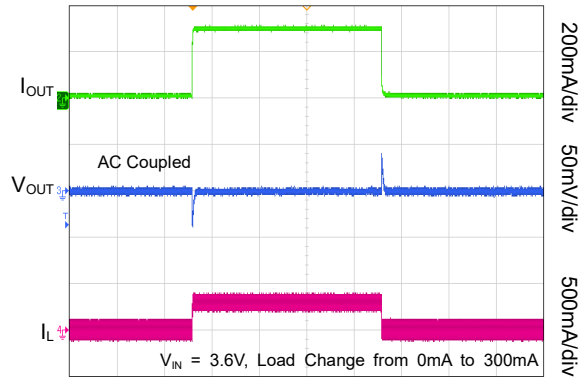
Time (400ns/div)

Load Transient Response



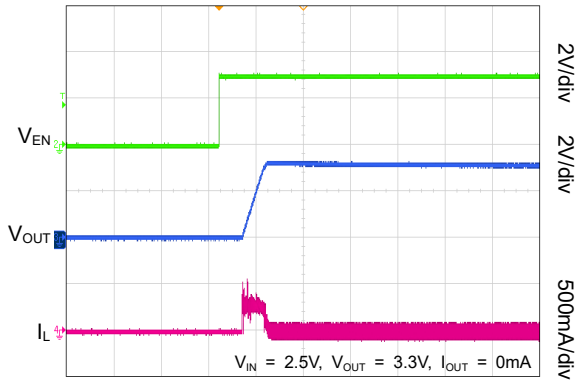
Time (500μs/div)

Load Transient Response



Time (500μs/div)

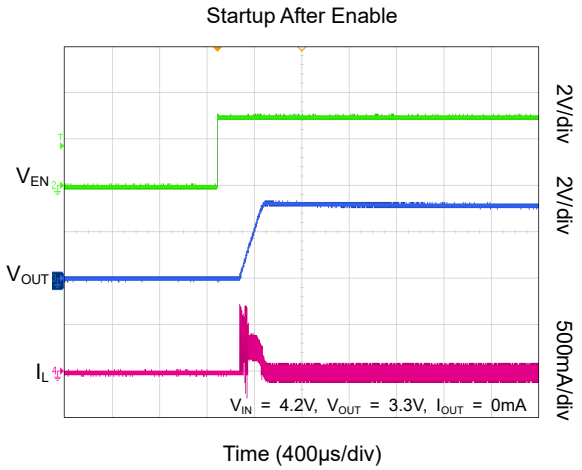
Startup After Enable



Time (400μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{IN} = 10μF, L = 1.5μH and C_{OUT} = 2 × 10μF, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

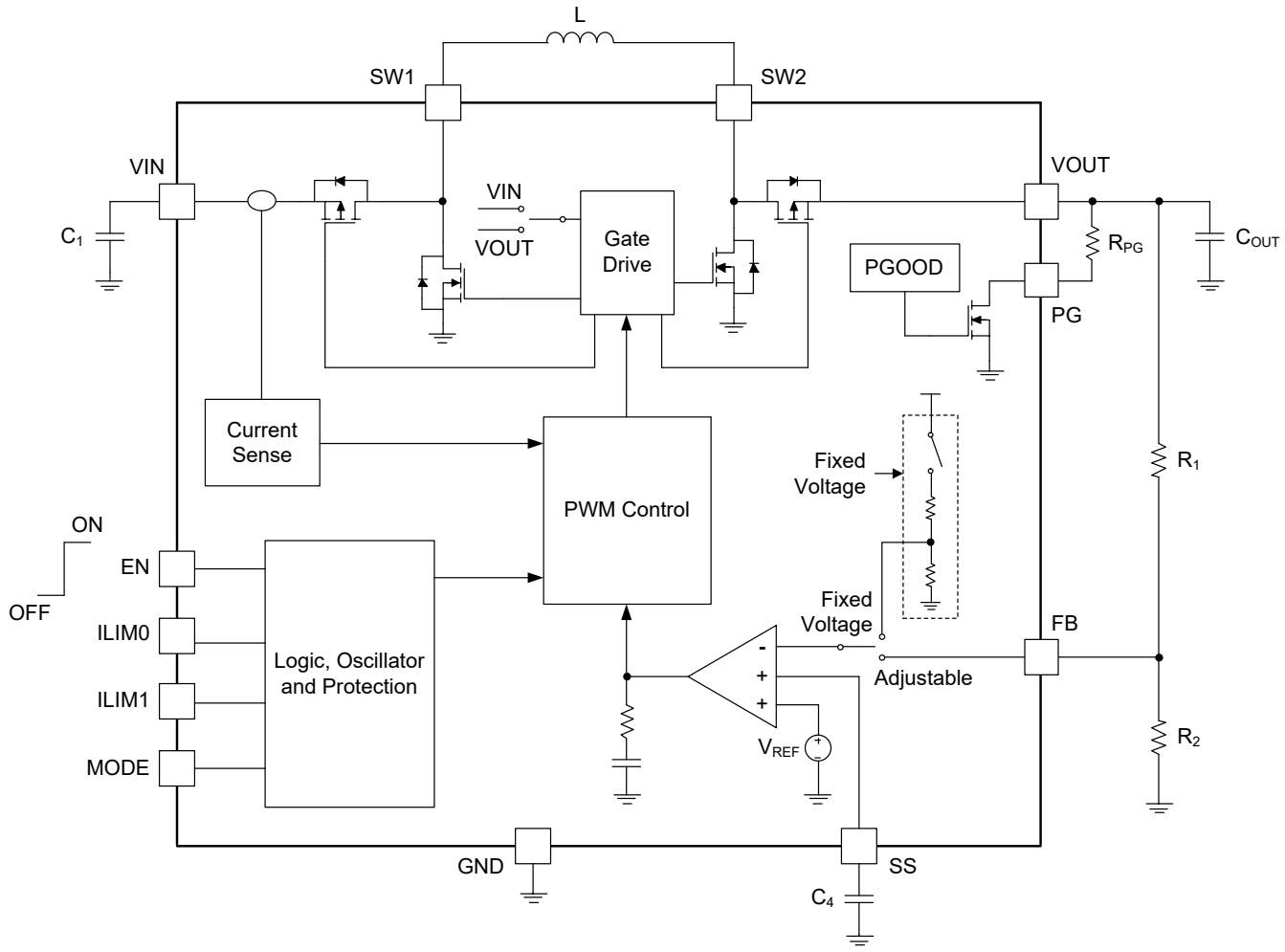


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM62115 is a fully integrated synchronous Buck-Boost converter that delivers high efficiency across the entire input and output voltage range. The device automatically transitions between Buck, Boost, and Buck-Boost modes based on input and output conditions. It operates in Buck mode when V_{IN} >> V_{OUT}, Boost mode when V_{IN} << V_{OUT}, and 4-switch Buck-Boost mode when V_{OUT} is approximately equal to V_{IN}. In Buck-Boost mode, the four switches are controlled to turn on and off alternately, reducing RMS current in the inductor and output capacitors. This minimizes output voltage ripple and maintains high efficiency across the entire input voltage range.

The SGM62115 features an external power-good pin. In addition, the device provides programmable input current limit adjustment via the ILIMx pins.

Feature Description

Power-Good

The PG pin of the device is an open-drain output, requiring an external pull-up resistor for proper operation. When the output voltage reaches above 95% of the programmed value, the PG pin is pulled high. If the output voltage falls below 90% of the programmed value, the PG pin is pulled low to indicate a power-not-good condition. The PG output must be pulled up to a voltage rail below 5.5V. The power-good signal remains valid while the device is enabled and the input voltage is above the UVLO threshold. Fault events including over-current and thermal shutdown will pull the PG signal low to GND.

Table 1 below lists the possible PG output logics. When the EN pin is pulled to logic low or either of the ILIMx pins is pulled to logic high, the PG pin output is low. When both pins are pulled to logic low, the output of PG pin is open-drain, and the PG pin follows the pull-up voltage.

Table 1. Power-Good Settings

EN	ILIM1	ILIM0	PG
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	Open-Drain

Over-Voltage Protection

The SGM62115 integrates output over-voltage protection (OVP). If the output voltage exceeds the OVP threshold of 6V (TYP) during operation, switching is terminated to protect the device from damage.

Device Enable

The EN pin is used to enable or disable the device. A logic high signal enables the device, while a logic low signal disables it.

Under-Voltage Lockout (UVLO)

The device incorporates under-voltage lockout (UVLO) protection to prevent malfunction under insufficient input voltage. The device only operates when the input voltage exceeds the UVLO rising threshold of 1.9V (TYP), and shuts down if the input voltage drops below the UVLO falling threshold of 1.8V (TYP).

Thermal Shutdown

The device incorporates thermal protection to prevent damage from overheating. When the junction temperature exceeds the thermal shutdown threshold of +140℃, the device shuts down. It automatically resumes operation once the junction temperature falls below the recovery threshold of +120℃.

Soft-Start

The SGM62115 integrates a soft-start function to minimize the inrush current during startup. The SGM62115-3.3 sources a 1μA (TYP) current and the SGM62115-ADJ sources a 3μA (TYP) current to a capacitor connected on the SS pin. When the voltage at the SS pin ramps up to 0.8V (TYP), it indicates the end of soft-start. The input current follows the current used to charge the SS capacitor. If the SS pin is left floating, the soft-start time is internally fixed. Refer to Switching Characteristics for details.

After the EN pin is pulled high, the soft-start current begins sourcing and the device initiates switching following a typical delay of 192μs. Soft-start time varies with load current and output capacitance; larger output capacitors and higher load currents result in longer startup durations.

Short-Circuit Protection

The SGM62115 provides short-circuit protection to improve the device robustness. If the output voltage is pulled below 1V (TYP), the device will be in a fault event.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Control Loop Description

The SGM62115 employs the peak current mode control architecture. The peak current of the Buck high-side MOSFET is sensed to provide current information for the control loop. This sensed current is compared with the output of the voltage loop, which consists of the FB network and internal reference voltage. The voltage generates an error signal between the FB voltage and the reference voltage, which ultimately sets the appropriate inductor current level to maintain tight output voltage regulation.

Figure 3 is a simplified drawing of the internal control loop, which consists of an error amplifier, a type-2 compensation network of the voltage loop and a PFM control block.

Pulse Frequency Modulation (PFM)

With the MODE pin pulled low, the SGM62115 operates in continuous current mode (CCM) with a fixed switching frequency under medium-to-heavy load conditions. To improve light-load efficiency, the device automatically switches to pulse frequency modulation (PFM) mode. In PFM mode, burst switching pulses are generated to regulate the output voltage, followed by idle off periods, as shown in Figure 4.

The burst sequence is triggered when the error amplifier output exceeds the PFM threshold voltage. The device dynamically adjusts the burst-mode switching frequency according to the load to ensure high output voltage regulation accuracy.

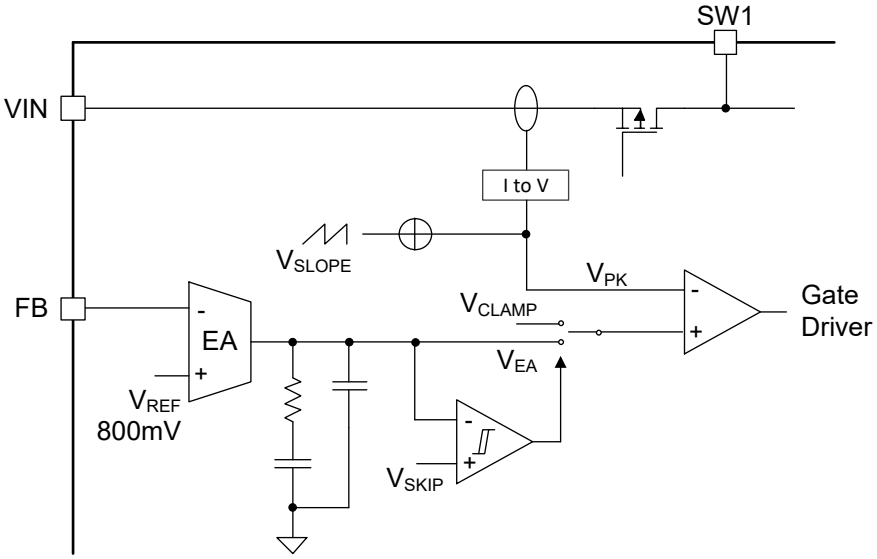


Figure 3. Control Loop Architecture Scheme

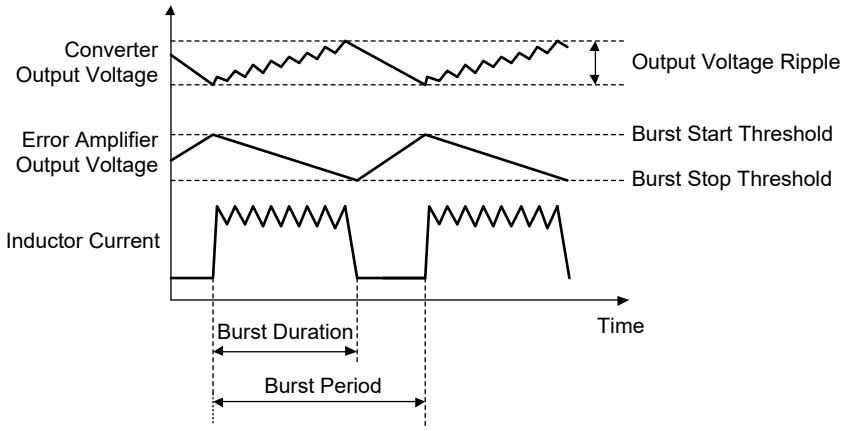


Figure 4. PFM Mode

DETAILED DESCRIPTION (continued)

In PFM mode, switching loss is reduced due to fewer switching cycles. Some internal blocks are disabled to further improve the light-load efficiency. However, output voltage ripple, DC output voltage accuracy, and load transient performance are degraded in PFM mode (see Table 2).

Table 2. Comparison of the FPWM and PFM Performances

Parameter	Best Operating Mode
Light Load Efficiency	PFM
DC Output Voltage Accuracy	FPWM
Transient Response	FPWM
Output Voltage Ripple	FPWM

Forced PWM Operation (FPWM)

Force PWM mode is enabled by setting the MODE pin high. In FPWM mode, the synchronous switches remain enabled under light load conditions even when the inductor current goes negative, maintaining a constant switching frequency. Compared with PFM operation, FPWM provides lower output voltage ripple and superior load transient response. However, at light output currents, FPWM exhibits higher switching and conduction losses, resulting in lower efficiency.

Adjustable Current Limit

The SGM62115 features programmable input current limit during startup to minimize inrush current. At startup, the input current is clamped according to the current limit setting programmed by the ILIM0 and ILIM1 combination (see Table 3). If a longer startup time is desired, adjust the capacitor connected to the SS pin.

Table 3. Adjustable Current Limit

ILIM1	ILIM0	Current-Limit Set (WLCSP)	Current-Limit Set (TQFN)
Low	Low	$0.44 \times I_{IN_MAX}$	Not Available
Low	High	$0.52 \times I_{IN_MAX}$	Not Available
High	Low	$0.68 \times I_{IN_MAX}$	$0.68 \times I_{IN_MAX}$
High	High	I_{IN_MAX}	I_{IN_MAX}

The ILIM0 and ILIM1 pins configuration can be dynamically adjusted during operation.

Based on the ILIM0 and ILIM1 setting and maximum average input current curve, the output current capability of Boost mode can be calculated using Equation 1 and 2, while Buck mode can be calculated using Equation 3 and 4.

$$\text{Duty Cycle Boost } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

$$\text{Output Current Boost } I_{OUT} = \eta \times I_{IN} (1 - D) \quad (2)$$

where:

- η = Estimated conversion efficiency.
- I_{IN} = Minimum average input current.

$$\text{Duty Cycle Buck } D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

$$\text{Output Current Buck } I_{OUT} = (\eta \times I_{IN})/D \quad (4)$$

where:

- η = Estimated conversion efficiency.
- I_{IN} = Minimum average input current.

APPLICATION INFORMATION

The SGM62115 is a high efficiency, Buck-Boost converter with low quiescent current designed for applications where the input voltage can be either higher or lower than the output voltage. It delivers a continuous output current of up to 500mA in Boost mode and up to 1A in Buck mode.

Table 4 lists the external components selection to ensure the proper operation of the SGM62115 within the recommended operating conditions. Table 5 lists the possible combinations of different inductor and output capacitor.

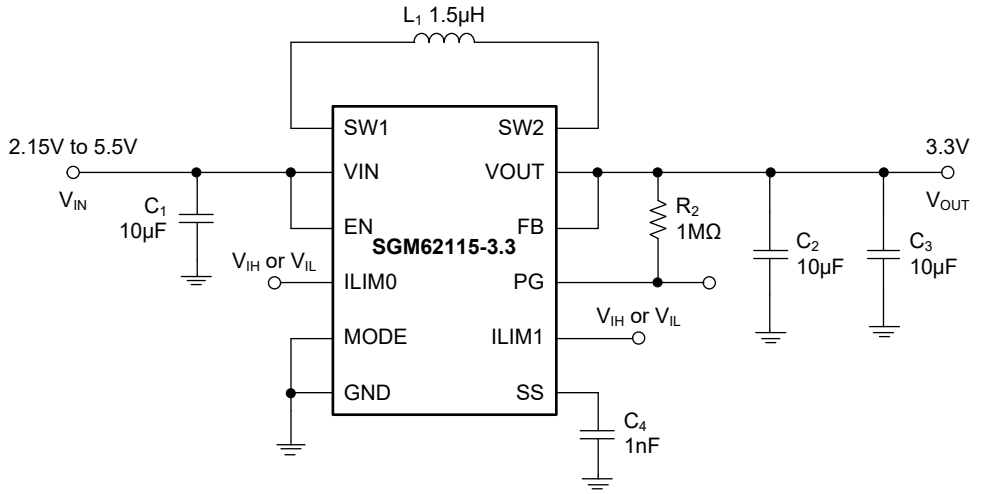


Figure 5. Parameter Measurement Circuit for SGM62115-3.3

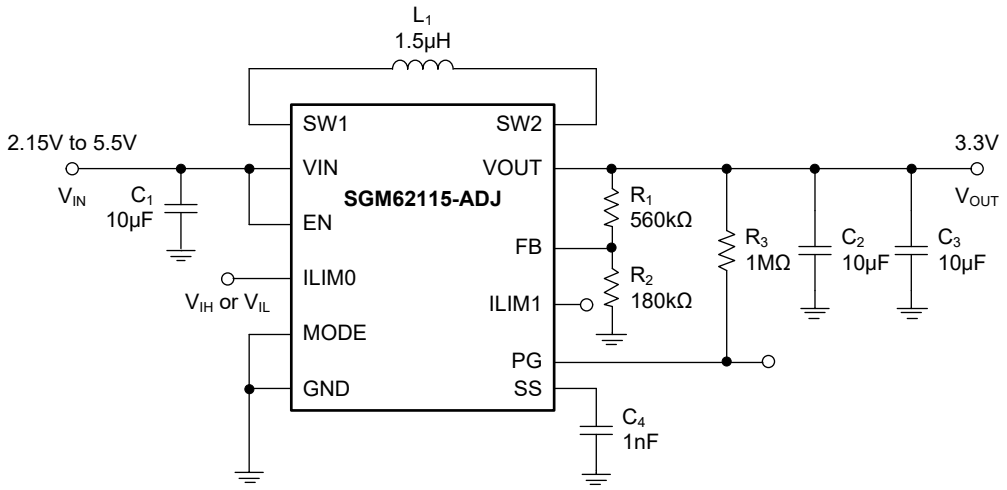


Figure 6. Parameter Measurement Circuit for SGM62115-ADJ

Table 4. Components for Application Characteristic Curves

Reference	Description	Manufacturer
L_1	1.5μH, 2.7A, 57mΩ	HEI252012A-1R5M-Q8, Chilisin
C_1, C_2, C_3	10μF, 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C_4	C_{SS}	
R_1	Depending on the output voltage of SGM62115, 0Ω with SGM62115-3.3	
R_2	Depending on the output voltage of SGM62115, not used with SGM62115-3.3	
R_3	1MΩ	

APPLICATION INFORMATION (continued)

Output Filter Design

Table 5. Matrix of Output Capacitor and Inductor Combinations

Nominal Inductor Value	Nominal Output Capacitor Value				
	10μF	20μF	44μF	66μF	100μF
1μH			+	+	+
1.5μH	+	+	+	+	+
2.2μH			+	+	+

Inductor Selection

A 1.5μH inductor is recommended for the SGM62115. Inductors with low DCR are preferred for improved efficiency. The saturation current rating (I_{SAT}) of the inductor must be at least 20% higher than the maximum peak current under worst-case conditions, including load transients. Such worst-case conditions typically occur in Boost mode at the lowest input voltage, highest output voltage, and maximum load. Use Equation 5 to calculate the maximum duty cycle in Boost mode, which corresponds to the peak inductor current.

$$D_{MAX} = \frac{V_{OUT_MAX} - V_{IN_MIN}}{V_{OUT_MAX}} \quad (5)$$

where:

- D_{MAX} is the maximum duty cycle in Boost mode.
- V_{IN_MIN} is the minimum input voltage.
- V_{OUT_MAX} is the maximum output voltage.

In this application:

$$D_{MAX} = \frac{3.3V - 2.5V}{3.3V} \times 100\% = 24\%$$

The maximum inductor current can be calculated by:

$$I_{LM} = \frac{I_{OUT_MAX}}{\eta(1 - D_{MAX})} + \frac{D_{MAX} \times V_{IN_MIN}}{2 \times f_{SW} \times L} \quad (6)$$

where:

- I_{LM} is the peak inductor current.
- I_{OUT_MAX} is the maximum output current.
- η is the converter efficiency (use application curves or choose 90%).
- f_{SW} is the switching frequency (2.5MHz).
- L is the inductance (1.5μH).

$$I_{LM} = \frac{0.5A}{0.9 \times (1 - 0.24)} + \frac{0.24 \times 2.5V}{2 \times 2.5MHz \times 1.5\mu H} = 0.81A$$

Choose the I_{SAT} value at least 20% higher than the calculated I_{LM} value. In this example, $I_{LM} \approx 0.81A$, $I_{OCP} \approx 2A$ and the selected inductor saturation current is 2.4A.

Table 6. List of Recommended Inductors

Inductor Value	Component Supplier	Size (mm^3) (L × W × H)	I_{SAT}/DCR
1μH	1286AS-H-1R0M, TOKO	2 × 1.6 × 1.2	2.1A/68mΩ
1.5μH	1286AS-H-1R5M, TOKO	2 × 1.6 × 1.2	2.5A/95mΩ
1.5μH	HEI252012A-1R5M-Q8, Chilisin	2.5 × 2 × 1	2.7A/57mΩ
1.5μH	74438324015, WE	2.5 × 2 × 1.2	4.7A/99mΩ
2.2μH	1286AS-H-2R2M, TOKO	2 × 1.6 × 1.2	2A/160mΩ

Capacitor Selection

Input Capacitor

To improve the line transient response of the regulator and EMI performance of the overall power system, it is recommended to use at least a 10μF/6.3V input capacitor. An X5R or X7R ceramic capacitor is recommended, placed as close as possible to the VIN and GND pins of the IC. If the power source is located far from the device, additional Bulk capacitance (e.g., a 47μF electrolytic or tantalum capacitor) is suggested for improved stability.

Output Capacitor

It is recommended to use two 10μF/6.3V ceramic capacitors. To reduce high-frequency noise, a 100nF ceramic capacitor in 0201 or 0402 package should be placed as close as possible to the VOUT and GND pins, in parallel with the other output capacitors.

The SGM62115 imposes no upper limit on the output capacitance. However, excessive output capacitance may lead to slower transient response and other issues during output discharge.

Setting the Output Voltage

The output voltage of the ADJ version is programmable via an external resistor divider connected to the FB pin. To minimize the effect of FB pin leakage current, the current through the resistor divider should be at least 100 times the FB input current. With a typical FB leakage current of 0.01μA and a typical internal reference voltage of 0.8V, the lower feedback resistor R_2 is chosen as 180kΩ for a 3.3V output. The upper feedback resistor R_1 can be calculated using Equation 7. A 560kΩ resistor is used to set the output voltage to 3.3V.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (7)$$

LAYOUT

Layout plays a significant role for all switch modes in DC/DC power supplies. Improper layout could result in poor EMI performance, device instability, and potential device damage.

1. The input capacitor, output capacitor and the inductor should be placed as close as possible to the IC.
2. The SGM62115 implements a power ground and control ground pins to minimize the ground noise effect on sensitive analog circuits. Connect the analog ground trace to the main power ground at a single point.
3. The trace routed to the FB pin is a sensitive signal path. Maintain adequate separation between these traces and the SW1/SW2 switching nodes.
4. The lower feedback resistor of the FB divider should be connected to the IC GND via the shortest trace.

Layout Example

Figure 7 is an example of TQFN package layout which is also the PCB layout used to collect the data and curve in the Typical Performance Characteristics section.

Figure 8 is an example of WLCSP package layout which is also the PCB layout used to collect the data and curve in the Typical Performance Characteristics section.

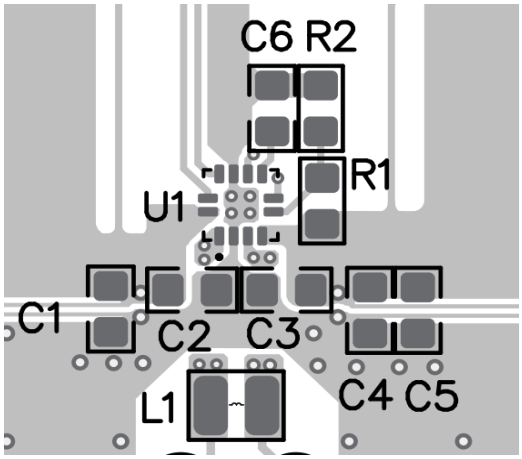


Figure 7. SGM62115 Layout (TQFN Package)

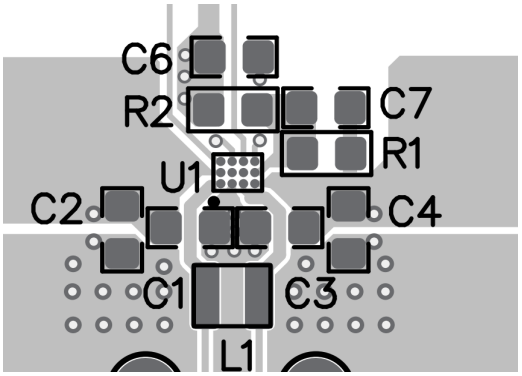


Figure 8. SGM62115 Layout (WLCSP Package)

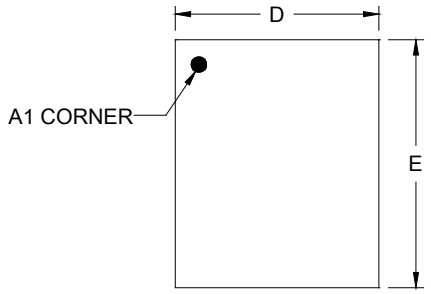
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

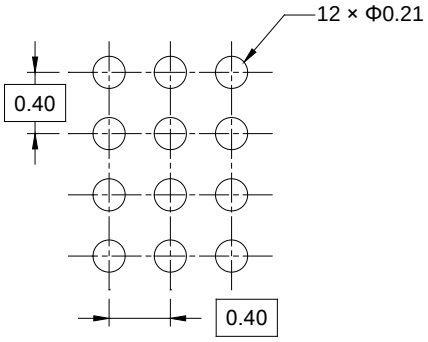
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

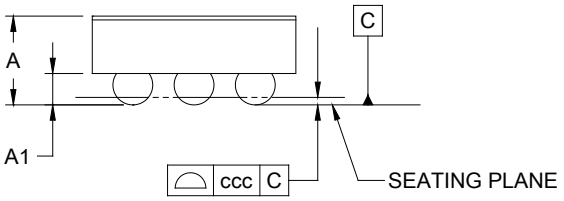
WLCSP-1.33×1.62-12B



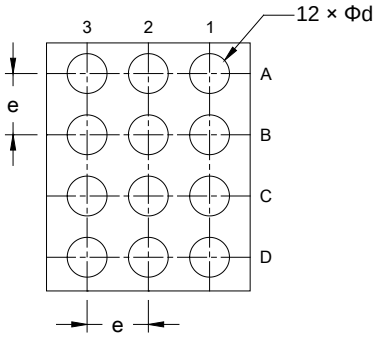
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



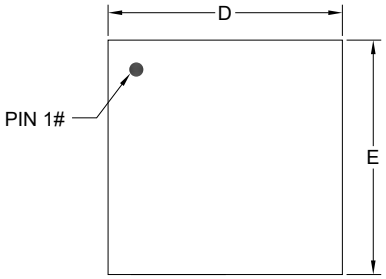
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.625
A1	0.185	-	0.225
D	1.300	-	1.360
E	1.590	-	1.650
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

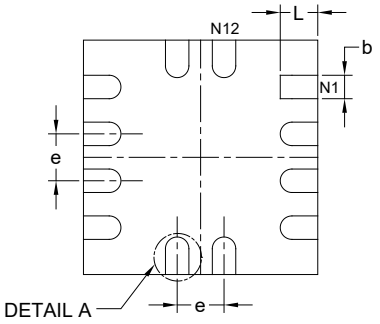
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

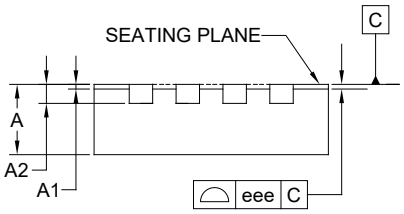
TQFN-2.5×2.5-12L



TOP VIEW



BOTTOM VIEW

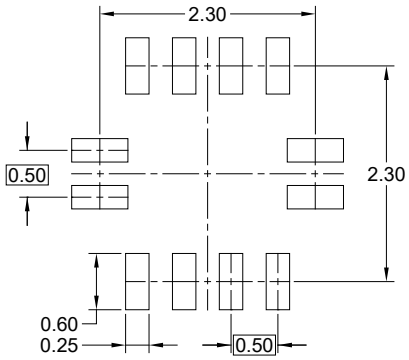


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



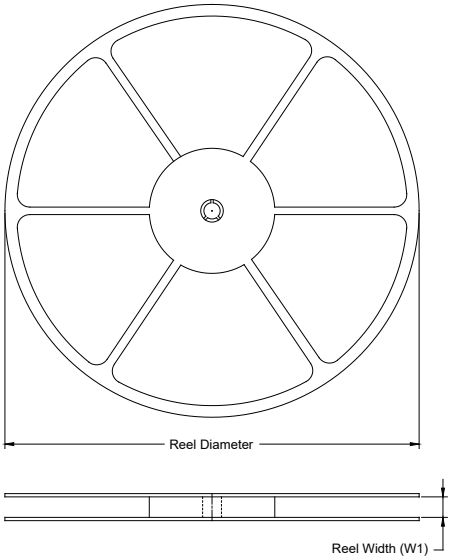
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.100
A2	0.203 REF		
b	0.200	-	0.300
D	2.400	-	2.600
E	2.400	-	2.600
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

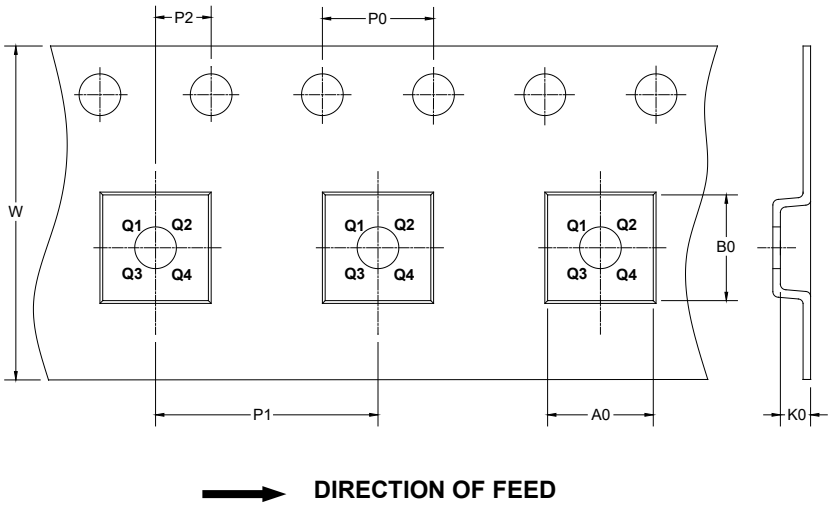
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



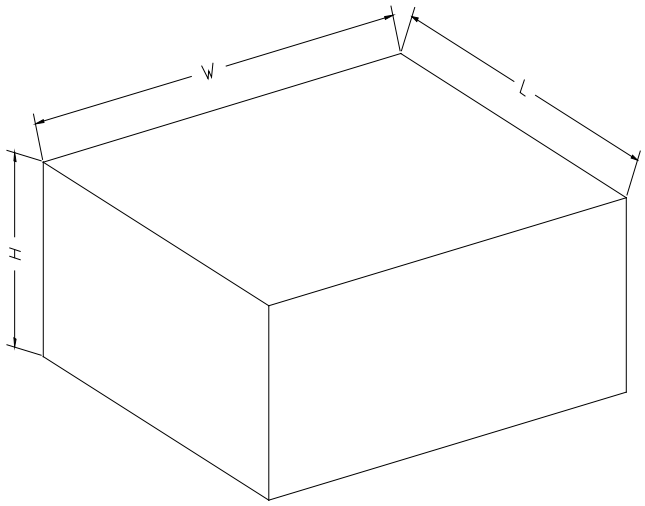
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.33×1.62-12B	7"	9.5	1.42	1.80	0.69	4.0	4.0	2.0	8.0	Q1
TQFN-2.5×2.5-12L	7"	9.5	2.70	2.70	0.90	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002