SGM861xQ
High Accuracy OV/UV Detection Reset IC with Time Delay and Manual Reset for Automotive Applications

GENERAL DESCRIPTION

The SGM861xQ is a high precision voltage supervisor with over-voltage (OV) and under-voltage (UV) monitor in a small package. It is very suitable for low-voltage systems that need extremely small tolerance. To prevent error events when the monitored signal is within the normal range, this device integrates very small threshold hysteresis, as well as built-in deglitch capability and noise immunity.

The SGM861xQ provides UV and OV threshold monitor function internally so that external resistor divider is not needed any more. As a result, overall cost and peripheral circuit size are reduced, and system reliability can be enhanced. Two factory-set reset delay time can be selected when CT pin is floating or pulled up to VDD through a resistor. The reset delay time can also be adjusted by placing a capacitor between CT pin and GND. The VDD pin and the SENSE pin are separated to provide redundancy for high reliability. The SGM861xQ has low quiescent current of 1.24μA (TYP). This device is recommended to be used in industrial automation and process control, or conditions that monitor voltages for UV and OV threshold with very high precision.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM861xQ is available in a Green TDFN-1.5×1.5-6L package. It operates over the junction temperature range of -40℃ to +125℃.

TYPICAL APPLICATION

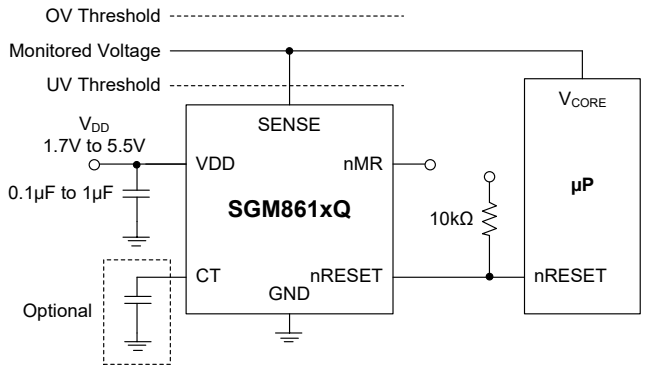


Figure 1. Typical Application Circuit

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  - **Device Temperature Grade 1**
  - **T_A = -40℃ to +125℃**
- **Input Voltage Range: 1.7V to 5.5V**
- **Under-Voltage Lockout (UVLO): 1.7V**
- **Low Quiescent Current: 1.24μA (TYP)**
- **High Threshold Accuracy:**
  - **±1% (TYP) at +25℃**
  - **±2% (MAX) at -40℃ to +125℃**
- **Fixed Window Threshold Levels**
  - **0.5V to 5V**
  - **4 Available Window Tolerance: ±4%, ±5%, ±6% and ±7%**
- **Programmable Voltage Threshold Levels**
- **Deglitch Capability and Hysteresis**
- **Factory-Set Reset Delay: 50μs, 1ms, 5ms, 10ms, 20ms, 100ms, 200ms**
- **Adjustable Reset Delay with Different CT Capacitor**
- **Active-Low Open-Drain Output**
- **nRESET Voltage Latch Function**
- **Available in a Green TDFN-1.5×1.5-6L Package**

APPLICATIONS

Advanced Driver Assistance System (ADAS)
ADAS Domain Controller
Automotive Infotainment and Cluster
Digital Cockpit
HEV/EV

PACKAGE/ORDERING INFORMATION

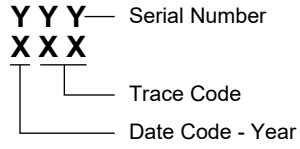
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM861A4-0.85Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A4-0.85QTHR6G/TR	39I XXX	Tape and Reel, 3000
SGM861A4-1.25Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A4-1.25QTHR6G/TR	39J XXX	Tape and Reel, 3000
SGM861A4-3.30Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A4-3.30QTHR6G/TR	40C XXX	Tape and Reel, 3000
SGM861A5-0.85Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A5-0.85QTHR6G/TR	33K XXX	Tape and Reel, 3000
SGM861A7-0.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-0.50QTHR6G/TR	33L XXX	Tape and Reel, 3000
SGM861A7-0.90Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-0.90QTHR6G/TR	33M XXX	Tape and Reel, 3000
SGM861A7-1.15Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-1.15QTHR6G/TR	40B XXX	Tape and Reel, 3000
SGM861A7-1.20Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-1.20QTHR6G/TR	33N XXX	Tape and Reel, 3000
SGM861A7-1.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-1.50QTHR6G/TR	33O XXX	Tape and Reel, 3000
SGM861A7-1.80Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-1.80QTHR6G/TR	33P XXX	Tape and Reel, 3000
SGM861A7-3.30Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-3.30QTHR6G/TR	2J9 XXX	Tape and Reel, 3000
SGM861A7-5.00Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861A7-5.00QTHR6G/TR	2JA XXX	Tape and Reel, 3000
SGM861B7-0.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-0.50QTHR6G/TR	2JB XXX	Tape and Reel, 3000
SGM861B7-0.90Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-0.90QTHR6G/TR	33Q XXX	Tape and Reel, 3000
SGM861B7-1.20Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-1.20QTHR6G/TR	33R XXX	Tape and Reel, 3000
SGM861B7-1.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-1.50QTHR6G/TR	33S XXX	Tape and Reel, 3000
SGM861B7-1.80Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-1.80QTHR6G/TR	33T XXX	Tape and Reel, 3000
SGM861B7-3.30Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-3.30QTHR6G/TR	33U XXX	Tape and Reel, 3000
SGM861B7-5.00Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861B7-5.00QTHR6G/TR	33V XXX	Tape and Reel, 3000
SGM861C4-5.00Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861C4-5.00QTHR6G/TR	3Z6 XXX	Tape and Reel, 3000
SGM861D7-0.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-0.50QTHR6G/TR	33W XXX	Tape and Reel, 3000
SGM861D7-0.90Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-0.90QTHR6G/TR	33X XXX	Tape and Reel, 3000
SGM861D7-1.20Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-1.20QTHR6G/TR	33Y XXX	Tape and Reel, 3000
SGM861D7-1.50Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-1.50QTHR6G/TR	33Z XXX	Tape and Reel, 3000
SGM861D7-1.80Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-1.80QTHR6G/TR	340 XXX	Tape and Reel, 3000
SGM861D7-3.30Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-3.30QTHR6G/TR	341 XXX	Tape and Reel, 3000
SGM861D7-5.00Q	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM861D7-5.00QTHR6G/TR	342 XXX	Tape and Reel, 3000

NOTE: For more models not listed above, please contact your local SGMICRO sales representatives.

PACKAGE/ORDERING INFORMATION (continued)

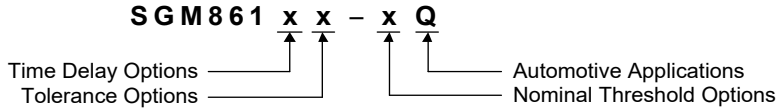
MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

Device Naming Description



Time Delay Options: Every part has two fixed time delay and adjustable delay option via external capacitor part number.		
Window (OV & UV)	A	CT pin open = 10ms, CT pin tied to VDD = 200ms, CT programmable with external capacitor
	B	CT pin open = 1ms, CT pin tied to VDD = 20ms, CT programmable with external capacitor
	C	CT pin open = 5ms, CT pin tied to VDD = 100ms, CT programmable with external capacitor
	D	CT pin open = 50μs, CT pin tied to VDD = 50μs, CT not programmable
Tolerance Options: Trigger or threshold voltage as a percentage of the monitored threshold voltage.		
4	Window threshold from nominal value = OV: +4%; UV: -4%	
5	Window threshold from nominal value = OV: +5%; UV: -5%	
6	Window threshold from nominal value = OV: +6%; UV: -6%	
7	Window threshold from nominal value = OV: +7%; UV: -7%	

Nominal Monitor Threshold Voltage Options							
0.50	0.50V	0.70	0.70V	0.90	0.90V	1.30	1.30V
0.55	0.55V	0.72	0.72V	0.95	0.95V	1.50	1.50V
0.60	0.60V	0.74	0.74V	1.00	1.00V	1.80	1.80V
0.62	0.62V	0.75	0.75V	1.05	1.05V	2.50	2.50V
0.64	0.64V	0.76	0.76V	1.10	1.10V	2.80	2.80V
0.65	0.65V	0.78	0.78V	1.15	1.15V	2.90	2.90V
0.66	0.66V	0.80	0.80V	1.20	1.20V	3.30	3.30V
0.68	0.68V	0.85	0.85V	1.25	1.25V	5.00	5.00V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 6V
nRESET, CT, SENSE, nMR Voltage ..... -0.3V to 6V
nRESET Current ..... ±40mA
Package Thermal Resistance
TDFN-1.5×1.5-6L, θ_{JA} ..... 164.4℃/W
TDFN-1.5×1.5-6L, θ_{JB} ..... 62.6℃/W
TDFN-1.5×1.5-6L, θ_{JC} ..... 134.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} ..... 1.7V to 5.5V
SENSE, nRESET Voltage ..... 0V to 5.5V
CT Voltage (1) ..... V_{DD}
nMR Voltage (2) ..... 0V to 5.5V
nRESET Current (3) ..... 0.3mA to 6mA
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:

1. It is recommended connecting a 10kΩ pull-up resistor between CT pin and VDD pin. The maximum value is V_{DD} or 5.5V, whichever is smaller.

2. If the voltage at nMR is smaller than V_{DD}, extra current will flow from the VDD pin to the nMR pin.

3. The minimum pull-down current of nRESET is greater than 6mA at T_A = +25℃.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

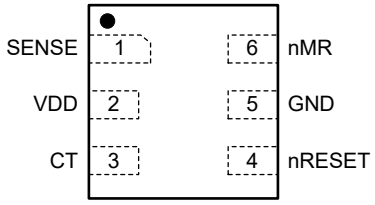
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-1.5×1.5-6L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SENSE	I	SENSE Voltage Input Pin. Short this pin with VDD pin if the VDD voltage is deserved to be monitored.
2	VDD	I	Supply Voltage Input Pin. Usually, a 0.1μF to 1μF ceramic capacitor is placed close to this pin.
3	CT	I	Capacitor Time Delay Pin. The CT pin provides two factory-set delay time options: one by connecting it to VDD, and another by keeping it floating. The reset delay time can also be adjusted by placing a capacitor between CT pin and GND except for SGM861Dx-xxQ.
4	nRESET	O	Active-Low Open-Drain Output Pin. It rises to logic high when the SENSE pin voltage falls into the range of the UV threshold (V_{IT-UV}) and OV threshold (V_{IT+OV}). Otherwise, it falls to logic low. Pull up this pin to the VDD pin or other voltage rail through a resistor.
5	GND	G	Ground.
6	nMR	I	Active-Low Manual Reset Pin. When the nMR pin turns high, the output holds low for the reset delay time (t_D) and then goes high. Leave this pin floating when not used.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.7V to 5.5V, CT, nMR = Open, V_{nRESET} = 10kΩ to VDD, C_{nRESET} = 10pF, T_A = -40℃ to +125℃, typical values are measured at T_A = +25℃ and V_{DD} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.7		5.5	V
Under-Voltage Lockout (1)	UVLO	V_{DD} falling below 1.7V	1.3	1.48	1.7	V
Power-On Reset Voltage (2)	V_{POR}	V_{OL_MAX} = 0.25V, I_{OUT} = 15μA		0.6	1	V
Positive-Going Threshold Accuracy	V_{IT+OV}		-2	±1	2	%
Negative-Going Threshold Accuracy	V_{IT-UV}		-2	±1	2	%
Hysteresis Voltage (3)	V_{HYS}		0.1	0.6	2	%
Supply Current	I_{DD}	V_{DD} ≤ 5.5V		1.24	4	μA
Input Current, SENSE Pin	I_{SENSE}	V_{SENSE} = 5V		0.64	1.5	μA
Low-Level Output Voltage	V_{OL}	V_{DD} = 1.7V, I_{OUT} = 0.4mA			0.25	V
		V_{DD} = 2V, I_{OUT} = 3mA			0.25	
		V_{DD} = 5V, I_{OUT} = 5mA			0.25	
Open-Drain Output Leakage Current	I_{LKG}	V_{DD} = V_{nRESET} = 5.5V			300	nA
nMR Logic Low Input	V_{nMR_L}				0.3	V
nMR Logic High Input	V_{nMR_H}		1.4			V
High Level CT Pin Voltage	V_{CT_H}		1.4			V
Manual Reset Internal Pull-up Resistance	R_{nMR}			102		kΩ
CT Pin Charge Current	I_{CT}		335	375	415	nA
CT Pin Comparator Threshold Voltage (4)	V_{CT}		1.13	1.15	1.17	V

NOTES:

1. If V_{DD} falls below UVLO, nRESET will be driven low (here, V_{IT-UV} < V_{SENSE} < V_{IT+OV}).
2. V_{POR} represents the minimum VDD voltage to ensure a controlled output condition.
3. Hysteresis is with respect to the corresponding UV/OV tripoint (V_{IT-UV}, V_{IT+OV}).
4. V_{CT} represents the comparator threshold for measuring the voltage level of the external capacitor at CT pin.

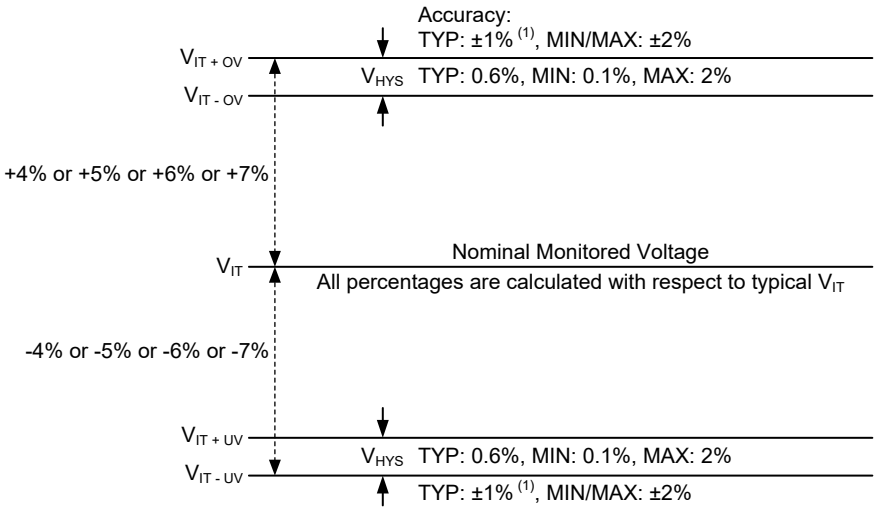
TIMING REQUIREMENTS

(V_{DD} = 1.7V to 5.5V, CT, nMR = Open, V_{nRESET} = 10kΩ to VDD, C_{nRESET} = 10pF, typical values are measured at T_A = +25℃ and V_{DD} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Time Delay, SGM861AxQ	t_D	CT = Open	7.5	10.8	14	ms
		CT = 10kΩ to VDD	150	216	280	
Reset Time Delay, SGM861BxQ	t_D	CT = Open	0.75	1.08	1.4	ms
		CT = 10kΩ to VDD	15	21.6	28	
Reset Time Delay, SGM861CxQ	t_D	CT = Open	3.75	5.4	7	ms
		CT = 10kΩ to VDD	75	108	140	
Reset Time Delay, SGM861DxQ	t_D	CT = Open, CT = 10kΩ to VDD, SENSE trigger		65		μs
		CT = Open, CT = 10kΩ to VDD, nMR trigger		45		
Propagation Detect Delay (1) (2)	t_{PD}			20	35	μs
Output Rise Time (1) (3)	t_R			2.2		μs
Output Fall Time (1) (3)	t_F			0.2		μs
Startup Delay (4)	t_{SD}			290		μs
Glitch Immunity Under-Voltage $V_{IT - UV}$, 5% Overdrive (1)	t_{GI_VIT-}			14		μs
Glitch Immunity Over-Voltage $V_{IT + OV}$, 5% Overdrive (1)	t_{GI_VIT+}			13		μs
Glitch Immunity nMR Pin	t_{GI_nMR}				25	ns
Propagation Delay from nMR Low to Assert nRESET	t_{PD_nMR}			270		ns
nMR Pin Pulse Width Duration to Assert nRESET	t_{nMR_W}		1			μs
nMR Reset Time Delay	t_{D_nMR}			t_D		ms

NOTES:
1. 5% Overdrive from threshold. Overdrive% = (V_{SENSE} - V_{IT})/V_{IT}; V_{IT} refers to either $V_{IT - UV}$ or $V_{IT + OV}$.
2. t_{PD} measures the time interval between the threhold trip point ($V_{IT - UV}$ or $V_{IT + OV}$) and the nRESET V_{OL} voltage.
3. Output transitions from V_{OL} to 90% for rise times and 90% to V_{OL} for fall times.
4. During the power-on period, V_{DD} must be equal to or higher than V_{DD_MIN} for at least t_{SD} + t_D before the output is in the correct state.

Timing Diagrams



NOTE: 1. Factory-Set Accuracy.

Figure 2. Voltage Threshold and Hysteresis Accuracy

TIMING REQUIREMENTS (continued)

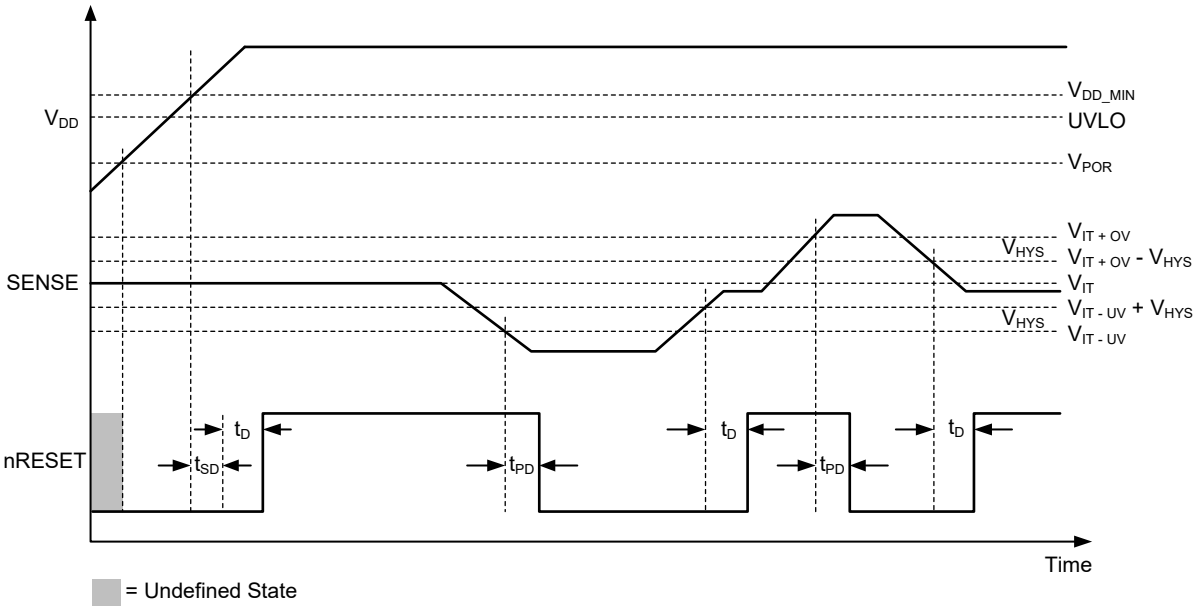
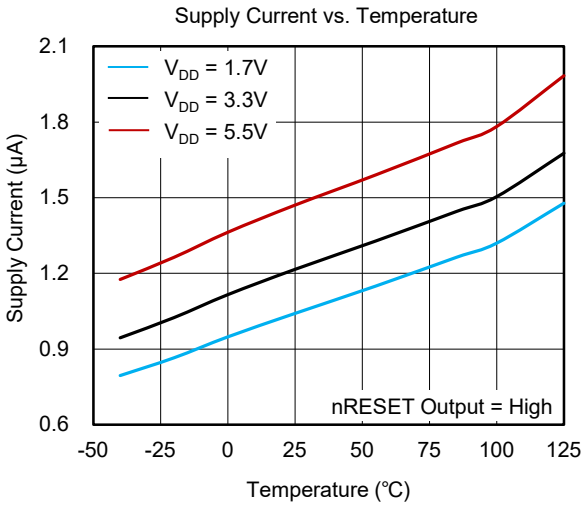
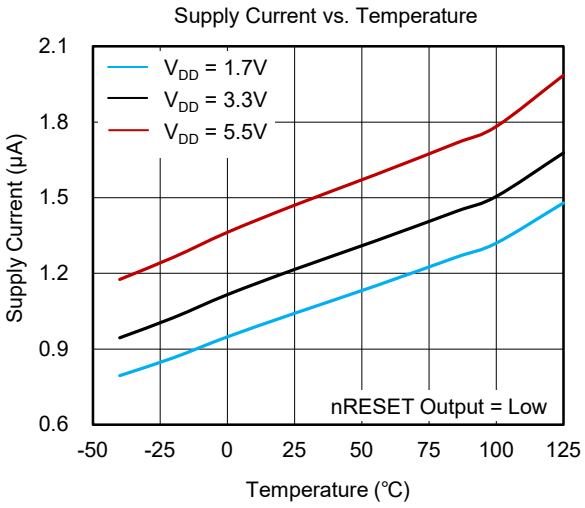


Figure 3. SENSE Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{DD} = 3.3V and R_{PU} = 10kΩ, unless otherwise noted.

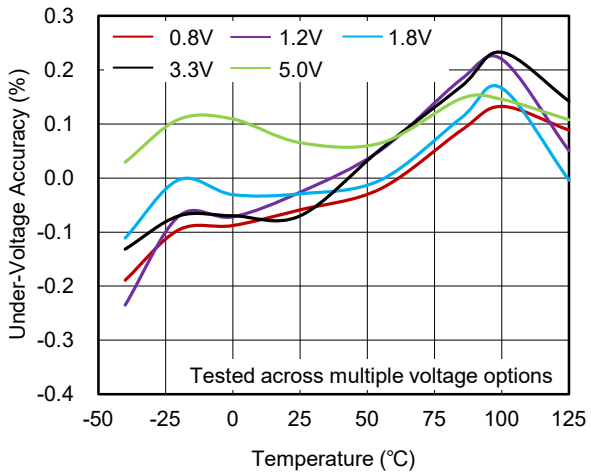




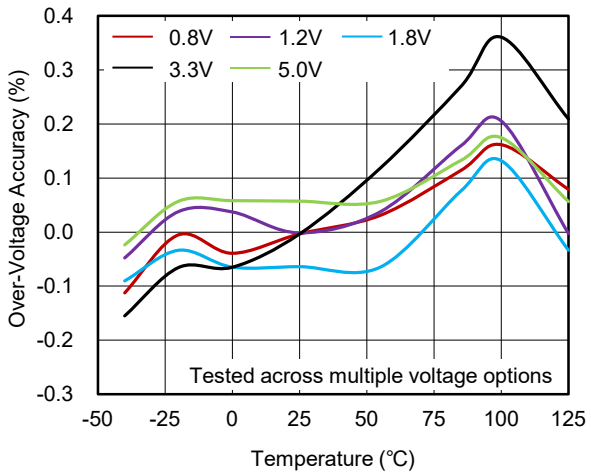
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V and R_{PU} = 10kΩ, unless otherwise noted.

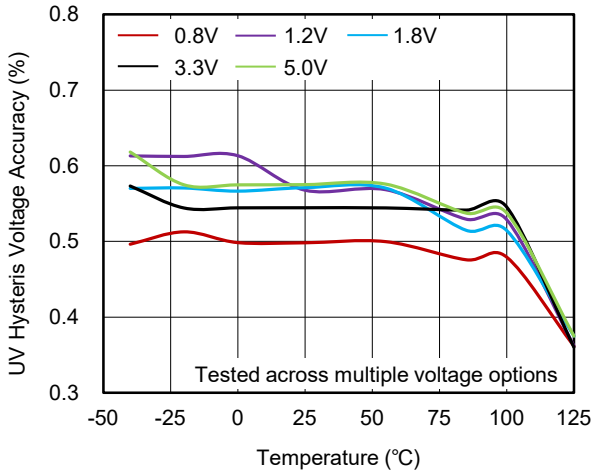
Under-Voltage Accuracy vs. Temperature



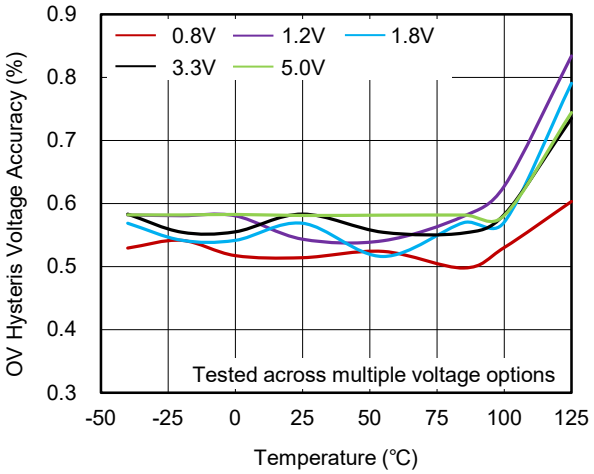
Over-Voltage Accuracy vs. Temperature



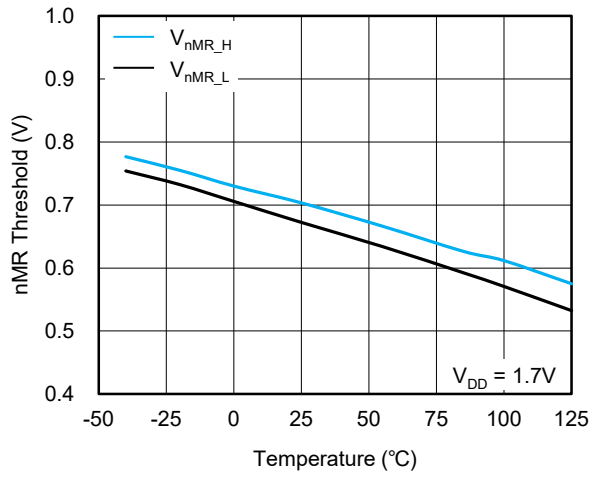
Under-Voltage Hysteresis Voltage Accuracy vs. Temperature



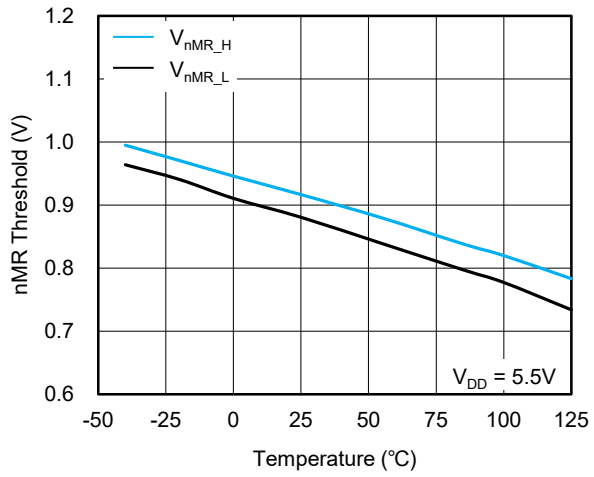
Over-Voltage Hysteresis Voltage Accuracy vs. Temperature



nMR Threshold vs. Temperature



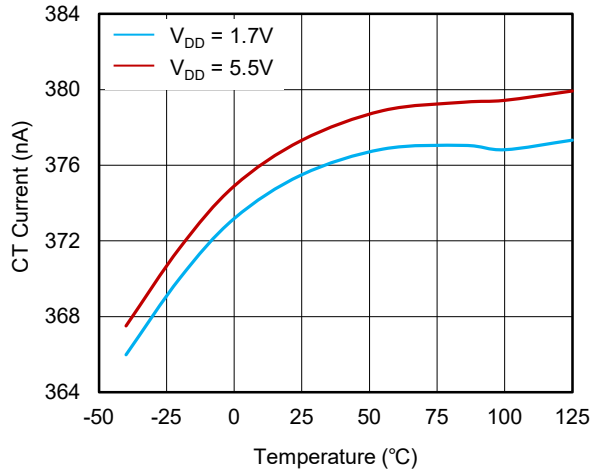
nMR Threshold vs. Temperature



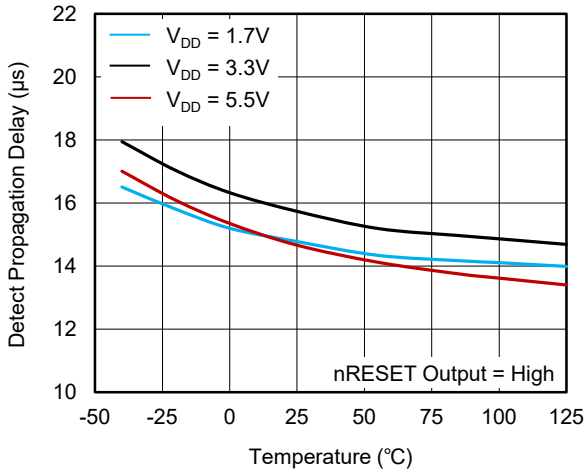
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V and R_{PU} = 10kΩ, unless otherwise noted.

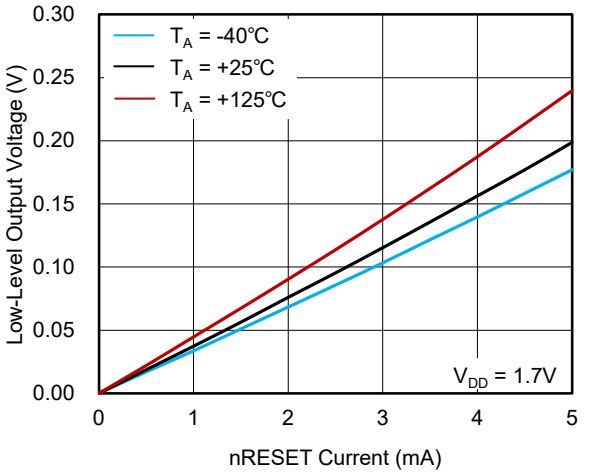
CT Current vs. Temperature



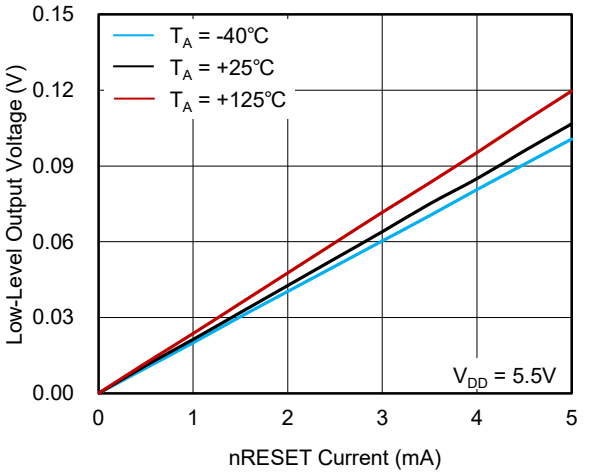
Detect Propagation Delay vs. Temperature



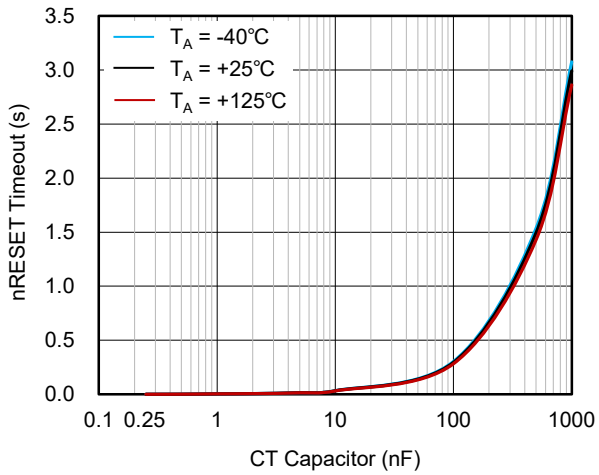
Low-Level Output Voltage vs. nRESET Current



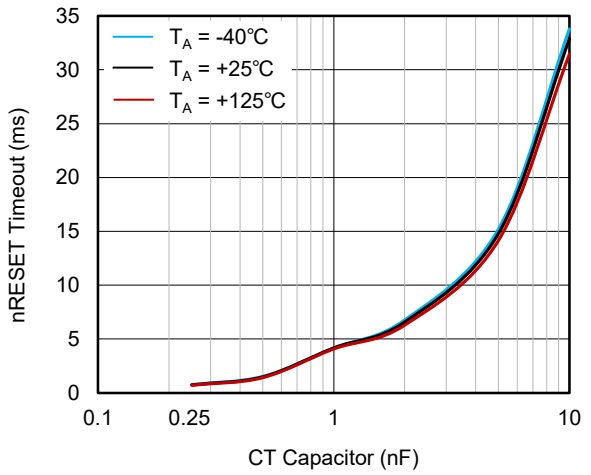
Low-Level Output Voltage vs. nRESET Current



nRESET Timeout vs. CT Capacitor (0.25nF to 1000nF)



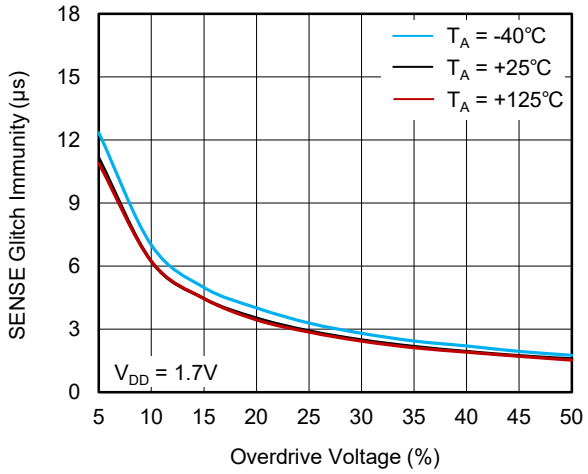
nRESET Timeout vs. CT Capacitor (0.25nF to 10nF)



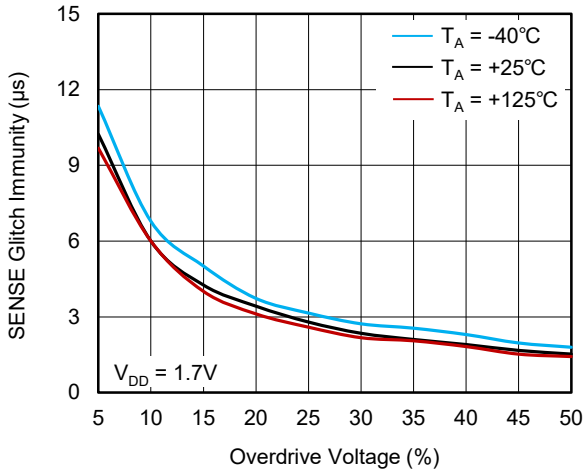
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V and R_{PU} = 10kΩ, unless otherwise noted.

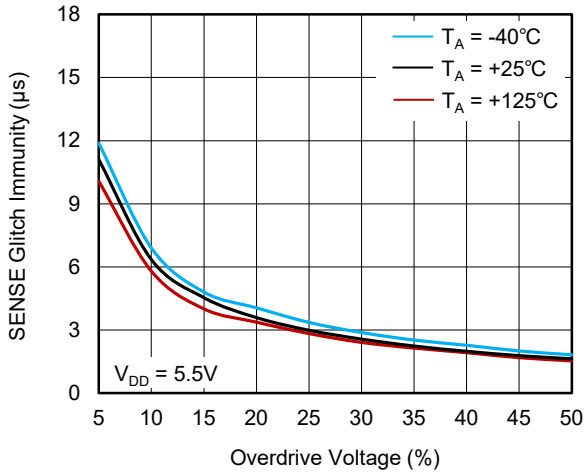
SENSE Glitch Immunity (V_{IT-}) vs. Overdrive



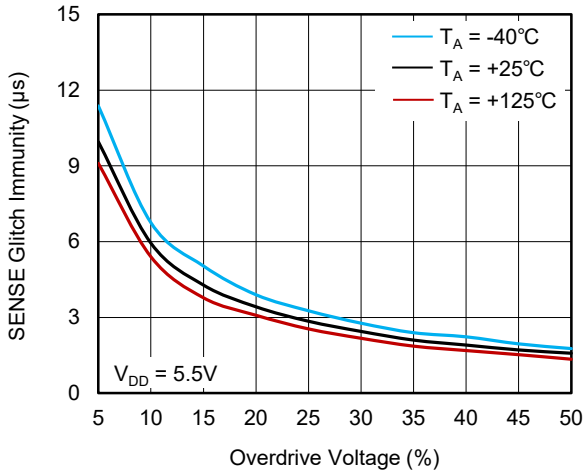
SENSE Glitch Immunity (V_{IT+}) vs. Overdrive



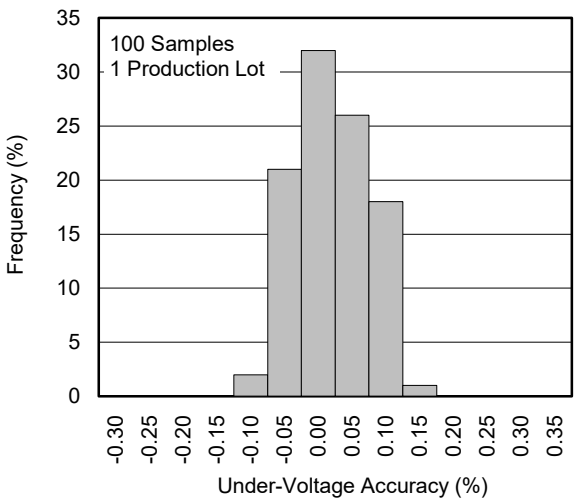
SENSE Glitch Immunity (V_{IT-}) vs. Overdrive



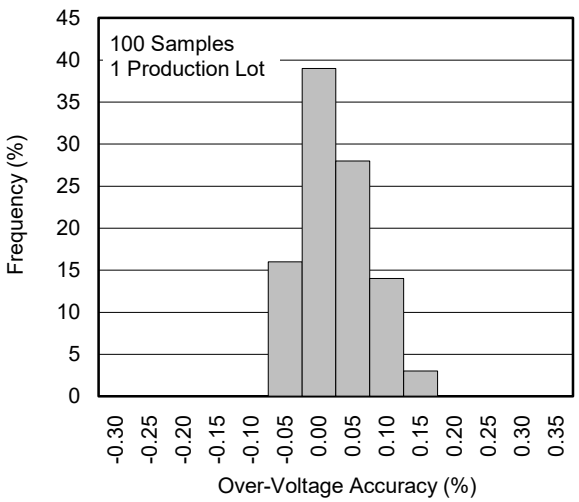
SENSE Glitch Immunity (V_{IT+}) vs. Overdrive



Under-Voltage Accuracy Distribution



Over-Voltage Accuracy Distribution



FUNCTIONAL BLOCK DIAGRAM

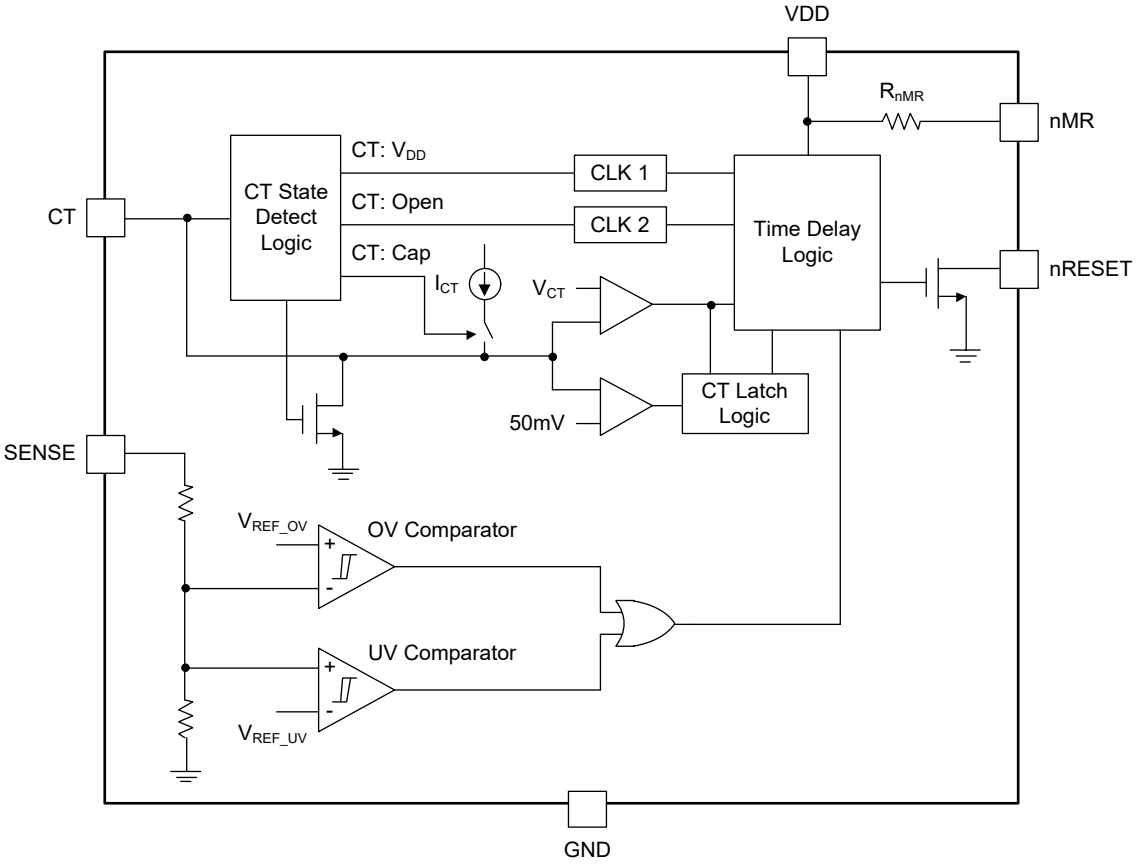


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM861xQ incorporates an over-voltage (OV) detector and an under-voltage (UV) detector, as well as a precise voltage reference. Besides, it has a series of sense thresholds with highly exact windowed threshold voltages, which varies ±2% (MAX) over -40℃ to +125℃.

The SGM861xQ has built-in resistors to precisely determine the OV/UV thresholds. As a result, external divider resistors are not needed so that the number of external components is reduced and the design process is simplified.

The SGM861Ax-xQ/SGM861Bx-xQ/SGM861Cx-xQ has three t_D options with CT pulled up to VDD, floating or connecting to GND with a capacitor. The SGM861Dx-xQ has two t_D options with CT pulled up to VDD or floating, where connecting to GND with a capacitor is not permitted.

Manual reset (nMR) is used to pull down the nRESET pin by pulling down the nMR pin itself for the aim of hardware reset. Leave this pin floating when not used.

The nRESET pin of SGM861xQ is used to indicate whether the monitored signal is located within the sense window. Once the monitored signal falls outside the sense window, the nRESET pin turns low soon. Details please refer to Table 1.

Feature Description

VDD

The SGM861xQ is recommended working under voltage ranging from 1.7V to 5.5V for the VDD pin. Placing an input capacitor is not strictly demanded but useful under a noisy environment. In such a noisy condition, a capacitor of 1μF is recommended to be placed between the VDD pin and GND.

In the power on process, the VDD voltage should be higher than its minimum voltage, and the delay time should be longer than the start-up delay (t_{SD} + t_D) so that the SGM861xQ can function normally.

SENSE

The SGM861xQ incorporates an OV detector and a UV detector, as well as a precise voltage reference. Besides, it has a built-in divider resistor network for the SENSE pin to reduce the overall component number and improve the detection accuracy as well. Both the OV detector and UV detector adopt precise hysteresis in order to give noise suppression and deglitch capability.

Similar to the VDD pin, a capacitor of 1nF to 10nF is recommended to be placed between the SENSE pin and GND once the SGM861xQ is placed in a noisy environment.

If the VDD pin voltage is to be monitored, connecting the SENSE pin and VDD pin together is advised.

nRESET

The SGM861xQ output pin nRESET is designed to be used as a reset input or an enable input for typical applications like a micro-processor (μP), a DC/DC converter or a low dropout linear regulator (LDO).

The nRESET pin is an open-drain output. There must be a pull-up resistor to pull up the nRESET voltage to the demanded level. The determination of this resistor should take low-level output voltage (V_{OL}), capacitance between the nRESET and GND, and leakage current into consideration. Note that open-drain pins can be wired-OR with other open-drain pins. Hence, the nRESET pin of SGM861xQ can be connected with other open-drain signals (e.g. nRESET pin of another SGM861xQ).

Figure 5 depicts the timing diagram for the SENSE pin input and nRESET pin output.

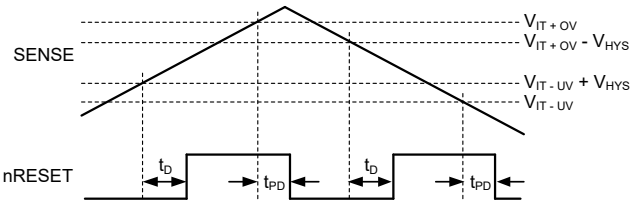


Figure 5. Timing Diagram of SENSE and nRESET

Capacitor Time (CT)

The CT pin gives user the option to adopt the preset reset delay by connecting CT to VDD or leave it floating. Users can also take the user-programmed reset delay by connecting CT to an external capacitor greater than 250pF; otherwise, it will be regarded as floating. Once the SENSE voltage falls into the valid window (V_{IT-UV} < V_{SENSE} < V_{IT+OV}), the CT pin state is detected in 450μs with the built-in state machine. When the CT pin is connected to VDD, a pull-up resistor of 10kΩ is advised.

DETAILED DESCRIPTION (continued)

Manual Reset (nMR)

The manual reset (nMR) is designed as an external input pin to manually pull down the nRESET pin. When nMR goes low, the nRESET pin asserts low after t_{PD_nMR}. Once the nMR pin turns high again in the precondition that the SENSE pin voltage is within the valid window ($V_{IT\ -\ UV}$ < V_{SENSE} < $V_{IT\ +\ OV}$), the nRESET pin keeps low for t_{D_nMR} and then turns high. The nMR pin can be pulled up to VDD directly or just left open when no external control signals exist. Note that the nMR pin is pulled up to VDD internally through R_{nMR}. Figure 6 shows the relation between nMR and nRESET.

Device Functional Modes

Table 1 below shows the functional mode truth table.

Normal Operation (V_{DD} > V_{DD_MIN})

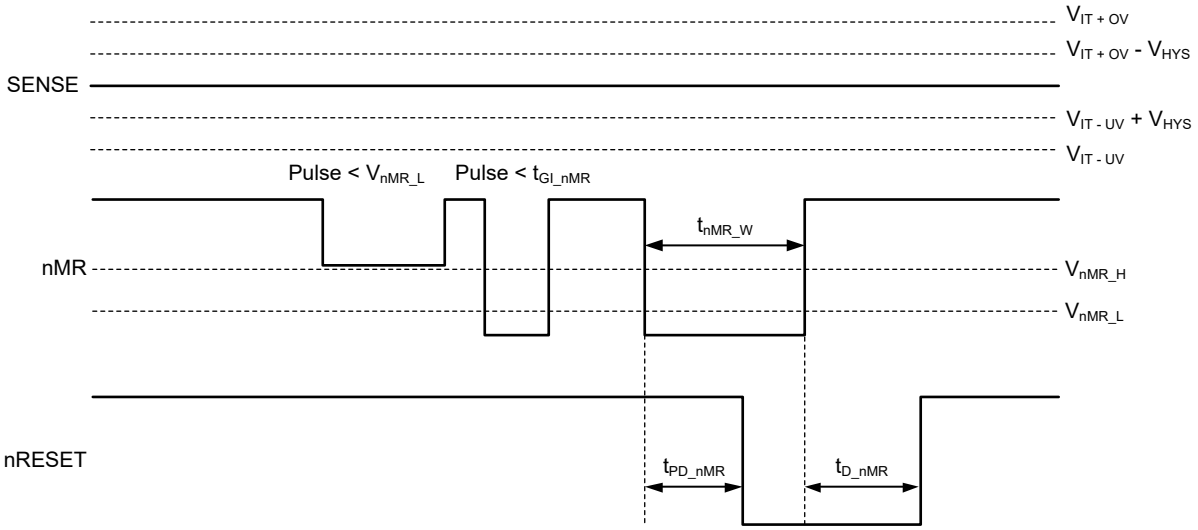
When V_{DD} > V_{DD_MIN} continues longer than (t_{SD} + t_D), the nRESET output state is determined by the SENSE pin voltage. When the SENSE pin voltage is within the valid window ($V_{IT\ -\ UV}$ < V_{SENSE} < $V_{IT\ +\ OV}$), nRESET turns high. When the SENSE pin voltage goes outside of the valid window (V_{SENSE} < $V_{IT\ -\ UV}$ or V_{SENSE} > $V_{IT\ +\ OV}$), nRESET turns low.

Under-Voltage Lockout (V_{POR} < V_{DD} < UVLO)

When V_{POR} < V_{DD} < UVLO, the nRESET pin maintains low no matter what the SENSE pin voltage is.

Power-On Reset (V_{DD} < V_{POR})

When V_{DD} < V_{POR}, nRESET signal is undefined and is not to be relied upon for proper device function.



NOTES:

1. Pull nRESET to VDD with a 10kΩ resistor.
2. In order to initiate and continue the time reset counter, V_{nMR} must be higher than V_{nMR_H} or floating and V_{SENSE} must be between $V_{IT\ -\ UV}$ + V_{HYS} and $V_{IT\ +\ OV}$ - V_{HYS}.
3. During nRESET outputs low, nMR is ignored.

Figure 6. Relation Between nMR and nRESET

Table 1. Functional Mode Truth Table

Description	Condition	nMR Pin	VDD Pin	Output (nRESET Pin)
Normal Operation	$V_{IT\ -\ UV}$ < SENSE < $V_{IT\ +\ OV}$	Open or Above V_{nMR_H}	V_{DD} > V_{DD_MIN}	High
Over-Voltage Detection	SENSE > $V_{IT\ +\ OV}$	Open or Above V_{nMR_H}	V_{DD} > V_{DD_MIN}	Low
Under-Voltage Detection	SENSE < $V_{IT\ -\ UV}$	Open or Above V_{nMR_H}	V_{DD} > V_{DD_MIN}	Low
Manual Reset	$V_{IT\ -\ UV}$ < SENSE < $V_{IT\ +\ OV}$	Below V_{nMR_L}	V_{DD} > V_{DD_MIN}	Low
UVLO Engaged	$V_{IT\ -\ UV}$ < SENSE < $V_{IT\ +\ OV}$	Open or Above V_{nMR_H}	V_{POR} < V_{DD} < UVLO	Low

APPLICATION INFORMATION

Voltage Threshold Accuracy

Voltage monitoring effect is determined by both the supply voltage margin and the reset detection accuracy. Because of the high precision of SGM861xQ (maximum deviation is 2%), supply voltage with larger deviation can be applied under tight tolerance applications.

For example, an MCU core voltage rail, which accepts error no more than ±8% of the nominal value, is supplied by a DC/DC converter. Here, judge that ±5% error is allowed for the DC/DC converter and ±2% error is allowed for the supervisor. As mentioned above, the SGM861xQ has high accuracy (error < ±2%) so that more voltage margin is given for the DC/DC converter to be selected or designed. As a result, smaller output capacitor or inductor can be adopted for more relaxed requirements of output voltage ripple and transient fluctuation. Moreover, lower system voltage and tighter tolerance is allowed for the MCU without SGM861xQ nRESET pin asserted for possible failure or malfunction.

Figure 7 illustrates the DC/DC converter output voltage deviation range and SGM861xQ voltage threshold accuracy is mentioned above.

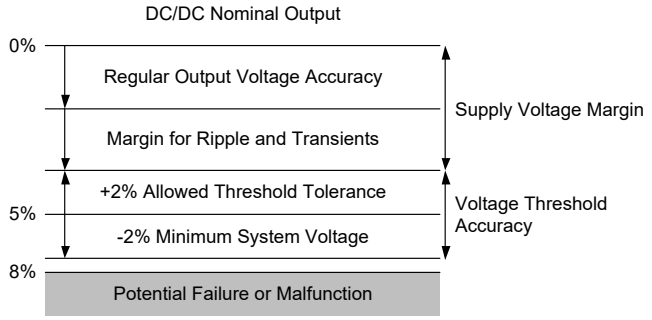


Figure 7. DC/DC Converter Output Voltage Deviation Range and SGM861xQ Voltage Threshold Accuracy

CT Reset Time Delay

The CT pin gives user three options to adopt the preset reset delay by connecting CT to VDD or leaving it floating, or taking the user-programmed reset delay by connecting CT to an external capacitor. The nRESET delay time (t_D) is determined by the CT configuration. Figure 8 shows the three configurations of CT. Once the SENSE voltage falls into the valid window (V_{IT-UV} < V_{SENSE} < V_{IT+OV}), the CT pin state is detected in 450μs with the built-in state machine.

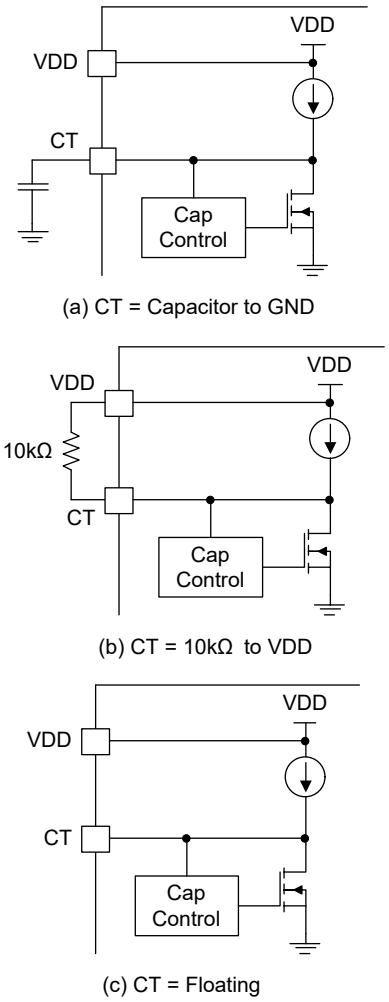


Figure 8. CT Configuration Diagram

Factory-Programmed Reset Delay Timing

The CT pin gives user the options to adopt the preset reset delay by connecting CT to VDD with a 10kΩ pull-up resistor or leave it floating. Table 2 describes the preset t_D options for SGM861xQ.

Table 2. Reset Delay Time for Factory-Programmed Reset Delay Timing

Model	Capacitor to GND	Floating	10kΩ to VDD
SGM861Ax-xQ	Programmable t_D	t_D = 10ms	t_D = 200ms
SGM861Bx-xQ	Programmable t_D	t_D = 1ms	t_D = 20ms
SGM861Cx-xQ	Programmable t_D	t_D = 5ms	t_D = 100ms
SGM861Dx-xQ	N/A	t_D = 50μs	t_D = 50μs

APPLICATION INFORMATION (continued)

Programmable Reset Delay-Timing

The CT pin gives user the option to adopt the user-programmed reset delay by connecting CT to an external capacitor (C_{CT}) between the CT pin and GND. The reset delay time t_D is decided by three factors: CT charging current I_{CT}, CT voltage threshold V_{CT}, and C_{CT}. Note that only C_{CT} > 250pF can be identified as a capacitor for t_D. In order to charge the CT capacitor, one must guarantee that the initial CT pin voltage is near zero. If so, there is no upper limit of t_D for the SGM861xQ. The relationship between t_D and C_{CT} is described in Equation 1.

$$t_D\,(ms) = 3.060 \times C_{CT}\,(nF) + 0.57ms \quad (1)$$

The CT pin voltage rising slope (coefficient of C_{CT} in Equation 1) is equal to the value of V_{CT} divided by I_{CT}. Considering the deviation of V_{CT} and I_{CT}, one can calculate the minimum and maximum of t_D, which is listed in Equation 2 and Equation 3, respectively.

$$t_{D_MIN}\,(ms) = 2.7397 \times C_{CT}\,(nF) + 0.30ms \quad (2)$$

$$t_{D_MAX}\,(ms) = 3.5088 \times C_{CT}\,(nF) + 0.79ms \quad (3)$$

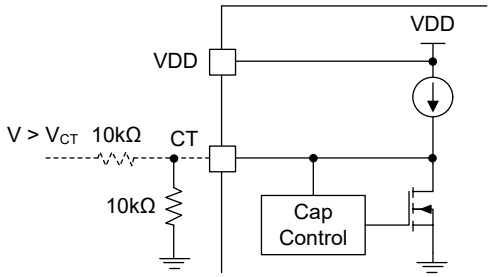
When the VDD voltage and SENSE voltage are both higher than their rising threshold (nMR is assumed to be floating), the SGM861xQ begins to charge C_{CT} until V_{CT} = 1.15V. Once V_{CT} = 1.15V, C_{CT} is discharged by the internal resistor and soon nRESET is released. In order to obtain a precise t_D, choosing high quality ceramic capacitor like C0G, X5R, X7R and placing the CT capacitor close to the chip are both highly recommended. Table 3 presents the examples between t_D and ideal C_{CT}.

Table 3. User-Programmable Reset Delay Time for Ideal Capacitor Values

C_{CT}	nRESET Delay Time (t_D, TYP)
250pF	1.34ms
1nF	3.63ms
3.26nF	10.5ms
32.6nF	100.33ms
65.2nF	200.08ms
1μF	3060.57ms

nRESET Latch Mode

The SGM861xQ enters latch mode when the CT pin is pulled low. Placing a resistor to pull down CT voltage is advised because of less current consumed. In latch mode, the nRESET pin stays low whatever SENSE voltage is. In order to exit the latch mode, apply a voltage higher than 1.15V on the CT pin so that the nRESET pin goes high immediately with nearly no delay. For more safe unlatch, V_{CT} = 1.4V is more recommended. Besides, a series resistor between the unlatch voltage and CT pin is useful to reduce the current that flows into the CT pin. Details please refer to Typical Application 2: nRESET Latch Mode section.



NOTE: 10kΩ resistor to GND to latch, voltage at CT to unlatch.

Figure 9. nRESET Latch/Unlatch Circuit

Adjustable Voltage Thresholds

Thanks for the high accuracy of SGM861xQ (maximum error is 2%), a resistor divider outside the device SENSE pin can be used to generate a user-defined and relatively precise sense threshold. When no variant of the SGM861xQ meets the user threshold requirements, the practice that placing external resistor divider outside the device SENSE pin is a good choice (see Figure 10). It is recommended that taking a variant with 1.2V sense threshold for the SGM861xQ because these candidates share an internal bypass resistor ladder. Note that the internal sense resistance is 7.6MΩ. As mentioned above, the SGM861B7-1.20Q is a qualified candidate.

Take SGM861B7-1.20Q as an example to supervise a 3V voltage rail, which is marked as V_{MON} here. The relationship between V_{SENSE} and V_{MON} is illustrated in Equation 4. Note that the nominal voltage threshold for SGM861B5-1.20Q is V_{SENSE} = 1.2V. If users want to supervise V_{MON} = 3V with R_2 = 10kΩ, choose R_1 = 15kΩ as a result. Considering the window threshold for SGM861B7-1.20Q is ±7%, one can calculate the UV/OV thresholds as $V_{IT\,-\,UV}$ = 1.116V and $V_{IT\,+\,OV}$ = 1.284V separately.

$$V_{SENSE} = V_{MON} \times R_2/(R_1 + R_2) \quad (4)$$

With the help of Equation 4, the UV/OV threshold for V_{MON} can be calculated as $V_{IT\,-\,UV}$ = 2.79V and $V_{IT\,+\,OV}$ = 3.21V separately. If wider tolerance or UV only threshold devices are more preferred, refer to Device Naming Description section for suitable models.

APPLICATION INFORMATION (continued)

Both the outside resistor divider and internal resistor ladder must be considered for the final sense voltage threshold accuracy. It is usually assumed that the SENSE pin is always in a high impedance state. In fact, the SENSE pin input impedance can be calculated by the sense voltage (V_{SENSE}) divided by the sense current (I_{SENSE}). According to Figure 10, I_{SENSE} can be calculated using Equation 5 where the internal sense resistance is determined by Equation 6 (nearly 7.6MΩ).

$$I_{SENSE} = (V_{MON} - V_{SENSE})/R_1 - V_{SENSE}/R_2 \quad (5)$$

$$R_{SENSE} = V_{SENSE}/I_{SENSE} \quad (6)$$

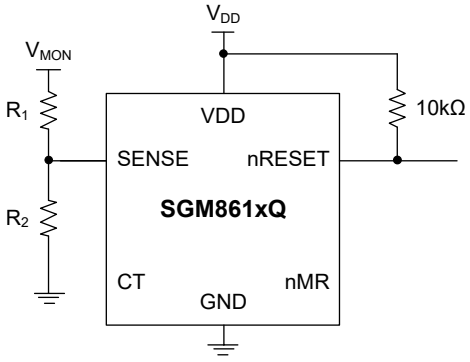


Figure 10. Adjustable Voltage Threshold with External Resistor Dividers

Immunity to SENSE Pin Voltage Transients

The SGM861xQ can suppress short spikes or glitches on both VDD and SENSE pin. The immunity ability is decided by the duration time and overdrive.

When V_{DD} is lower than the trip point for a long time, then the nRESET is asserted and the output is pulled low. When V_{DD} is just a few nanosecond lower than the trip point, the nRESET does not assert and the output continues to be high. Alter the time length that asserts the nRESET by increasing the proportion where V_{DD} is lower than the trip point. For example, when V_{DD} is 10% lower than the trip point, the comparator responds much faster and the nRESET is asserted much quicker than when just below the trip point voltage. Calculation of the percentage overdrive is shown in Equation 7:

$$\text{Overdrive\%} = |(V_{SENSE} - V_{IT-UV} \text{ or } V_{IT+OV})/V_{IT_NOM} \times 100\%| \quad (7)$$

where:

V_{SENSE} is the SENSE pin voltage.

V_{IT_NOM} is the nominal threshold voltage.

V_{IT-UV} and V_{IT+OV} represent the actual UV or OV tripping voltage.

Hysteresis

The SGM861xQ incorporates UV and OV comparators with separate hysteresis to prevent malfunction or error report for the microprocessor under noisy environment. When V_{SENSE} rises upon V_{IT+UV} or falls below V_{IT-OV}, nRESET turns high. On the contrary, when V_{SENSE} falls below V_{IT-UV} or rises upon V_{IT+OV}, nRESET turns low. Figure 11 shows the relation between V_{IT-UV}, V_{IT+OV} and hysteresis voltage (V_{HYS}).

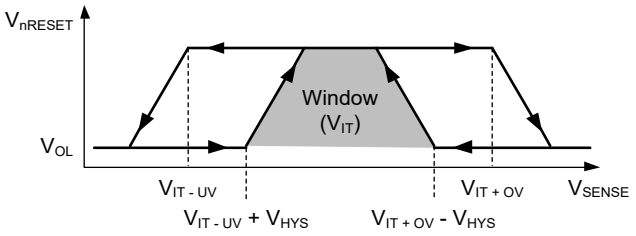


Figure 11. SENSE Pin Hysteresis

Typical Application 1: Multi-Rail Window Monitoring for Microcontroller Power Rails

Figure 12 illustrates how to use two SGM861xQ devices to monitor several voltage rails for a microprocessor. One SGM861xQ is used to supervise the core voltage and another is used to supervise the I/O voltage, which both devices need precise monitoring threshold and reset delay time.

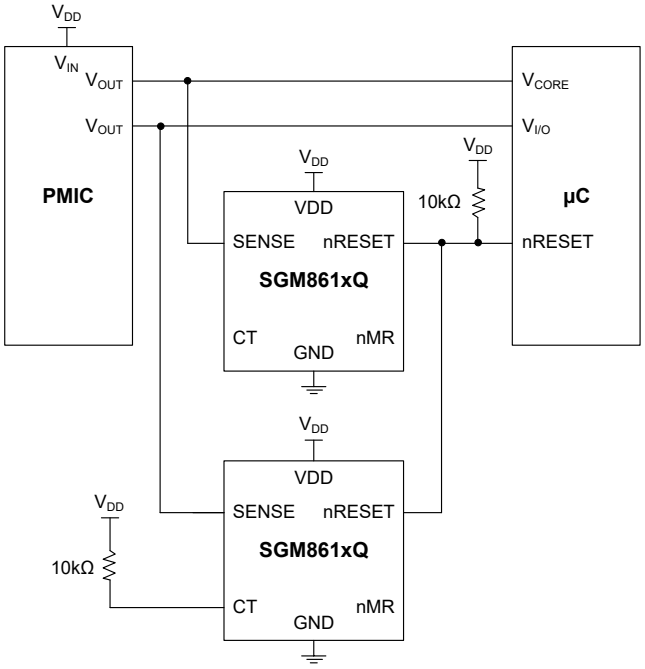


Figure 12. Monitoring Two Voltage Rails of a Microprocessor with Two SGM861xQ Devices

APPLICATION INFORMATION (continued)

Design Requirements

Table 4. Design Parameters

Parameter	Design Requirement	Design Result
Monitored Rails	$V_{I/O}$ = 3.3V (nominal), nRESET asserted if outside of ±10% of 3.3V (including device accuracy), t_D = 200ms	Maximum V_{IT+OV} = 3.597V (9%), Minimum V_{IT-UV} = 3.003V (-9%)
	V_{Core} = 1.2V (nominal), nRESET asserted if outside of ±8% of 1.2V (including device accuracy), t_D =10ms	Maximum V_{IT+OV} = 1.284V (7%), Minimum V_{IT-UV} = 1.116V (-7%)
Output Logic Voltage	5V CMOS	5V CMOS
Maximum System Supervision Current Consumption	50μA	8μA (4μA MAX each)

Detailed Design Procedure

According to the voltage rail requirements listed in Device Naming Description section, one should choose a suitable model of SGM861xQ from the aspects of SENSE threshold and window tolerance. The reset delay time t_D can be realized by choosing a proper model of SGM861xQ from the Electrical Characteristics section. Note that SENSE threshold variants range from 0.5V to 5.0V. Hence, the I/O voltage can be supervised with 3.3V threshold device and the core voltage can be supervised with 1.2V threshold device. In order to meet the threshold tolerance requirements, the I/O voltage can be supervised with ±7% threshold tolerance and the core voltage can be supervised with ±5% threshold tolerance. After that, calculate the maximum V_{IT+OV} and minimum V_{IT-UV} to further validate the effectiveness of design procedure mentioned above. Equation 8 and Equation 9 show how to calculate the maximum V_{IT+OV} and minimum V_{IT-UV} for the core voltage:

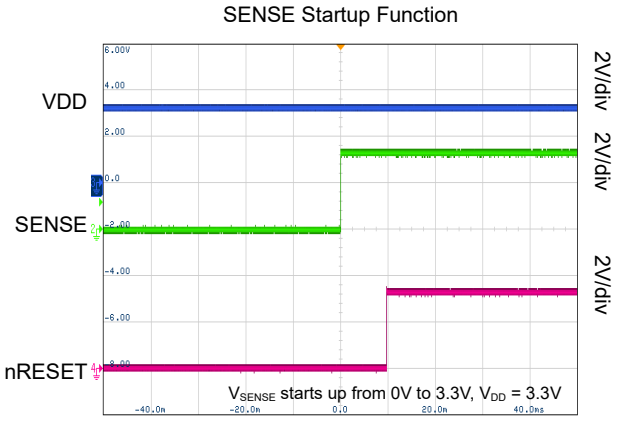
$$V_{IT+(OV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold + 2\%) = 1.2 \times (1 + 7\%) = 1.284V \quad (8)$$

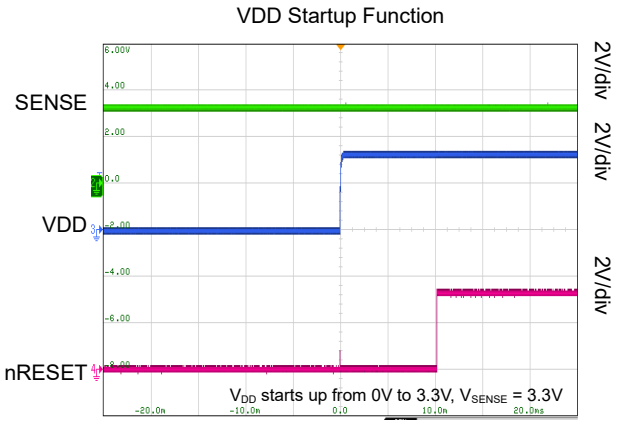
$$V_{IT-(UV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold - 2\%) = 1.2 \times (1 - 7\%) = 1.116V \quad (9)$$

The rising time of nRESET is determined by the pull-up resistor and possible capacitor at this pin. Select a suitable pull-up resistor for the nRESET pin to meet the requirements of backward timing and sinking current capability for V_{OL} listed in Electrical Characteristics section. If little capacitance exists at the nRESET pin, take the pull-up resistors ranging from 10kΩ to 1MΩ.

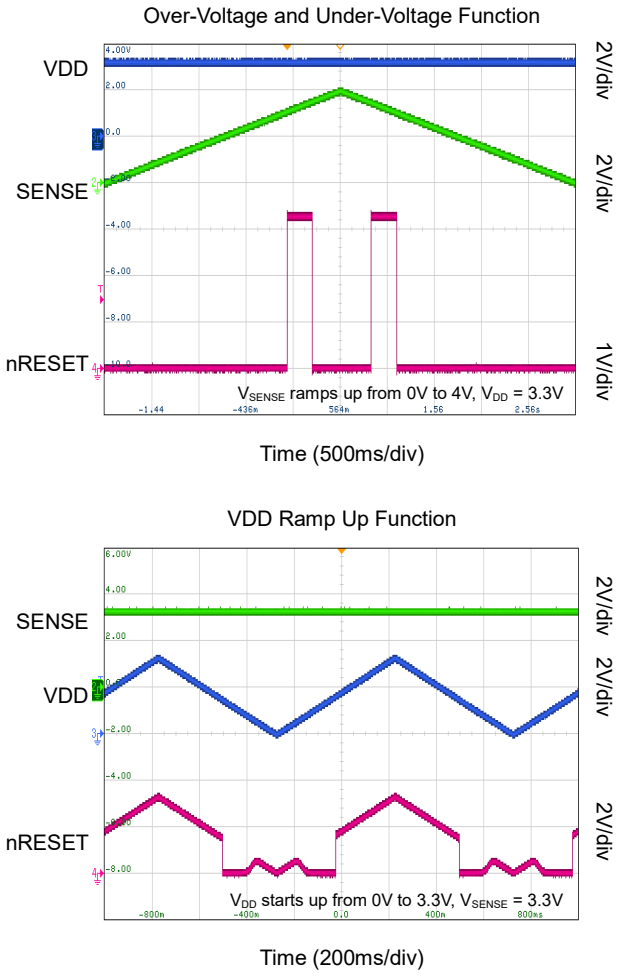
Application Curves

Conditions: SGM861A7-3.30Q, V_{nRESET} = V_{DD} = 3.3V, CT = Open.





APPLICATION INFORMATION (continued)



Typical Application 2: nRESET Latch Mode

Figure 13 shows how to monitor the core voltage of a microprocessor in latch mode. In latch mode, the nRESET pin maintains low whatever the SENSE pin voltage value is. Similarly, the nRESET pin maintains low whatever the SENSE pin voltage value is if the nRESET pin is already low during the power-up process.

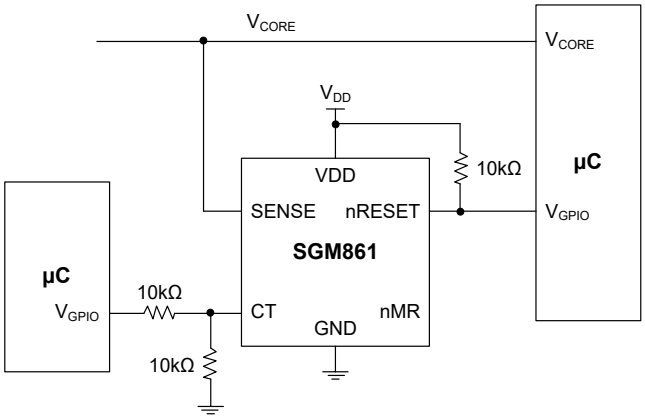


Figure 13. Monitoring Voltage Rail in Latch Mode

Detailed Design Procedure

The SGM861xQ enters latch mode when the CT pin is pulled low. Placing a resistor to pull down CT voltage is advised because of less current is consumed. Usually, placing a 10kΩ resistor is advised. In latch mode, the nRESET pin stays low whatever the SENSE pin voltage is. In order to exit the latch mode, apply a voltage higher than 1.15V on the CT pin so that the nRESET pin goes high immediately with nearly no delay. For safe unlatch, V_{CT} = 1.4V is recommended. Besides, placing a series resistor between the unlatch voltage supply source (V_{GPIO}) and the CT pin is useful to reduce the current that flows into the CT pin.

Design Requirements

Table 5. Design Parameters

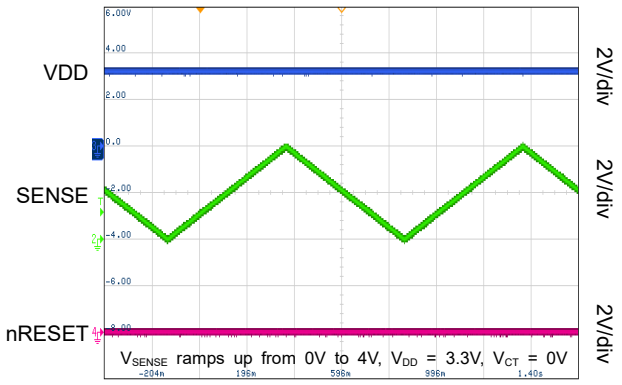
Parameter	Design Requirement	Design Result
Monitored Rail	V_{Core} = 1.2V (nominal), nRESET asserted if outside of ±8% of 1.2V (including device accuracy), Latch when nRESET is low, until voltage is applied on CT pin.	Maximum V_{IT+OV}= 1.284V (7%), Minimum V_{IT-UV} = 1.116V (-7%)
Output Logic Voltage	5V CMOS	5V CMOS
Maximum System Supervision Current Consumption	15µA	1.24µA (TYP), 4µA (MAX)

APPLICATION INFORMATION (continued)

Application Curves

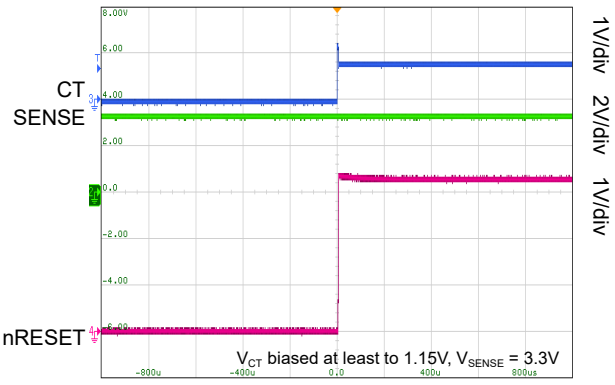
Conditions: SGM861A7-3.30Q, V_{nRESET} = V_{DD} = 3.3V. In the over-voltage and under-voltage latch function curve, V_{nRESET} = V_{DD}, CT is pulled down after nRESET is low, nRESET becomes latched.

SENSE Ramp Latch Function



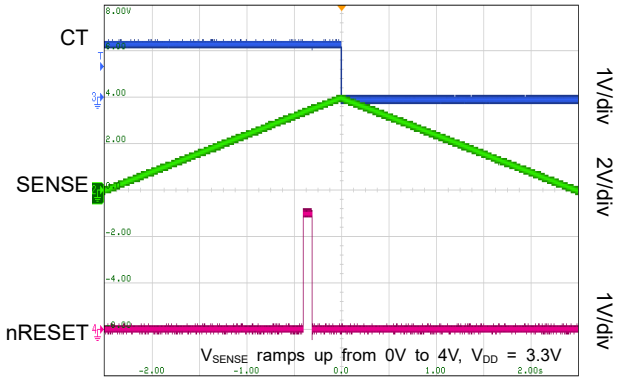
Time (200ms/div)

CT Bias Unlatch Function



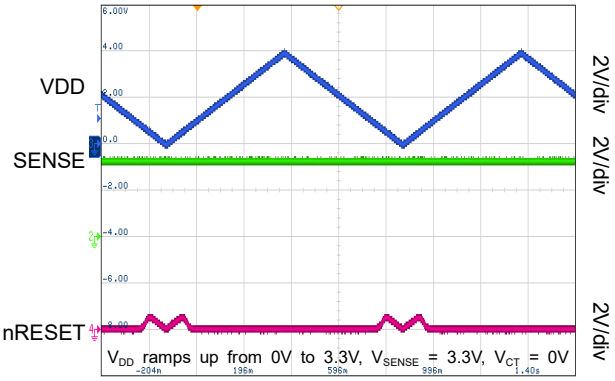
Time (200μs/div)

Over-Voltage and Under-Voltage Latch Function



Time (500ms/div)

VDD Ramp Latch Function



Time (200ms/div)

Power Supply Recommendations

This apparatus is configured to function normally with an input voltage ranging from 1.7V to 5.5V. Note that the maximum voltage at VDD pin is 6V, which highlights the need for voltage constraint. Adhering to standard analog design principles, incorporating a capacitor ranging from 0.1μF to 1μF between the VDD and GND pins is advisable, depending on the noise characteristics of the input voltage supply. This capacitor acts as a buffer, helping stabilize the power supply and protect against potential voltage fluctuations.

In cases where the VDD voltage source is prone to experiencing significant voltage transients that might exceed 6V, additional safeguards become imperative. Such measures ensure the continued reliability and longevity of the device by mitigating the risk of damage caused by voltage spikes or sudden drops.

LAYOUT

Positioning the external components in close proximity to the device is crucial, as this configuration minimizes the potential for parasitic errors that can disrupt signal integrity.

Limiting the length of VDD supply trace is essential. Note that the VDD capacitor will couple with supply parasitic inductance to form an LC circuit that may induce ringing, resulting in peak voltages exceeding the maximum VDD value. In addition, due to the short trace of the SENSE pin, the parasitic inductance is reduced and higher monitoring accuracy can be achieved.

Separating sensitive analog traces from digital ones is also critical, with an emphasis on avoiding parallel runs and only allowing perpendicular crossings when absolutely necessary, to prevent crosstalk and ensure signal purity.

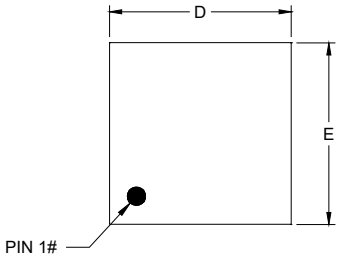
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

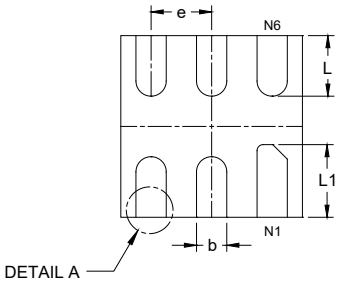
Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

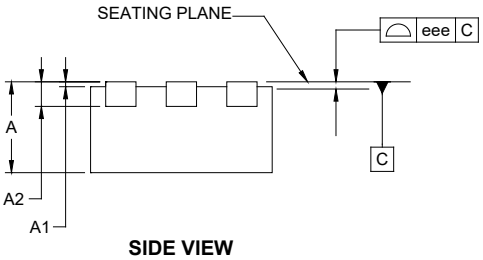
TDFN-1.5×1.5-6L



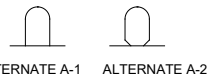
TOP VIEW



BOTTOM VIEW

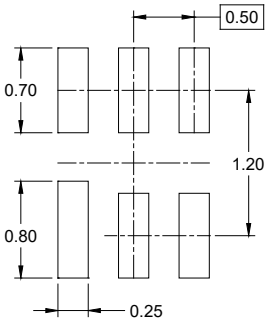


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



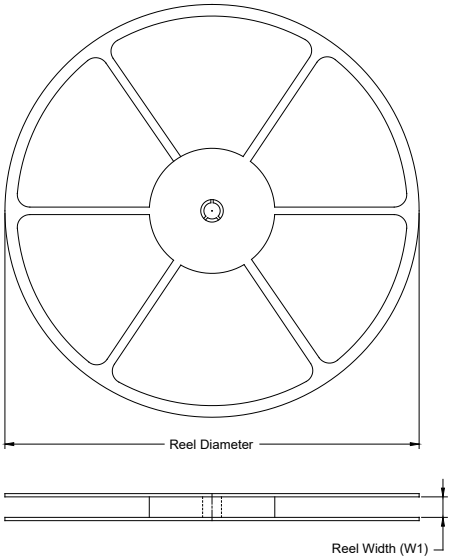
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	1.400	-	1.600
E	1.400	-	1.600
e	0.500 BSC		
L	0.400	-	0.600
L1	0.500	-	0.700
eee	0.080		

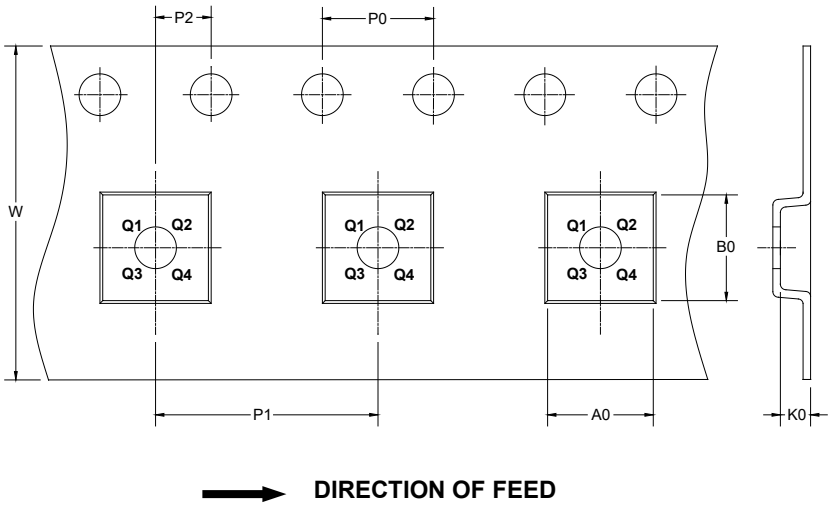
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



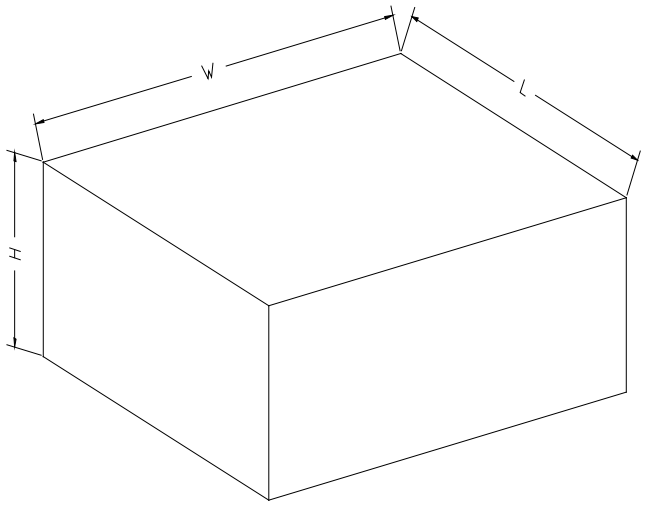
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-1.5×1.5-6L	7"	9.5	1.70	1.70	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002