SGM42210Q 6mΩ, 1-Channel High-side Driver for 12V Automotive Applications

GENERAL DESCRIPTION

The SGM42210Q is a high-side driver intended for 12V automotive applications. It is usually used to drive resistive/inductive/capacitive loads with the other terminal connected to ground. If low energy spike occurs on VCC, the internal VCC voltage clamp protects the device.

The device integrates current sense function for sensing load current through the current sense pin current out. If any of following occurs, overload, over-temperature, short-to-VCC, short-to-ground, or open-load during off-state, the sense pin will function to report these faults.

The SGM42210Q SSOP-16 (Exposed Pad) package will be reset by pulling low the nFR_STBY pin. Pulling the IN, nFR_STBY and SEn pins low will disable the device and leave it in standby mode.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM42210Q is available in Green SSOP-16 (Exposed Pad) and SSOP-14 (Exposed Pad) packages.

FEATURES

- AEC-Q100 Qualified for Automotive Applications
 Device Temperature Grade 1
 - $T_A = -40^{\circ}C$ to +125°C
- Max Transient Supply Voltage: 40V
- Operating Voltage Range: 5V to 28V
- On-Resistance: 6mΩ (TYP)
- Nominal Load Current (T_A = +25°C): 15A
- Adjustable External Current Limit: 66A, 78A, 88A
- High-side Switch with Diagnosis and Embedded Protection
- Low Off-State Supply Current
- 3V and 5V Compatible Logic Inputs
- Full Set of Protections:
 - Thermal Shutdown with Latch or Restart Option
 - Loss-of-GND and Loss-of-Battery Protection
 - Open-Load Detection in Off-State
 - Short-to-GND Protection by Current Limit
 - Inductive Load Negative Voltage Clamp
 - Under-Voltage Protection
 - Over-Voltage Clamp
 - Reverse Battery Protection with External Ground Network
 - Electrostatic Discharge Protection

TYPICAL APPLICATION

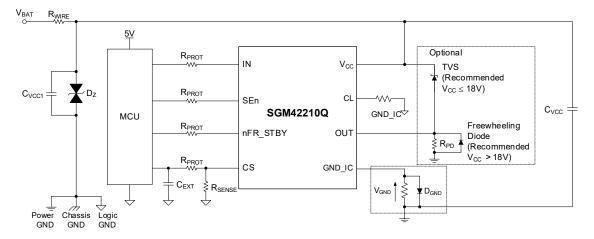


Figure 1. Typical Application Circuit of SSOP-16 (Exposed Pad) Package

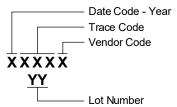


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42210Q	SSOP-16 (Exposed Pad)	-40°C to +125°C	SGM42210QPQS16G/TR	XXXXX YY 16K	Tape and Reel, 3000
	SSOP-14 (Exposed Pad)	-40°C to +125°C	SGM42210QPSS14G/TR	XXXXX YY 10D	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS
DC Supply Voltage, V _{CC} 38V
Reverse DC Supply Voltage, -V _{CC} 0.3V
Load Dump Voltage (ISO 16750-2:2010 Test B Clamped to
$40V$, $R_L = 4Ω$), V_{CCPK}
DC Reverse Ground Pin Current, -I _{GND} 200mA (1)
DC Output Current, I _{OUT} Internally Limited
DC Input Current
I _{IN} 1mA to 10mA ⁽¹⁾
I _{SEn} 1mA to 10mA ⁽¹⁾
nFR_STBY DC Input Current, I _{nFR_STBY} 1mA to 1.5mA ⁽¹⁾
CS Pin DC Output Current (V _{GND} = V _{CC} and V _{SENSE} < 0V),
I _{SENSE}
CS Pin DC Output Current in Reverse (V _{CC} < 0V), I _{SENSE}
20mA ⁽¹⁾
Maximum Switching Energy (Single Pulse) (t _{DEMAG} = 0.4ms,
T _{ASTART} = +125°C), E _{MAX} 118mJ
Junction TemperatureInternally Limited
Package Thermal Resistance
SSOP-16 (Exposed Pad), θ _{JA}
SSOP-16 (Exposed Pad), θ _{JB} 16.3°C/W
SSOP-16 (Exposed Pad), θ _{JC (TOP)} 41.9°C/W
SSOP-16 (Exposed Pad), $\theta_{JC (BOT)}$ 8.7°C/W
SSOP-14 (Exposed Pad), θ _{JA}
SSOP-14 (Exposed Pad), θ _{JB} 15.1°C/W
SSOP-14 (Exposed Pad), θ _{JC (TOP)} 41.4°C/W
SSOP-14 (Exposed Pad), $\theta_{JC (BOT)}$ 8.7°C/W
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10s)+260°C
ESD Susceptibility (2) (3)
HBM (VCC, OUT)±6000V
HBM (IN, SEn, CS, CL nFR_STBY)±4000V
CDM±1000V

- 1. Guaranteed by design, and not included in the production testing.
- 2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
- 3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

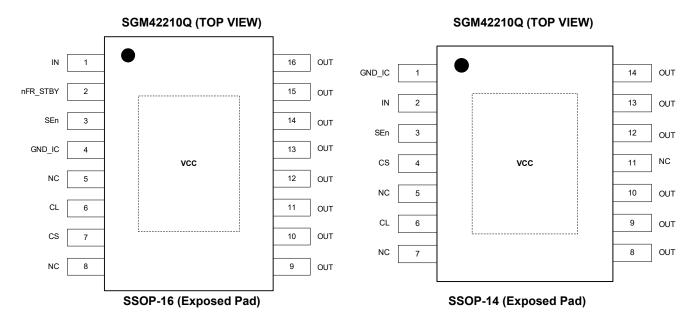
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

P	IN				
SSOP-16 (Exposed Pad)	SSOP-14 (Exposed Pad)	NAME	FUNCTION		
1	2	IN	Control Input, Active-High.		
2	-	nFR_STBY	Active-Low Reset Output/Standby Mode Pin. When over-temperature or over-current occurs and latches, pull nFR_STBY pin down to reset the device. If IN, nFR_STBY and SEn pins are low, the device will enter into standby state. Connect it to the ground through a 15kΩ resistor if not used.		
3	3	SEn	Active-High to Enable Device Diagnosis.		
4	1	GND_IC	Device Ground. Connect an external diode/resistor network for reverse battery protection.		
6	6	CL	Adjustable Current Limit. Connect respective resistor to GND_IC to set the current limit foldback level. If the current limit foldback function is not used, open load this pin.		
5, 8	5, 7, 11	NC	No Connection.		
7	4	CS	Output Load Current Sense Pin.		
9, 10, 11, 12, 13, 14, 15, 16	8, 9, 10, 12, 13, 14	OUT	Power Output. All the output pins should be shorted together.		
Expos	ed Pad	VCC	Battery Connection.		

NOTE: All OUT pins must be shorted together on PCB layout.

Table 1. Recommended Connections

Connection/Pin	IN	NC	cs	SEn, nFR_STBY	OUT
Floating	X	X ⁽¹⁾	Not Allowed	X	Х
To Ground	Through 15kΩ Resistor	Х	Through 1kΩ Resistor	Through 15kΩ Resistor	Not Allowed

NOTE: 1. X = do not care.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 7V \text{ to } 28V, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}. \text{ Typical values are measured at } V_{CC} = 13V, T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted.})$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Supplies							
Operating Supply Voltage	V_{CC}			5	13	28	V
Under-Voltage Shutdown	V _{USD}			3.7		4.5	V
Under-Voltage Shutdown Reset	$V_{USD_{R}}$			4		5	V
Under-Voltage Shutdown Hysteresis	V _{USD_HYS}				0.45		V
On Basistanaa	D	V _{CC} = 7V, I _{OUT} = 5A			8.5	20	0
On-Resistance	R_{DSON}	V _{CC} = 13V, I _{OUT} = 5A			6	12	mΩ
Clamp Voltage	V_{CLAMP}	I _S = 20mA		41	48.5	57	V
		V _{CC} = 13V, V _{IN} = V _{SEn} = V _{OUT}	T _A = +25°C		0.3	0.7	
Supply Current in Standby ⁽¹⁾	I _{STBY}	= V _{nFR_STBY} = 0V	T _A = +125°C		2	5.5	μΑ
Standby Mode Blanking Time	t _{D_STBY}	$V_{CC} = 13V, V_{IN} = 5V, V_{SEn} = 0.00$	$V_{nFR_STBY} = 0V,$	30	50	70	ms
Supply Current	I _{S_ON}	$I_{OUT} = 0A$ $V_{CC} = 13V, V_{SEn} = V_{nFR_STBY}$	= 0V, V _{IN} = 5V,		3.5	5	mA
Control Stage Current Consumption in		I _{OUT} = 0A All channels active, V _{CC} = 13	V, V _{SEn} = 5V.		4.5		
On-State	I _{GND_ON}	$V_{nFR STBY} = 0V, V_{IN} = 5V, I_{OUT}$			4.5	6	mA
Off-State Output Current (1)	l	$V_{IN} = V_{OUT} = 0V$, $V_{CC} = 13V$	T _A = +25°C		0.1	0.3	μA
On-State Output Gurrent	I_{L_OFF}	VIN - VOUT - UV, VCC - 13V	T _A = +125°C			5	μΑ
Output - V _{CC} Diode Voltage	V_{F}	I _{OUT} = -5A, T _A = +125°C				0.7	V
Switching (V _{cc} = 13V)					•		
Turn-On Delay Time	t _{D_ON}	D 000 T 0500 F		7	20	35	
Turn-Off Delay Time	t _{D_OFF}	$R_L = 2.6\Omega$, $T_A = +25$ °C, see F	4	10	16	μs	
Turn-On Voltage Slope	dV _{OUT} /dt _{ON}			0.3	0.9	1.8	\ //
Turn-Off Voltage Slope	dV _{OUT} /dt _{OFF}	$R_L = 2.6\Omega$, $T_A = +25$ °C, see F	igure 2	0.3	1.1	1.8	V/µs
Switching Energy Losses at t _{WON} (2)	W _{ON}	$R_L = 2.6\Omega$			0.24	0.4	mJ
Switching Energy Losses at twoff (2)	W_{OFF}	$R_L = 2.6\Omega$			0.16	0.4	mJ
Differential Pulse Skew	t _{SKEW}	$R_L = 2.6\Omega$, $t_{PHL} - t_{PLH}$		-40	0	40	μs
IN							•
Low-Level Input Voltage	V _{IL}					0.9	V
High-Level Input Voltage	V _{IH}			2.1			V
Low-Level Input Current	I _{IL}	V _{IN} = 0.9V		1			μΑ
High-Level Input Current	I _{IH}	V _{IN} = 2.1V				10	μΑ
Input Hysteresis Voltage	V _{I_HYS}				0.5		V
Innut Claren Valtaria	\/	I _{IN} = 1mA		5.3	5.6	6.2	
Input Clamp Voltage	V_{ICL}	I _{IN} = -1mA			-0.6		V
nFR_STBY (SSOP-16 (Exposed Pad) O	nly)						
Low-Level Input Voltage	V_{nFR_STBYL}					0.9	V
High-Level Input Voltage	$V_{nFR_STBY_H}$			1.2			V
Low-Level Input Current	I _{nFR_STBY_L}	V _{IN} = 0.9V		1			μΑ
High-Level Input Current	I _{nFR_STBY_H}	V _{IN} = 2.1V				10	μΑ
Input Hysteresis Voltage	$V_{nFR_STBY_HYS}$				0.5		V
Input Clamp Voltage	V _{nFR_STBY_CL}	I _{IN} = 1mA		5.3	5.6	6.2	V
input claimp voltage	v n⊦k_STBY_CL	I _{IN} = -1mA			-0.6		

- 1. MOS leakage included.
- 2. Guaranteed by design.



ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC}$ = 7V to 28V, T_A = -40°C to +125°C. Typical values are measured at V_{CC} = 13V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	C	CONDITIONS		TYP	MAX	UNITS
SEn		1					
Low-Level Input Voltage	V_{SEn_L}					0.9	V
High-Level Input Voltage	V _{SEn_H}			2.1			V
Low-Level Input Current	I _{SEn_L}	V _{IN} = 0.9V		1			μΑ
High-Level Input Current	I _{SEn_H}	V _{IN} = 2.1V				10	μΑ
Input Hysteresis Voltage	V _{SEn_HYS}				0.5		V
Input Clamp Valtage	V	I _{IN} = 1mA		5.3	5.6	6.2	V
Input Clamp Voltage	V_{SEn_CL}	$I_{IN} = -1mA$			-0.6		\ \ \
Protections		•				_	-
CL Pin Current	1	CL = 0V	V _{CC} = 7V to 18V		10		
CL FIII Guirein	I_{CL}	CL = UV	V _{CC} = 21V to 28V		20		μA
		CL = open, V _{CC} =		50	66	82	
DC Short-Circuit Current (1)	I _{LIMH_13V}	$CL = 39k\Omega$ to 56 18V	$k\Omega$ to GND_IC, V_{CC} = 7V to	58	78	97	A
La chieft direant darrent		CL short to GND_IC, V _{CC} = 7V to 18V		70	88	106	
	I _{LIMH_28V}	V _{CC} = 21V to 28V	,	15	32	42	
Short-Circuit Current during Thermal	I _{LIML_13V}	V _{CC} = 7V to 18V		13	26	48	A
Cycling ⁽¹⁾	I _{LIML_28V}	V _{CC} = 21V to 28V	,	6	13	26	
Shutdown Temperature (1)	T_{SD}				155		°C
Thermal Hysteresis (T _{SD} - T _R) ⁽¹⁾	T _{HYS}				10		°C
Reset Temperature (1)	T_R				145		°C
Thermal Reset of Fault Diagnostic Indication (1)	T_{TRS}				125		°C
Fault Reset Time for Output Unlatch (1)	t _{LATCH_RST}	$V_{nFR_STBY} = 5V to$	0V, V _{SEn} = 5V, V _{IN} = 5V		25		μs
Turn-Off Output Voltage Clamp	V_{DEMAG}	I _{OUT} = 20mA		39	44	48	V
Off-State Diagnostic		•				_	-
Open-Load Voltage Detection Threshold	V _{OL}	V _{IN} = 0V, V _{SEn} = 5V		2	3	4	V
Output Sink Current	I _{L_OFF2}	V _{IN} = 0V, V _{OUT} = 4V		-80	-32	-10	μΑ
Diagnostic Delay Time from Falling Edge of Input	t _{DSTKON}	V_{IN} = 5V to 0V, V_{SEn} = 5V, I_{OUT} = 0A, V_{OUT} = 4V, see Figure 3		200	350	500	μs
Settling Time for Valid Off-State Open-Load Diagnostic Indication from Rising Edge of SEn	$t_{D_OL_V}$	V _{IN} = 0V, V _{nFR_STBY} = 0V, V _{OUT} = 4V, V _{SEn} = 0V to 5V			85	150	μs
Delay Time	t _{D_VOL}	$V_{IN} = 0V, V_{SEn} =$ rising edge of V_{C}	5V, V _{OUT} = 0V to 4V, from		7	15	μs

NOTE: 1. Parameter guaranteed by design and characterization; not subject to production test.

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC}$ = 7V to 28V, T_A = -40°C to +125°C. Typical values are measured at V_{CC} = 13V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Characteristics (7V < Vo	_{:c} < 18V)						
	.,	V _{SEn} = 0V, I _{SENSE} = -1mA		-15	-13.5	-12	.,
Current Sense Clamp Voltage	V_{SENSE_CL}	V _{SEn} = 0V, I _S	_{ENSE} = 1mA		9		V
I _{OUT} /I _{SENSE} (1)	K ₀	V _{CC} = 13V, I ₀ = 5V	$_{\text{OUT}}$ = 0.25A, V_{SENSE} = 0.5V, V_{SEn}	3050	4500	5900	
Current Sense Ratio Drift (2)	dK_0/K_0	V _{CC} = 13V, T	_A = +25°C	-10		10	%
I _{OUT} /I _{SENSE} (1)	K ₁	V _{CC} = 13V, I _C	DUT = 1A, V _{SENSE} = 4V, V _{SEn} = 5V	4100	4700	5200	
Current Sense Ratio Drift (2)	dK₁/K₁	V _{CC} = 13V, T	_A = +25°C	-4		4	%
I _{OUT} /I _{SENSE} (1)	K ₂	V _{CC} = 13V, I _C	$_{DUT} = 6A, V_{SENSE} = 4V, V_{SEn} = 5V$	4500	4900	5200	
Current Sense Ratio Drift (2)	dK ₂ /K ₂	V _{CC} = 13V, T		-4		4	%
I _{OUT} /I _{SENSE} (1)	K ₃	V _{CC} = 13V, I 5V	$_{OUT}$ = 18A, V_{SENSE} = 4V, V_{SEn} =	4500	4900	5200	
Current Sense Ratio Drift (2)	dK ₃ /K ₃	V _{CC} = 13V, T	_A = +25°C	-4		4	%
CS Current for OL Detection	I _{SENSE_OL}	I _{OUT} = 0.01A,	V _{SENSE} = 0.5V, V _{SEn} = 5V			28	μΑ
	I _{SENSE0}	CS disabled CS enabled	V _{SEn} = 0V, V _{SENSE} = -1V to 0V			0.5	
Current Sense Leakage Current			V _{SEn} = 0V, V _{SENSE} = 5V		0.3		μΑ
			V_{SEn} = 5V, channel on, I_{OUT} = 0A, diagnostic selected, V_{IN} = 5V, I_{OUT} = 0A			25	
			V_{SEn} = 5V, channel off, diagnostic selected, V_{IN} = 0V			0.5	
CS Saturation Voltage	V_{SENSE_SAT}	$V_{CC} = 7V, R$ 5V, $I_{OUT} = 18$	$_{\text{SENSE}}$ = 2.7k Ω , V_{SEn} = 5V, V_{IN} =	5	6.5		V
CS Saturation Current (3)	I _{SENSE_SAT}	V _{CC} = 7V, V _S	_{ENSE} = 4V, V _{IN} = 5V, V _{SEn} = 5V	4			mA
Output Saturation Current (3)	I _{OUT_SAT}	V _{CC} = 7V, V _S	_{ENSE} = 4V, V _{IN} = 5V, V _{SEn} = 5V	22			Α
Fault Diagnostic Feedback (See Truth	Table)						_
Current Sense Output Voltage in Fault Condition	V _{SENSEH}	$V_{CC} = 13V,$ $V_{OUT} = 4V,$ R	$V_{IN} = 0V$, $V_{SEn} = 5V$, $I_{OUT} = 0A$, $I_{SENSE} = 1k\Omega$	5		6	V
Current Sense Output Current in Fault Condition	I _{SENSEH}	V _{CC} = 13V, V	/ _{SENSE} = 5V	8	15	22	mA
Current Sense Timings (Current Sense	Mode) (V _{cc} =	13V)					
Current Canaa Cattling Time	t _{DSENSE1H}	From rising edge of SEn, $V_{IN} = 5V$, $V_{SEn} = 0V$ to $5V$, $R_{SENSE} = 1k\Omega$, $R_{I} = 2.6\Omega$, see Figure 4			5	30	μs
Current Sense Settling Time	t _{DSENSE2H}	to 5V, R_{SENSE} = 1k Ω , R_L = 2.6 Ω , see Figure 4 From rising edge of IN, V_{IN} = 0V to 5V, V_{SEN} = 5V, R_{SENSE} = 1k Ω , R_L = 2.6 Ω , see Figure 4			100	200	μs
Delay Response Time between Rising Edge of Output Current and Rising Edge of Current Sense	$\Delta t_{\text{DSENSE2H}}$	$\begin{array}{l} V_{IN}=5V,V_{SEn}=5V,R_{SENSE}=1k\Omega,R_L=2.6\Omega,\\ I_{SENSE}=80\% \ \ of \ \ I_{SENSEMAX},I_{OUT}=80\% \ \ of \\ I_{OUTMAX} \end{array}$		_		150	μs
Current Sense Disable Delay Time	t _{DSENSE1L}	5V to 0V, F Figure 4	edge of SEn, V_{IN} = 5V, V_{SEn} = R_{SENSE} = 1k Ω , R_L = 2.6 Ω , see		3	20	μs
Current Sense Turn-Off Delay Time	t _{DSENSE2L}		edge of IN, V_{IN} = 5V to 0V, V_{SEn} = 1k Ω , R_L = 2.6 Ω , see Figure 4		3	20	μs

- 1. Not include lifetime drift.
- 2. +25°C lifetime drift.
- 3. Parameter guaranteed by design and characterization; not subject to production test.

TIMING DIAGRAM

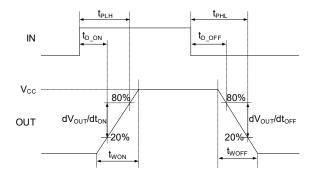


Figure 2. Timing Diagram

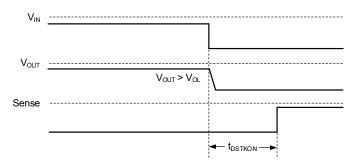


Figure 3. Diagnostic Delay Time from Falling Edge of Input (t_{DSTKON})

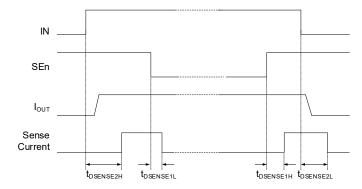
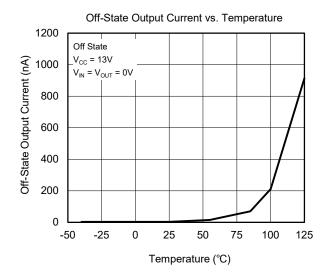
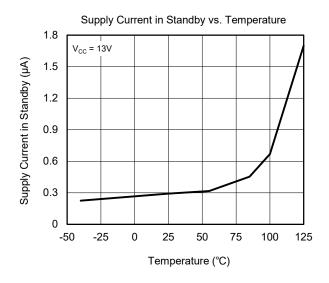
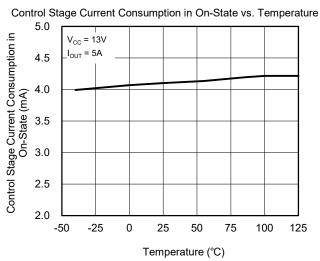


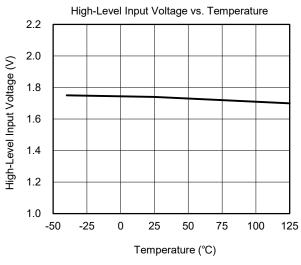
Figure 4. Current Sense Timing (Current Sense Mode)

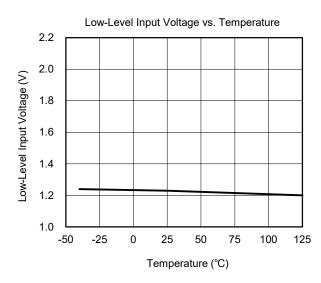
TYPICAL PERFORMANCE CHARACTERISTICS

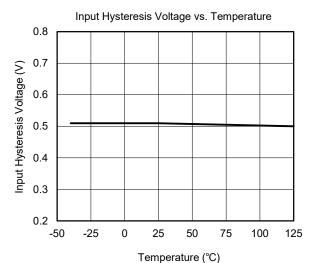




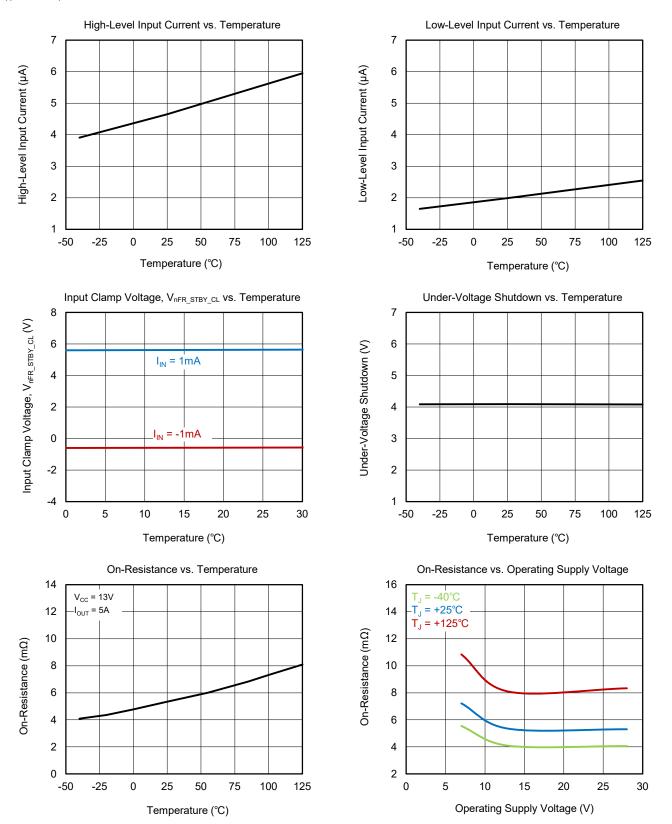




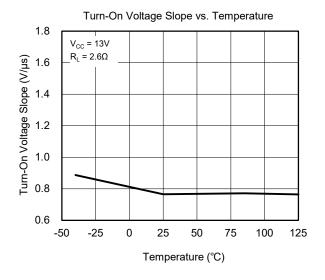


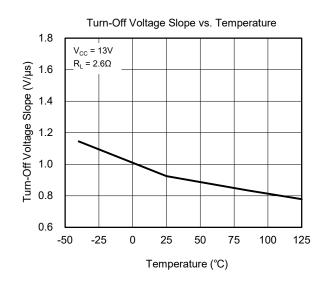


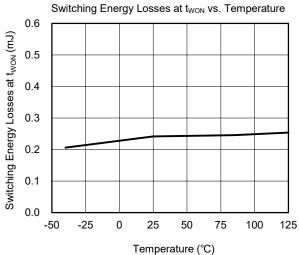
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

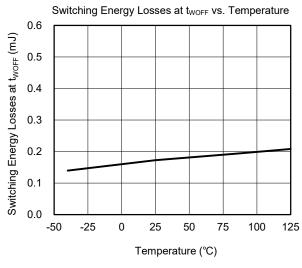


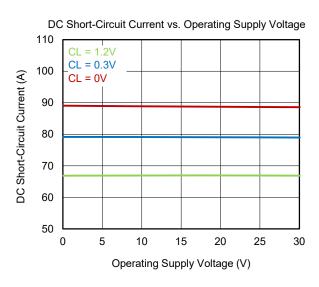
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

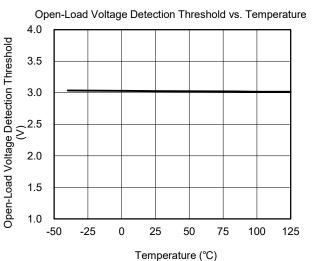




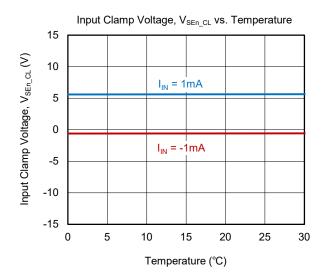


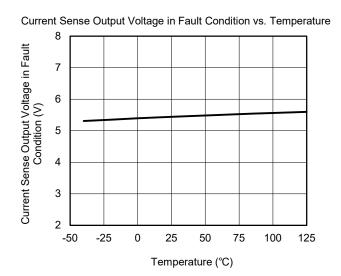


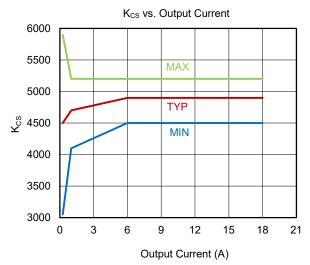


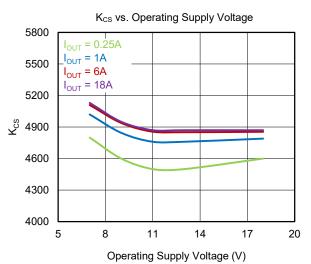


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

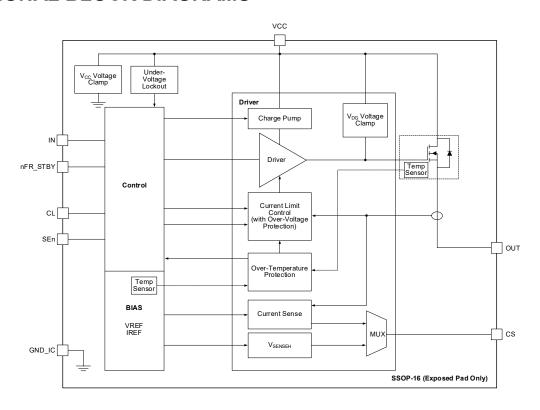








FUNCTIONAL BLOCK DIAGRAMS



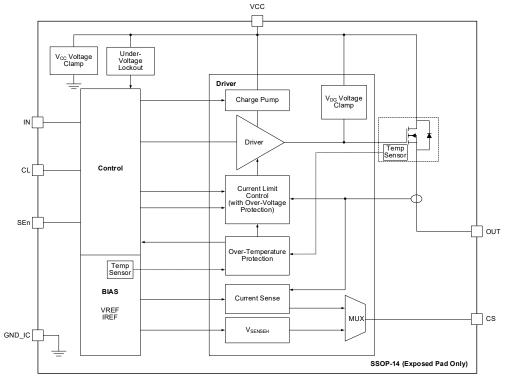


Figure 5. Block Diagrams

DETAILED DESCRIPTION

Latch Functionality:

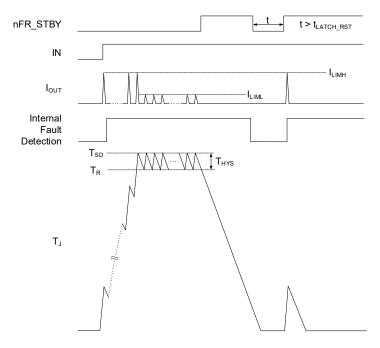


Figure 6. Device Behavior in Hard Short-Circuit Condition

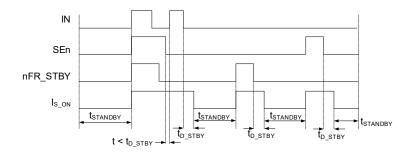


Figure 7. Standby Mode Activation

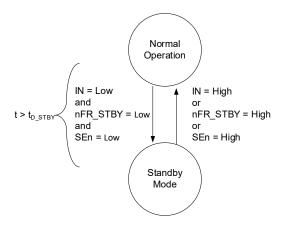


Figure 8. Standby State Diagram

DETAILED DESCRIPTION (continued)

Table 2. Truth Table of SSOP-16 (Exposed Pad) Package

Mode	Conditions	IN	nFR_STBY	SEn	OUT	Current Sense	Comments	
Standby	All logic inputs low	L	L	L	L	Hi-Z	Low quiescent current consumption	
	Naminal land connected	L	Х		L			
Normal	Nominal load connected, T _A ≤ +125°C	Н	L	Refer to Table 5	Н	Refer to Table 5	Outputs configured for auto-restart	
	.A = .120 0	Н	Н		Н		Outputs configured for latch-off	
	Overload or short-to-GND	L	Х		L			
Overload	causing:		Н	L	Refer to Table 5	Н	Refer to Table 5	Output cycles with temperature hysteresis
	I FET > I SD OI I CTR > I SD	Н	Н		L		Output latches-off	
Under-Voltage	V _{CC} < V _{USD} (falling)	Х	Х	Х	L	Hi-Z	Restart when V _{CC} > V _{USD} + V _{USD_HYS} (rising)	
Off-State	Short-to-V _{CC}	L	Х	Refer to	Н	Refer to		
Diagnostics	Open-load	L	Х	Table 5	Н	Table 5	External pull-up	
Negative Output Voltage	Inductive loads turn-off	L	Х	Refer to Table 5	< 0V	Refer to Table 5		

Table 3. Truth Table of SSOP-14 (Exposed Pad) Package

able 5. Truth Table of 550F-14 (Exposed Fau) Fackage									
Mode	Conditions	IN	SEn	OUT	Current Sense	Comments			
Standby	All logic inputs low	L	L	L	Hi-Z	Low quiescent current consumption			
Normal	Nominal load connected,	L	Refer to	L	Refer to				
Nomiai	T _A ≤ +125°C	H	Table 5	Н	Table 5	Outputs configured for auto-restart			
• • •	Overload or short-to-GND causing:	L	Refer to	L	Refer to				
Overload	T _{FET} > T _{SD} or T _{CTR} > T _{SD}	Н	Table 5	Н	Table 5	Output cycles with temperature hysteresis			
Under-Voltage	V _{CC} < V _{USD} (falling)	Х	Х	L	Hi-Z	Restart when $V_{CC} > V_{USD} + V_{USD_HYS}$ (rising)			
Off-State	Short-to-V _{CC}	L	Refer to	Н	Refer to				
Diagnostics	Open-load	L	Table 5	Н	Table 5	External pull-up			
Negative Output Voltage	Inductive loads turn-off	L	Refer to Table 5	< 0V	Refer to Table 5				

DETAILED DESCRIPTION (continued)

Table 4. Local Thermal Sense Based T_{SD} and T_{TRS} Truth Table

Power FET	Controller	Driver Behavior				
Power FET	Controller	Current Limit	State			
T _{FET} < T _{TRS_FET}		I _{LIMH}	On			
$T_{TRS_FET} < T_{FET} < T_{SD_FET}$	$T_{CTR} < T_{TRS_CTR}$	1	On			
T _{SD_FET} < T _{FET}		ILIML	Off			
$T_{FET} < T_{SD_FET}$	т .т .т		On			
T _{SD_FET} < T _{FET}	$T_{TRS_CTR} < T_{CTR} < T_{SD_CTR}$	I _{LIML}	Off			
Don't Care	T _{SD_CTR} < T _{CTR}		Off			

SGM42210Q implemented local thermal sense function in power FET and controller. The behavior of power FET depends on the external command and the thermal information. Each power FET has independent thermal sense and current limit regulation capability while controller temperature is lower than T_{TRS} . Besides, the controller has higher priority in thermal protection. Once the T_{SD} signal of controller thermal sense is triggered, all power FET will be shut down immediately until the controller temperature lower than T_{SD} - T_{HYS} . Then in thermal cycling period, current limit will be reduced to I_{LIML} until controller temperature lower than T_{TRS} .

Table 5. Current Sense

SEn	se Output								
SEII	Mode	Normal Mode	Overload	Off-State Diagnostic	Negative Output				
L			Hi-Z						
Н	Output Diagnostic	I _{SENSE} = 1/K × I _{OUT}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z				

NOTE: If the output channel is latched off while the input is low, the CS pin delivers feedback according to off-state diagnostic.

Example 1: nFR STBY = 1, IN = 0, OUT = L (latched), channel = diagnostic, CS = 0.

Example 2: nFR STBY = 1, IN = 0, OUT = latched, V_{OUT} > V_{OL}, channel = diagnostic, CS = V_{SENSEH}.

Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_{FET} > T_{SD}$ or $T_{CTR} > T_{SD}$. When thermal shutdown occurs, the output turns off. The nFR_STBY pin is used to configure the behavior after the thermal shutdown occurs.

- ◆ When the nFR_STBY pin is low, thermal shutdown operates in the auto-restart mode. The output automatically recovers when T_{FET} < T_R or T_{CTR} < T_R, but the current is limited to I_{LIM_L} during thermal cycling. The fault signal is cleared when T_{FET} < T_{TRS} or T_{CTR} < T_{TRS} or after toggling the related IN pin.
- When the nFR_STBY pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the nFR_STBY pin goes from high to low, thermal shutdown changes to auto-restart mode.

APPLICATION INFORMATION

Reverse Battery Protection with External Ground Network

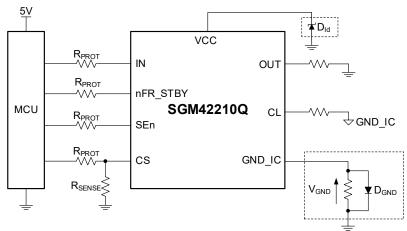


Figure 9. Reverse Battery Protection with External Ground Network of SSOP-16 (Exposed Pad) Package

D_{GND} in the GND Line

Adding a GND network. The reverse current through the GND_IC is blocked. The reverse current through the FET is limited by the load itself. A resistor in parallel with the diode is recommended as a GND network. The recommended selection is $4.7 k\Omega$ resistor in parallel with the diode.

The reverse current protection diode will bring about 0.6V level shift on the input voltage threshold.

Immunity Test According to Automotive Standard

Testing the device for compliance with EMC/EMI standards is important for automotive customers.

ISO 7637 is titled "road vehicles - electrical disturbances from conduction and coupling", and part 2 is specifically "electrical transient conduction along supply lines only." As high-side driver is connected directly from automotive battery power supply, this is very relevant. Also load dump test according to ISO 16750-2:2010 is one of the crucial test for automotive customers.

Functional Class B

All functions of the device/system are performed as designed during the test. However, one or more may go beyond the specified tolerance. All functions return automatically to within normal limits after the test.

Table 6. Flectrical Transient Requirements

ISO 7637-2: _2011(E)	Chahua		Minimum Number of Pulses or Test Time	Burst Cycle/Pulse Repetition Time		Pulse Duration and Pulse Generator Internal			
Test Pulse	Level	U _s ⁽¹⁾		MIN	MAX	Impedance			
1	III	-112V	500 pulses	0.5s		2ms, 10Ω			
2a ⁽³⁾	III	+55V	500 pulses	0.2s	5s	50μs, 2Ω			
3a	IV	-220V	1h	90ms	100ms	0.1μs, 50Ω			
3b	IV	+150V	1h	90ms	100ms	0.1μs, 50Ω			
4 (2)	IV	-7V	1 pulse			100ms, 0.01Ω			
	Load dump according to ISO 16750-2:2010								
Test B (3)		40V	5 pulse	1min		400ms, 2Ω			

- 1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
- 2. Test pulse from ISO 7637-2:2004(E).
- 3. With 40V external suppressor referred to ground (-40°C < T_A < +125°C).



APPLICATION INFORMATION (continued)

MCU I/Os Protection

In some severe conditions, such as the ISO7637-2 test or the loss-of-battery with inductive loads, a negative pulse occurs on the GND pin. This pulse can cause damage on the connected microcontroller. Serial resistors are recommended to protect the microcontroller, when choosing the serial resistor, there are several factors need to consider, the MCU IO leakage current/high-side driver input threshold level/MCU IO latch-up current limit. Please refer to example calculation below:

$$V_{CC PEAK}/I_{LATCHUP} \le R_{PROT} \le (V_{OH\mu C} - V_{IH} - V_{GND})/I_{IHMAX}$$
 (1)

where V_{CC_PEAK} = -150V, $I_{LATCHUP}$ \geq 20mA, $V_{OH\mu C}$ \geq 4.5V, 7.5k Ω \leq R_{PROT} \leq 140k Ω .

Recommended values: $R_{SERIAL} = 15k\Omega$.

Analog Current Sense (CS)

Current sense allows for immediate feedback to the user on the status of the system. As a diagnostic tool, it allows the user to monitor the current flowing into the load while maintaining the efficiency of the system, and also report the fault status during overload/over-temperature/open-load situation. Current monitor: current mirror of channel output current. Please refer to Table 5 for more details about the current sense multiplexer.

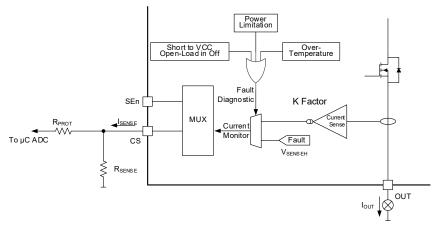


Figure 10. Current Sense and Diagnostic

Principle of Current Sense Signal Generation

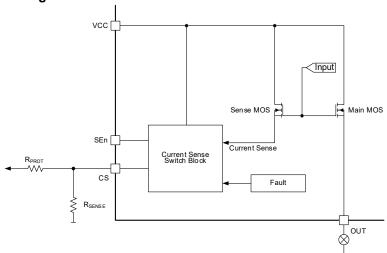


Figure 11. Current Sense Block Diagram

APPLICATION INFORMATION (continued)

Current Sense

A current mirror is a circuit that is specially designed to copy the current flowing through an active device. This ratio K is a fixed value and cannot be changed by the user. The CS pin can also report a fault with V_{SENSEH} voltage during fault condition.

Normal Operation

While device is working in normal conditions, output is on, no fault and SEn is active.

One integrated current mirror can source 1/Kcs of the load current: $I_{SENSE} = I_{OUT} \times 1/K_{CS}$.

$$V_{SENSE} = R_{SENSE} \times I_{SENSE} = R_{SENSE} \times I_{OUT} / K_{CS}$$
 (2)

where:

V_{SENSE} is the voltage on R_{SENSE}.

I_{SENSE} is the current source out from CS pin.

I_{OUT} is the current flowing through output.

K_{CS} is the current mirror ratio.

Fault Indication

During a fault condition, for example over-temperature/overload/open-load, the CS pin outputs V_{SENSEH} voltage to indicate the fault.

SSOP-16 (Exposed Pad) Package:

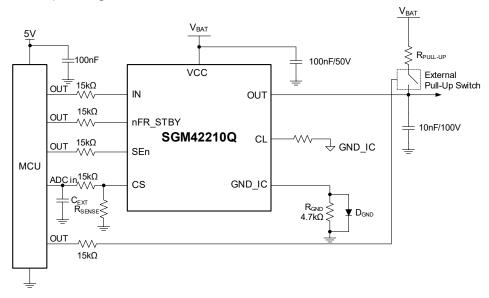


Figure 12. Open-Load Detection in Off-State (Analog HSD)

APPLICATION INFORMATION (continued)

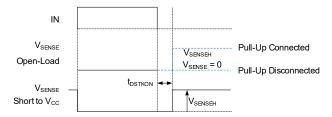


Figure 13. Open-Load/Short-to-VCC

Table 7. Current Sense Pin Levels in Off-State

Condition	Output	cs	SEn
Open-Load	V 5 V	Hi-Z	L
	$V_{OUT} > V_{OL}$	V _{SENSEH}	Н
	V ~V	Hi-Z	L
	$V_{OUT} < V_{OL}$	0	Н
Short-to-VCC	V 5V	Hi-Z	L
	$V_{OUT} > V_{OL}$	V _{SENSEH}	Н
Nominal	V _{OUT} < V _{OL}	Hi-Z	L
	VOUT ~ VOL	0	Н

Short-to-Battery

In off-state, short-to-battery has the same detection mechanism and behavior as open-load detection.

Off-State Open-Load Pull-Up Resistor

There is always a leakage current I_{L_OFF} present on the output due to internal logic control path or external humidity, corrosion, and so forth. In off-state, external pull-up resistor is needed for open-load detection. R_{PU} should be selected to make sure that $V_{OUT} > V_{OL_MAX}$ please refer to the calculation below:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L OFF2 MIN}@4V}$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)

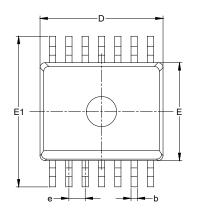
Page

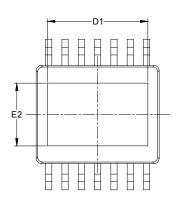
Changed from product preview to production data.....

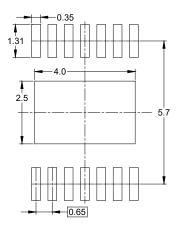


.All

PACKAGE OUTLINE DIMENSIONS SSOP-14 (Exposed Pad)



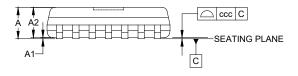


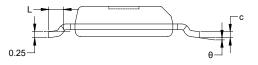


TOP VIEW

BOTTOM VIEW

RECOMMENDED LAND PATTERN (Unit: mm)

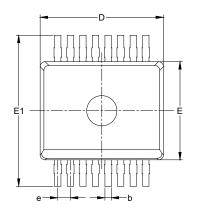


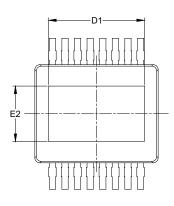


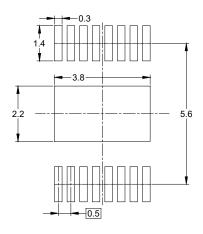
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Symbol	MIN	NOM	MAX			
Α	-	-	1.400			
A1	0.000	-	0.100			
A2	1.200 REF					
b	0.200	-	0.300			
С	0.190	-	0.280			
D	4.800	-	5.000			
D1	3.800	-	4.200			
E	3.800	-	4.000			
E1	5.800	6.200				
E2	2.300	2.700				
е	0.650 BSC					
L	0.400	-	0.850			
θ	0°	-	8°			
ccc	0.100					

- 1. This drawing is subject to change without notice.
- 2. The dimensions do not include mold flashes, protrusions or gate burrs.

PACKAGE OUTLINE DIMENSIONS SSOP-16 (Exposed Pad)



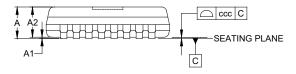


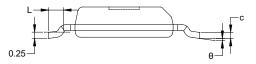


TOP VIEW

BOTTOM VIEW

RECOMMENDED LAND PATTERN (Unit: mm)



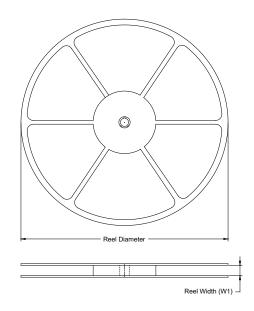


0bl	Dimensions In Millimeters						
Symbol	MIN	NOM	MAX				
А	-	-	1.400				
A1	0.000	-	0.100				
A2		1.200 REF					
b	0.200	-	0.300				
С	0.190	-	0.280				
D	4.800	-	5.000				
D1	3.600	-	4.200				
Е	3.800	-	4.000				
E1	5.800	-	6.200				
E2	1.900	1.900 -					
е	0.500 BSC						
L	0.400	-	0.850				
θ	0°	-	8°				
ccc	0.100						

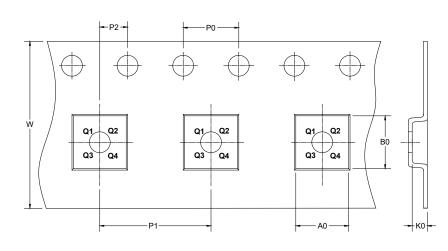
- 1. This drawing is subject to change without notice.
- 2. The dimensions do not include mold flashes, protrusions or gate burrs.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



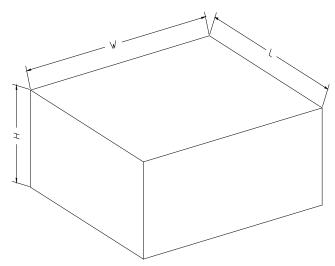
DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-16 (Exposed Pad)	13"	12.4	6.50	5.25	1.70	4.0	8.0	2.0	12.0	Q1
SSOP-14 (Exposed Pad)	13"	12.4	6.50	5.25	1.70	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
13″	386	280	370	5	DD0002