SGM61167
16V, 6A, High-Efficiency, Buck Converter with Adjustable Current Limit

GENERAL DESCRIPTION

The SGM61167 is a high-efficiency high-frequency synchronous Buck DC/DC converter with a wide input voltage range and 6A output current, optimized for compact solutions. With an internally compensated adaptive constant on-time (ACOT) control architecture, ultra-fast dynamic response is achieved, and loop stabilization is guaranteed with ease.

The SGM61167 provides multiple configurable functions: internal LDO or external VCC bias, three switching frequency 600kHz/1100kHz/2000kHz, PSM or FCCM operating mode at light load, internal fixed or external adjustable soft-start time, internal reference or external trackable reference input, and programed current limit with R_{CS} resistor.

The device integrates comprehensive protection features to ensure reliable operation, such as output over-voltage protection (OVP), output under-voltage protection (UVP), output overshoot reducing mode (ORM), over-current protection (OCP), input under-voltage lockout (UVLO), VCC UVLO and thermal shutdown.

The SGM61167 is available in a Green TQFN-2×3-14L package.

TYPICAL APPLICATION

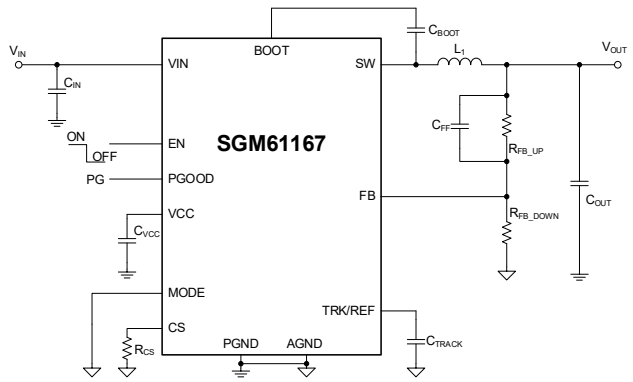


Figure 1. Typical Application Circuit

FEATURES

- **Wide Input Voltage Range:**
  - **2.7V to 16V with External 3.3V VCC Bias**
  - **4V to 16V with Internal LDO or External 3.3V VCC Bias**
- **Wide Output Adjustable Voltage Range:**
  - **0.6V to 5.5V**
- **0.5% Reference Voltage at +25℃**
- **1% Reference Voltage Over -40℃ to +150℃ Junction Temperature Range**
- **Integrated Low R_{DSON} Power FETs: 20mΩ/8mΩ**
- **Adjustable Current Limit**
- **Selectable Switching Frequency: 600kHz, 1100kHz and 2000kHz**
- **Selectable Pulse Skip Mode (PSM) and Forced Continuous Conduction Mode (FCCM)**
- **ACOT Control for Ultra-Fast Transient Response Stable with Low-ESR Output Capacitor**
- **Outstanding Load Regulation**
- **PG Open-Drain Output**
- **PG Active Low Clamping at Power Failure**
- **Support External Reference and Tracking**
- **Output Discharge Function**
- **Internal Fixed or External Adjustable Soft-Start Time**
- **Pre-Bias Startup**
- **Non-Latch Protections: OCP, Output OVP, Output UVP, VIN UVLO, VCC UVLO and Thermal Shutdown**
- **Available in a Green TQFN-2×3-14L Package**

APPLICATIONS

Sever

Telecom, Base Stations

SSD

Optical Module

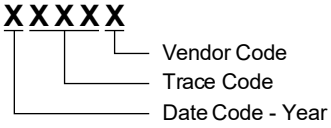
General Purpose Point-of-Load

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61167	TQFN-2×3-14L	-40℃ to +150℃	SGM61167TTUM14G/TR	2NTTUM XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{IN} 18V
$V_{SW\ (DC)}$ ..... -0.3V to 18V
$V_{SW\ (25ns)}$ (1) ..... -5V to 21V
V_{BOOT} ..... V_{SW} + 4V
V_{CC}, EN ..... -0.3V to 4.5V
V_{PGOOD} ..... -0.3V to 5.5V
All Other Pins ..... -0.3V to 4.3V
Package Thermal Resistance
TQFN-2×3-14L, θ_{JA} ..... 55.2℃/W
TQFN-2×3-14L, θ_{JB} ..... 2.4℃/W
TQFN-2×3-14L, θ_{JC} ..... 57℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:
1. When the input voltage is 16V, the rated voltage is in the range of -3.7V to 19V for a period shorter than 25ns.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 4V to 16V
$V_{SW\ (DC)}$ ..... -0.3V to (V_{IN} + 0.3V)
Output Voltage Range, V_{OUT} ..... 0.6V to 5.5V
External VCC Bias, V_{CC_EXT} ..... 3.12V to 3.6V
Maximum Output Current, I_{OUT_MAX} 6A
EN Voltage, V_{EN} 3.6V
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

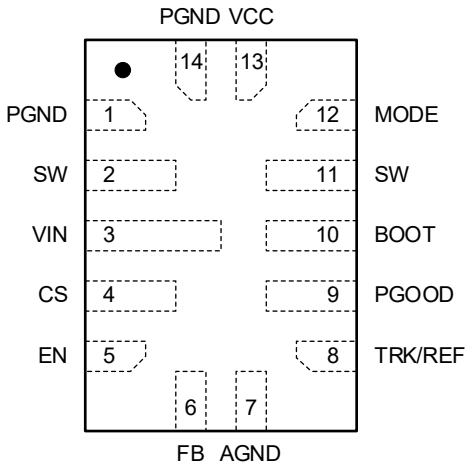
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2×3-14L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 14	PGND	P	Power Ground. System Power Ground.
2, 11	SW	P	Switching Node. Connect it to the power inductor and bootstrap capacitor.
3	VIN	P	Input Voltage. Connect a low ESR ceramic capacitor from this pin to PGND.
4	CS	AI	Current Limit Setting. Connect a resistor from this pin to AGND to set the current limit.
5	EN	AI	Enable Input. This pin is pulled low by a 6.1MΩ internally resistor. Do not leave EN floating.
6	FB	AI	Feedback of Output Voltage. Connect an external resistor divider from the output to this pin to adjust output voltage.
7	AGND	P	Analog Ground. Connect to PGND with PCB trace and avoid introducing noise from the power circuit.
8	TRK/REF	AI	External Reference and Tracking Input. This pin has two functions. Connecting an external reference to this pin can override the internal reference. Connecting a capacitor between TRK/REF and AGND can set the soft-start time.
9	PGOOD	DO	Open-Drain Power-Good Output. A pull-up resistor is needed if it is used.
10	BOOT	P	Bootstrap Supply for the High-side Gate Driver. Connect a bootstrap capacitor between SW and BOOT pins.
12	MODE	AI	Mode Selection. Connect different resistor to select FCCM or PSM operation mode, and switching frequency 600kHz, 1100kHz, or 2000kHz.
13	VCC	AO	Internal LDO Output. A recommended 2.2μF decoupling ceramic capacitor with X5R or X7R dielectrics must be placed as close to VCC pin as possible.

NOTE: AI = analog input, AO = analog output, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40℃ to +150℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN Supply Current						
Shutdown Current	I_{SD}	V_{EN} = 0V		13		μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = V_{REF} + 0.02V (no switching)		672		μA
Power MOSFETs						
High-side Leakage Current	I_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0.05		μA
Low-side Leakage Current	I_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		27		μA
High-side On-State Resistance	$R_{DS\_ON\_HS}$	V_{EN} = 2V		20		mΩ
Low-side On-State Resistance	$R_{DS\_ON\_LS}$	V_{EN} = 2V		8		mΩ
Current Limit						
Current Limit Clamp		Valley current on LS FET, 0Ω ≤ R_{CS} ≤ 3.16kΩ, T_J = +25℃	7.5	9.7	12.5	A
Current Limit Threshold	I_{OCL}	Valley current on LS FET, R_{CS} = 4.99kΩ, T_J = +25℃	4.6	6	7.4	A
		Valley current on LS FET, R_{CS} = 10kΩ, T_J = +25℃	1.8	2.9	4	A
K_{OCL} Constant for R_{CS} Equation	K_{OCL}			30000		
Negative Current Limit Threshold in ORM	I_{NOCL_ORM}			-4.3		A
Negative Current Limit Threshold in OVP	I_{NOCL_OVP}			-8.7		A
Zero-Cross Detection Current Threshold, Open Loop	I_{ZCD}	V_{IN} = 12V, V_{CC} = 3V		250		mA
Negative Current Limit Time-Out	t_{NCL_Timer}			120		ns
Timer						
Switching Frequency	f_{SW}	R_{MODE} = 60.4kΩ, I_{OUT} = 3A, V_{OUT} = 2.5V		690		kHZ
		R_{MODE} = 0Ω, I_{OUT} = 3A, V_{OUT} = 2.5V		1190		
		R_{MODE} = 30.1kΩ, I_{OUT} = 3A, V_{OUT} = 2.5V		2100		
Minimum On Time	t_{ON_MIN}			60		ns
Minimum Off Time	t_{OFF_MIN}				220	ns
Over-Voltage and Under-Voltage Protection						
Over-Voltage Threshold	V_{OVP}		113%	116%	119%	V_{REF}
Overshoot Reducing Mode Threshold	V_{ORM}		102%	105%	108%	V_{REF}
Under-Voltage Threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft-Start						
Feedback Voltage	V_{REF}	T_J = +25℃	597	600	603	mV
		T_J = 0℃ to +85℃	596.4	600	603.6	
		T_J = -40℃ to +150℃	594	600	606	
TRK/REF Sourcing Current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		15	21	μA
TRK/REF Sinking Current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 0.7V		5	7.5	μA
Soft-Start Time	t_{SS}	C_{TRACK} = 33nF		2.2		ms
Error Amplifier						
Error Amplifier Offset	V_{OS}		-4		4	mV
Feedback Current	I_{FB}	V_{FB} = V_{REF}			50	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, T_J = -40℃ to +150℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

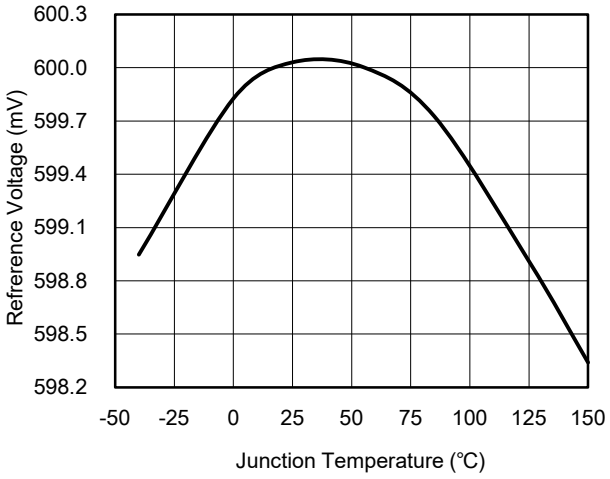
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable						
Enable Input Rising Threshold	V_{EN_IH}		1.1	1.2	1.3	V
Enable Hysteresis	V_{EN_HYS}			200		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0.32	0.6	μA
Discharge FET	R_{ON_DISCH}			85		Ω
VIN UVLO						
VIN Under-Voltage Lockout Threshold Rising	$V_{IN\_UVLO\_R}$	V_{CC} = 3.3V	2.4	2.55	2.7	V
VIN Under-Voltage Lockout Threshold Falling	$V_{IN\_UVLO\_F}$		1.85	2	2.15	V
VCC Regulator						
VCC Under-Voltage Lockout Threshold Rising	$V_{CC\_UVLO\_R}$		2.6	2.75	2.9	V
VCC Under-Voltage Lockout Threshold Falling	$V_{CC\_UVLO\_F}$		2.4	2.55	2.7	V
VCC Output Voltage	V_{CC}	I_{CC} = 5mA	2.9	3.05	3.15	V
VCC Load Regulation		Percentage change of V_{CC} with I_{CC} from 5mA to 25mA		0.2		%
Power-Good						
Power-Good High Threshold	$V_{PG\_HIGH\_R}$	FB from low to high	89%	92%	95%	V_{REF}
Power-Good Low Threshold	$V_{PG\_LOW\_R}$	FB from low to high	113%	116%	119%	V_{REF}
	$V_{PG\_LOW\_F}$	FB from high to low	77%	80%	83%	
Power-Good Low-to-High Delay	t_{PG}			1		ms
Power-Good Sink Current Capability	V_{PG}	I_{PG} = 7.5mA		0.3	0.4	V
Power-Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		1.3	2.2	μA
Power-Good Low-Level Output Voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor		780	1100	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor		900	1200	
Thermal Protection						
Thermal Shutdown (1)	T_{SD}			170		℃
Thermal Shutdown Hysteresis (1)	T_{SD_HYS}			30		℃

NOTE:

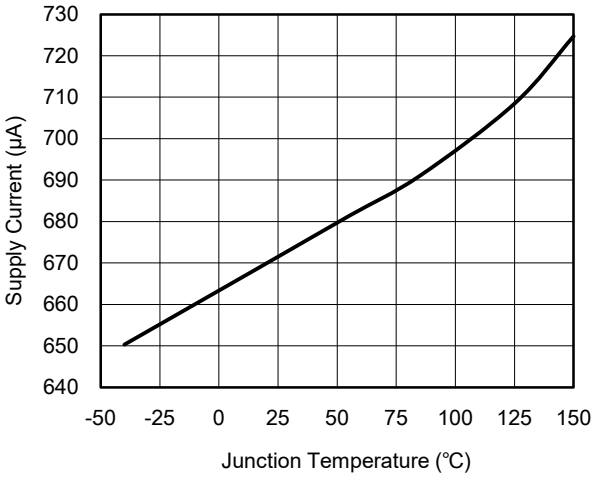
1. Guaranteed by design not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

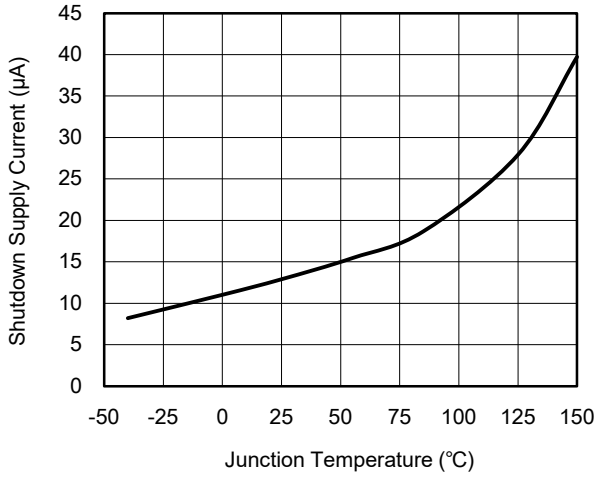
V_{REF} vs. Junction Temperature



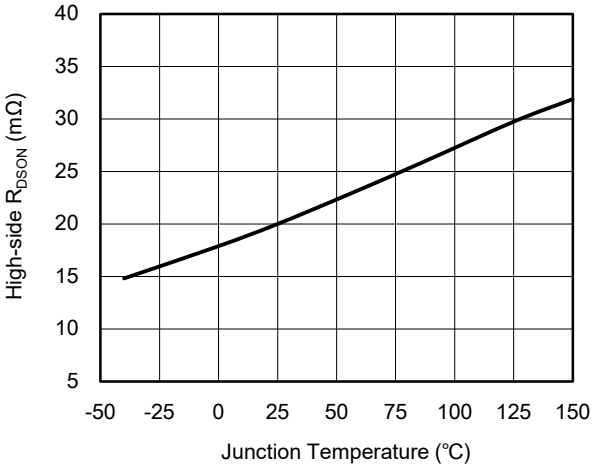
Supply Current vs. Junction Temperature



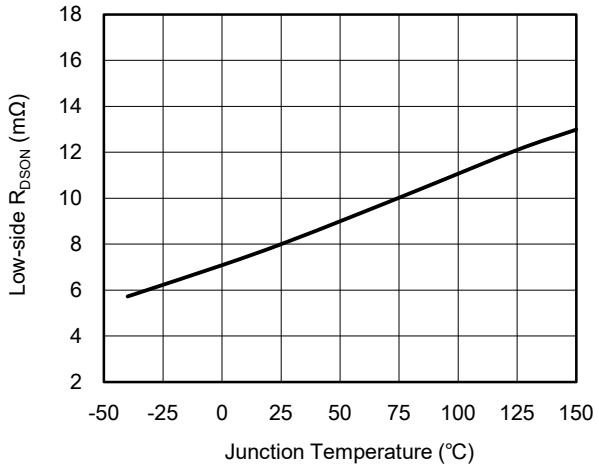
Shutdown Supply Current vs. Junction Temperature



High-side R_{DSON} vs. Junction Temperature



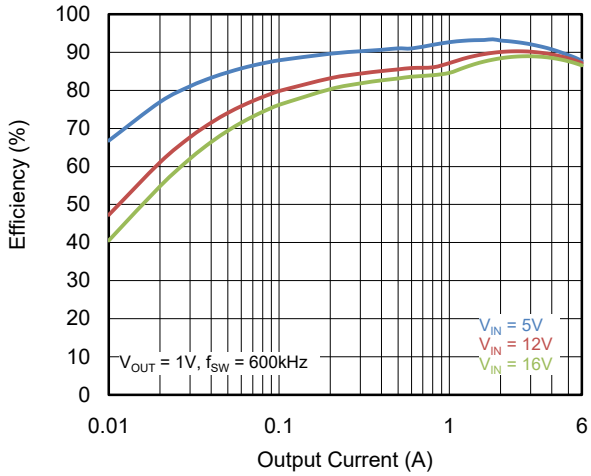
Low-side R_{DSON} vs. Junction Temperature



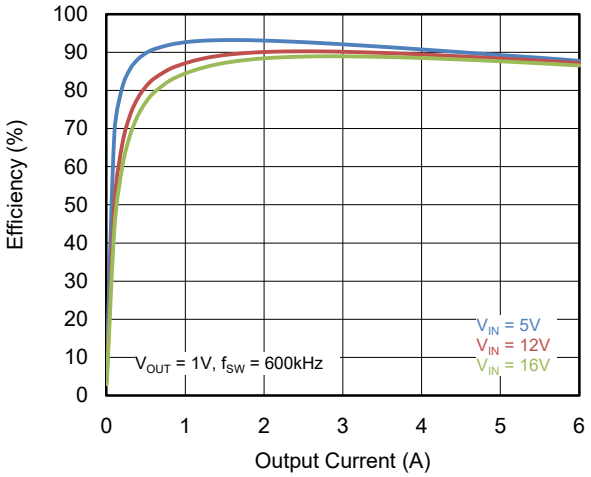
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

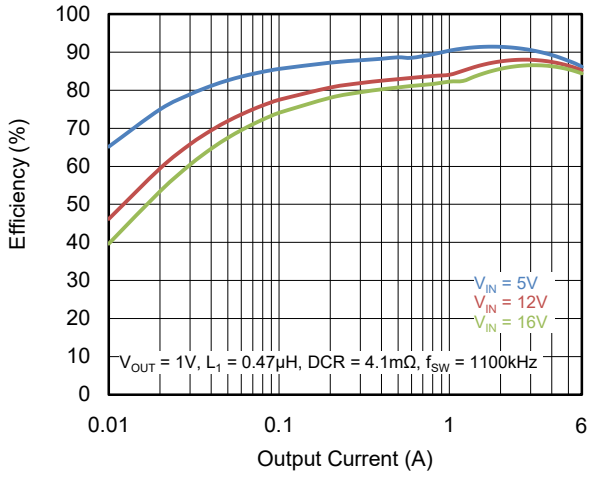
Efficiency vs. Output Current (PSM Mode)



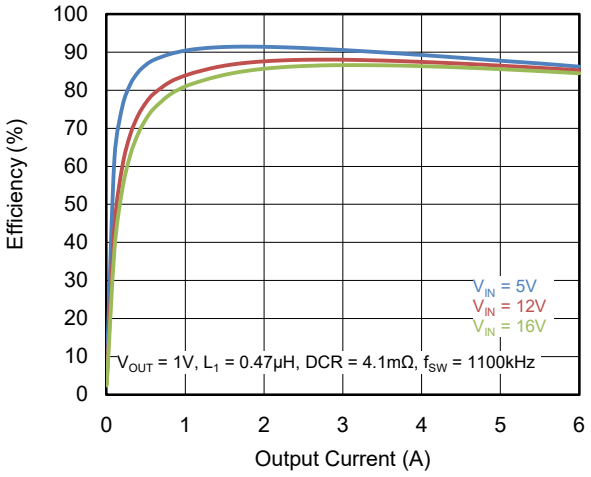
Efficiency vs. Output Current (FCCM Mode)



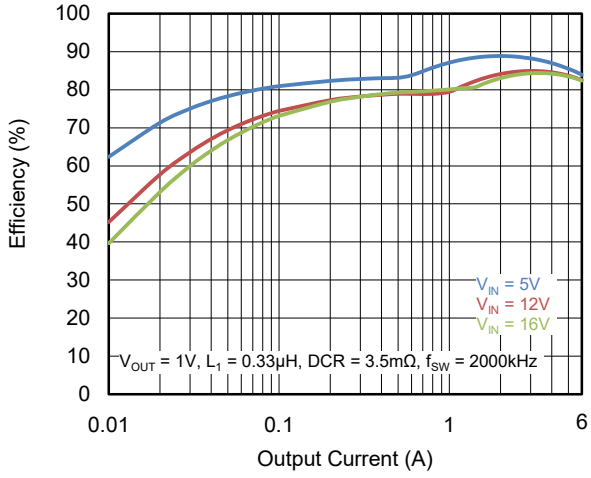
Efficiency vs. Output Current (PSM Mode)



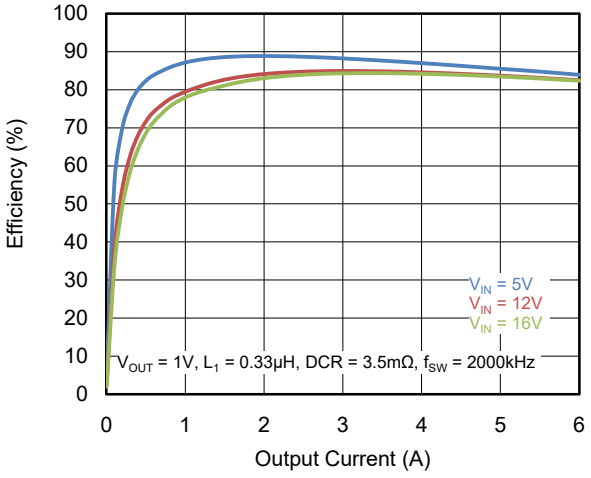
Efficiency vs. Output Current (FCCM Mode)



Efficiency vs. Output Current (PSM Mode)



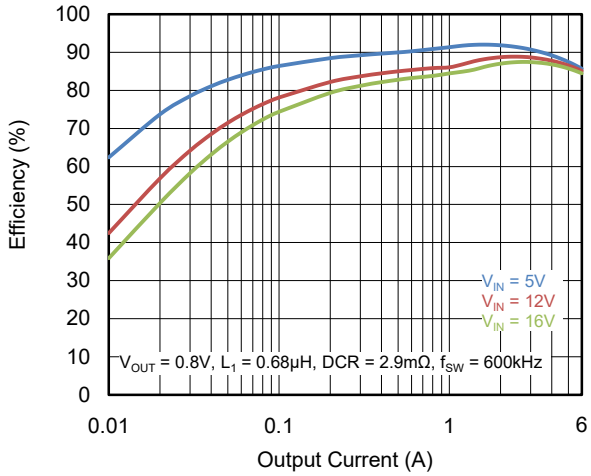
Efficiency vs. Output Current (FCCM Mode)



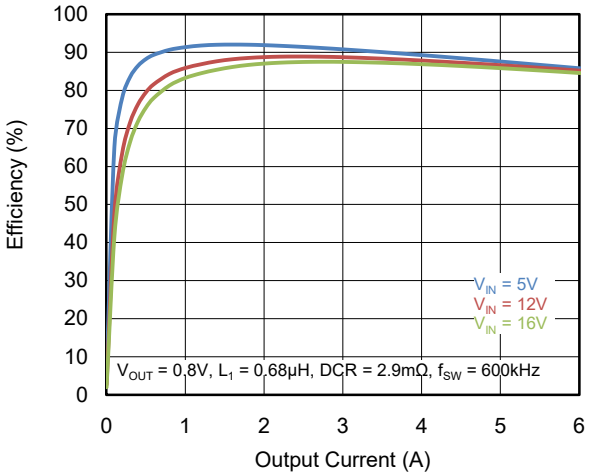
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

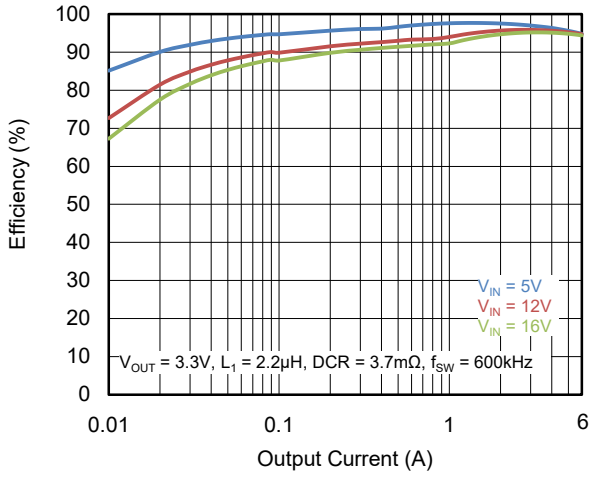
Efficiency vs. Output Current (PSM Mode)



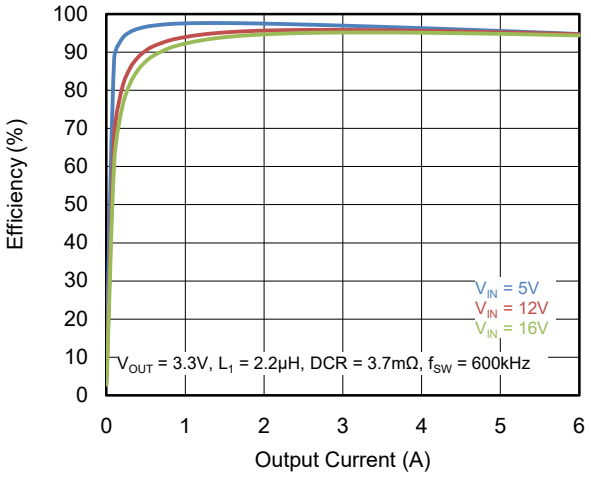
Efficiency vs. Output Current (FCCM Mode)



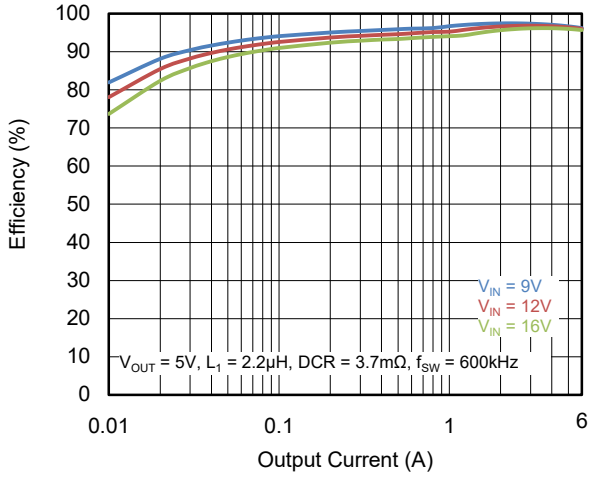
Efficiency vs. Output Current (PSM Mode)



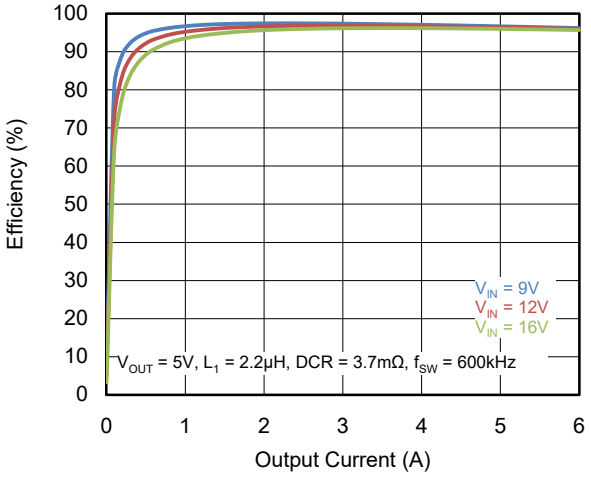
Efficiency vs. Output Current (FCCM Mode)



Efficiency vs. Output Current (PSM M Mode)



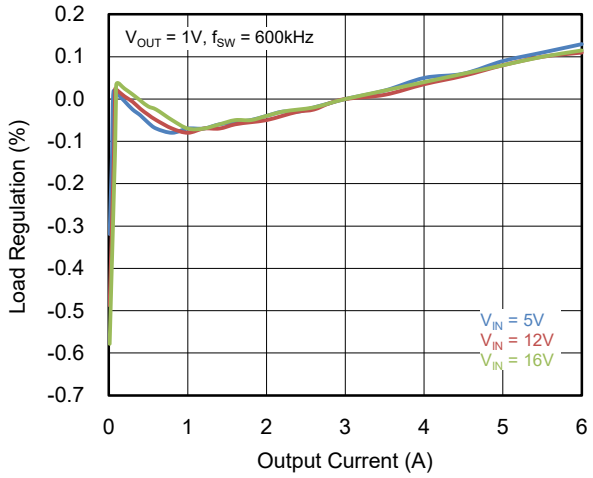
Efficiency vs. Output Current (FCCM Mode)



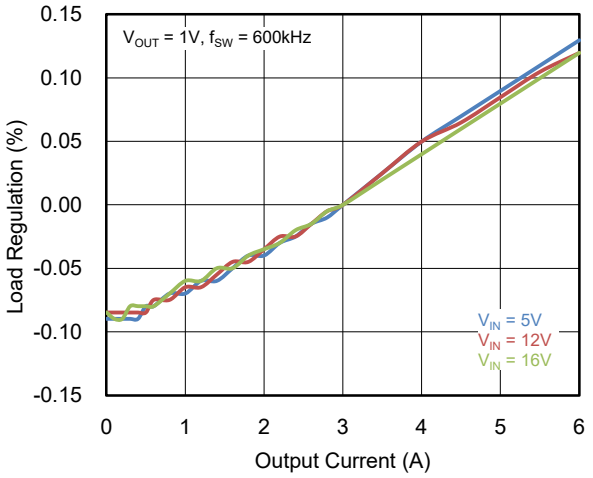
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

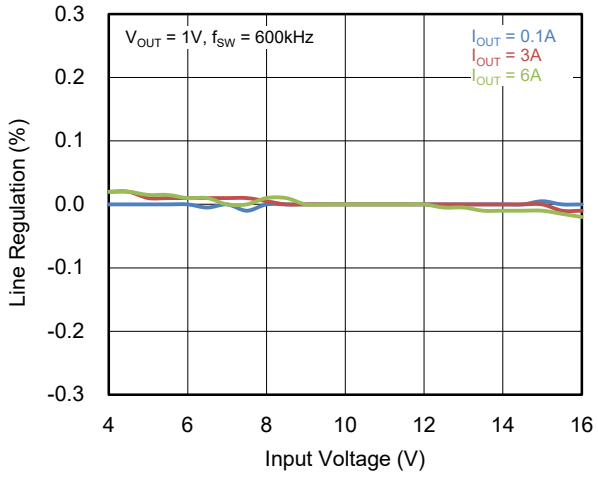
Load Regulation vs. Output Current (PSM Mode)



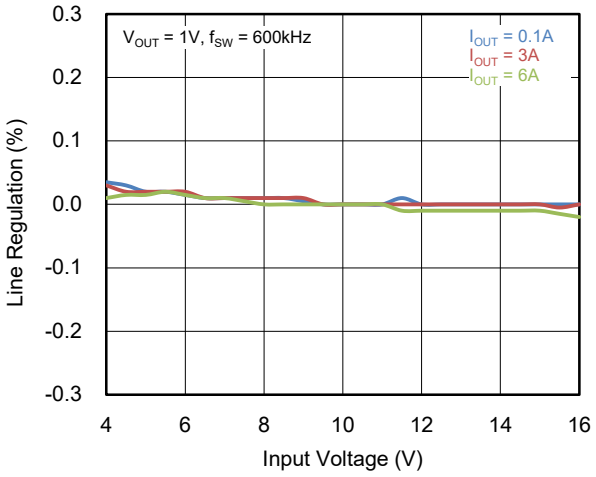
Load Regulation vs. Output Current (FCCM Mode)



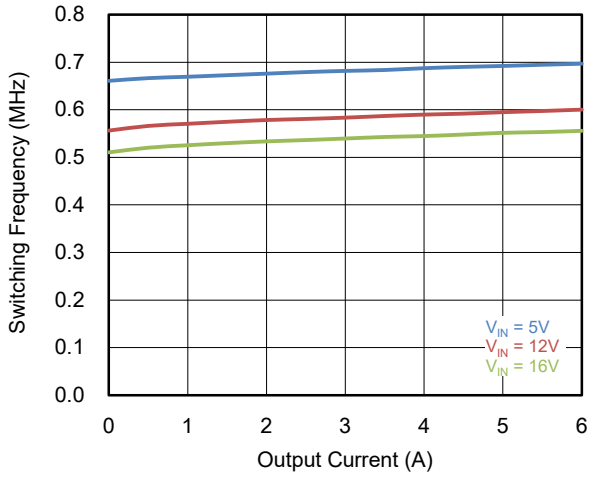
Line Regulation vs. Input Voltage (PSM Mode)



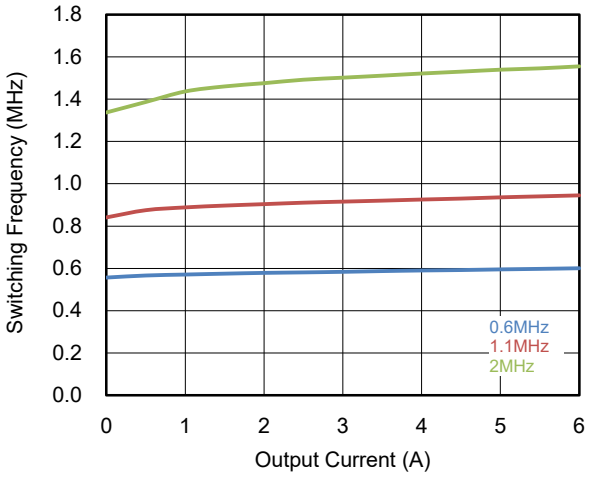
Line Regulation vs. Input Voltage (FCCM Mode)



Switching Frequency vs. Output Current (FCCM Mode)



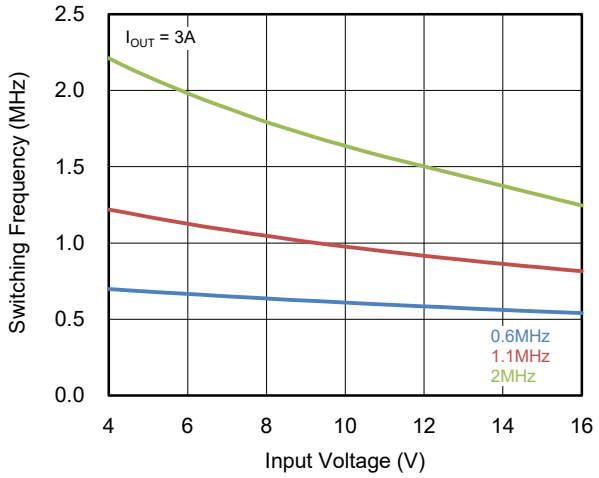
Switching Frequency vs. Output Current (FCCM Mode)



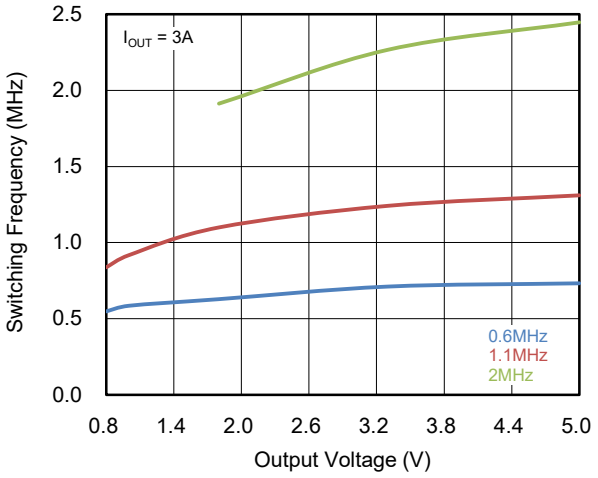
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

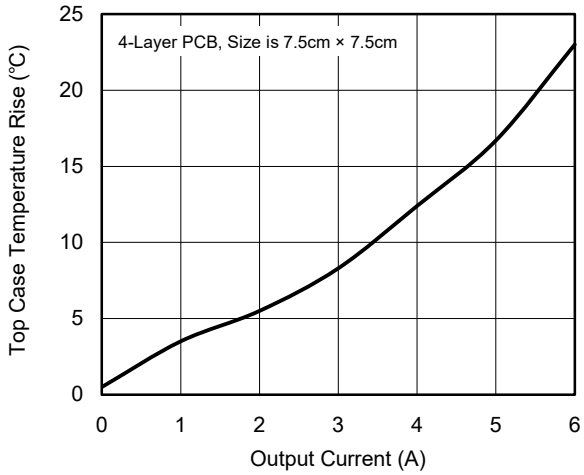
Switching Frequency vs. Input Voltage (FCCM Mode)



Switching Frequency vs. Output Voltage (FCCM Mode)



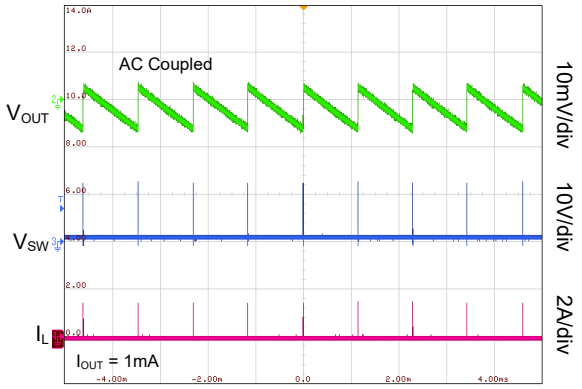
Top Case Temperature Rise vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

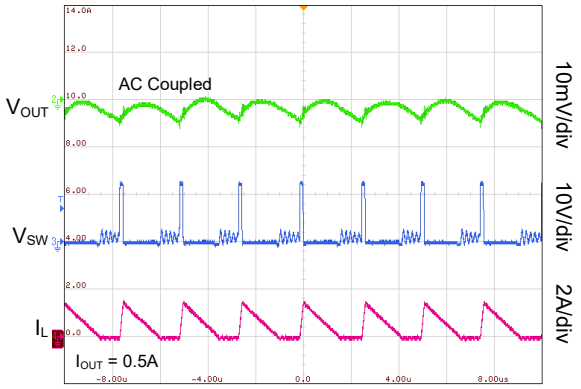
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

Output Voltage Ripple (PSM Mode)



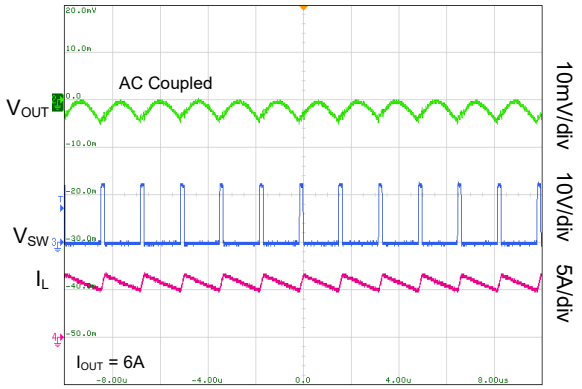
Time (1ms/div)

Output Voltage Ripple (PSM Mode)



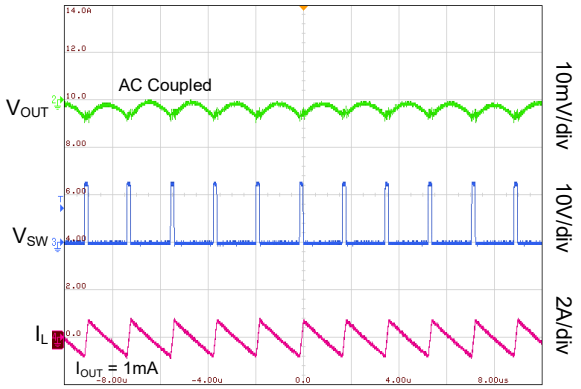
Time (2μs/div)

Output Voltage Ripple (PSM Mode)



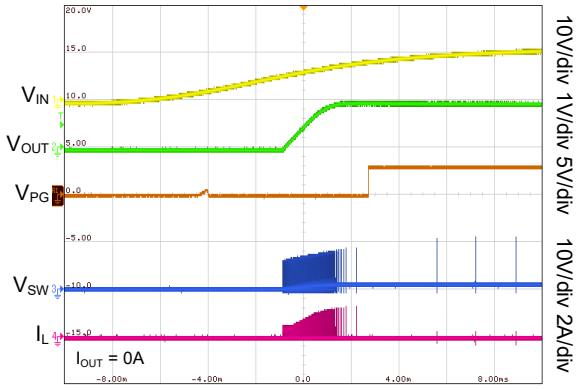
Time (2μs/div)

Output Voltage Ripple (FCCM Mode)



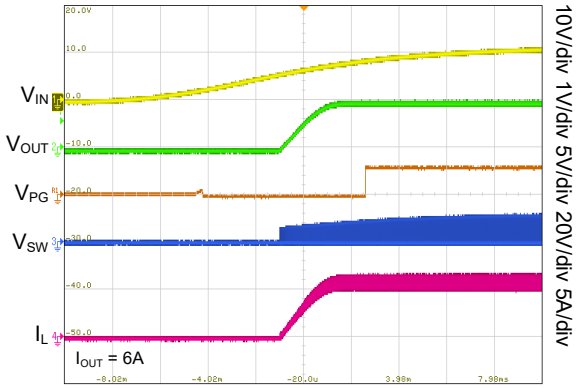
Time (2μs/div)

VIN Startup (PSM Mode)



Time (2ms/div)

VIN Startup (PSM Mode)

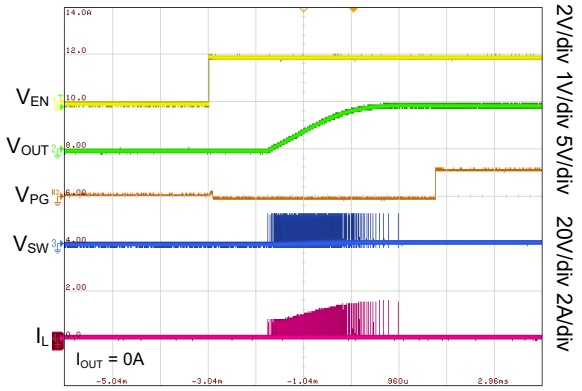


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

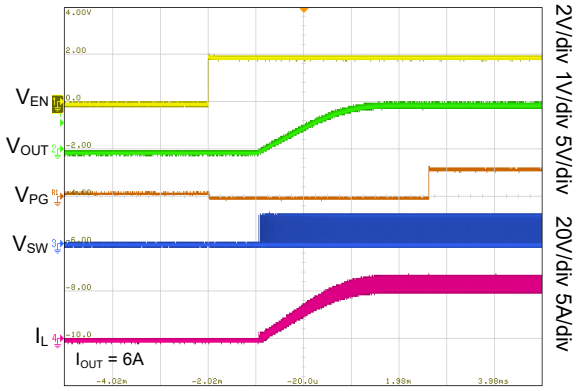
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

EN Startup (PSM Mode)



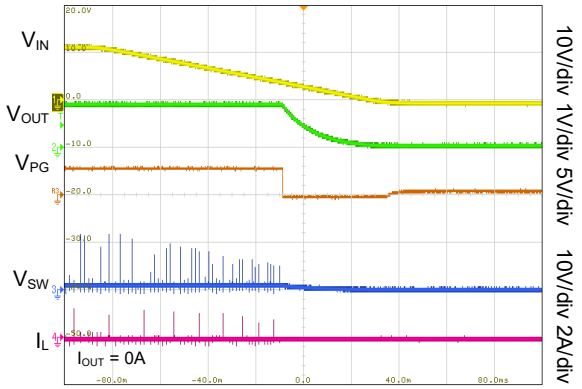
Time (1ms/div)

EN Startup (PSM Mode)



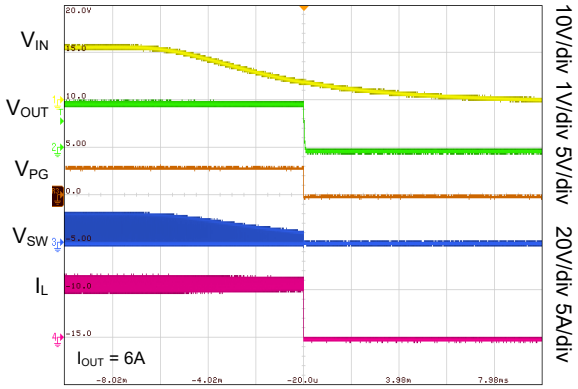
Time (1ms/div)

VIN Shutdown (PSM Mode)



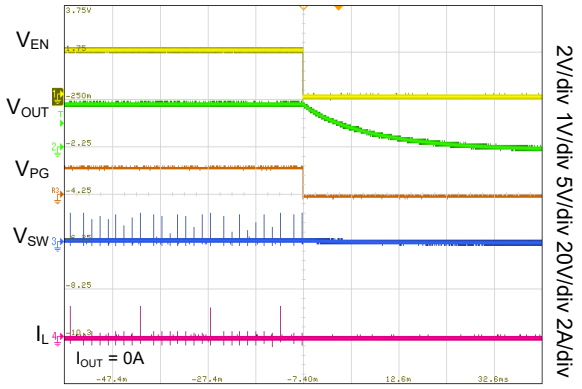
Time (20ms/div)

VIN Shutdown (PSM Mode)



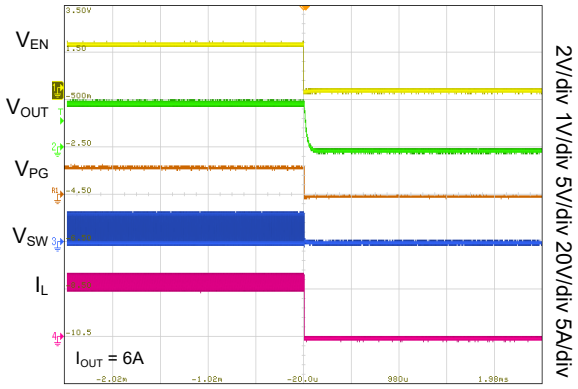
Time (2ms/div)

EN Shutdown (PSM Mode)



Time (10ms/div)

EN Shutdown (PSM Mode)

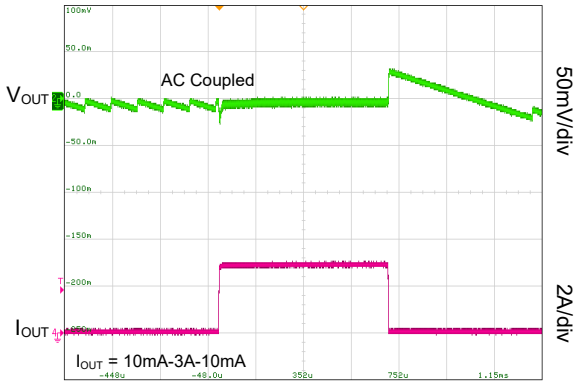


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

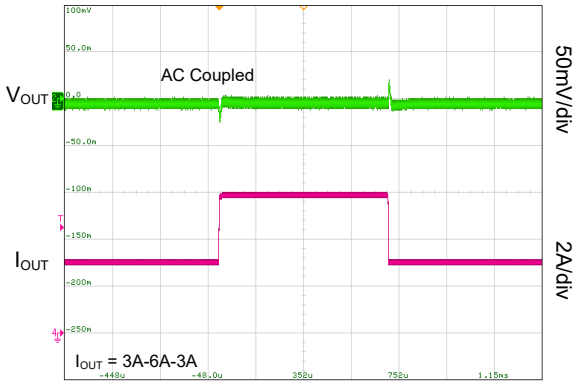
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1V, L_1 = 1μH, DCR = 4mΩ, and f_{SW} = 600kHz, unless otherwise noted.

Load Transient (PSM Mode)



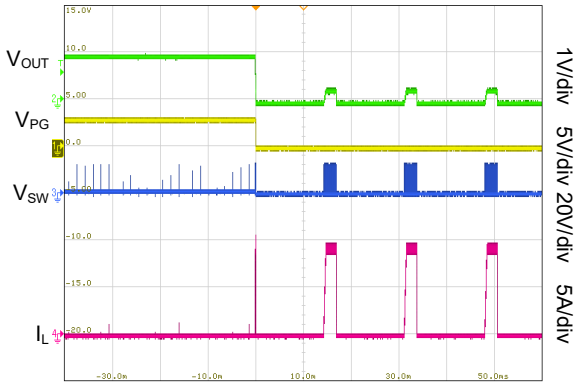
Time (200μs/div)

Load Transient (PSM Mode)



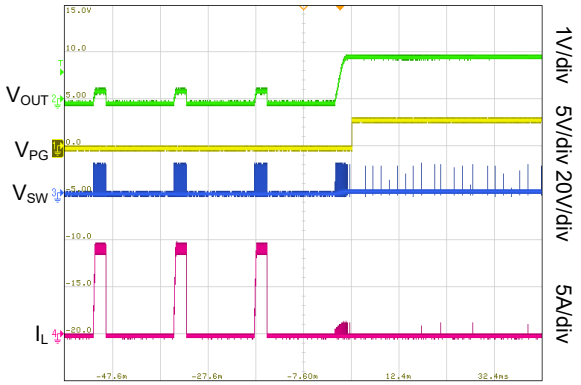
Time (200μs/div)

Short-Circuit Entry (PSM Mode)



Time (10ms/div)

Short-Circuit Recovery (PSM Mode)



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

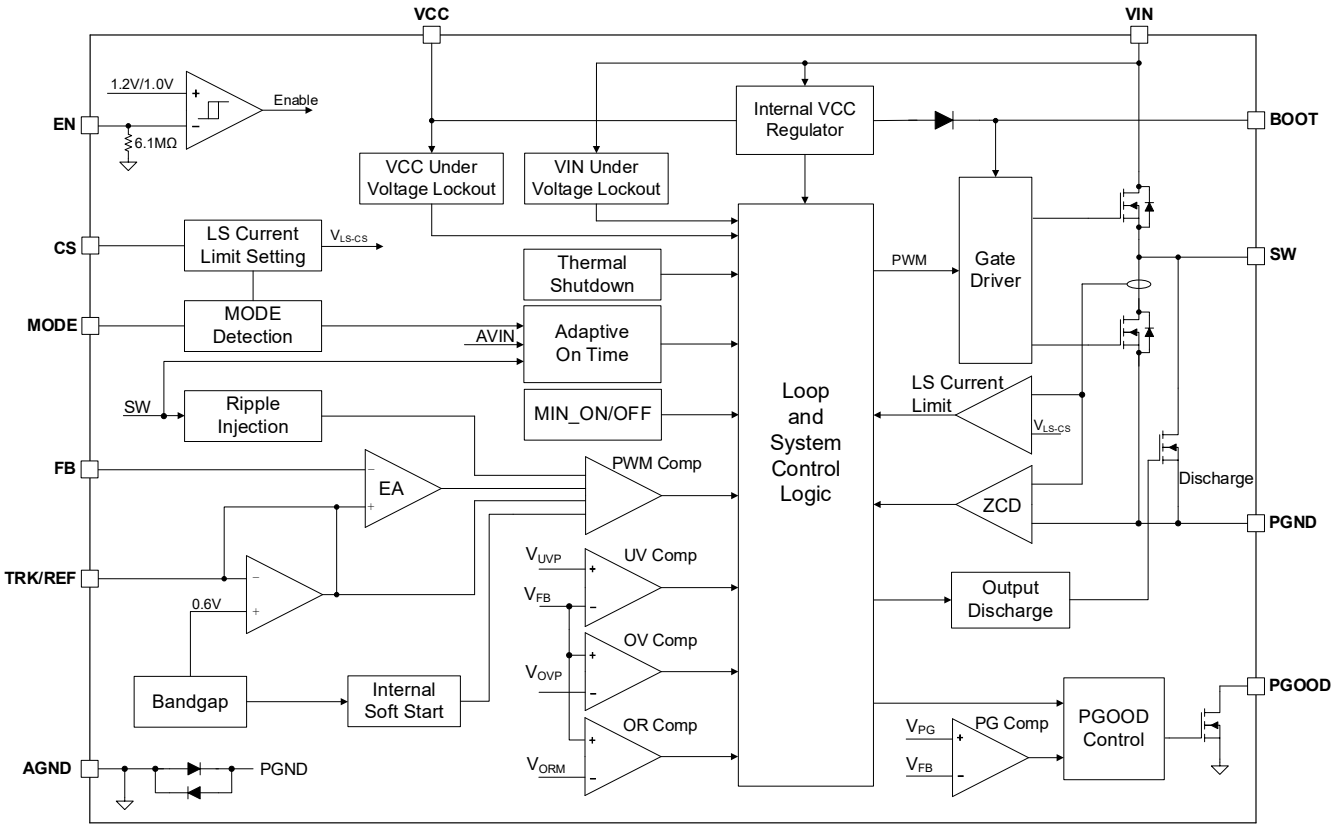


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

SGM61167 is a high-efficiency, compact synchronous Buck converter designed for point-of-load power applications requiring up to 6A output current in computing systems such as servers and storage equipment. The SGM61167 supports output voltages from 0.6V to 5.5V. The power input accepts a supply ranging from 2.7V to 16V, with the dedicated VCC bias supply operates from 3.16V to 3.6V.

The device incorporates an adaptive constant on-time control (ACOT), enabling optimal performance in low-duty-cycle applications while delivering ultra-rapid response to load transients. Internal loop compensation simplifies design implementation and reduces the number of external components. Furthermore, this control technique ensures stable operation with various low-ESR output capacitors, including ceramic and polymer types.

Internal VCC LDO and External Bias

SGM61167 integrates an internal 3.05V low-dropout regulator (LDO) powered from the VIN pin, with its output connected to VCC. When the voltage applied to the EN pin exceeds the enable threshold, the internal low-dropout regulator activates and initiates regulation of the VCC pin voltage. This VCC voltage supplies bias to the internal analog circuits and also powers the gate driver. A 2.2μF ceramic capacitor with a voltage rating of at least 6.3V must be connected to VCC for decoupling.

If an external bias voltage higher than the internal LDO output is applied, it overrides the internal LDO. This configuration improves overall power efficiency by sourcing the VCC current directly from the external bias supply rather than relying on the internal linear regulator. An under-voltage lockout (UVLO) circuit monitors the VCC voltage and shuts down the converter when the voltage level falls beneath its specified falling threshold. A well-regulated and low-noise VCC voltage is critical for ensuring reliable operation of the device. If an external VCC bias voltage is used, please pay attention to the following three points.

• Applying an external bias to the VCC pin before EN signal forces the internal LDO to remain disabled.

• When using an external VCC, the recommended startup sequence requires that the VCC UVLO rising threshold be met first, followed by satisfying the VIN UVLO rising threshold, and lastly meeting the EN rising threshold.

• (Not Recommended) If external bias voltage is supplied to the VCC pin after the EN signal becomes active, the power-up and power-down sequence may be freely implemented provided that no excessive current is drawn from the VCC pin. Note that any external discharge path connected to this pin may draw current beyond the current limit of the internal LDO, potentially causing the LDO to shut down and disable the converter output.

Enable

EN has precise rising and falling threshold values. When the voltage on the EN pin exceeds the rising threshold (TYP 1.2V) and the input voltage rises above the VIN under-voltage lockout rising threshold, the device initiates its internal startup sequence.

DETAILED DESCRIPTION (continued)

When operating with the internal VCC LDO, the startup procedure consists of three consecutive phases. In the first phase, a constant current source charges the VCC decouple capacitor. The charging period depends on the capacitance connected to the VCC pin. If the input voltage rises very gradually, the LDO output may be constrained by the input voltage, potentially extending the LDO startup interval. This extended charging period allows sufficient time for the internal reference (V_{INTREF}) to stabilize. Once the VCC voltage exceeds the VCC UVLO rising threshold, the device proceeds to the second phase, a power-on initialization. During this interval, the MODE pin configuration is read, the TRK/REF pin status is detected, and the control loop is initialized. After the initialization phase is completed, soft-start ramp begins to rise.

Figure 3 illustrates a case in which the VIN under-voltage lockout rising threshold is met before the EN rising threshold. The VCC UVLO rising threshold serves as the trigger to initiate the internal power-up sequence. The typical delay time between EN and the first switching is about 960μs. The soft start circuit is internally set with a 50mV offset to avoid uncertainty in the initial state during startup, so the first switch pulse will not be emitted until the TRK/REF voltage rises over the offset.

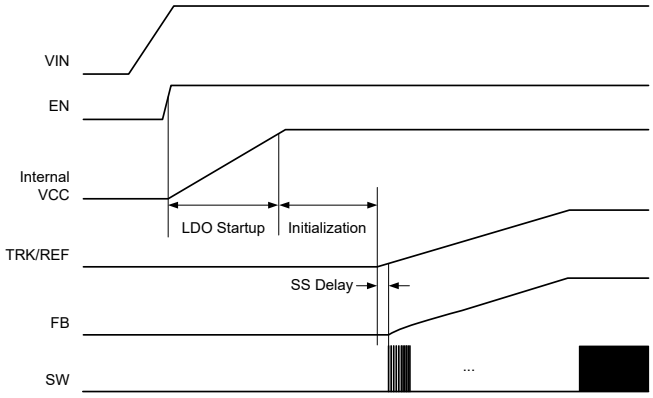


Figure 3. Power-up Sequence with Internal VCC

When operating with the external VCC bias, the startup procedure also consists of three consecutive phases. The difference from using internal LDO is that since VCC has already been established, the first period of time will be much shorter, and only used for internal V_{INTREF} build-up. The other phases are the same as that of internal LDO.

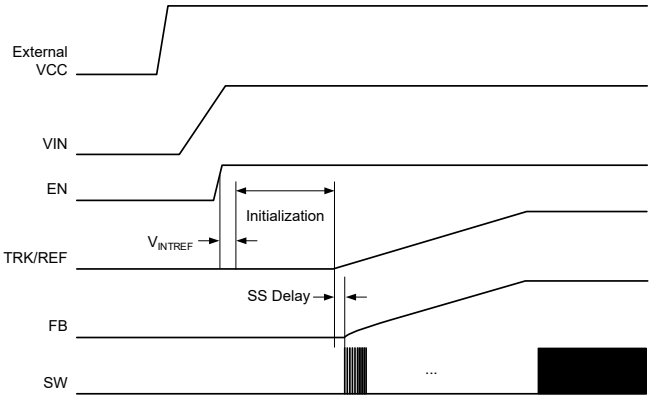


Figure 4. Power-up Sequence with External VCC

The EN pin incorporates an internal filter to prevent unintended activation or deactivation caused by minor disturbances. This RC filter has a time constant of 3μs (TYP). An internal pull-down resistor connects the EN pin to AGND. To prevent affecting the EN rising/falling thresholds, this resistor is configured at 6.1MΩ. With this pull-down implemented, leaving the EN pin floating before startup ensures the device remains disabled. However, during normal switching operation, this high-value resistor offers insufficient noise immunity to maintain a low state on the EN pin. The maximum voltage rating for the EN pin is 3.6V. Avoid direct connection between the EN and VIN pins.

Internal and External Soft-Start

The device features both an internal fixed soft-start time (TYP 2.2ms) and an externally adjustable soft-start time.

If the internal fixed 2.2ms soft-start time is used, a 33nF capacitor between the TRK/REF and AGND is required to filter the noise.

If the externally longer soft-start time is needed, connecting a larger capacitor between the TRK/REF and AGND as defined by Equation 1.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 15(\mu A)}{V_{REF}(V)} \quad (1)$$

When the FB voltage goes above V_{INTREF} - 50mV, the external soft-start is done. After both internal and external soft-start finishes, the total soft-start process of device is considered complete.

DETAILED DESCRIPTION (continued)

The TRK/REF pin is also used as the external reference input, causing the FB voltage to track this external signal precisely. When an active external reference is applied at this pin and identified by SGM61167, the internal fixed soft-start circuitry manages the output voltage ramp-up. In this case, the capacitance between TRK/REF and AGND is not limited, and larger capacitor can be used to obtain a more stable and lower noisy reference voltage.

External Reference and Tracking

The SGM61167 features an analog input (TRK/REF) that accepts an external DC voltage reference. The control loop continuously uses the voltage present on the TRK/REF pin as its reference signal. When an external reference is connected between the TRK/REF and AGND pins, the feedback voltage precisely tracks this external reference.

Before the internal soft-start process, monitoring circuitry checks the TRK/REF pin voltage to determine whether a valid DC source is present. Firstly, the TRK/REF pin is discharged to AGND by an internal 120Ω resistor. Subsequently, the pin voltage is compared to 89% (TYP) of the internal V_{INTREF} value. This discharge sequence prevents misinterpretation of residual energy in an SS capacitor as an external voltage reference.

If the external voltage reference is unable to deliver adequate current to maintain a level above 89% of V_{INTREF} (indicating no external reference), the device defaults to the internal fixed V_{INTREF} for setting the PG, OVP, and UVP thresholds. In this case, the soft-start time is determined with the capacitance between TRK/REF and AGND, which is detailed at soft start description.

If the detected voltage remains above 89% of V_{INTREF} (indicating an active external DC reference), the TRK/REF voltage is used as the reference instead of V_{INTREF}. In this case, the startup process is managed by the internal fixed 2.2ms soft-start circuitry. It is recommended to apply a stable DC reference to the TRK/REF pin before the EN signal is driven high. During the internal power-on delay period, the external reference must maintain the TRK/REF pin voltage at or above 89% of V_{INTREF} to ensure proper detection.

After soft-start, the external reference voltage can be configured within the 0.5V to 1.2V range. During normal operation, the external reference must sink over 15μA if its voltage is below the internal V_{INTREF} level, or supply more than 4.5μA if its voltage exceeds the internal V_{INTREF}. The slew rate of an external voltage source must not exceed 1mV/μs when ramping between different voltage levels.

Power-Good

The power-good indicator is implemented with an open-drain structure with a maximum sinking capacity of 7.5mA, and requires an external pull-up resistor (TYP 30kΩ) connected to either the VCC rail or an external supply not exceeding 4V. If PG function is not used, connect the pin to AGND or keep it floating.

After the total soft-start is completed, PG becomes high impedance state if output voltage is in regulated window and no EN shutdown, UVLO, thermal shutdown events occurs. PG is driven low once FB voltage falls below typically 80% of the reference voltage, or FB voltage goes higher than 116% of the reference voltage.

If the VCC supply is unable to power the device, for instance VCC remain at 0V, an internal low clamping circuit can ensure the PG staying at low state even with external pull-up resistor and pull-up power rail in place.

Output Voltage Setting

The output voltage of the device can be adjusted by resistors R_{FB_UP} and R_{FB_DOWN} which are connected to the FB pin. Use resistors with 1% tolerance or better for good output accuracy. Equation 2 can be used to calculate the R_{FB_UP} and R_{FB_DOWN} values based on the desired output voltage (V_{OUT}) and V_{REF}. Do not choose too large resistors that may cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

$$R_{FB\_DOWN}(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{FB\_UP}(k\Omega) \quad (2)$$

DETAILED DESCRIPTION (continued)

Mode Selection

The SGM61167 supports two operation mode: pulse skip mode (PSM) and forced continuous conduction mode (FCCM) under light load conditions. The device also provides three switching frequency: 600kHz, 1100kHz and 2000kHz. Configuration of the switching frequency and operational mode is accomplished by placing a resistor between the MODE pin and AGND. The combination is dictated by the resistance value applied, as detailed in Table 1. It is advised to utilize resistors with a ±1% tolerance.

Table 1. MODE Pin Selection

Mode Pin Connections	Operation Mode Under Light Load	Switching Frequency (f_{SW}) (kHz)(1)
Short to VCC or Floating	PSM	1100
243kΩ ± 10% to AGND		2000
121kΩ ± 10% to AGND		600
60.4kΩ ±10% to AGND	FCCM	600
30.1kΩ ±10% to AGND		2000
Short to AGND		1100

NOTE: 1. The operating frequency is specified with a 2.5V output. Actual frequency becomes dependent on the output voltage setting.

The operational configuration is established and stored internally throughout the power-up initialization sequence. Subsequent modifications to the MODE resistance value following this initialization phase will not alter the converter's configured behavior. If MODE remains unconnected during the critical power-on interval, the internal logic will default to a 1100kHz switching frequency with PSM operation.

For reliable recognition of the intended configuration, avoid adding any capacitive elements at the MODE pin.

Pulse Skip Mode

If PSM mode is selected, the device can move to discontinuous conduction mode (DCM) at light load. A zero-crossing detection circuit works during PSM to determine the inductor current zero point. By setting a positive zero-crossing threshold, the device prevents negative inductor current flow. The conduction time (t_{ON}) is approximately the same as that of CCM, therefore, the switching frequency will gradually decrease as the load decreases. This design approach enhances efficiency under light-load conditions.

Forced Continuous Conduction Mode

If FCCM mode is selected, the device operates at a fixed frequency across all load conditions, making it suitable for applications requiring a stable switching frequency at the cost of reduced light-load efficiency.

DETAILED DESCRIPTION (continued)

Positive Over-Current Protection and Current Limit Setting

The SGM61167 employs cycle-by-cycle valley current detection to implement over-current protection. During the low-side FET conduction interval, the current of low-side FET is monitored. If the sensed current exceeds the setting limit, the low-side FET remains conducting until the current drops below the limit threshold. This mechanism reduces the average current delivered to the output. Under output over-current conditions, the load demand surpasses the current supplied to the output capacitors, resulting in a decreasing output voltage. When the FB voltage drops below the UVP threshold (TYP 80% of V_{REF}), and lasts for 64μs. The device subsequently stops switching and enters a 14ms (TYP) hiccup mode before attempting to restart.

During startup, if an over-current condition is detected, the device continues to enforce cycle-by-cycle current limit based on the low-side valley current setting. After soft-start completion, an under-voltage event triggered by the over-current condition will stop switching and enter hiccup mode.

The current limit threshold is set by a resistor (R_{CS}) connected between the CS pin and AGND. Resistors with ±1% tolerance should be used, as resistors with wider tolerance may significantly reduce the accuracy of the over-current limit setting. Equation 3 calculates the R_{CS} value for a desired over-current limit threshold. To simplify calculations, a constant term K_{OCL} may be used in place of the numerical factor 3×10^4 (TYP). Equation 4 determines the relationship between the over-current threshold and the R_{CS}. The tolerance of K_{OCL}, specified in Electrical Characteristics, facilitates analysis of the overall variation in the current limit threshold.

An integrated fixed maximum over-current clamp circuit safeguards the device against fault conditions on the CS pin, such as too small R_{CS} resistance or an accidental short to ground.

$$R_{CS}=\frac{3\times10^4}{I_{OCLIM}-\frac{1}{2}\times\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}}\times\frac{1}{L\times f_{SW}}}=\frac{K_{OCL}}{I_{OCLIM}-\frac{1}{2}\times\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}}\times\frac{1}{L\times f_{SW}}} \quad (3)$$

$$I_{OCLIM}=\frac{K_{OCL}}{R_{TRIP}}+\frac{1}{2}\times\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}}\times\frac{1}{L\times f_{SW}} \quad (4)$$

where:

I_{OCLIM} is over-current limit threshold for load current in A
R_{CS} is TRIP resistor value in Ω
K_{OCL} is a constant for the calculation
V_{IN} is input voltage value in V
V_{OUT} is output voltage value in V
L is output inductor value in μH
f_{SW} is switching frequency in MHz

Negative Current Limit

The device also incorporates a negative cycle-by-cycle current limit. Mirroring the approach used for positive over-current limit, the inductor current is observed throughout the low-side FET's conduction period. To prevent excessive negative current through the low-side FET, the device turns it off when a current of -8.7A (TYP) is detected. The high-side FET is then turned on for a fixed 120ns (TYP) interval. Once this on time expires, the low-side FET is enabled again. Once this on-time expires, the low-side FET is enabled again.

Under normal operating conditions, the -8.7A negative current limit should not be triggered. This negative current protection is primarily used to discharge the output capacitor during output OVP.

DETAILED DESCRIPTION (continued)

Output Over-Voltage and Under-Voltage Protection

The device continuously checks the feedback voltage to identify over-voltage and under-voltage conditions. If the FB voltage falls below 80% of the V_{REF}, the output UVP comparator triggers and initiates an internal timer. Once the 64μs (TYP) UVP timer ends, the system enters hiccup mode and initiates a restart following a 14ms (TYP) interval. Note that UVP protection is only active after the soft-start phase has completed.

During the 64μs UVP timer period, if the output voltage rises above the UV threshold and therefore no longer meets the criteria for a UV event, the timer will be reset.

When the FB voltage exceeds 116% (TYP) of the V_{REF} level, the output OVP comparator triggers, causing the circuit to turn off the high-side MOSFET and turn on the low-side MOSFET until the negative current limit threshold (I_{NOCL_OVP}) is reached. Once this current threshold is detected, the low-side FET is turned off and the high-side FET is turned on for a fixed time of 120ns. The converter continues operating in this state until the FB voltage falls below 105% (TYP) of the V_{REF}.

Overshoot Reducing Mode

The device supports an overshoot reducing mode (ORM) to protect the output load, which serves as an early non-latch over-voltage protection. When the output voltage is greater than 105% of the reference voltage and OVP is not triggered, it enters ORM. The low-side FET is turned on until the negative current limit is triggered (TYP -4.3A). Then the low-side FET is turned off and the high-side FET is turned on for a fixed time of 120ns. This rapidly discharge of the output capacitor helps V_{OUT} quickly return to its target value.

The converter operates in this state repeatedly until the FB voltage falls below 102% (TYP) of the V_{REF} level.

Output Voltage Discharge

When the device is disabled via the EN pin, it enters an output discharge state. In this mode, both the high-side and low-side FETs are maintained off, while a dedicated discharge FET (connected between SW and PGND) is turned on to dissipate output energy. The discharge FET turns off once the FB voltage falls below 100mV (TYP).

This discharge mode can be triggered by any of the following fault conditions:

- EN Shutdown
- OTP
- VIN UVLO
- VCC UVLO

Thermal Shutdown

When the junction temperature exceeds the trigger point (TYP 170℃), the device stops switching and discharge the TRK/REF pin. Once the junction temperature cools by approximately 30℃ below the threshold, the device automatically restarts and initiates a new soft-start sequence. This thermal shutdown feature operates as a non-latching protection mechanism.

APPLICATION INFORMATION

In this section, power supply design with the SGM61167 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

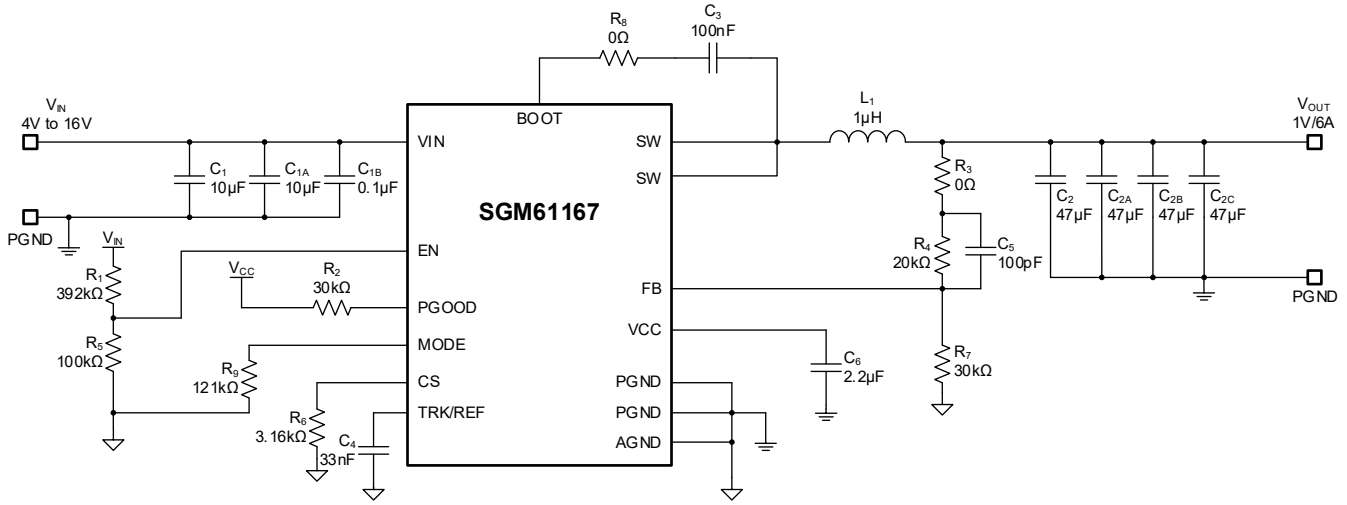


Figure 4. Application Circuit

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 4. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	4V to 16V
Output Voltage	1V
Maximum Output Current	6A
Switching Frequency	600kHz

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1, C_{1A}	Ceramic Capacitor, 10μF, 25V, X5R, Size 1206	Standard
C_{1B}, C_3	Ceramic Capacitor, 0.1μF, 25V, X7R, Size 0603	Standard
C_2-C_{2c}	Ceramic Capacitor, 47μF, 6.3V, X5R, Size 0805	Standard
C_4	Ceramic Capacitor, 33nF, 10V, X7R, Size 0603	Standard
C_5	Ceramic Capacitor,100pF, 50V,C0G , Size 0603	Standard
C_6	Ceramic Capacitor, 2.2μF, 10V, X7R, Size 0603	Standard
L_1	1μH, Power Inductor, DCR_{TYP} = 4mΩ, I_{SAT_TYP} = 23A, I_{RMS_TYP} = 20A P/N: MWFC0605S-1R0MT	Sunlord
R_1	392kΩ, Chip Resistor, 1%, Size 0603	Standard
R_2	30kΩ, Chip Resistor, 1%, Size 0603	Standard
R_3, R_8	0Ω, Chip Resistor, 1%, Size 0603	Standard
R_4	20kΩ, Chip Resistor, 1%, Size 0603	Standard
R_5	100kΩ, Chip Resistor, 1%, Size 0603	Standard
R_6	3.16kΩ, Chip Resistor, 1%, Size 0603	Standard
R_7	30kΩ, Chip Resistor, 1%, Size 0603	Standard
R_9	121kΩ, Chip Resistor, 1%, Size 0603	Standard

Table 4. SGM61167 Suggested Component Selections

V_{OUT}	R_{FB_UP}	R_{FB_DOWN}	L_1	Effective C_{OUT}	Normal C_{OUT} (1)	C_{FF}	Frequency Set
0.6V	0Ω	-	0.68μH	270.9μF	7×47μF	-	600kHz
1V	20kΩ	30kΩ	1μH	148μF	4×47μF	100pF	600kHz
	20kΩ	30kΩ	0.47μH	148μF	4×47μF	100pF	1100kHz
1.8V	20kΩ	10kΩ	1μH	96.9μF	3×47μF	100pF	600kHz
	20kΩ	10kΩ	0.68μH	96.9μF	3×47μF	100pF	1100kHz
	20kΩ	10kΩ	0.33μH	96.9μF	3×47μF	330pF	2000kHz
2.5V	20kΩ	6.34kΩ	1.5μH	82.5μF	3×47μF	330pF	600kHz
	20kΩ	6.34kΩ	0.82μH	82.5μF	3×47μF	330pF	1100kHz
	20kΩ	6.34kΩ	0.47μH	82.5μF	3×47μF	330pF	2000kHz
3.3V	16.2kΩ	3.6kΩ	2.2μH	45.6μF	3×47μF	270pF	600kHz
	16.2kΩ	3.6kΩ	1μH	45.6μF	3×47μF	150pF	1100kHz
	16.2kΩ	3.6kΩ	0.68μH	45.6μF	3×47μF	220pF	2000kHz
5V	20kΩ	2.7kΩ	2.2μH	31μF	2×47μF	220pF	600kHz
	20kΩ	2.7kΩ	1.5μH	31μF	2×47μF	150pF	1100kHz
	20kΩ	2.7kΩ	0.68μH	31μF	2×47μF	220pF	2000kHz

NOTE: 1. Ceramic Capacitor, 47μF, 6.3V, X5R, Size 0805, GRM21BR60J476ME11.

APPLICATION INFORMATION (continued)

Input Capacitor Selection

Use ceramic capacitors (X5R, or X7R) for decoupling between the VIN and PGND pins. These capacitors must be placed as close as possible to the device. For typical applications, it is recommended to use 10μF × 2 ceramic capacitors. Applications with long input traces may need additional input bulk capacitance. For high-frequency noise suppression, 0.1μF capacitors must be positioned directly adjacent to critical VIN pin and PGND pin on the same board layer as the device. The capacitor's voltage rating must exceed the maximum input voltage and leave enough margin. The total ripple current rating of capacitors must exceed the calculated maximum RMS capacitor current, derived from the regulator's operating parameters (e.g., duty cycle, load current), which can be calculated by Equation 5. Ceramic capacitance decreases under DC bias. The input ripple voltage depends on the input capacitance, switching frequency, and duty cycle. Worst-case ripple occurs near 50% duty cycle. It can be calculated by Equation 6.

$$I_{C\_RMS} = I_{OUT\_MAX} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \quad (5)$$

where:

I_{C_RMS} is the maximum RMS current of capacitor.

I_{OUT_MAX} is the maximum output DC current.

V_{IN_MIN} is minimum input voltage.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times f_{SW}} \quad (6)$$

where:

ΔV_{IN} is the input ripple voltage peak-to-peak.

I_{OUT_MAX} is the maximum output DC current.

C_{IN} is the effective input capacitance value (μF).

f_{SW} is switching frequency (MHz).

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 7 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (7)$$

where:

I_{OUT_MAX} is the maximum output DC current

ΔI_L is the inductor current ripple (peak-to-peak)

f_{SW} is switching frequency (MHz)

L is the inductance value (μH)

Output Capacitor Selection

The architecture of the SGM61167 allows use of ceramic-type output capacitors with low equivalent series resistance (ESR). To keep the capacitance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X5R or X7R dielectric. The bias voltage can cause the capacitance of the ceramic capacitor to decrease significantly, and the degree of decrease depends on the specification of the capacitor (size, nominal voltage, temperature standard). The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

Steady-state output ripple voltage depends on inductor current ripple and capacitor impedance. The minimum capacitance requirement is:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right) \quad (8)$$

where:

ΔV_{OUT} is the output ripple voltage (peak-to-peak).

L is the inductance value (μH).

f_{SW} is switching frequency (MHz).

R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

C_{OUT} is the output capacitance value (μF).

If the switching frequency is seriously reduced due to the decrease of the input voltage, it is recommended to increase the output capacitance to ensure system stability.

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 9 for selecting the feedback resistors (R_4 and R_7) in Figure 4 to set the desired output voltage (V_{OUT}):

$$V_{OUT} = V_{REF} \times (1 + \frac{R_4}{R_7}) \quad (9)$$

To avoid high noise sensitivity on the FB pin, the resistance value of R_7 is recommended not to exceed 200kΩ. The smaller the R_7 resistance value is, the stronger the anti-noise ability will be, but at the same time, the loss on the voltage divider will also be greater.

Bootstrap Capacitor

To maintain stable switching behavior, implement a 100nF ceramic capacitor across the BOOT-SW pins, prioritizing components with minimal DC voltage dependency.

Controlled MOSFET activation and transient suppression can be achieved by inserting a current-limiting resistor in the bootstrap path. While this configuration tempers switching-edge overshoot, it introduces measurable efficiency degradation due to increased switching losses. Prototype designs should integrate a default short-circuit (0Ω) path for bootstrap circuits, allowing subsequent impedance adjustment if PCB-induced parasitic effects amplify switching spikes beyond component tolerances.

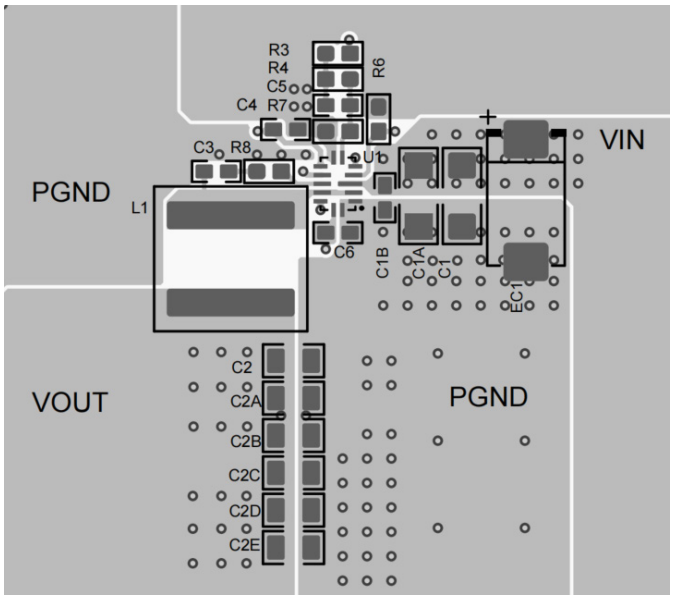
Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61187.

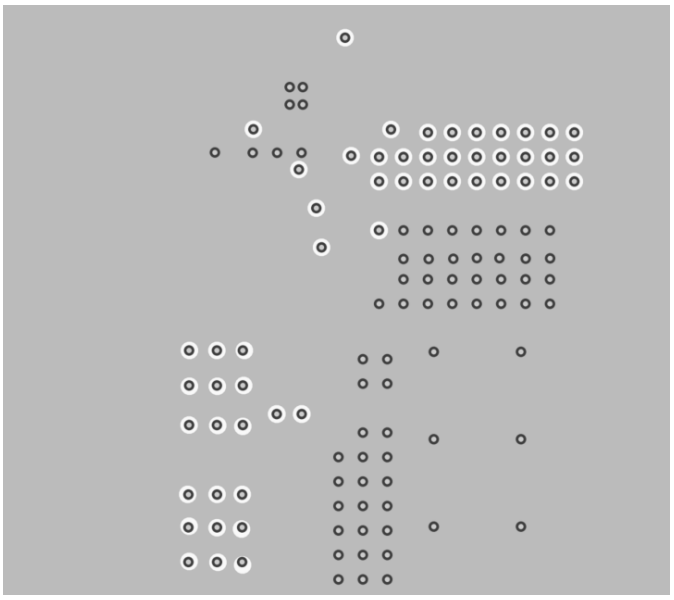
- Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- For better thermal performance, the VIN and PGND networks should be arranged in at least two layers.
- To achieve the best power integrity, place the 100nF low ESR decoupling capacitor as close as possible to the VIN-PGND pins. Place the remaining input capacitors closer to them. It is not recommended to place the remaining input capacitors on another layer of PCB. If such a situation occurs, it is suggested to use sufficient vias near them to reduce the impedance between them and the IC.
- Place the inductor as close as possible to SW pin to reduce the length of the SW node route.
- Connect the ground returns of the input and output capacitors close to the PGND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.
- Place the output voltage divider near the FB pin and on the same layer as the IC.
- Use as many vias as possible near the PGND pin to connect the PGND copper-clad networks of each layer directly beneath the chip together to facilitate noise reduction and heat dissipation.
- The AGND pin must be connected to the PGND network only through a few relatively concentrated vias. These vias cannot be too far from the AGND pin.
- Place the BOOT-SW capacitor as close as possible to the BOOT (pin 10) and SW (pin 2/pin11).
- The lower resistor of EN, the CS resistor, and the MODE resistor need to be connected with AGND island.

Refer to Figure 5 for a recommended PCB layout.

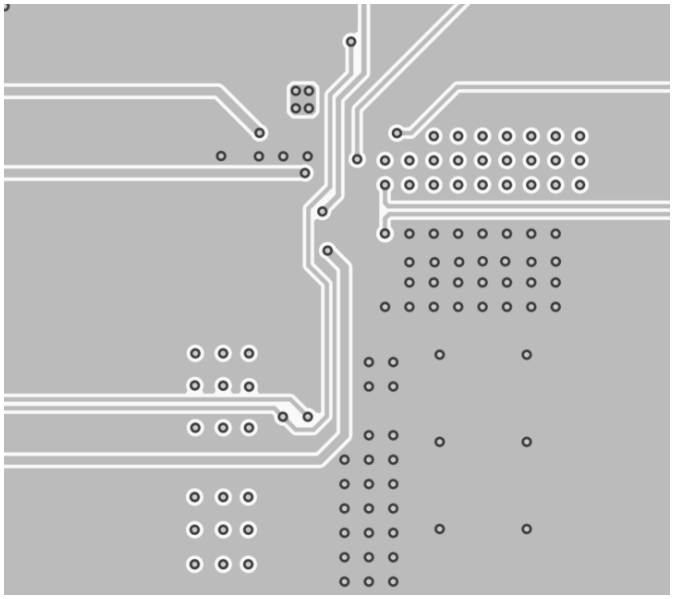
APPLICATION INFORMATION (continued)



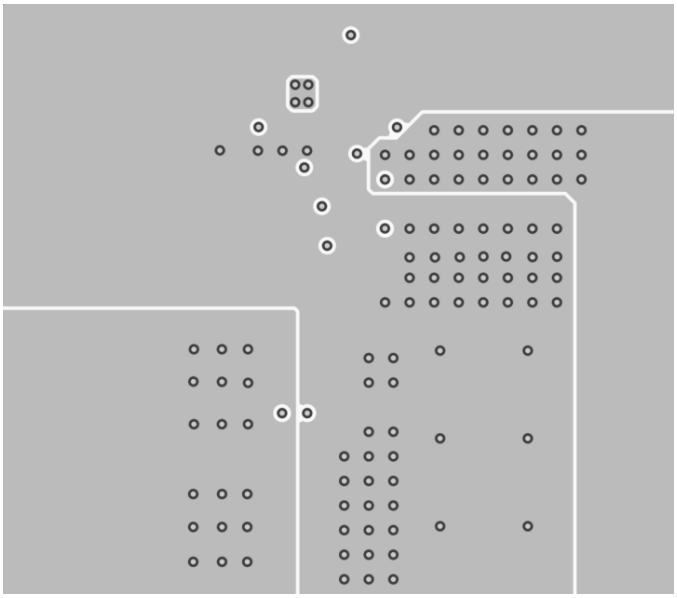
Top Layer



Middle Layer 2



Middle Layer 1



Bottom Layer

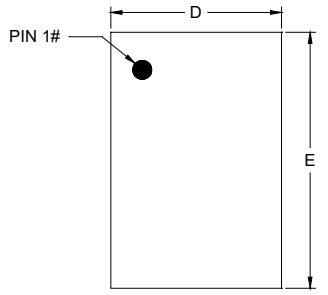
Figure 5. PCB Layout

Changes from Original to REV.A (AUGUST 2026) **Page**

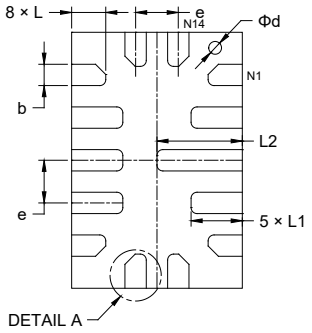
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

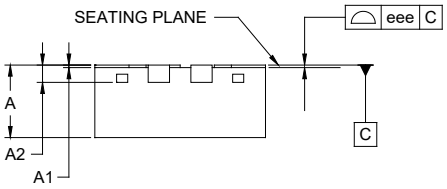
TQFN-2×3-14L



TOP VIEW

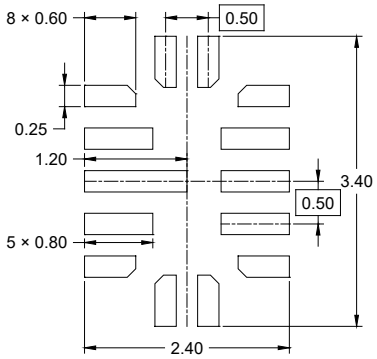


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



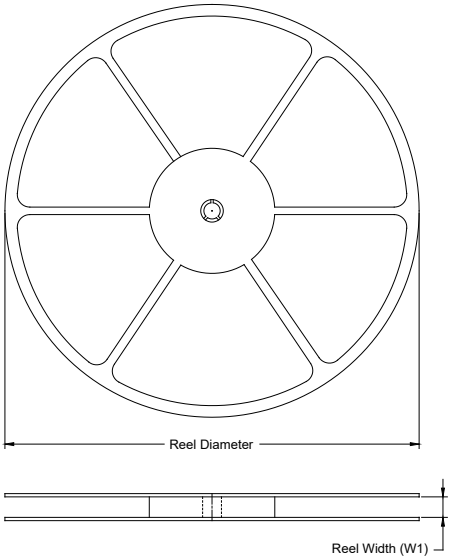
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
d	0.150 REF		
E	2.900	-	3.100
e	0.500 BSC		
L	0.300	-	0.500
L1	0.500	-	0.700
L2	0.900	-	1.100
eee	0.080		

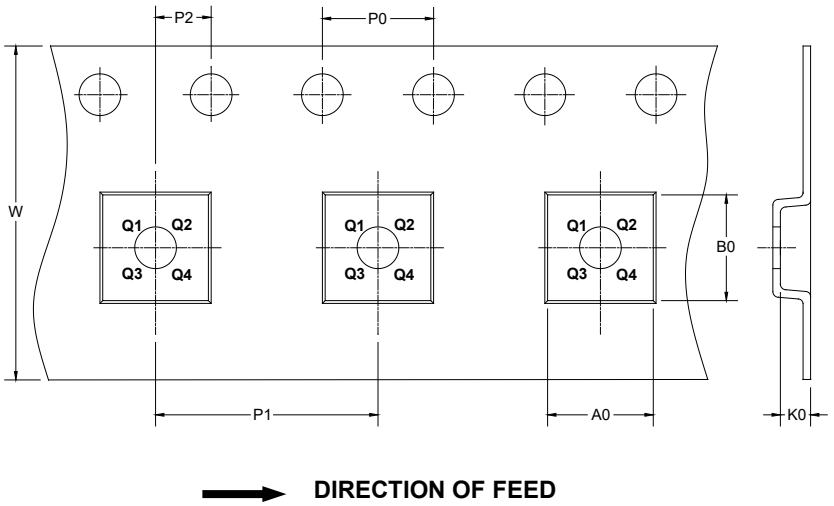
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



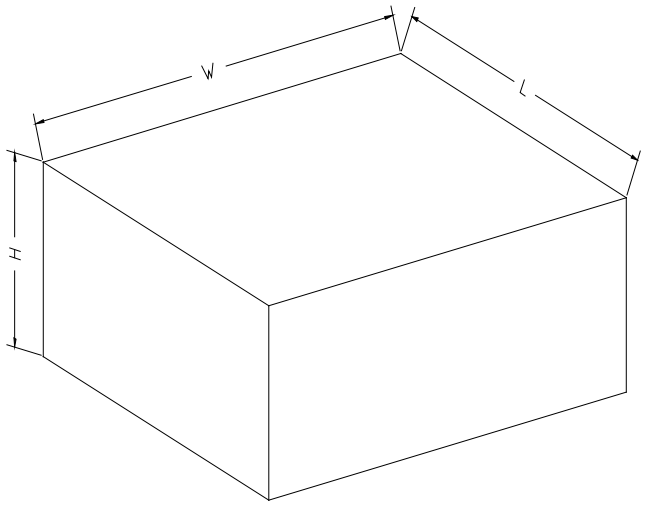
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×3-14L	13"	12.4	2.25	3.25	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002