

GENERAL DESCRIPTION

The SGM41052 family are protection ICs for Li-Ion/polymer rechargeable batteries, including the high-accuracy voltage detection circuits and deglitch circuits. The device is designed to protect 3-series cell to 5-series cell Li-Ion/polymer rechargeable battery packs against over-charge and over-discharge. And it is also suitable for 6-series or more series Li-Ion/polymer rechargeable battery packs through cascading.

The SGM41052 is available in a Green TSSOP-16 package.

SIMPLIFIED SCHEMATIC

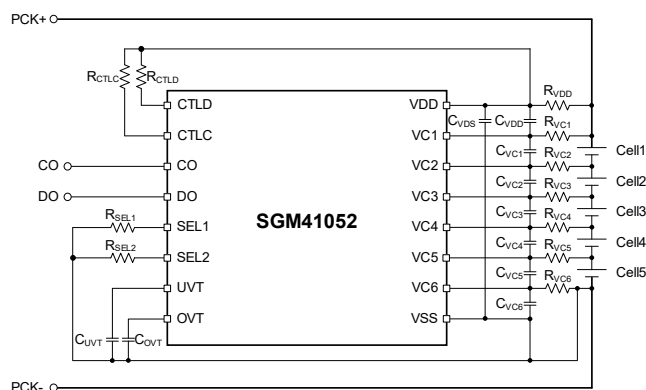


Figure 1. Simplified Schematic

FEATURES

- **High-Accuracy Voltage Detection Circuit**
 - ♦ **Over-Charge Detection Voltage:**
3.35V to 4.7V (25mV Step), Accuracy: $\pm 15\text{mV}$
 - ♦ **Over-Charge Hysteresis Voltage:**
0V to 400mV (50mV Step)
 - ♦ **Over-Discharge Detection Voltage:**
1.85V to 3.5V (50mV Step), Accuracy: $\pm 15\text{mV}$
 - ♦ **Over-Discharge Hysteresis Voltage:**
0V to 700mV (100mV Step)
- **Over-Charge and Over-Discharge Detection Deglitch Time is Settable by External Capacitor**
- **CO Pin and DO Pin are Controlled by CTLC Pin and CTLD Pin Respectively**
- **Support Selection between 3- to 5-Series Cell Configurations via SEL1 and SEL2 Pins**
- **Support Cascaded**
- **0V Battery Charge Enable**
- **28V Absolute Maximum Rating**
- **Low Current Consumption**
 - ♦ **During Operation:** 8 μA (TYP)
 - ♦ **During Power-Down:** 1.45 μA (TYP)
- **Operating Temperature Range: -40°C to +85°C**

APPLICATIONS

Li-Ion Rechargeable Battery Packs

Lithium Polymer Rechargeable Battery Packs

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

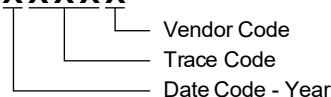
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41052-DB6B	TSSOP-16	-40°C to +85°C	SGM41052-DB6BYTS16G/TR	SGM3D3 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-F96B	TSSOP-16	-40°C to +85°C	SGM41052-F96BYTS16G/TR	SGM2S6 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-D98C	TSSOP-16	-40°C to +85°C	SGM41052-D98CYTS16G/TR	SGM3D4 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-DM9E	TSSOP-16	-40°C to +85°C	SGM41052-DM9EYTS16G/TR	SGM2S5 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-BT6B	TSSOP-16	-40°C to +85°C	SGM41052-BT6BYTS16G/TR	SGM3D5 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-DU6B	TSSOP-16	-40°C to +85°C	SGM41052-DU6BYTS16G/TR	SGM3D6 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-C28C	TSSOP-16	-40°C to +85°C	SGM41052-C28CYTS16G/TR	SGM2S4 YTS16 XXXXX	Tape and Reel, 4000
SGM41052-CD9E	TSSOP-16	-40°C to +85°C	SGM41052-CD9EYTS16G/TR	SGM3D7 YTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

PRODUCT LIST

Table 1. Product Name List

Product Name ⁽¹⁾	Over-Charge Detection Voltage (V _{ov})	Over-Charge Release Voltage (V _{ovr})	Over-Discharge Detection Voltage (V _{uv})	Over-Discharge Release Voltage (V _{uvr})
SGM41052-DB6B	4.350V	4.150V	2.3V	2.5V
SGM41052-F96B	4.525V	4.475V	2.3V	2.5V
SGM41052-D98C	4.350V	4.250V	2.5V	2.7V
SGM41052-DM9E	4.375V	4.125V	2.6V	2.8V
SGM41052-BT6B	4.225V	4.125V	2.3V	2.5V
SGM41052-DU6B	4.400V	4.300V	2.3V	2.5V
SGM41052-C28C	4.250V	4.250V	2.5V	2.7V
SGM41052-CD9E	4.275V	4.175V	2.6V	2.8V
SGM41052-xxxx	—	—	—	—

NOTE:

1. For products not mentioned above, please contact our sales representatives.

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

ABSOLUTE MAXIMUM RATINGS

Input Voltage between VDD Pin and VSS Pin, V_{DD}	$V_{SS} - 0.3V$ to $V_{SS} + 28V$
VC1, VC2, VC3, VC4, VC5 Pins Input Voltage Range, V_{VC1} , V_{VC2} , V_{VC3} , V_{VC4} , V_{VC5}	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
VC6 Pin Input Voltage Range, V_{VC6}	$V_{SS} - 0.3V$ to $6V$
CTLD, CTLC, OVT, UVT Pins Input Voltage Range, V_{CTLD} , V_{CTLC} , V_{OVT} , V_{UVT}	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
DO, CO Pins Output Voltage Range, V_{DO} , V_{CO}	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Package Thermal Resistance	
TSSOP-16, θ_{JA}	106.3°C/W
TSSOP-16, θ_{JB}	69.4°C/W
TSSOP-16, θ_{JC}	42.3°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM	±4000V
CDM	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	-40°C to +85°C
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OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

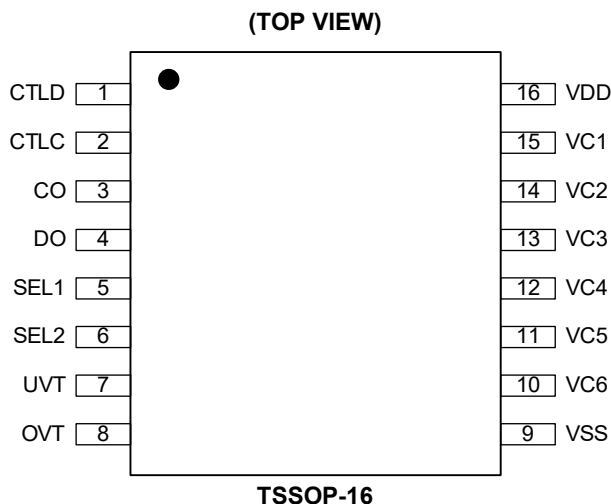
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CTLD	I	Output DO Control Pin.
2	CTLC	I	Output CO Control Pin.
3	CO	O	Over-Charge Detection Status Output Pin.
4	DO	O	Over-Discharge Detection Status Output Pin.
5	SEL1	I	The Number of Cell Select Pin.
6	SEL2	I	
7	UVT	I/O	Capacitor Connection Pin of Over-Discharge Voltage Detection Deglitch Time Control.
8	OVT	I/O	Capacitor Connection Pin of Over-Charge Voltage Detection Deglitch Time Control.
9	VSS	P	Negative Power Supply Input Pin. It is connected to the battery 5 negative voltage.
10	VC6	I	Battery 5 Negative Voltage Connection Pin.
11	VC5	I	Battery 5 Positive Voltage Connection Pin. Battery 4 Negative Voltage Connection Pin.
12	VC4	I	Battery 4 Positive Voltage Connection Pin. Battery 3 Negative Voltage Connection Pin.
13	VC3	I	Battery 3 Positive Voltage Connection Pin. Battery 2 Negative Voltage Connection Pin.
14	VC2	I	Battery 2 Positive Voltage Connection Pin. Battery 1 Negative Voltage Connection Pin.
15	VC1	I	Battery 1 Positive Voltage Connection Pin.
16	VDD	P	Positive Power Supply Input Pin. It is connected to the battery 1 positive voltage.

NOTE: I = input, O = output, I/O = input/output, P = power.

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

ELECTRICAL CHARACTERISTICS

($T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, typical values are measured at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Detection Voltage							
Over-Charge Detection Voltage	V _{OV}	T _J = +25°C		V _{OV} - 0.015	V _{OV}	V _{OV} + 0.015	V
		T _J = -20°C to +60°C		V _{OV} - 0.025	V _{OV}	V _{OV} + 0.02	
		T _J = -40°C to +85°C		V _{OV} - 0.03	V _{OV}	V _{OV} + 0.025	
Over-Charge Release Voltage	V _{OVR}	V _{OV} ≠ V _{OVR}	T _J = +25°C	V _{OVR} - 0.015	V _{OVR}	V _{OVR} + 0.015	V
			T _J = -20°C to +60°C	V _{OVR} - 0.025	V _{OVR}	V _{OVR} + 0.02	
			T _J = -40°C to +85°C	V _{OVR} - 0.03	V _{OVR}	V _{OVR} + 0.025	
		V _{OV} = V _{OVR}	T _J = +25°C	V _{OVR} - 0.015	V _{OVR}	V _{OVR} + 0.015	
			T _J = -20°C to +60°C	V _{OVR} - 0.025	V _{OVR}	V _{OVR} + 0.02	
			T _J = -40°C to +85°C	V _{OVR} - 0.03	V _{OVR}	V _{OVR} + 0.025	
Over-Discharge Detection Voltage	V _{UV}	T _J = +25°C		V _{UV} - 0.02	V _{UV}	V _{UV} + 0.02	V
		T _J = -20°C to +60°C		V _{UV} - 0.025	V _{UV}	V _{UV} + 0.025	
		T _J = -40°C to +85°C		V _{UV} - 0.025	V _{UV}	V _{UV} + 0.025	
Over-Discharge Release Voltage	V _{UVR}	V _{UV} ≠ V _{UVR}	T _J = +25°C	V _{UVR} - 0.02	V _{UVR}	V _{UVR} + 0.02	V
			T _J = -20°C to +60°C	V _{UVR} - 0.025	V _{UVR}	V _{UVR} + 0.025	
			T _J = -40°C to +85°C	V _{UVR} - 0.025	V _{UVR}	V _{UVR} + 0.025	
		V _{UV} = V _{UVR}	T _J = +25°C	V _{UVR} - 0.02	V _{UVR}	V _{UVR} + 0.02	
			T _J = -20°C to +60°C	V _{UVR} - 0.025	V _{UVR}	V _{UVR} + 0.025	
			T _J = -40°C to +85°C	V _{UVR} - 0.025	V _{UVR}	V _{UVR} + 0.025	
Input Voltage							
Operation Voltage between VDD Pin and VSS Pin	V _{DD}			3.5		28	V
CTLC Pin Voltage "H"	V _{CTCH}			V _{DD} - 0.8			V
CTLC Pin Voltage "L "	V _{CTCL}					V _{DD} - 3	V
CTLD Pin Voltage "H"	V _{CTDH}			V _{DD} - 0.8			V
CTLD Pin Voltage "L "	V _{CTDL}					V _{DD} - 3	V
SEL1 Pin Voltage "H""	V _{SEL1H}			0.8 × V _{DD}			V
SEL1 Pin Voltage "L"	V _{SEL1L}					0.2 × V _{DD}	V
SEL 2 Pin Voltage "H"	V _{SEL2H}			0.8 × V _{DD}			V
SEL2 Pin Voltage "L"	V _{SEL2L}					0.2 × V _{DD}	V
Output Voltage							
CO Pin Voltage "H"	V _{COH}			6	8	10	V
DO Pin Voltage "H"	V _{DOH}			6	8	10	V

ELECTRICAL CHARACTERISTICS (continued)(T_J = -40°C to +85°C, typical values are measured at T_J = +25°C, unless otherwise noted.)

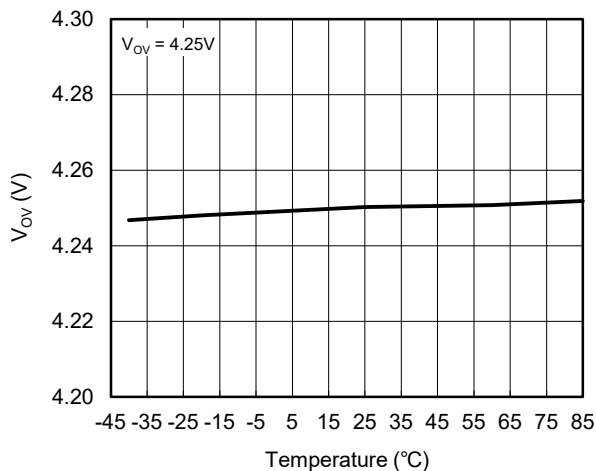
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current							
Current Consumption during Operation	I _{OPE}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V	T _J = +25°C		8	12	μA
			T _J = -40°C to +85°C		8	16	
Current Consumption during Power-Down	I _{PDN}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 1.5V	T _J = +25°C		1.45	3.5	μA
			T _J = -40°C to +85°C		1.45	4.4	
VC1 Pin Input Current	I _{VC1}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V			0.05	0.15	μA
VC2/3/4/5 Pins Input Current	I _{VC2/3/4/5}			-0.1		0.1	
VC6 Pin Input Current	I _{VC6}			-0.15	-0.05		
CTLIC Pin Input Current "H"	I _{CTCH}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V		0.3	0.6	0.88	μA
CTLD Pin Input Current "H"	I _{CTDH}			0.3	0.6	0.88	
SEL1 Pin Input Current "H"	I _{SEL1H}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V	T _J = +25°C			0.15	μA
			T _J = -40°C to +85°C			0.3	
SEL1 Pin Input Current "L"	I _{SEL1L}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V	T _J = +25°C	-0.1			
			T _J = -40°C to +85°C	-0.3			
SEL2 Pin Input Current "H"	I _{SEL2H}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V	T _J = +25°C			0.15	
			T _J = -40°C to +85°C			0.3	
SEL2 Pin Input Current "L"	I _{SEL2L}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V	T _J = +25°C	-0.1			
			T _J = -40°C to +85°C	-0.3			
Output Current							
CO Pin Output Current	I _{COO}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V		10			μA
CO Pin Sink Current	I _{COS}	V _{BAT1} = 4.8V, V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V		10			
DO Pin Output Current	I _{DOO}	V _{BAT1} = V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V		10			μA
DO Pin Sink Current	I _{DOS}	V _{BAT1} = 1.8V, V _{BAT2} = V _{BAT3} = V _{BAT4} = V _{BAT5} = 3.4V		10			
Deglitch Time							
Over-Charge Detection Deglitch Time	t _{OV}	C _{OVT} = 0.1μF	T _J = +25°C	0.77	1	1.12	s
			T _J = -40°C to +85°C	0.71	1	1.29	
Over-Discharge Detection Deglitch Time	t _{UV}	C _{UVT} = 0.1μF	T _J = +25°C	0.77	1	1.12	s
			T _J = -40°C to +85°C	0.71	1	1.29	
OVT Pin Voltage	V _{OVT}	C _{OVT} = 0.1μF			1.1	1.35	V
UVT Pin Voltage	V _{UVT}	C _{UVT} = 0.1μF			1.1	1.35	V

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

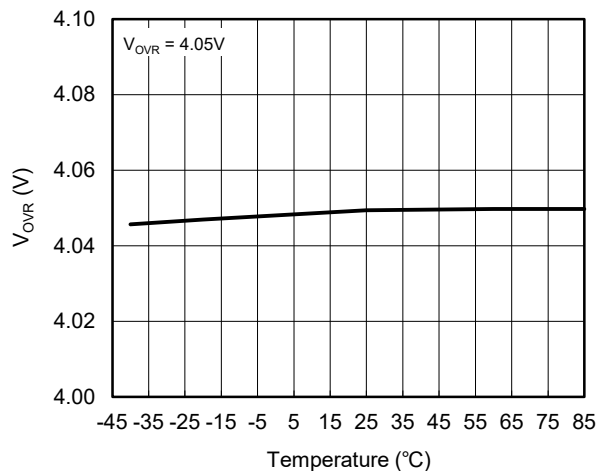
TYPICAL PERFORMANCE CHARACTERISTICS

$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.

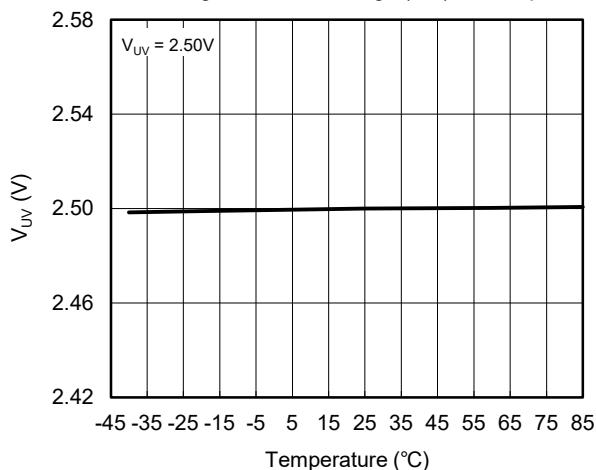
Over-Charge Detection Voltage (V_{OV}) vs. Temperature



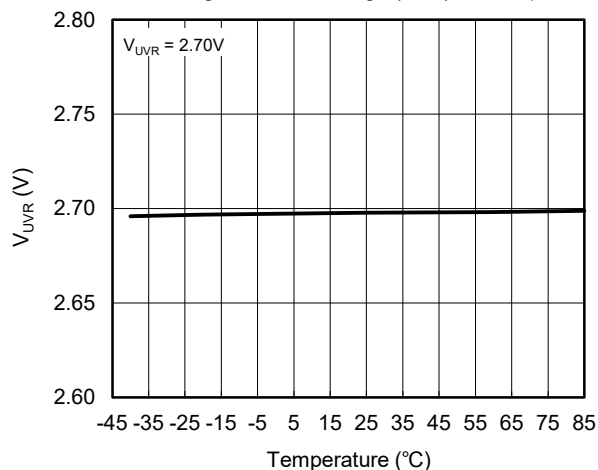
Over-Charge Release Voltage (V_{OVR}) vs. Temperature



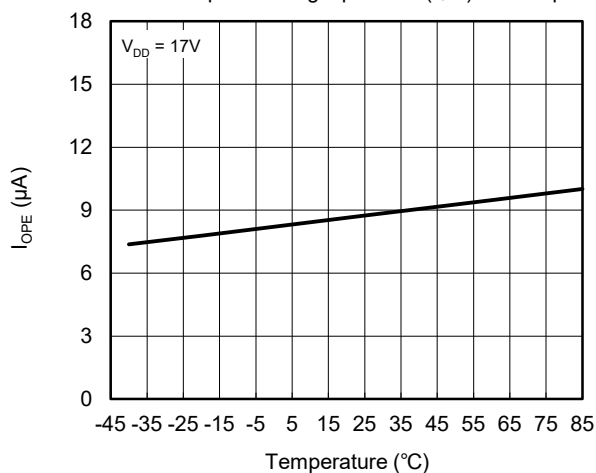
Over-Discharge Detection Voltage (V_{UV}) vs. Temperature



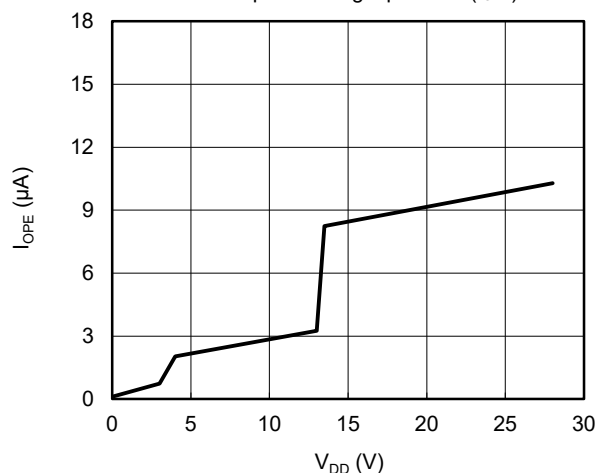
Over-Discharge Release Voltage (V_{UVR}) vs. Temperature



Current Consumption during Operation (I_{OPE}) vs. Temperature



Current Consumption during Operation (I_{OPE}) vs. V_{DD}

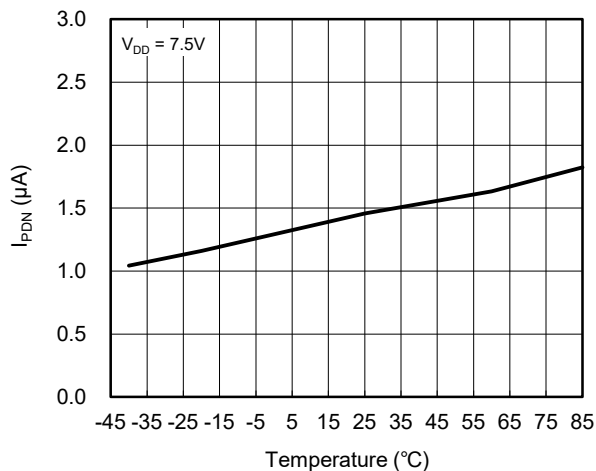


SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

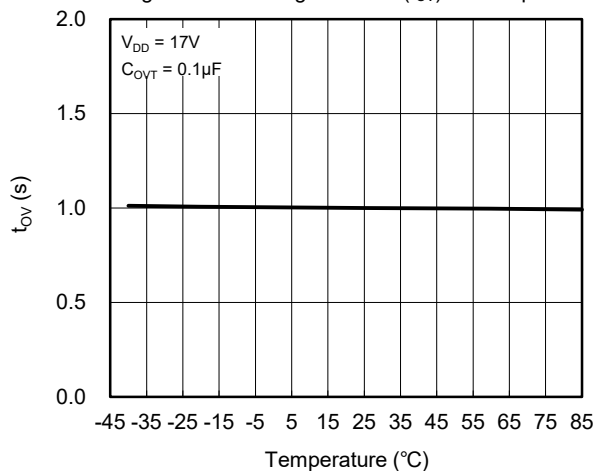
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.

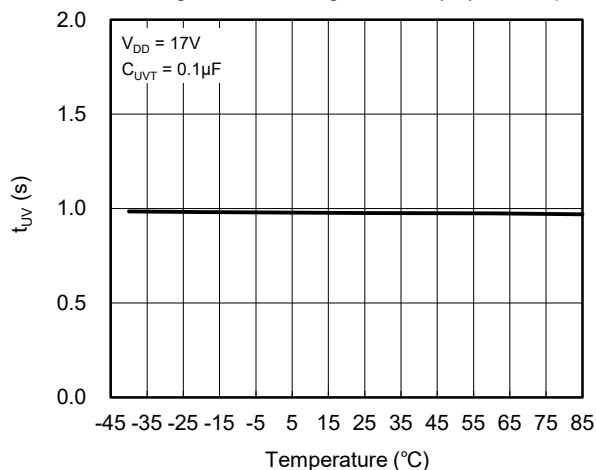
Current Consumption during Power-Down (I_{PDN}) vs. Temperature



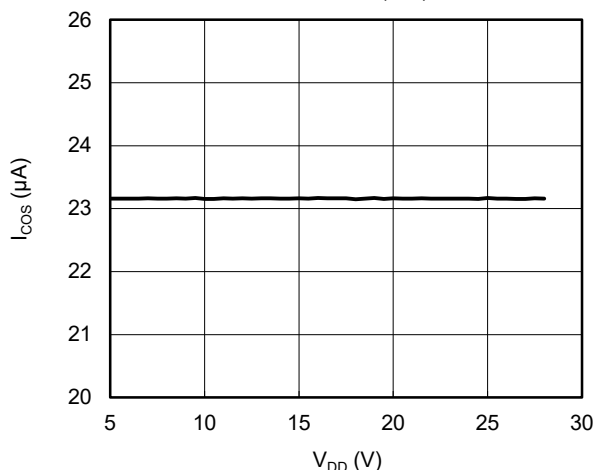
Over-Charge Detection Deglitch Time (t_{OV}) vs. Temperature



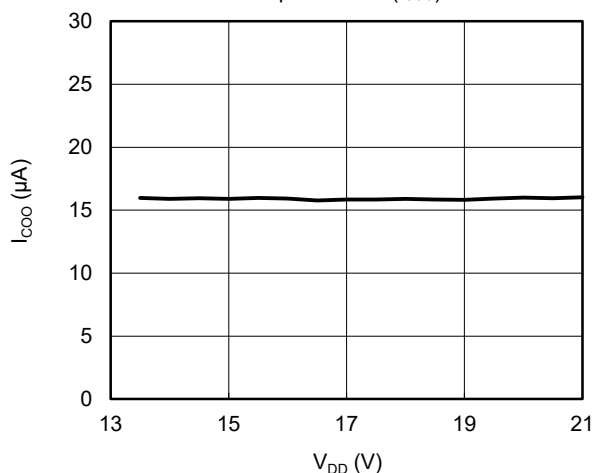
Over-Discharge Detection Deglitch Time (t_{UV}) vs. Temperature



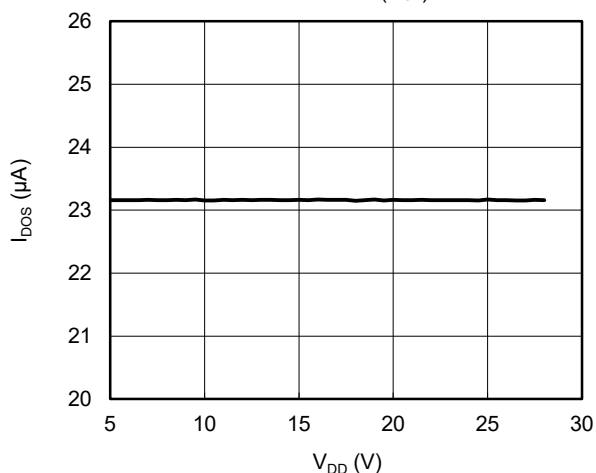
CO Pin Sink Current (I_{COS}) vs. V_{DD}



CO Pin Output Current (I_{COO}) vs. V_{DD}



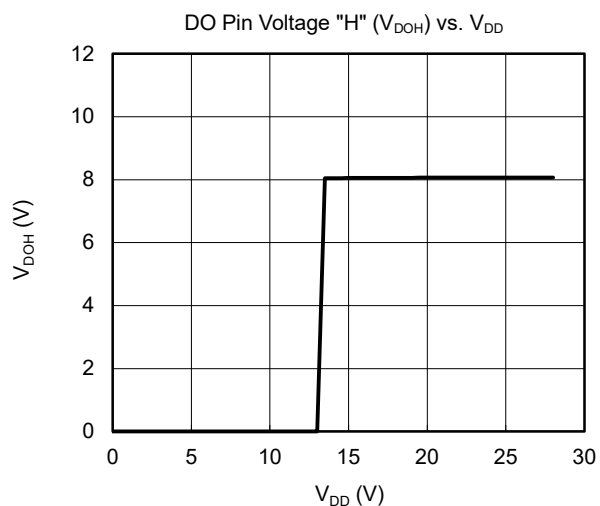
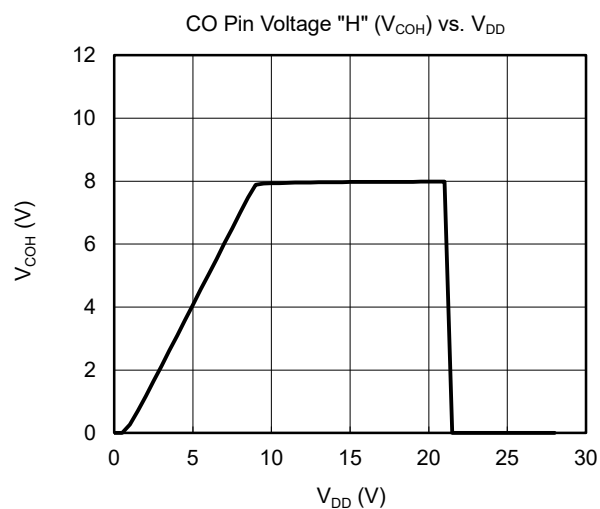
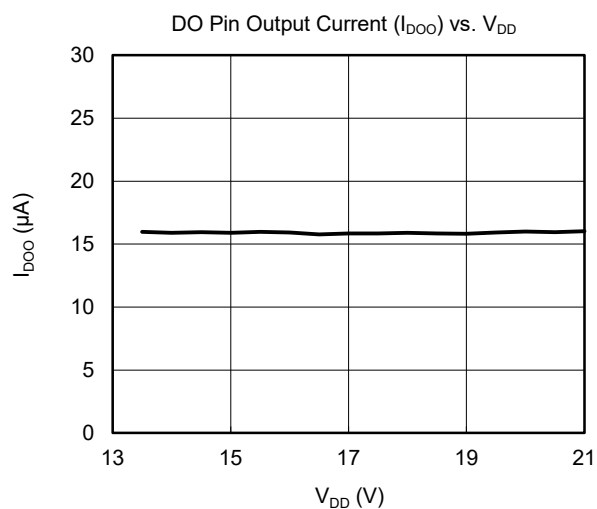
DO Pin Sink Current (I_{DOS}) vs. V_{DD}



SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.



SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

FUNCTIONAL BLOCK DIAGRAM

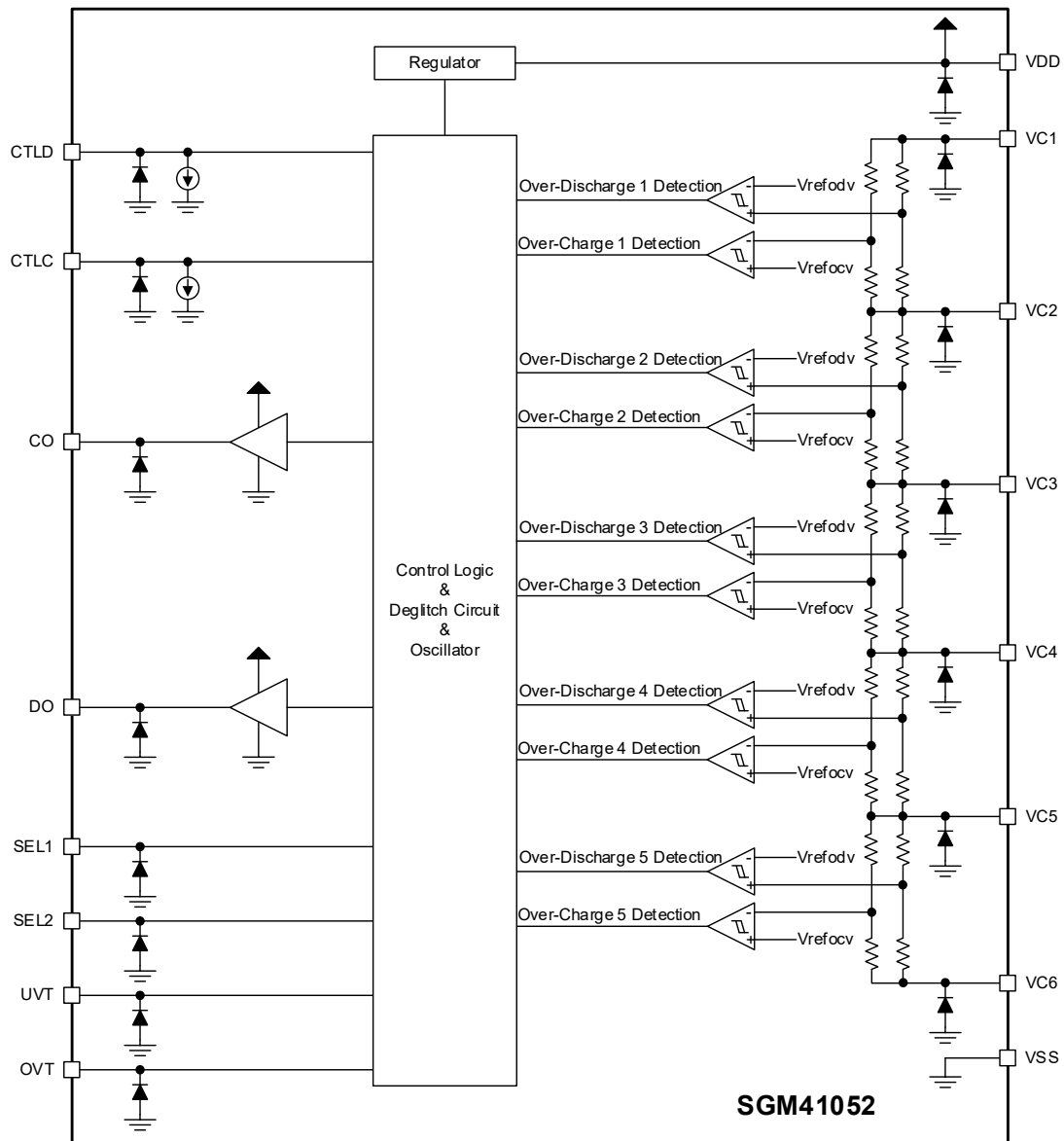


Figure 2. Block Diagram

DETAILED DESCRIPTION

Operation

Normal Status

The SGM41052 monitors all the five batteries voltage to detect over-charge or over-discharge status.

When all the batteries voltage is between V_{OV} (over-charge detection voltage) and V_{UV} (over-discharge detection voltage), the CTLC pin voltage is equal to or higher than V_{CTCH} (the CTLC pin voltage "H") and the voltage of the CTLD pin is equal to or higher than V_{CTDH} (the CTLD pin voltage "H"), the SGM41052 pulls up both CO and DO pins. This status is referred to as the normal operating status.

Over-Charge Status

In normal status, if any of the batteries voltage rises higher than V_{OV} and it lasts for t_{OV} (over-charge detection deglitch time) or longer, the SGM41052 will pull down the CO pin. This status is referred to as the over-charge status.

During over-charge status, the voltage of each individual battery cell $\leq V_{OVR}$, the SGM41052 will be released from the over-charge status.

Over-Discharge Status

In normal status, if any of the batteries voltage falls below V_{UV} and it lasts for t_{UV} (over-discharge detection deglitch time) or longer, the SGM41052 will pull down the DO pin. This status is referred to as the over-discharge status.

During over-discharge status, the voltage of each individual battery cell $\geq V_{UVR}$, the SGM41052 will be released from the over-discharge status.

Over-Charge Detection Deglitch Time & Over-Discharge Detection Deglitch Time

In normal status, if any of the batteries voltage rises higher than V_{OV} during charging, the SGM41052 charges the C_{OVT} which is connected to the OVT pin. The voltage of the OVT pin will increase rapidly up to V_{OVT} . At the same time, t_{OV} starts counting until the voltage of C_{OVT} falls to a specific reference level or lower through the sink current with 100nA.

The typical value of t_{OV} can be calculated by Equation 1:

$$t_{OV} (s) = 10s/\mu F \times C_{OVT} (\mu F) \quad (1)$$

In normal status, if any of the batteries voltage falls below V_{UV} during discharging, the SGM41052 charges the C_{UVT} which is connected to the UVT pin. The voltage of the UVT pin will increase rapidly up to V_{UVT} . At the same time, t_{UV} starts counting until the voltage of C_{UVT} falls to a specific reference level or lower through the sink current with 100nA.

The typical value of t_{UV} can be calculated by Equation 2:

$$t_{UV} (s) = 10s/\mu F \times C_{UVT} (\mu F) \quad (2)$$

The SGM41052 series is designed with a high-speed charging circuit for its deglitch capacitor. When the capacitance is low, the voltages at both OVT and UVT pins rise accordingly, which results in a discrepancy between the theoretically calculated deglitch time and the actual value. When the capacitance is sufficiently high to prevent the rapid charging from finishing within the built-in deglitch period, the output pin will switch to the detection status once the internal deglitch terminates.

In addition, the charging current of the deglitch capacitor is routed via the VDD pin. Accordingly, a high resistance connected to the VDD pin will result in a substantial drop in supply voltage during fast charging, thus triggering abnormal device operation.

CTLC Pin and CTLD Pin

The SGM41052 integrates two control pins, CTLC and CTLD. When the CTLC pin is set to low or floating, the CO will be pulled down to VSS. When the CTLC pin is set to high, the CO is controlled by the voltage detection circuit. When the CTLD pin is set to low or floating, the DO will be pulled down to VSS. When the CTLD pin is set to high, the DO is controlled by the voltage detection circuit.

Table 2. CO Status Set by CTLC Pin

CTLC PIN	CO PIN
High	Normal Status ⁽¹⁾
Low or Floating	VSS

NOTE: 1. The CO output status is controlled by the voltage detection circuit.

Table 3. DO Status Set by CTLD Pin

CTLD PIN	DO PIN
High	Normal Status ⁽¹⁾
Low or Floating	VSS

NOTE: 1. The DO output status is controlled by the voltage detection circuit.

SEL1 Pin and SEL2 Pin

SGM41052 has two pins, SEL1 and SEL2, which can be used to configure 3-cell to 5-cell batteries.

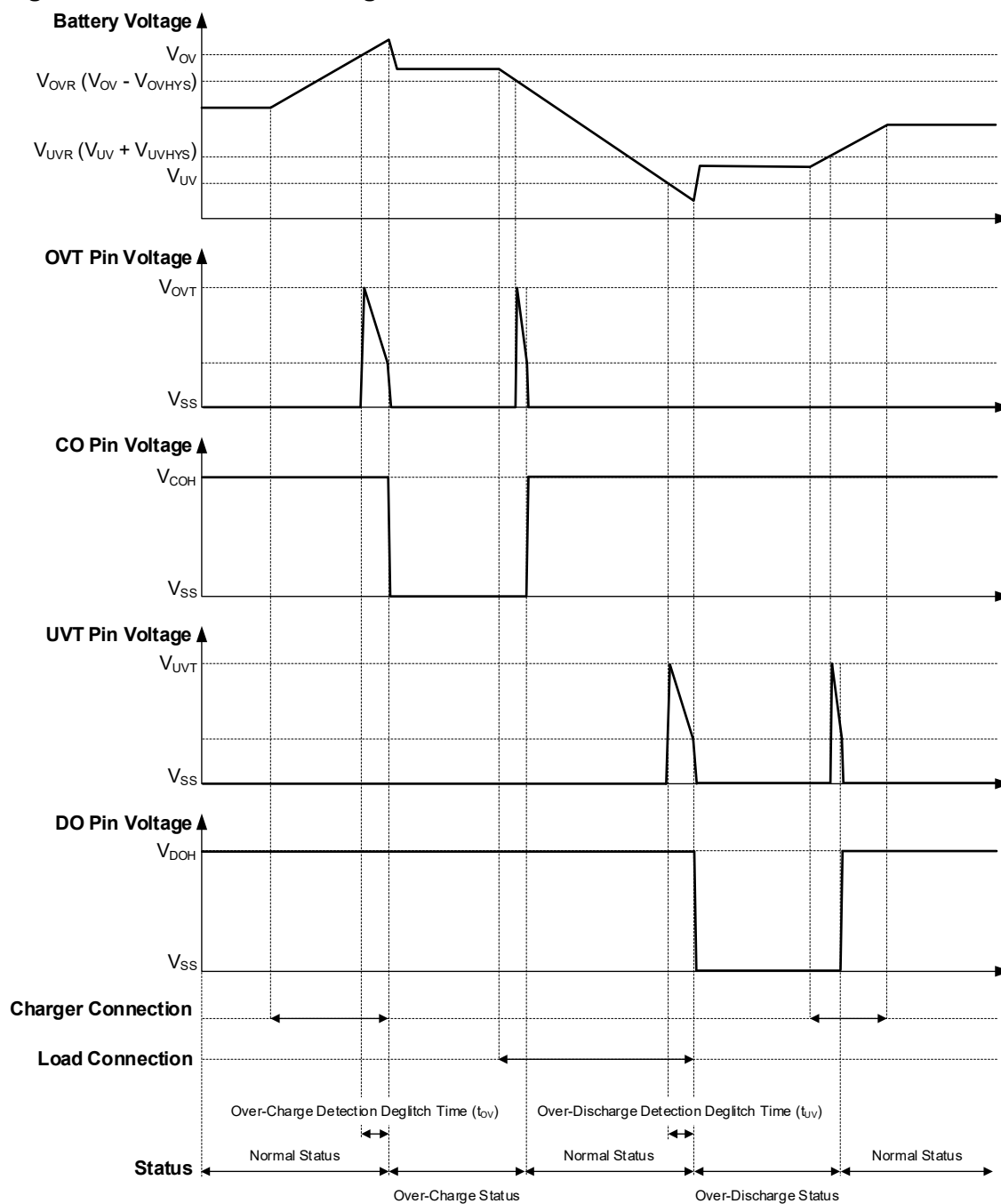
Table 4. Number of Batteries Selection

SEL1 PIN	SEL2 PIN	NUM.
High	High	Prohibition
High	Low or Floating	3-Cell
Low or Floating	High	4-Cell
Low or Floating	Low or Floating	5-Cell

DETAILED DESCRIPTION (continued)

Timing Charts

Over-Charge Detection, Over-Discharge Detection



NOTE: Assume that the charger charges at constant current.

Figure 3. Over-Charge Detection, Over-Discharge Detection

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

DETAILED DESCRIPTION (continued)

Battery Protection IC Connection Example

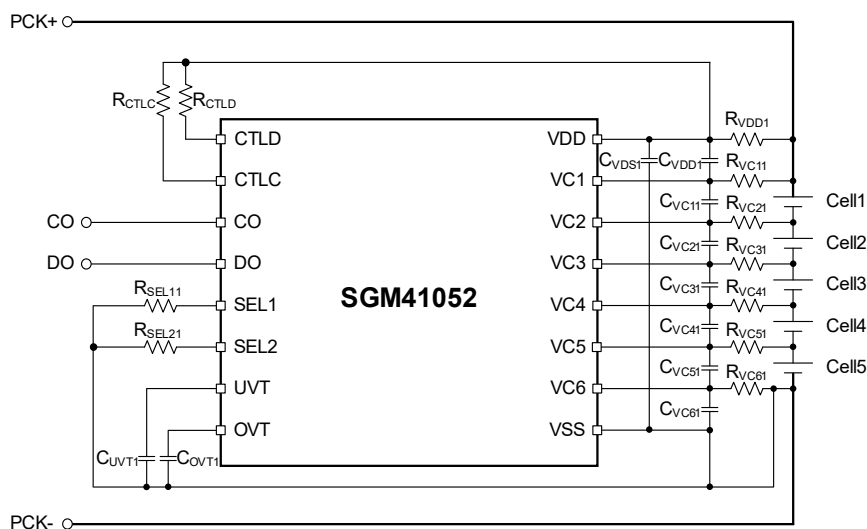


Figure 4. Battery Protection IC Connection Example for 5-Cell

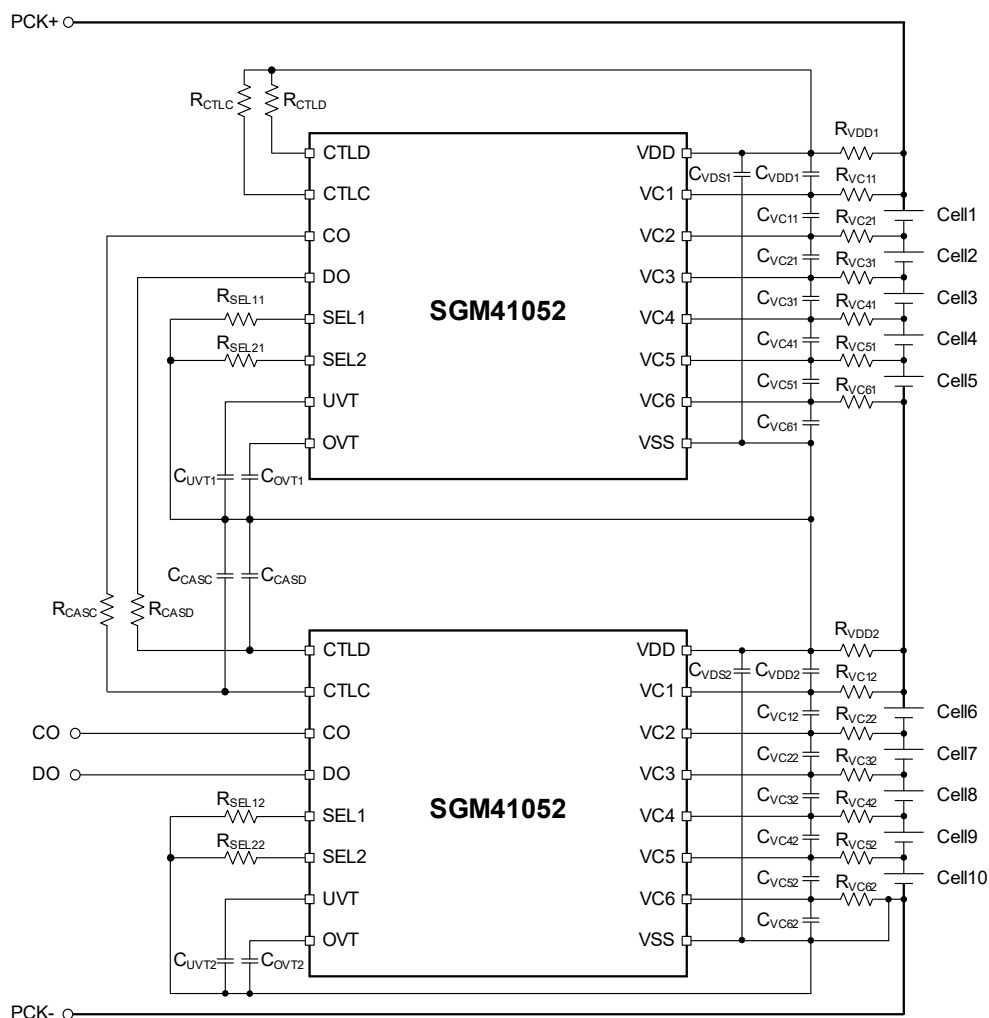


Figure 5. Battery Protection IC Connection Example for 10-Cell

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

DETAILED DESCRIPTION (continued)

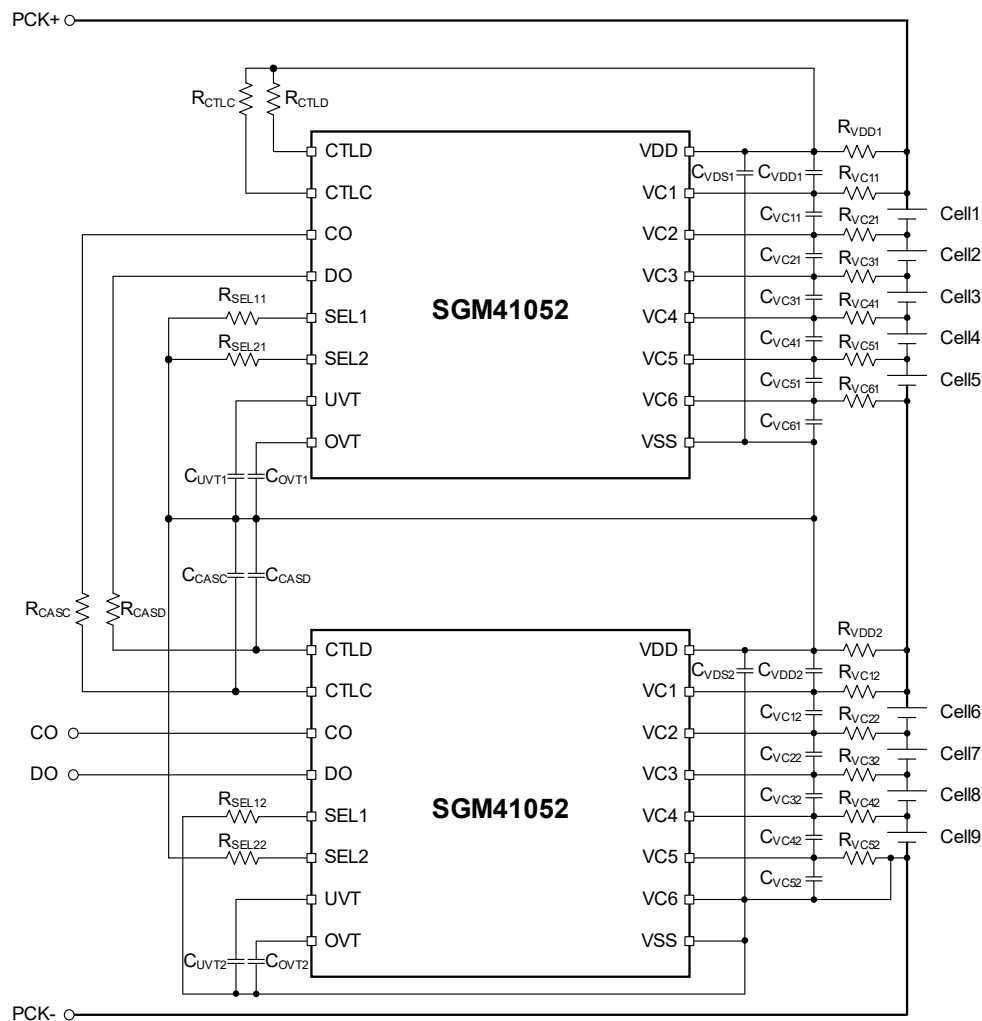


Figure 6. Battery Protection IC Connection Example for 9-Cell

SGM41052 Battery Protection IC for 3- to 5-Series Cell Battery Pack

DETAILED DESCRIPTION (continued)

Table 5. External Component Configuration Parameters for 10-Cell

SYMBOL	PART	PURPOSE	MIN	TYP	MAX
R_{VDD1}, R_{VDD2}	Resistor	ESD Protection, for Power Fluctuation	50Ω	100Ω	1000Ω
$R_{VC11} \sim R_{VC61}, R_{VC12} \sim R_{VC62}$	Resistor	ESD Protection, for Power Fluctuation ⁽¹⁾	0.75kΩ	1kΩ	2kΩ
R_{CTLG}, R_{CTLD}	Resistor	ESD Protection, for Power Fluctuation		1kΩ	
R_{CASC}, R_{CASH}	Resistor	ESD Protection, for Power Fluctuation		5.1MΩ	
$R_{SEL11}, R_{SEL21}, R_{SEL12}, R_{SEL22}$	Resistor	ESD Protection, for Power Fluctuation	0.5kΩ	1kΩ	
C_{VDS1}, C_{VDS2}	Capacitor	For Power Fluctuation	0.01μF	0.1μF	1μF
C_{VDD1}, C_{VDD2}	Capacitor	For Power Fluctuation	0μF		1μF
$C_{VC11} \sim C_{VC61}, C_{VC12} \sim C_{VC62}$	Capacitor	For Power Fluctuation	0.01μF	0.1μF	1μF
$C_{OVT1}, C_{OVT2}, C_{UVT1}, C_{UVT2}$	Capacitor	For Power Fluctuation	0.001μF	0.1μF	0.22μF
C_{CASC}, C_{CASH}	Capacitor	For Power Fluctuation		1000pF	

NOTE:

1. Accuracy of over-charge/over-discharge detection voltage is guaranteed by $R_{VCn} = 1k\Omega$. Connecting resistors with other values will worsen the accuracy.

Caution:

- Specifications for external components are subject to change without prior notice.
- Performance has only been verified in the context of the reference design. Functionality under alternate configurations is not guaranteed. It is imperative that customers conduct comprehensive validation tests under actual operating conditions to determine appropriate parameter settings.

Precautions

- The combined electrical stress from input and output voltages must not exceed the device's maximum allowable power dissipation.
- If an over-charged battery and an over-discharged batteries intermix, the IC operates in both over-charge and over-discharge statuses.
- Exercise caution to ensure that no electrostatic discharge exceeds the clamping capability of the device's internal protection circuitry.
- Disclaim any dispute arising out of or in connection with the infringement of third party patents by products including this IC.

REVISION HISTORY

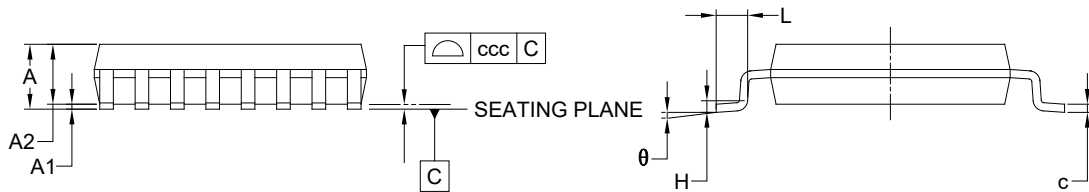
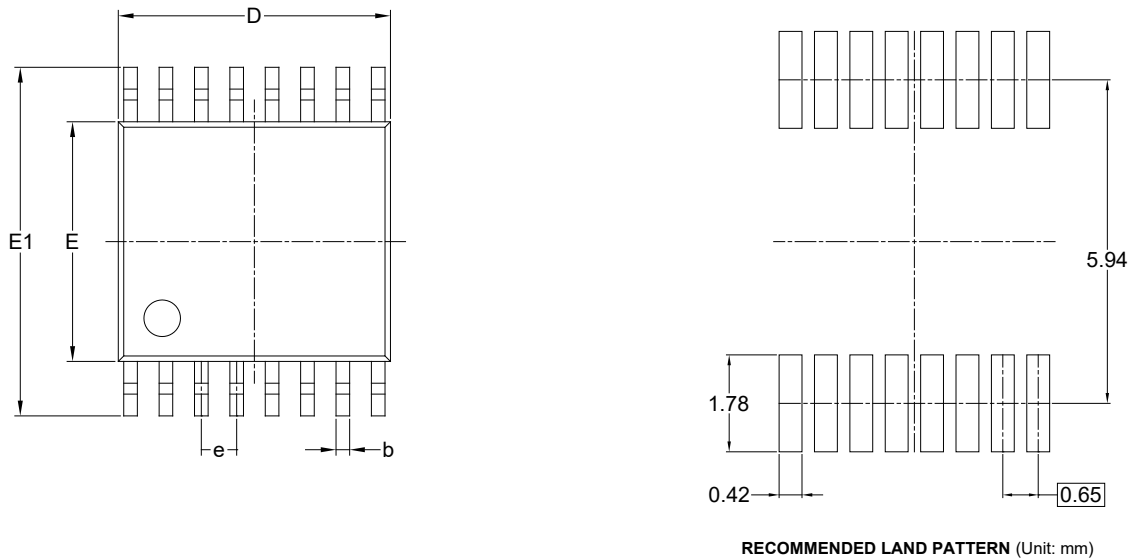
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2026)

	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

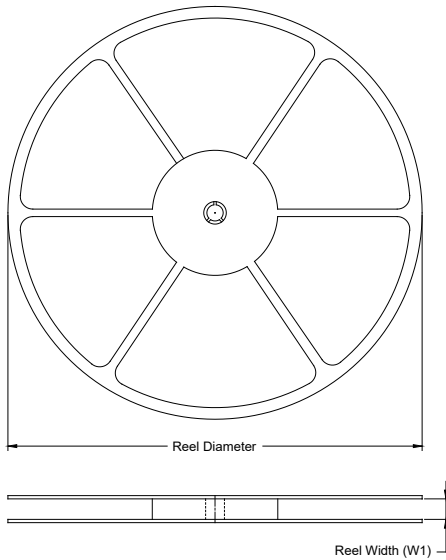
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

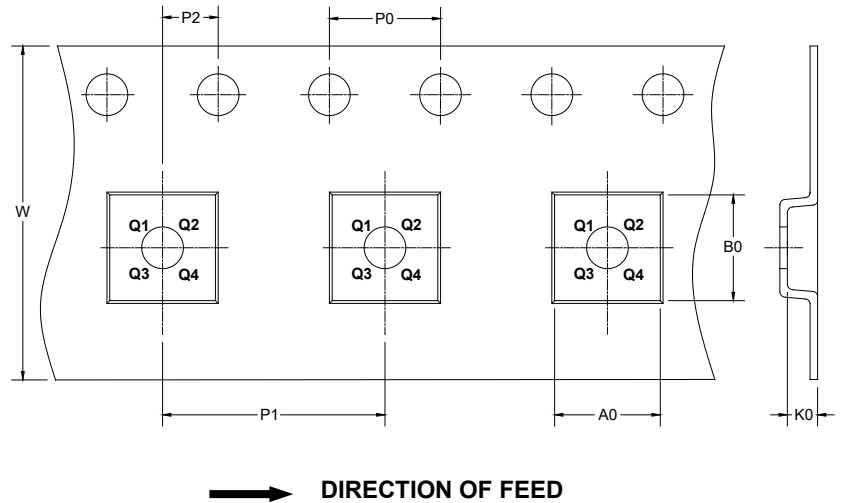
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

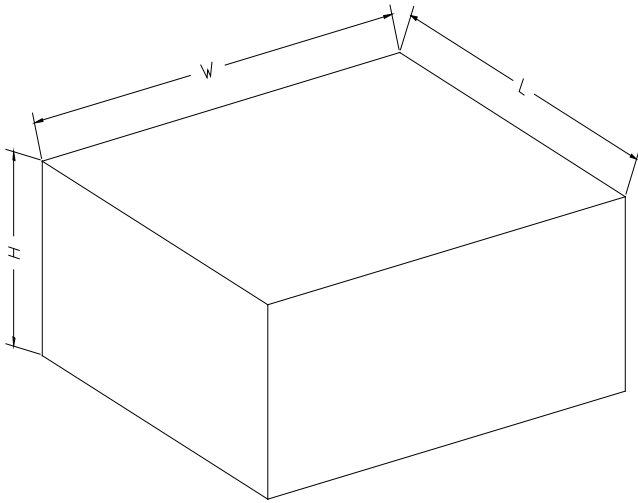
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002