SGM2548
2.7V to 23V, 5.5A Electronic Fuse with Ideal Diode Function, Input Reverse Polarity and Over-Voltage Protection

GENERAL DESCRIPTION

The SGM2548 is a compact electronic fuse (eFuse) with a full suite of protection functions. With very few external components, the SGM2548 can provide multiple protection modes. To encounter overload, short-circuit, high inrush current, voltage surge and reverse polarity, the device is suitable as a robust defense.

Due to the back-to-back FETs packaged inside the chip, SGM2548 prohibits reverse current flow from output to input, which is ideal for power MUX/ORing applications and systems requiring load side energy hold up storage when input power supply fails. Through linear ORing circuit architecture, these devices effectively suppress reverse DC current to negligible levels and approximate perfect diode functionality, with carefully engineered minimization of both voltage drop across the forward path and associated energy dissipation.

The V_{OUT} rise time can be programmed by setting an additional capacitor to the SS pin, which can minimize inrush current. Programmable over-voltage protection is used to turn off the device or clamp the output to a fixed voltage (pin-selectable) if the IN rises over a threshold value. The IMON pin is used for load current monitoring. In case of output overload, the device actively senses the current or disconnects the circuit.

The SGM2548 is available in a Green TQFN-2×2-10L package.

APPLICATIONS

Power MUX/ORing
Adapter Input Protection
Set-Top Box
USB PD Port Protection
Smart Speakers
Power Tools/Chargers
POS Device

FEATURES

- **Input Voltage Range: 2.7V to 23V Surge up to 28V**
  - **Up to -15V Withstands Negative Voltage**
- **On-Resistance: R_{DSON} = 29mΩ (TYP)**
- **Ideal Diode Function with True Reverse Current Blocking**
- **Fast Over-Voltage Protection**
  - **Response Time: 1.2μs (TYP)**
  - **Adjustable Over-Voltage Lockout (OVLO)**
- **Fast-Trip Response to Transient Over-Currents during Steady State**
  - **Response Time: 500ns (TYP)**
  - **Latch-Off After Fault**
- **Analog Load Current Monitor (IMON)**
  - **Current Range: 0.5A to 5.5A**
  - **Accuracy: ±4.5% (I_{OUT} ≥ 1A)**
- **Enable Input (Active-High) with Adjustable Under-Voltage Lockout Threshold (UVLO)**
- **Programmable Output Ramp Time (SS)**
- **Over-Temperature Protection**
- **Indication: PG & PGTH**
- **Available in a Green TQFN-2×2-10L Package**

SIMPLIFIED SCHEMATIC

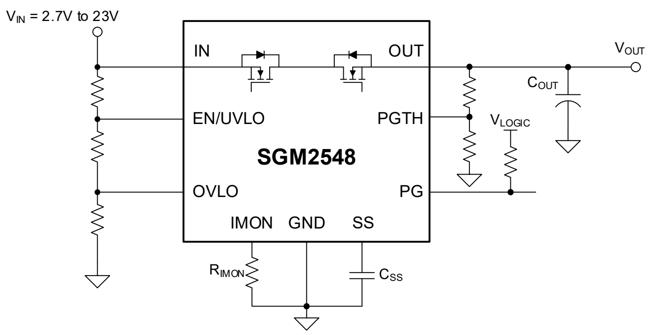


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2548	TQFN-2×2-10L	-40℃ to +125℃	SGM2548XTSP10G/TR	2548 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.

XXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN}
- -40℃ to +125℃ .... MAX (-15V, V_{OUT} - 21V) to 28V
- -10℃ to +125℃ .... MAX (-15V, V_{OUT} - 22V) to 28V

Output Voltage Range, V_{OUT}
- -40℃ to +125℃ .... -0.3V to MIN (28V, V_{IN} + 21V)
- -10℃ to +125℃ .... -0.3V to MIN (28V, V_{IN} + 22V)

Output Voltage Pulse (< 1μs), V_{OUT_PLS} .... > -0.8V
Enable Voltage Range, $V_{EN/UVLO}$ (1) .... -0.3V to 6.5V
OVLO Voltage Range, V_{OVLO} (1) .... -0.3V to 6.5V
SS Voltage Range, V_{SS} .... Internally Limited
PGTH Voltage Range, V_{PGTH} (1) .... -0.3V to 6.5V
PG Voltage Range, V_{PG} .... -0.3V to 6.5V
IMON Voltage Range, V_{IMON} 1.8V
Continuous Switch Current, I_{MAX} 5.5A
Package Thermal Resistance
- TQFN-2×2-10L, θ_{JA} .... 66.7℃/W
- TQFN-2×2-10L, θ_{JB} .... 3.8℃/W
- TQFN-2×2-10L, θ_{JC} .... 50.6℃/W

Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility (2) (3)
HBM (NC OUT) .... ±4000V
HBM (OUT Only to GND) .... ±2000V
CDM .... ±1000V

NOTES:

1. If this pin is pulled up to V_{IN}, a 350kΩ or higher pull-up resistance is recommended which is to limit the current when input voltage is negative.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .... 2.7V to 23V
Output Voltage Range, V_{OUT} .... MIN (23V, V_{IN} + 20V)
Enable Voltage Range, $V_{EN/UVLO}$ 5V (1)
OVLO Voltage Range, V_{OVLO} .... 0.5V to 1.5V
SS Capacitor Voltage Rating, V_{SS} .... V_{IN} + 5V (2)
PGTH Voltage Range, V_{PGTH} 5V (3)
PG Voltage Range, V_{PG} 5V (3)
IMON Voltage, V_{IMON} 1.5V
Continuous Switch Current, I_{MAX}, T_J ≤ +125℃ 5.5A
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:

1. For input voltages ≤ 5V, direct connection of the EN/UVLO pin to the supply rail is permissible. In applications where VIN exceeds 5V or where input polarity reversal may occur, implementation of a pull-up resistor ≥ 350kΩ is mandatory to ensure proper biasing and fault protection.
2. In PowerMUX/ORing setups with unequal supplies, select the SS capacitor rating for each device based on the higher of the two rails.
3. In applications where input polarity reversal may occur, if connecting the enable pin directly to the power input, a pull-up resistor of at least 350kΩ should be used to maintain safe current levels through the terminal during fault conditions.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

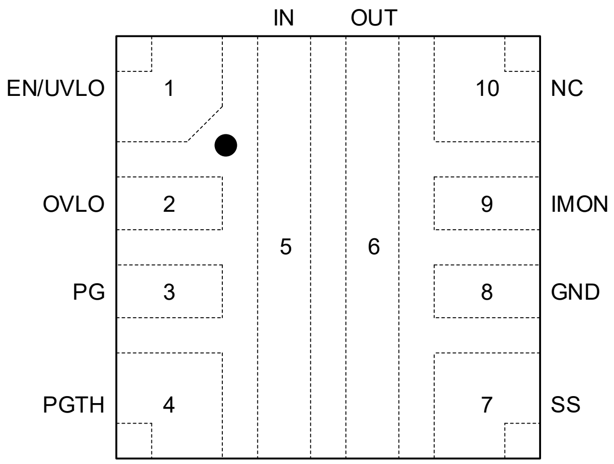
OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-2×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	AI	Enable and Under-Voltage Lockout Input. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is programmed by an external resistor divider. This pin cannot be left floating.
2	OVLO	AI	Over-Voltage Lockout Pin. The over-voltage lockout threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. The device is enabled when this pin is tied to low level. This pin cannot be left floating.
3	PG	DO	Power Good Indication. This is an open-drain pin, when the internal channels of the chip are all turned on and the PGTH signal value is higher than the set value, the pin is set to high level.
4	PGTH	AI	Power Good Threshold.
5	IN	Power	Input Supply Voltage.
6	OUT	P	Output of the Device.
7	SS	AO	Soft-Start Pin. The capacitor between SS and GND pins will set the slew rate according to the application requirements. When this pin is left floating, the device will start up at the fastest rate.
8	GND	G	GND.
9	IMON	AO	Analog Load Current Monitor. Use this pin for monitoring the output current. This pin cannot be left floating.
10	NC	-	No Connection.

NOTE: AI = analog input, AO = analog output, DO = digital output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{IMON} = 549Ω, SS, PG, PGTH, OUT are open, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply (IN)						
Under-Voltage Protection Threshold	V_{UVP_R}	Rising	2.46	2.55	2.64	V
	V_{UVP_F}	Falling	2.23	2.31	2.39	V
Supply Quiescent Current	I_{Q_ON}	V_{IN} = 12V		200	300	μA
Supply Quiescent Current during RCB	I_{Q_RCB}	V_{OUT} = V_{IN} + 1V		180		μA
Supply Disabled State Current	I_{Q_OFF}	V_{SD_F} < V_{EN} < V_{UVLO_R}		67	115	μA
Supply Shutdown Current	I_{SD}	V_{EN} < V_{SD_F}		8.0	21.0	μA
IN Supply Off Current	I_{Q_OVLO}	OVLO condition, V_{OUT} > V_{IN}		170	260	μA
IN Supply Leakage Current	I_{INLKG_IRPP}	V_{IN} = -14V, V_{OUT} = 0V		-13.0		μA
On-Resistance (IN - OUT)						
On-Resistance	R_{DSON}	V_{IN} = 12V, I_{OUT} = 3A, T_J = +25℃		29		mΩ
		V_{IN} = 12V, I_{OUT} = 3A, T_J = -40℃ to +125℃			48	
Enable/Under-Voltage Lockout (EN/UVLO)						
EN/UVLO Threshold	V_{UVLO_R}	Rising	1.185	1.210	1.235	V
	V_{UVLO_F}	Falling	1.065	1.090	1.115	V
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}		0.30	0.73		V
EN/UVLO Leakage Current	I_{ENLKG}		-0.7		0.7	μA
Over-Voltage Lockout (OVLO)						
OVLO Threshold	V_{OV_R}	Rising	1.185	1.210	1.235	V
	V_{OV_F}	Falling	1.065	1.090	1.115	V
OVLO Leakage Current	I_{OVLKG}	0.5V < V_{OVLO} < 1.5V	-0.9		0.9	μA
OUT Leakage Current	I_{OVLKG_OVLO}	OVLO condition, V_{OUT} > V_{IN}		1880	2700	μA
Fixed Fast-Trip (OUT)						
Fixed Fast-Trip Current Threshold	I_{FT}			22		A
Output Load Current Monitor (IMON)						
Analog Load Current Monitor Gain (I_{MON}: I_{OUT})	G_{IMON}	I_{OUT} = 0.5A to 1A	170	190	215	μA/A
		I_{OUT} = 1A to 5.5A	165	182	200	
Reverse Current Blocking (IN - OUT)						
V_{IN} - V_{OUT} Forward Regulation Voltage	V_{FWD}	I_{OUT} = 10mA	5	18		mV
V_{IN} - V_{OUT} Threshold for Fast BFET Turn Off	V_{REVTH}	Enter reverse current blocking	-42	-26	-10	mV
V_{IN} - V_{OUT} Threshold for Fast BFET Turn On	V_{FWDTH}	Exit reverse current blocking	40	110	170	mV
Reverse Leakage Current	I_{REVLKG_OFF}	Unpowered condition, V_{OUT} = 12V, V_{IN} = 0V		4.3		μA
	I_{REVLKG}	V_{OUT} - V_{IN} = 21.5V		6.0		μA
OUT Leakage Current during On-State with RCB	I_{OUTLKG_RCB}	V_{OUT} - V_{IN} = 1V		60		μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{IMON} = 549Ω, SS, PG, PGTH, OUT are open, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Good Indication (PG)						
PG Low Voltage While De-Asserted	V_{PGD}	V_{IN} < V_{UVP_F}, V_{EN} < V_{SD}, I_{PG} = 26μA		0.51	0.71	V
		V_{IN} < V_{UVP_F}, V_{EN} < V_{SD}, I_{PG} = 242μA		0.64	0.84	
		V_{IN} > V_{UVP_R}		0.0		
PG Leakage Current While Asserted	I_{PGLKG}			0.9	2.0	μA
Power Good Threshold (PGTH)						
PGTH Threshold	V_{PGTH_R}	Rising	1.175	1.210	1.245	V
	V_{PGTH_F}	Falling	1.055	1.090	1.125	V
PGTH Leakage Current	$I_{PGTHLKG}$		-1.5		1.5	μA
Over-Temperature Protection (OTP)						
Thermal Shutdown Rising Threshold	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			10		℃
SS						
SS Pin Charging Current	I_{SS}		0.90	2.20	3.50	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	V_{OVLO} > V_{OV_R} to V_{OUT}↓		1.2		μs
Fixed Fast-Trip Response Time	t_{FT}	I_{OUT} > I_{FT} to I_{OUT}↓		500		ns
Reverse Current Blocking Recovery Time	t_{SWRCB}	V_{IN} - V_{OUT} > V_{FWDTH} to V_{OUT}↑		50		μs
Reverse Current Blocking Comparator Response Time	t_{RCB}	V_{OUT} - V_{IN} > 1.3 × V_{REVTH} to BFET OFF		1		μs
PG Assertion De-Glitch Time	t_{PGA}			12		μs
PG De-Assertion De-Glitch Time	t_{PGD}			12		μs

SWITCHING CHARACTERISTICS

In the entire normal voltage range, the output voltage rise rate is set by the internal circuit and remains unchanged to ensure that the load state does not affect the start-up sequence. Adding capacitance between the SS pin and GND can change the OUT rising slope. Increasing capacitor C_{SS} will reduce the rate of rise (SR) of the output voltage. For a detailed description, please refer to the relevant sections on inrush current suppression (SS) and slew rate. However, the time that V_{OUT} falls when the device is turned off is determined by the RC time constants of the load resistor (R_L) and load capacitor (C_{OUT}). The control of the switch only affects the power-on sequence when the chip is turned on.

(R_L = 100Ω, C_{OUT} = 1μF, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	V_{IN}	C_{SS} = Open	C_{SS} = 1800pF	C_{SS} = 3300pF	UNITS
Output Rising Slew Rate	SR_{ON}	2.7V	11.85	1.10	0.62	V/ms
		12V	31.87	1.21	0.66	
		23V	50.83	1.23	0.67	
Turn-On Time	t_{ON}	2.7V	0.26	1.06	1.75	ms
		12V	0.33	1.85	3.40	
		23V	0.34	2.78	4.84	
Rise Time	t_R	2.7V	0.18	1.98	3.49	ms
		12V	0.30	7.91	14.29	
		23V	0.36	14.95	27.46	
Turn-On Delay	t_{D_ON}	2.7V	0.44	3.04	5.24	ms
		12V	0.69	9.76	17.69	
		23V	0.70	17.73	32.30	
Turn-Off Delay	t_{D_OFF}	2.7V	10.95	10.16	10.21	μs
		12V	6.67	6.66	6.73	
		23V	4.90	4.89	4.91	

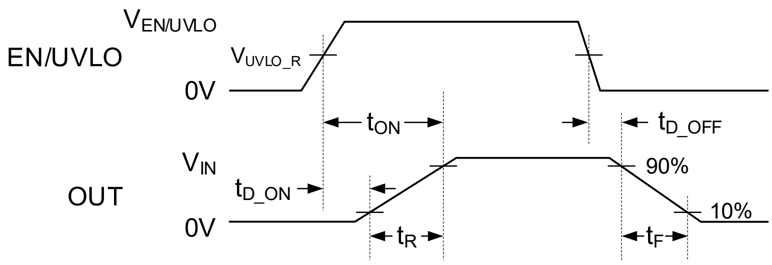
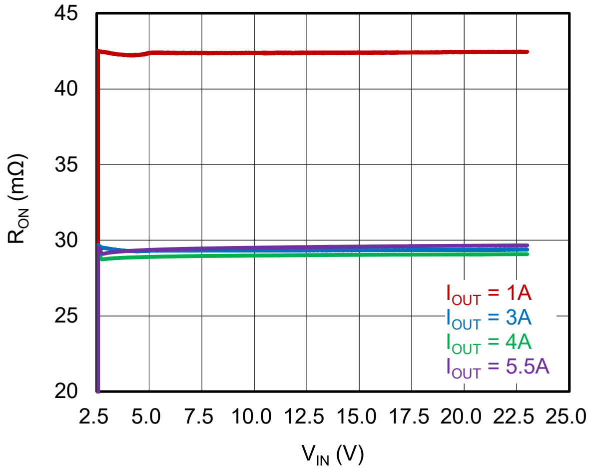


Figure 2. SGM2548 Switching Times

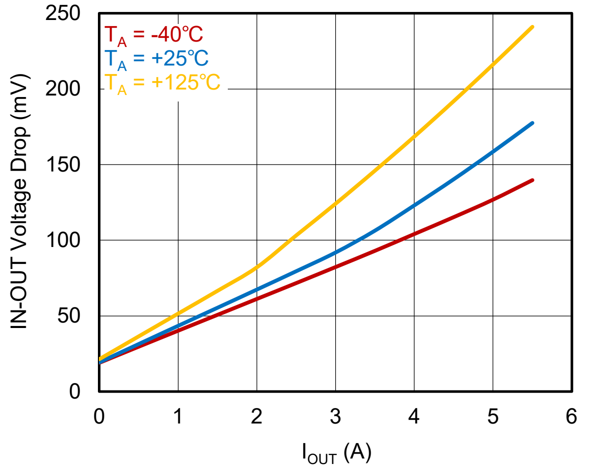
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

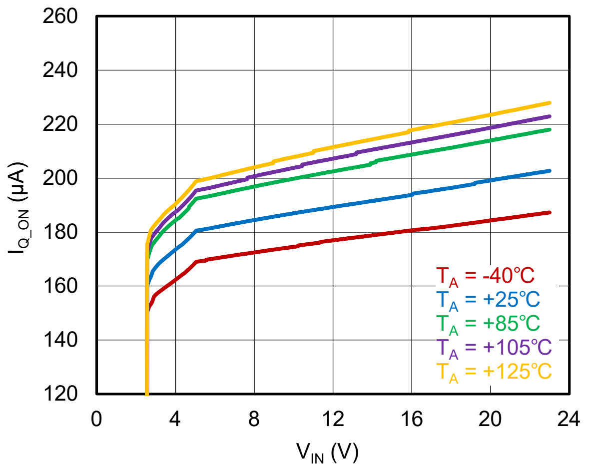
R_{ON} vs. V_{IN}



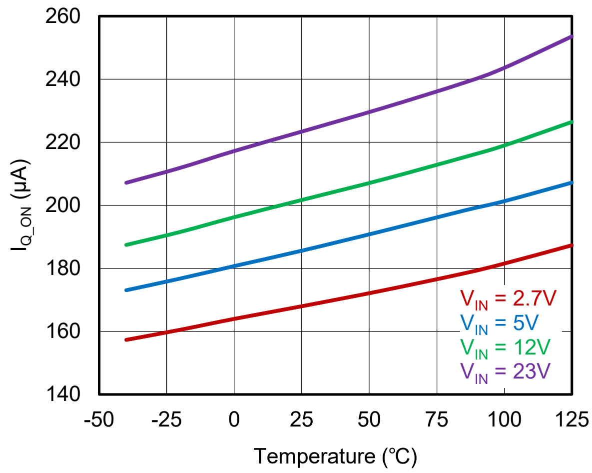
IN-OUT Voltage Drop vs. I_{OUT}



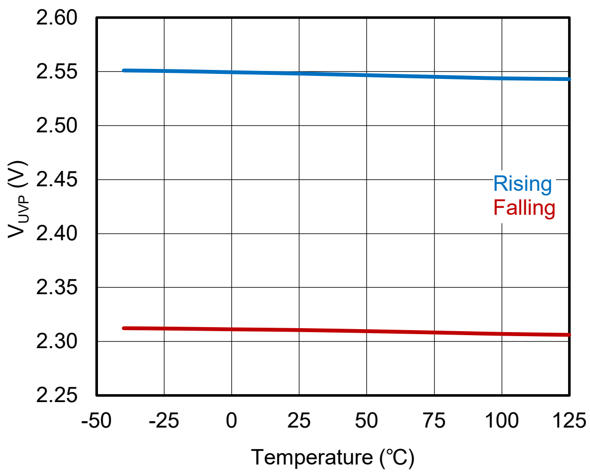
I_{Q_ON} vs. V_{IN}



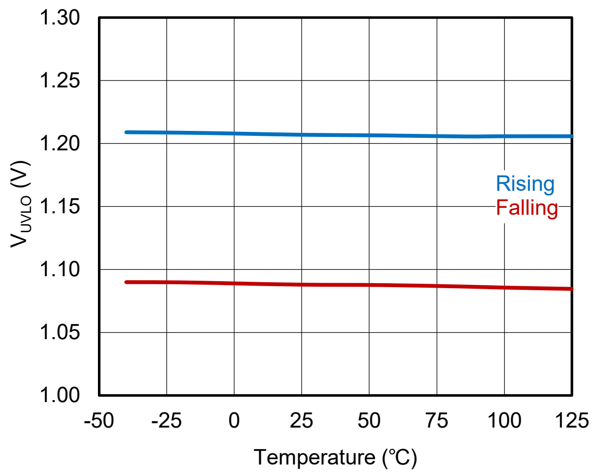
I_{Q_ON} vs. Temperature



V_{UVP} vs. Temperature

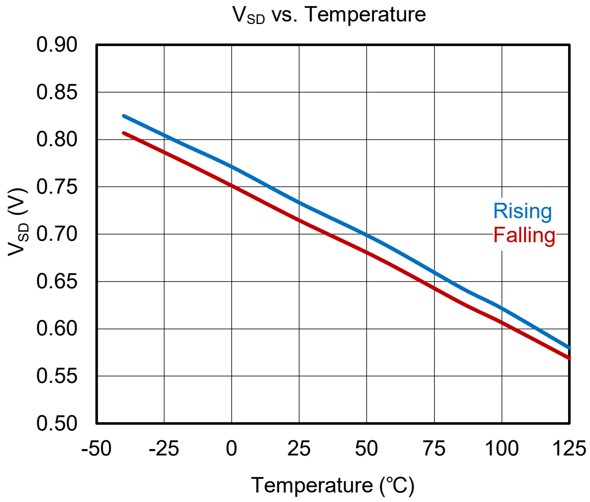


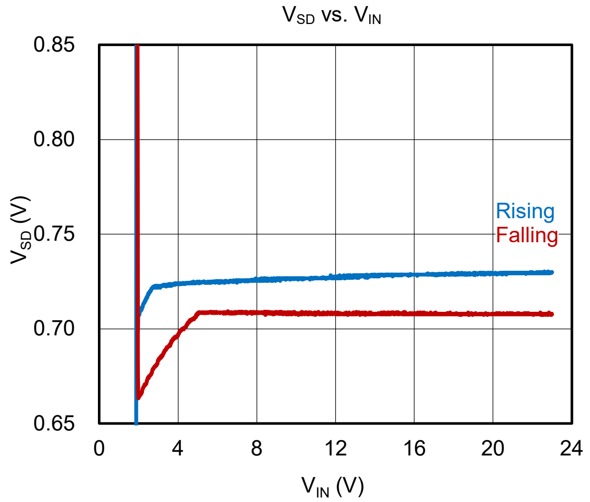
V_{UVLO} vs. Temperature

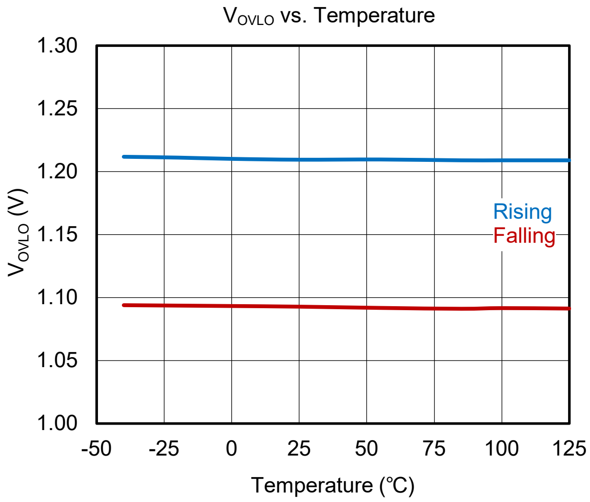


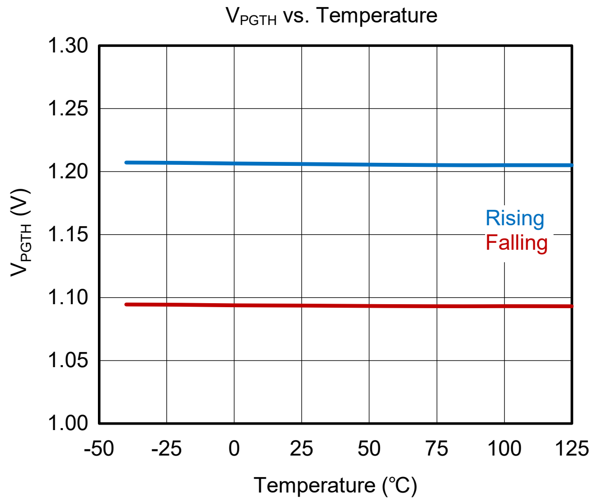
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

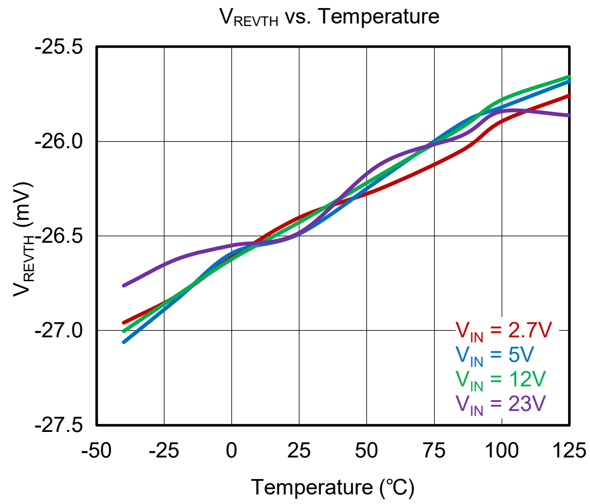
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

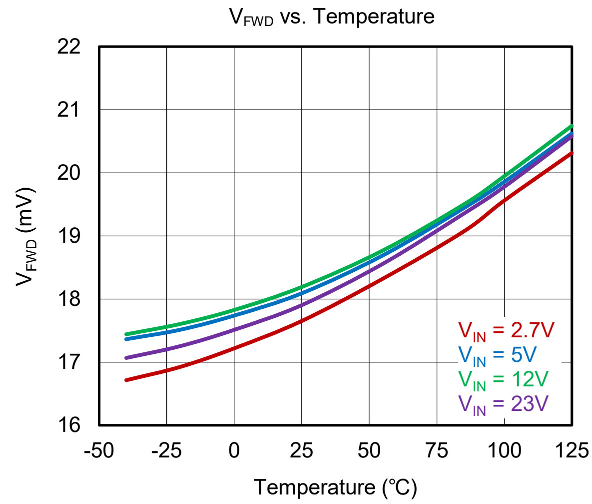






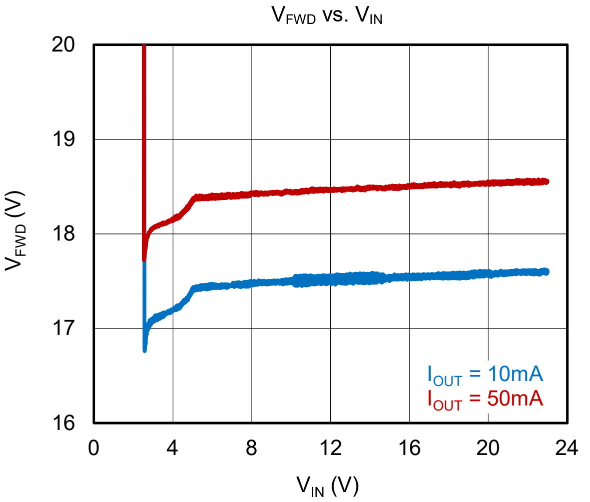


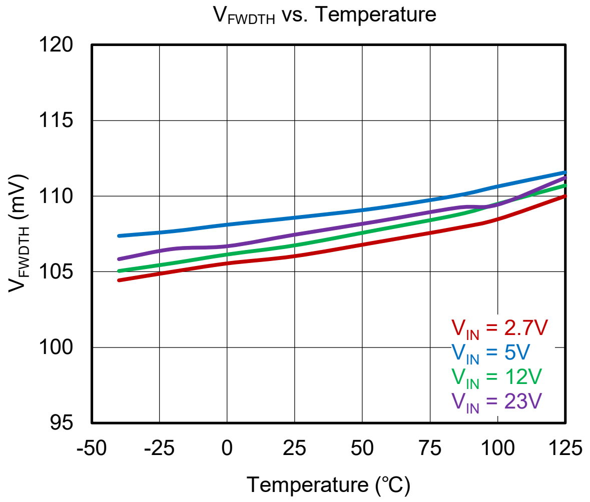


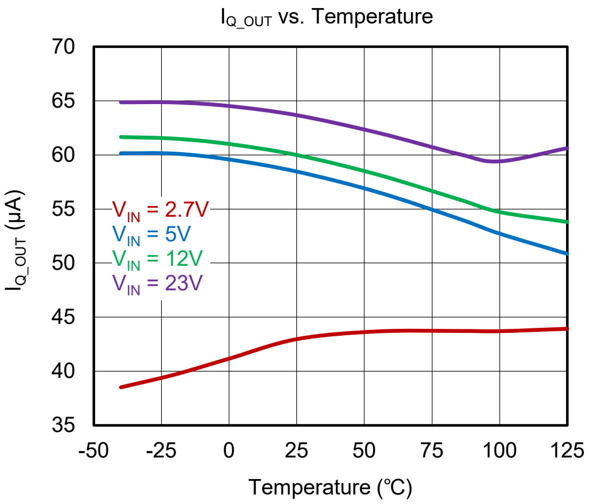


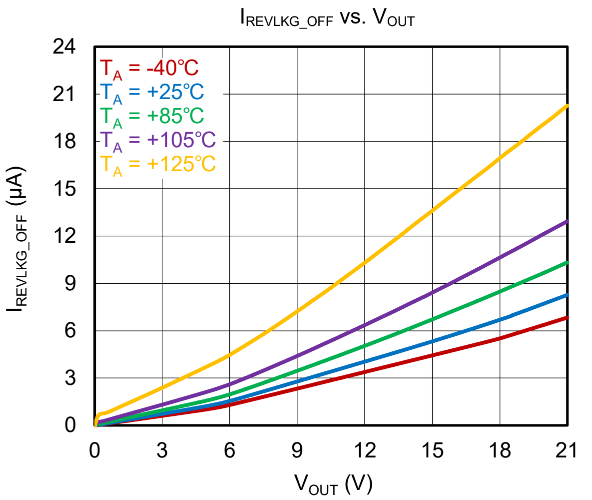
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

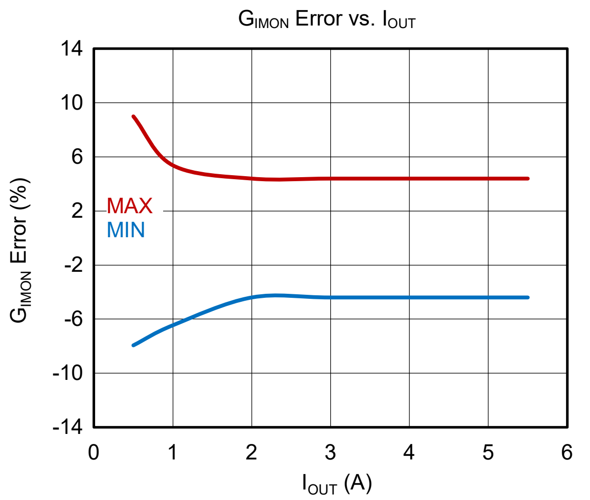
V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

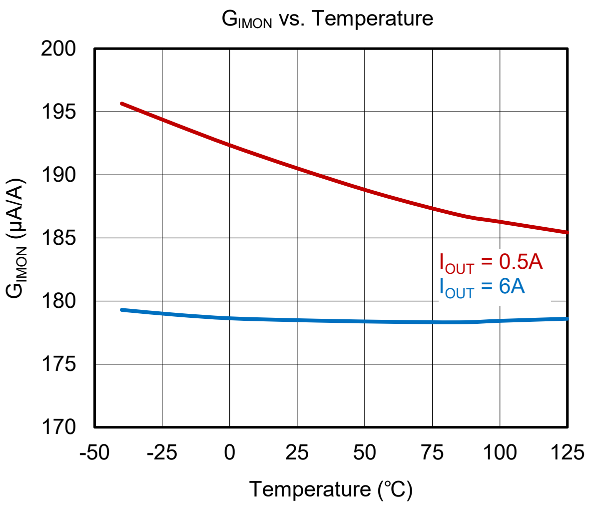








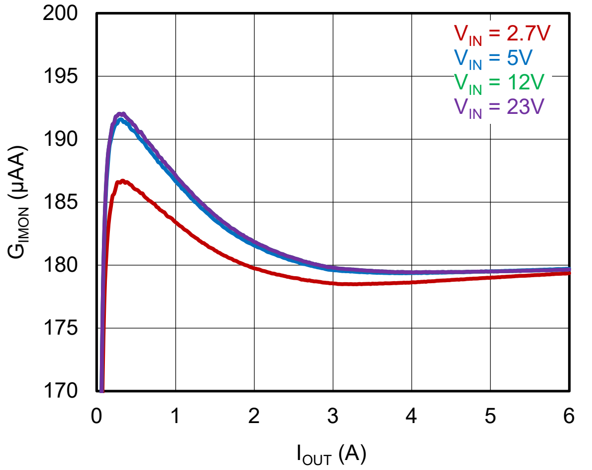




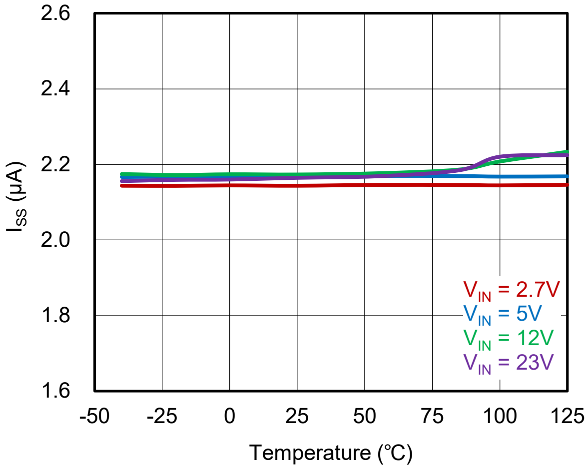
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

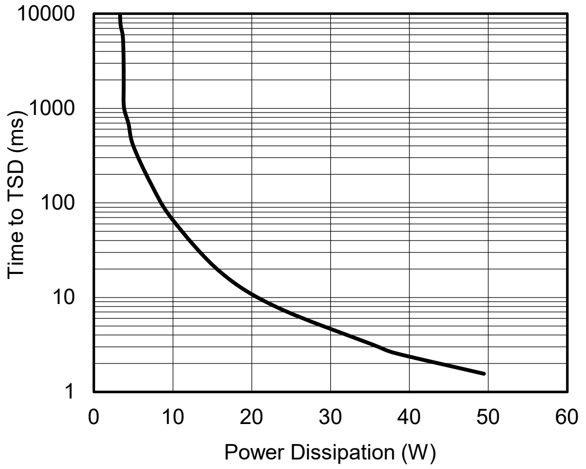
G_{IMON} vs. I_{OUT}



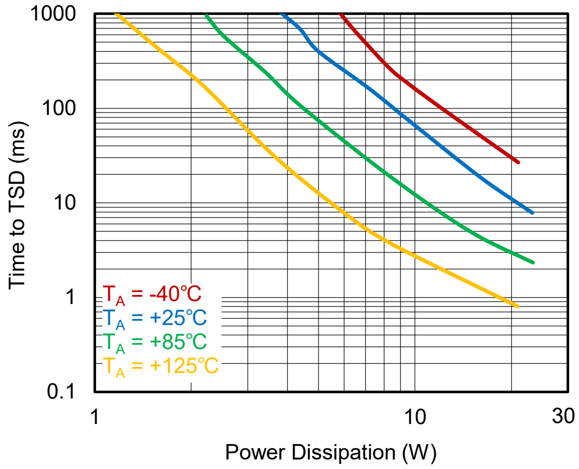
I_{SS} vs. Temperature



Time to TSD vs. Power Dissipation (Inrush State)



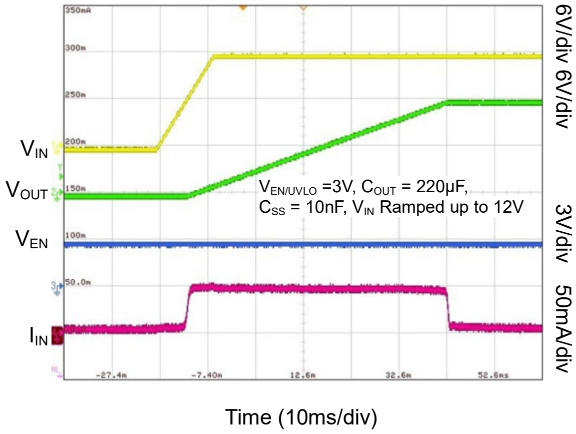
Time to TSD vs. Power Dissipation (Steady State)



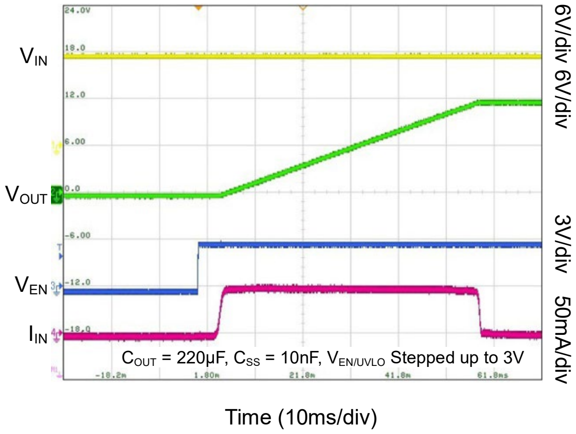
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, unless otherwise noted.

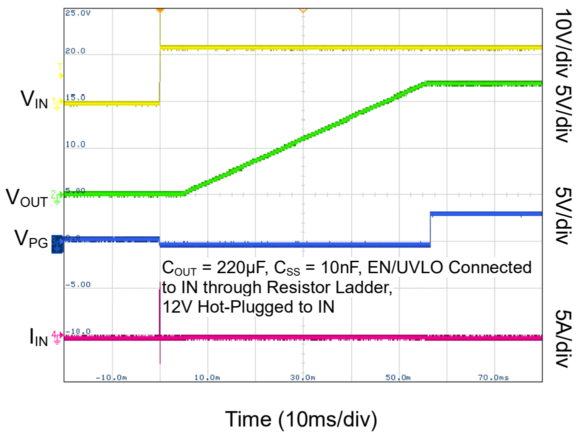
Start-Up with Supply



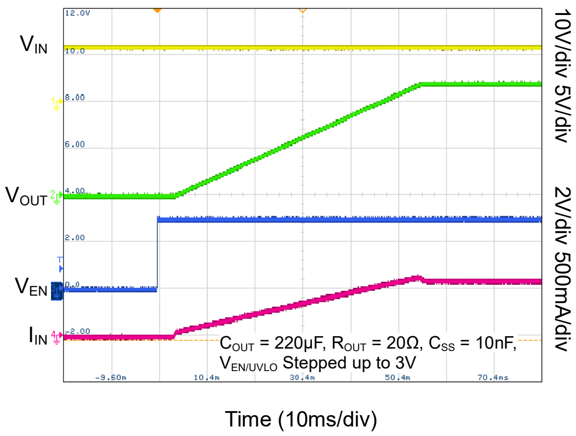
Start-Up with Enable



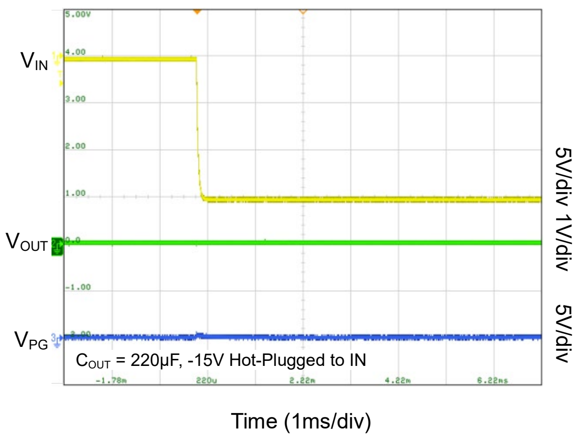
Input Hot-Plug



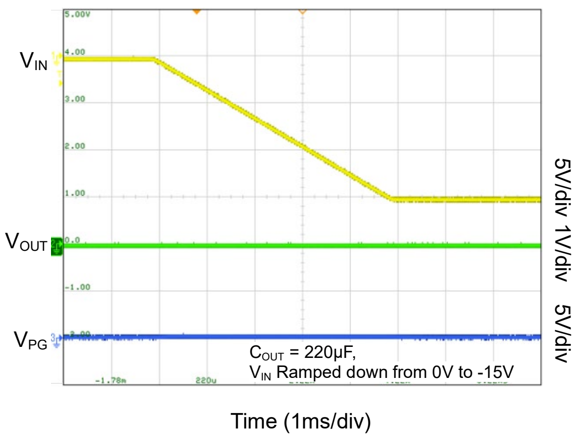
Inrush Current with Resistive and Capacitive Load



Input Reverse Polarity Protection - Fast Ramp



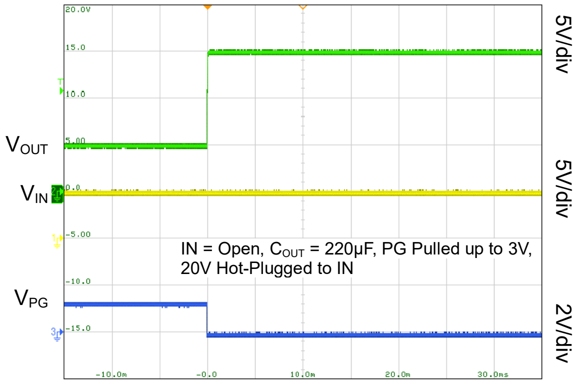
Input Reverse Polarity Protection - Slow Ramp



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

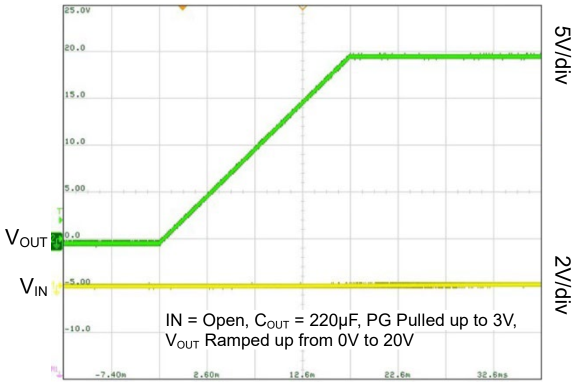
T_A = +25℃, unless otherwise noted.

Reverse Current Blocking Response in OFF State



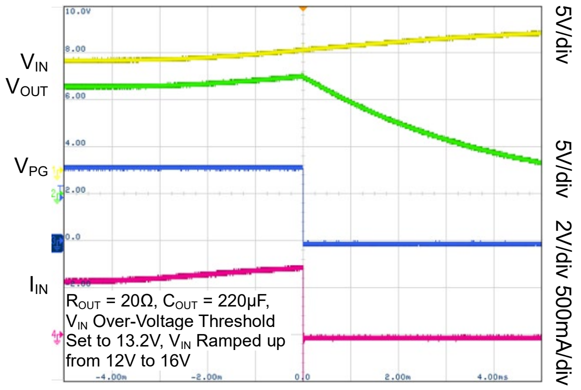
Time (2ms/div)

Reverse Current Blocking Response in OFF State



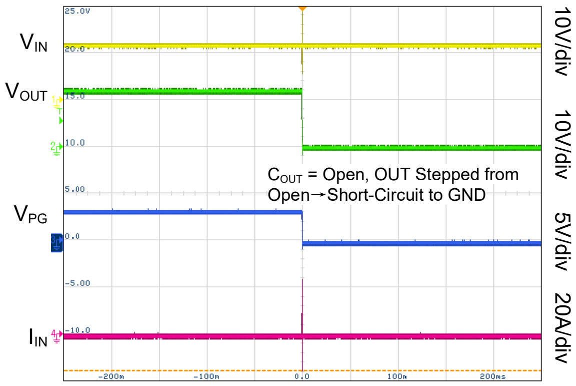
Time (5ms/div)

Over-Voltage Lockout Response



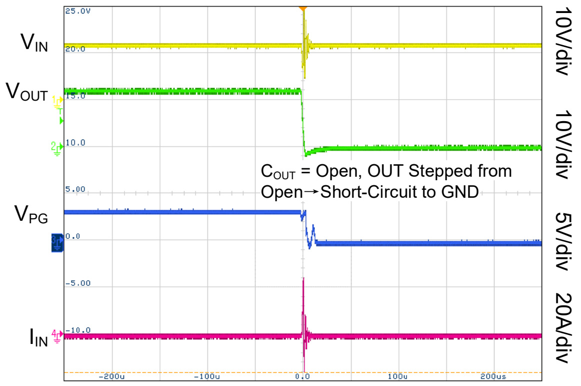
Time (1ms/div)

Fast-Trip Response During Steady State



Time (50ms/div)

Fast-Trip Response during Steady State (Zoomed)



Time (50μs/div)

BLOCK DIAGRAM

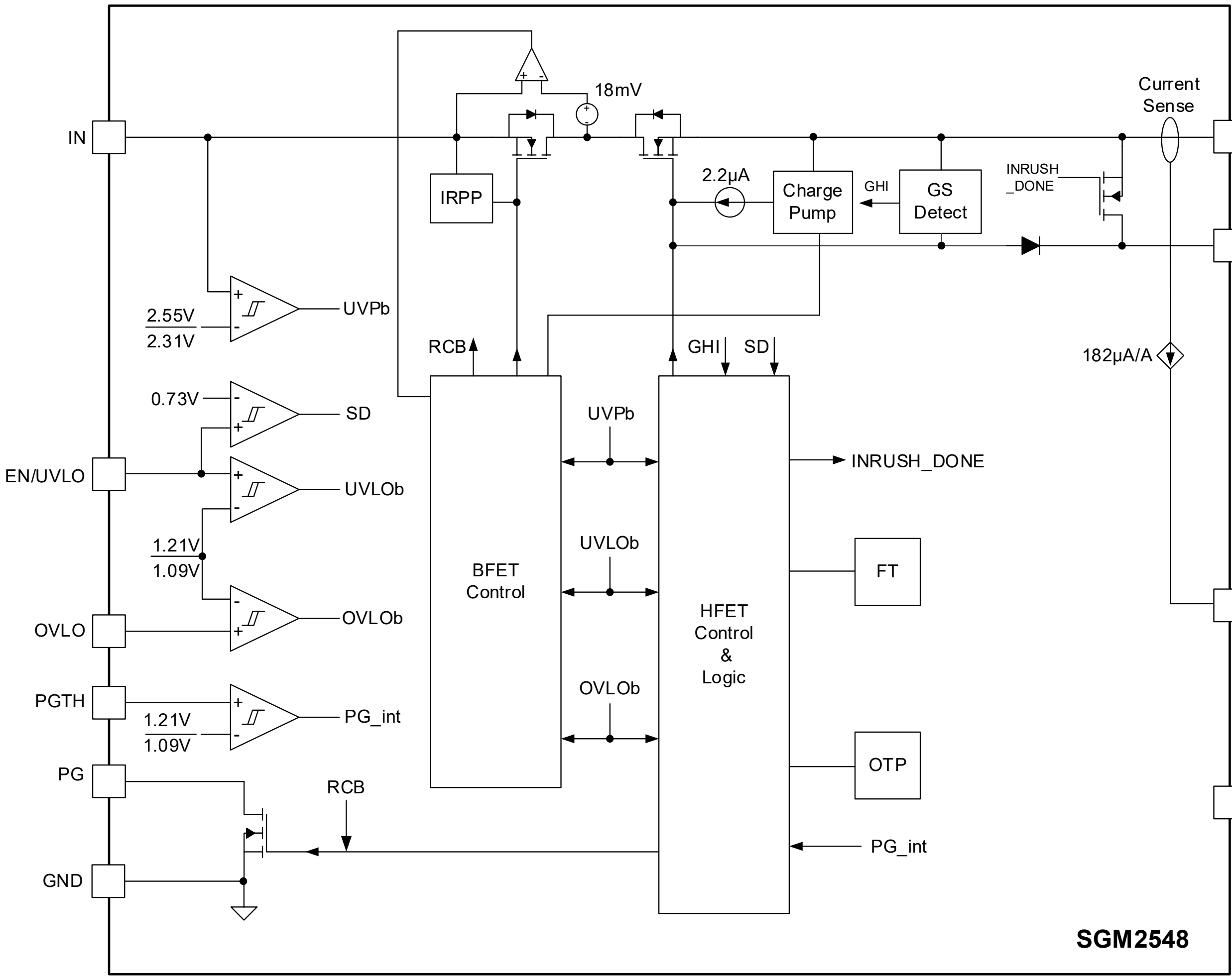


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM2548 is an eFuse with internal integration of FET. It ensures the safety of the power delivery system due to its rich features. When the V_{IN} is greater than V_{UVP_R}, the device starts to sample the voltage of the EN/UVLO pin ($V_{EN/UVLO}$). If $V_{EN/UVLO}$ exceeds V_{UVLO_R}, the internal FET starts conducting and the current can flow from IN to OUT. When the V_{IN} is less than V_{UVP_F} or $V_{EN/UVLO}$ < $V_{UVLO\_F,}$ the internal FET is turned off. Protection against reverse input voltage is maintained by keeping the power path in the OFF state.

After device start-up, the SGM2548 will monitor the VIN and forward current (from IN to OUT). During over-voltage event, the output voltage will be cut-off if it exceeds the user-adjustable over-voltage lockout threshold (V_{OVLO}). The fast-trip response of the device can provide rapid protection against serious over-current during short-circuit of OUT pin, so as to prevent the system from being damaged by harmful voltage and current.

The device integrates a reverse-current-blocking FET (BFET) that functions as an ideal diode. During forward conduction, the BFET is linearly regulated to maintain a constant low forward voltage drop (V_{FWD}). If V_{OUT} exceeds V_{IN}, the BFET shuts off completely to block reverse current.

The device incorporates an integrated thermal shutdown circuit. When the junction temperature (T_J) exceeds specified operational limits, this protection circuitry automatically disables the device to prevent thermal damage.

Designed for robust system protection, the compact SGM2548 integrates fault detection, protective responses, and status indication capabilities to safeguard power delivery during abnormal operating conditions.

Input Reverse Polarity Protection

The SGM2548 features integrated reverse-polarity protection at its input supply pin. It blocks negative voltages (down to -15V or V_{OUT} - 21V, whichever is higher) from reaching the output, safeguarding downstream circuits. No reverse current flows from output to input during such events. For signal pins connected to V_{IN} (EN/UVLO, OVLO, PGTH), use sufficiently large pull-up resistors to limit fault current. Refer to Absolute Maximum Ratings for details.

Under-Voltage Lockout (UVLO and UVP)

The SGM2548 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage (V_{UVP}) is provided inside the device for under-voltage protection. In addition, the comparator on the EN/UVLO terminal can be used to set the user-adjustable under-voltage protection threshold through the external resistor divider. Figure 6 and Equation 1 show how to set the specific value of under-voltage protection threshold using an external resistor divider.

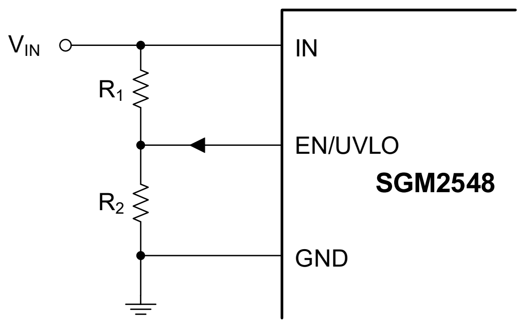


Figure 4. Adjustable Under-Voltage Protection

$$V_{IN\_UV} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \tag{1}$$

DETAILED DESCRIPTION (continued)

Over-Voltage Lockout (OVLO)

The SGM2548 implements over-voltage lockout at OVLO pin to prevent IN voltage from being too high for normal operation of system and equipment. The comparator on the OVLO pin is used to set the user-adjustable over-voltage protection threshold through the external resistor divider. If the voltage of OVLO pin exceeds the V_{OV_R}, the device will shut down the power path. When the voltage of OVLO pin is lower than the V_{OV_F}, the power path will be reopened with inrush control. There is a hysteresis between the rising threshold and falling threshold of OVLO. The Equation 2 and Figure 7 show how to set the specific value of over-voltage protection threshold using an external resistor divider.

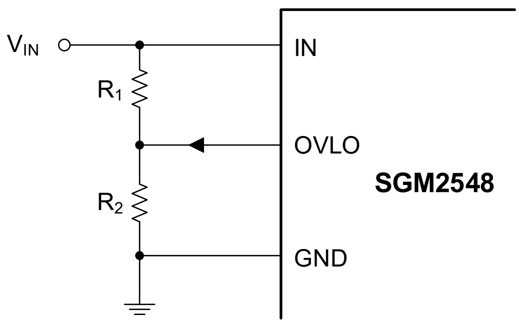


Figure 5. Adjustable Over-Voltage Protection

$$V_{IN\_OV} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

While recovering from an OVLO event, the SGM2548 start up with inrush control (SS).

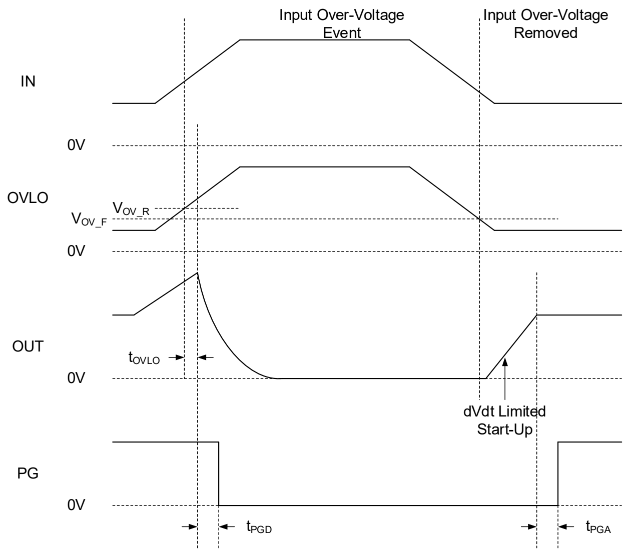


Figure 6. SGM2548 Over-Voltage Lockout and Recovery

Inrush Current, Over-Current, and Short Circuit Protection

SGM2548 adopts two levels of forward over-current protection function:

1. Programmable slew rate (SR) for inrush current protection.

2. Fixed I_{FT} for fast-trip function when short-circuit of OUT occurs.

Slew Rate (SS) and Inrush Current Control

When hot-plug or system charging large capacitive load occurs, a large inrush current is generated in the equipment power path. The input connector may be damaged or the input power rail voltage may drop, which affects the normal operation and even restarts other equipment in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. For a given C_{OUT}, the relationship between the slew rate (SR) and inrush current (I_{INRUSH}) is shown in Equation 3:

$$SR(V/ms) = \frac{I_{INRUSH}(mA)}{C_{OUT}(\mu F)} \quad (3)$$

The slew rate can be controlled by connecting a capacitor at the SS pin to reduce inrush current. For a given slew rate, the corresponding C_{SS} can be calculated by Equation 4.

$$C_{SS}(pF) = \frac{2200}{SR(V/ms)} \quad (4)$$

When the SS pin is left floating, the fastest output slew rate can be obtained.

DETAILED DESCRIPTION (continued)

Short-Circuit Protection

When a serious over-current event similar to a short-circuit event occurs, the SGM2548 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device. A fixed fast-trip threshold is set inside the device for fast protection against hard short-circuit events in steady state. The internal HFET will be completely turned off within t_{FT} if the current exceeds I_{FT}. Thereafter, the device remains latched-off until it is power cycled or re-enabled by toggling the EN/UVLO pin.

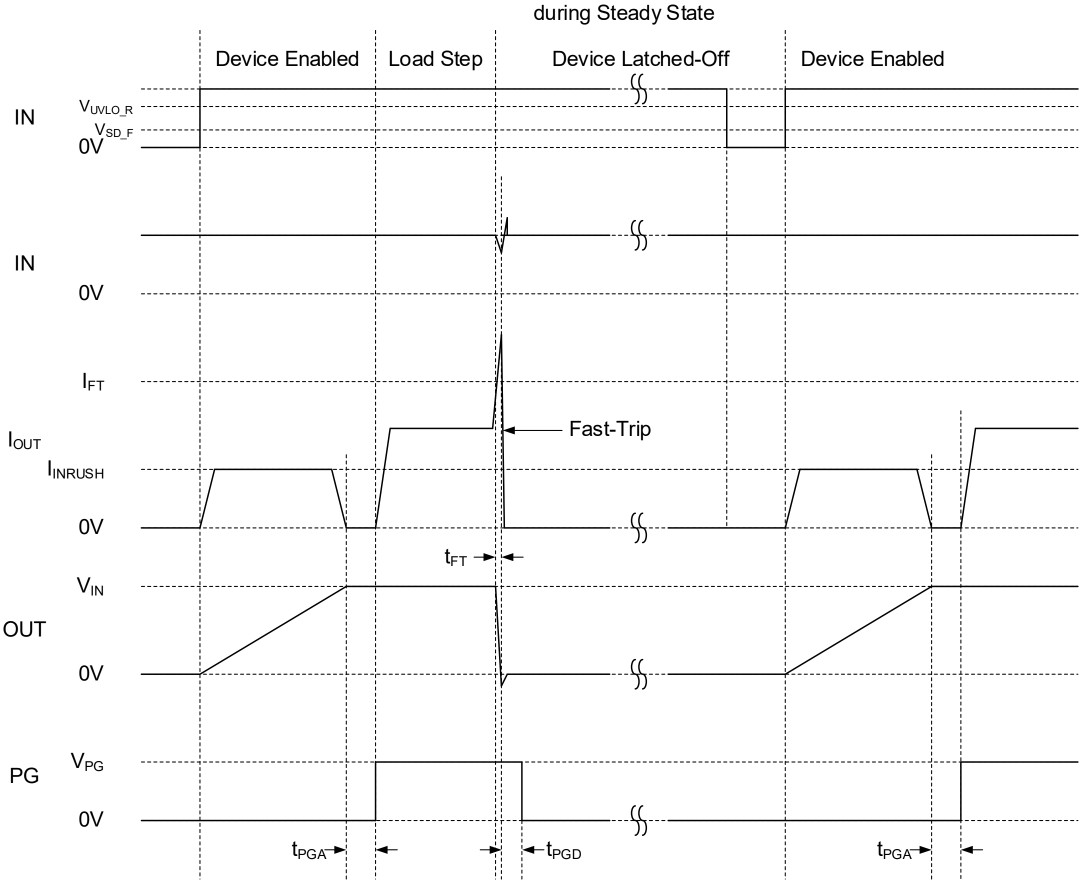


Figure 7. SGM2548 Short-Circuit Response

Analog Load Current Monitor

The device provides an analog current sensing output proportional to the load current at the IMON pin, which enables the device to monitor the load current (from IN to OUT). The user can calculate the load current through the voltage of the IMON pin connected to the R_{IMON}. The relationship between V_{IMON} and I_{OUT} is shown in Equation 5.

$$I_{OUT}(A) = \frac{V_{IMON}(\mu V)}{R_{IMON}(\Omega) \times G_{IMON}(\mu A / A)} \quad (5)$$

The waveform below shows the analog load current monitor response to a load step at the output.

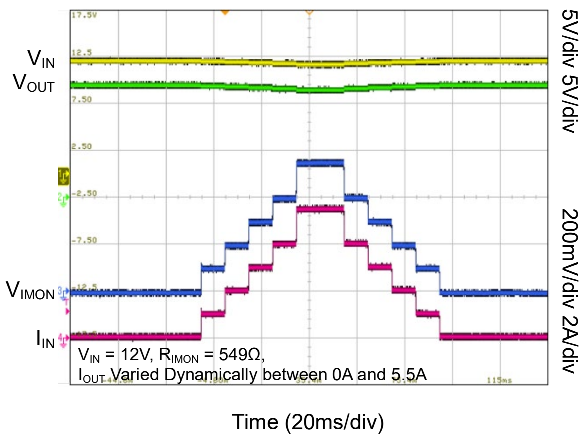


Figure 8. Analog Load Current Monitor Response

DETAILED DESCRIPTION (continued)

Reverse Current Protection

The device operates as an ideal diode, preventing any reverse current from flowing from the OUT to IN terminal under all operating conditions. It incorporates integrated back-to-back MOSFETs arranged in a shared drain configuration. The voltage drop across the IN and OUT pins is continuously monitored, and the gate drive of the blocking FET (BFET) is dynamically adjusted to maintain the forward voltage drop at a set level, V_{FWD}. This closed-loop regulation method, known as linear ORing control, allows for smooth MOSFET turn-off during reverse current situations and guarantees the absence of DC reverse current conduction.

The device further incorporates a traditional comparator-based reverse current suppression system (V_{REVTH}) to enable accelerated reaction (t_{RCB}) against transient reverse currents. Upon activating reverse current protection, the system delays recovery until the forward voltage differential (V_{IN} - V_{OUT}) surpasses the V_{FWDTH} threshold, subsequently executing rapid restoration to full operational conductivity. This mechanism introduces a robust hysteresis effect to eliminate interference from power supply fluctuations or electrical noise on the protective response. The reactivation process from reverse current blocking exhibits exceptional speed (t_{SWRCB}), effectively mitigating voltage sag in critical implementations including supply MUXing/ORing and USB Fast Role Swap (FRS).

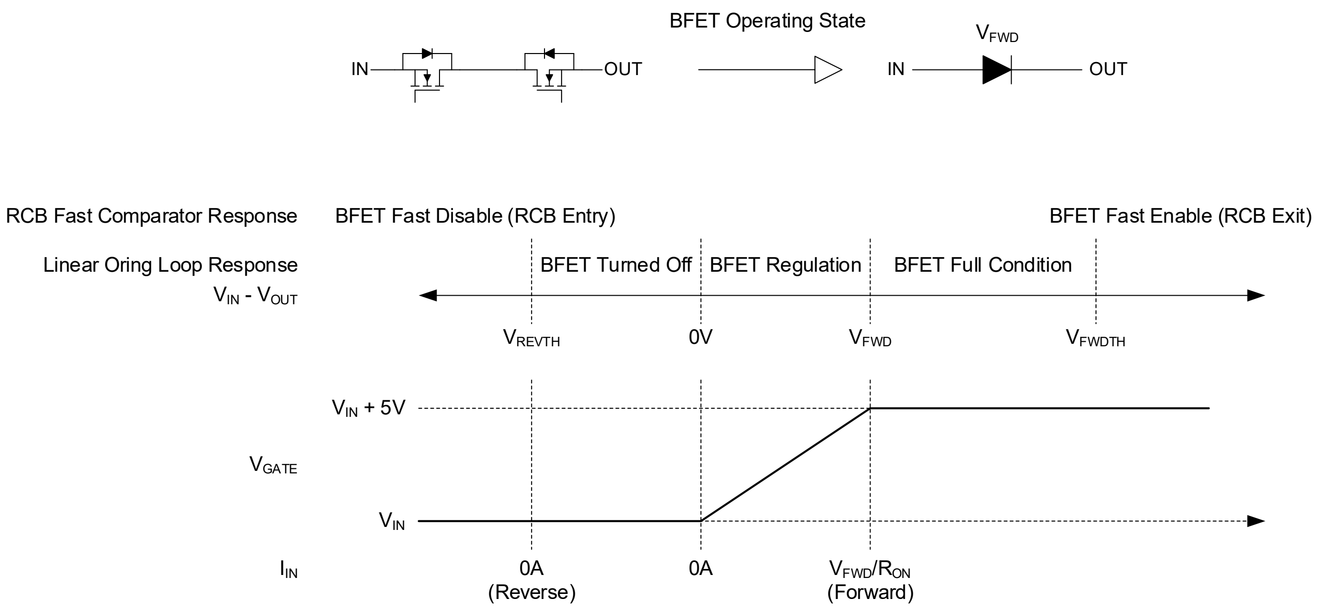


Figure 9. Reverse Current Blocking Response

The waveforms below demonstrate the reverse current blocking performance across different operating conditions.

When encountering rapid output voltage transients (such as hot-plug events), the rapid-response comparator-driven protection system maintains input stability by preventing significant voltage spikes or transient disturbances.

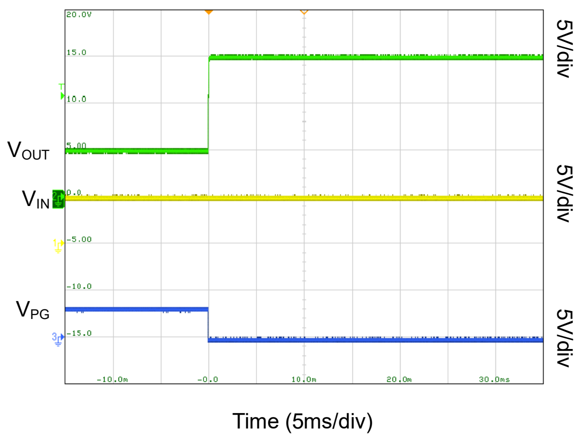


Figure 10. Reverse Current Blocking Performance during Fast Voltage Step at Output

DETAILED DESCRIPTION (continued)

When output voltages increase gradually, the linear ORing control architecture prevents DC reverse current conduction and maintains isolation between input and output terminals, effectively preventing input rail from getting slowly charged up by output voltage.

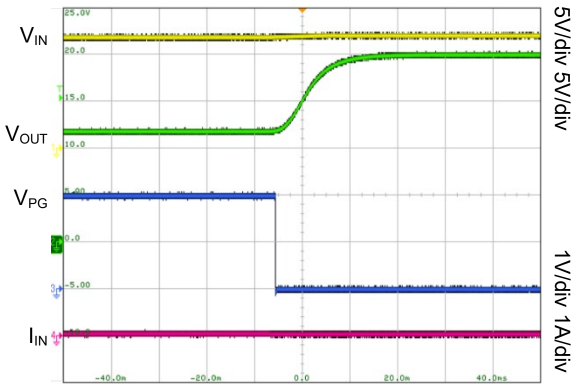


Figure 11. Reverse Current Blocking Performance during Slow Voltage Ramp at Output

The linear ORing configuration effectively suppresses reverse discharge pathways when input power becomes unavailable while energy storage components at output (such as bulk capacitors or super capacitors) remain at full charge potential. This operational principle optimizes energy preservation in reserve power systems by significantly reducing backward current transmission from output to input ports, thereby extending discharge latency periods for critical energy storage elements in during emergencies or power failures.

This feature also stops false power connection alerts in systems that sense input voltage to confirm whether an energy source remains properly connected.

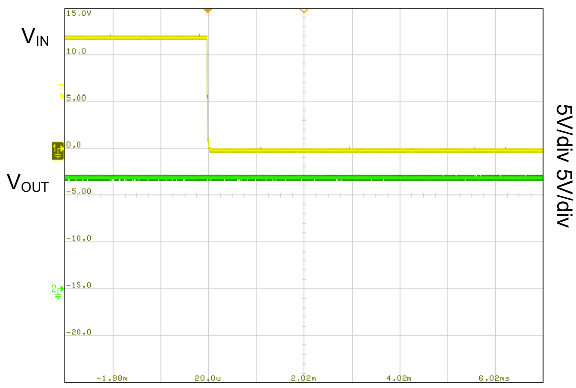


Figure 12. Reverse Current Blocking Performance during Input Supply Failure

Over-Temperature Protection (OTP)

The SGM2548 continuously monitors the temperature (T_J) of the internal die. Once the internal temperature exceeds the T_{SD}, the device shuts down immediately. The SGM2548 will not turn on until the internal temperature is lower than a safe threshold (T_{SD} - T_{HYS}).

When SGM2548 triggers the thermal shutdown, it shuts down and remains latched-off until V_{IN} power cycle or external reset.

Table 1. Thermal Shutdown

DEVICE	ENTER TSD	EXIT TSD
SGM2548	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} cycled to 0V and then above V_{UVP_R} OR EN/UVLO toggled below V_{SD_F}

Fault Response

Table 2 shows the protection response of equipment under different fault conditions.

DETAILED DESCRIPTION (continued)

Table 2. Fault Summary

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY
Over-Temperature	Shutdown	Y
Under-Voltage (UVP or UVLO)	Shutdown	N
Input Reverse Polarity	Shutdown	N
Input Over-Voltage	Shutdown	N
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	Reverse Current Blocking	N
Transient Over-Current during Steady State	Shutdown	Y

An internally latched fault can be cleared by power cycling (pulling V_{IN} to 0V) or re-enable (pulling EN/UVLO pin below V_{SD}).

During a latched fault, pulling the EN/UVLO just below the UVLO threshold cannot clear the latched fault.

Power-Good Indication (PG)

The SGM2548 provide an active-high open-drain output (PG) as the indication pin of power good. It is asserted as high according to the PGTH pin voltage and the device working state. PG pin needs to be pulled up to an external power supply.

At the initial stage of power-on, PG is pulled down. Then the device enters the start-up sequence, in which the internal HFET has been controlled and not fully conductive. When the gate voltage of the internal HFET reaches overdrive, it is fully conductive and the start-up sequence is completed, V_{PGTH} is higher than V_{PGTH_R}, and PG is asserted high after a de-glitch time (t_{PGA}).

The PG will be de-asserted when the PGTH voltage falls below V_{PGTH_F} or when the system has some faults. The de-glitch time is t_{PGD}, when PG is de-asserted.

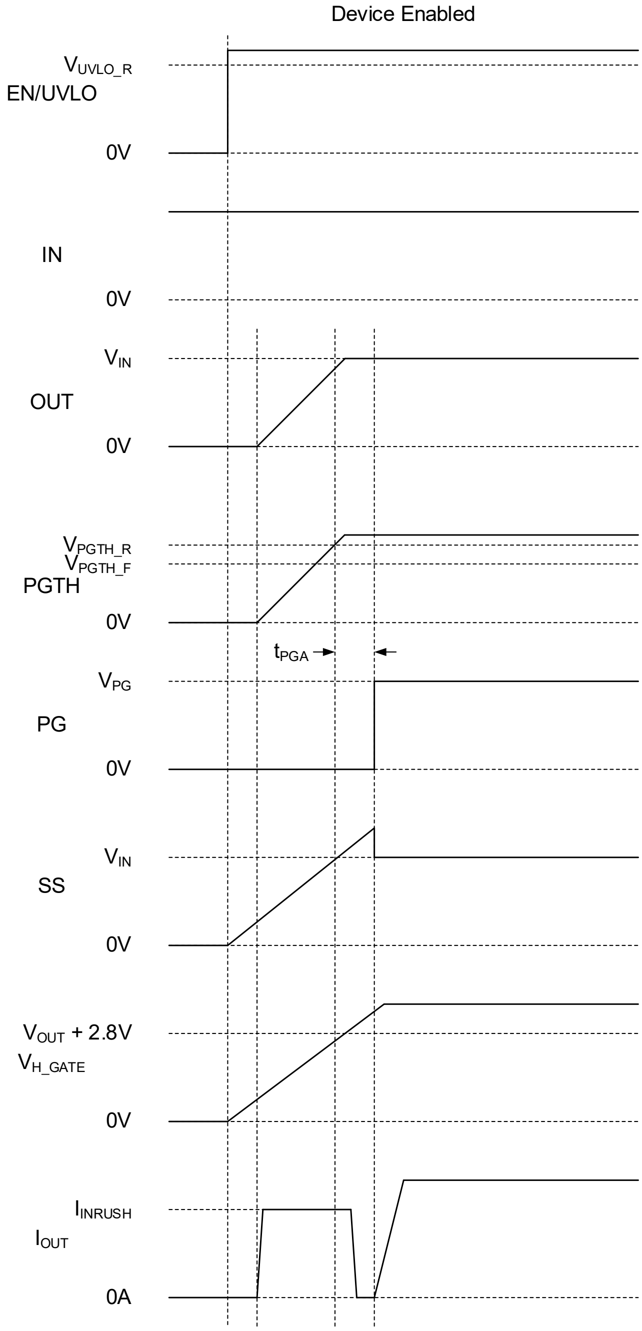


Figure 13. SGM2548 PG Timing Diagram

DETAILED DESCRIPTION (continued)

Table 3. SGM2548 PG Indication Summary

EVENT	DEVICE STATUS	PG PIN STATUS	PG PIN TOGGLE DELAY
Under-Voltage UVP or UVLO)	Shutdown	L	
Input Reverse Polarity	Shutdown	L	
Over-Voltage (OVLO)	Shutdown	L	t_{PGD}
Steady State	N/A	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Transient Over-Current during Steady State	Fast-Trip	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	Reverse Current Blocking	L	t_{PGD}
Over-Temperature	Shutdown	L	t_{PGD}

When the device is not powered, the PG pin should be low. However, there is no effective power supply to drive the PG pin down to GND in this case. If the PG is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the PG caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the PG. In order to avoid the small voltage on the PG pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized.

Device Functional Modes

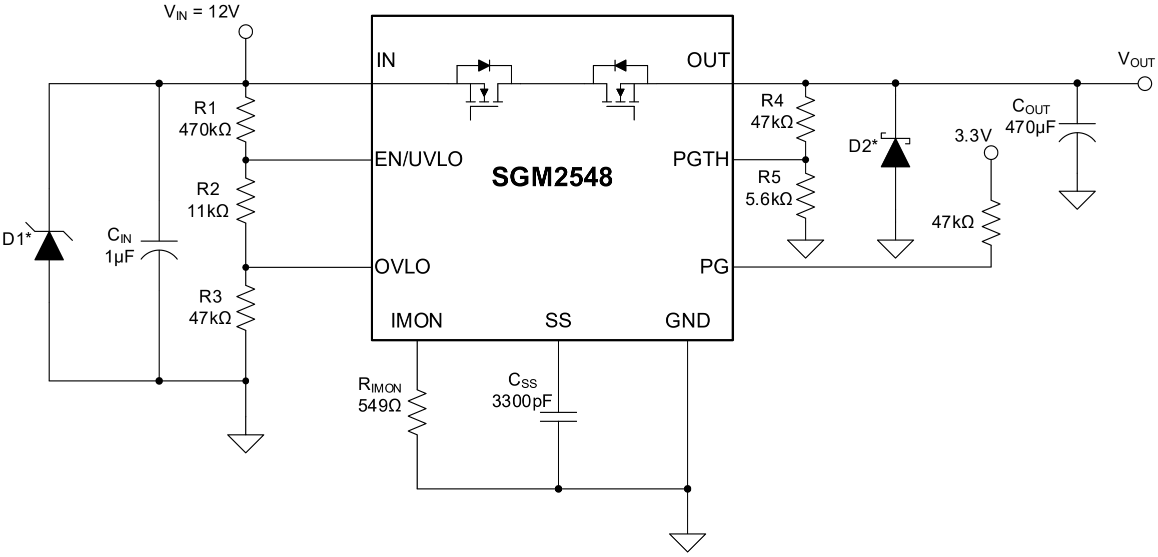
The SGM2548 have only one functional mode within the recommended operating conditions.

APPLICATION INFORMATION

The information in the following application section is not within the scope of SGMICRO's device specifications. SGMICRO does not guarantee the accuracy and completeness of this information. The customers of SGMICRO are responsible for determining whether the devices are suitable for their applications. The client should verify and test their design to ensure the functionality of the system.

Typical Application

The SGM2548 is an integrated 5.5A ideal diode that is typically used for power rail monitoring and protection applications. It operates from 2.7V to 23V with adjustable overvoltage and under-voltage protection. It provides ability to control inrush current and protection against input reverse polarity as well as reverse current conditions. It also has integrated analog load current monitoring and digital power good indication with adjustable threshold. It can be used in a variety of systems such as set-top boxes, smart speakers, handheld power tools/chargers, PC/notebooks and Retail ePOS (Point-of-sale) terminals.



* Supplementary circuit elements for transient protection may be required, with their necessity determined by the specific input and output inductance values. Detailed guidelines are provided in the Transient Protection section.

Figure 14. AC-DC Adapter Powered System - Barrel Jack Input Protection

Design Requirements

Table 4. Design Parameters

PARAMETER	VALUE
Adapter Nominal Output Voltage (V_{IN})	12V
Maximum Input Reverse Voltage	-12
Under-Voltage Threshold (V_{IN_UV})	10.8V
Over-Voltage Threshold (V_{IN_OV})	13.2V
Output Power-Good Threshold (V_{PG})	11.4V
Max Continuous Current	5A
Analog Load Current Monitor Voltage Range (V_{IMON_MAX})	0.5V
Output Capacitance (C_{OUT})	470μF
Output Rise Time (t_R)	20ms

Detailed Design Procedure

Setting Under-Voltage and Over-Voltage Thresholds

Resistors R1, R2, and R3 determine the supply's under-voltage and over-voltage thresholds, with their values derived from Equation 6 and Equation 7:

$$V_{IN\_UV} = \frac{V_{UVLO\_R} \times (R1 + R2 + R3)}{R2 + R3} \tag{6}$$

$$V_{IN\_OV} = \frac{V_{OV\_R} \times (R1 + R2 + R3)}{R3} \tag{7}$$

APPLICATION INFORMATION (continued)

Resistors R1, R2, and R3 establish both the under-voltage (V_{UVLO_R}) and over-voltage (V_{OVLO_R}) rising thresholds. Since these resistors draw current from the input supply (V_{IN}), their selection must account for permissible leakage current. The combined current through these resistors is calculated as $I_{R123} = V_{IN}$ / (R1 + R2 + R3). Note that leakage currents from external active components connected to this resistor network may introduce inaccuracies in these calculations. Therefore, the current through the resistor string (I_{R123}) should be designed to exceed the anticipated leakage current at the EN/UVLO and OVLO pins by a factor of 20.

Based on the device's technical specifications, the maximum leakage current for both the EN/UVLO and OVLO pins is 0.9μA (MAX), while the rising thresholds for OVLO and UVLO are both 1.21V. Per the design requirements, the over-voltage input (V_{IN_OV}) is set to 13.2V and the under-voltage input (V_{IN_UV}) to 10.8V. To determine the resistor values, start by assigning R1 as 470kΩ, then utilize the provided equations to calculate R2 as 10.7kΩ and R3 as 48.5kΩ.

Using the closest standard 1% resistor values, we get R1 = 470kΩ, R2 = 11kΩ, and R3 = 47kΩ.

Setting Output Voltage Rise Time (t_R)

To achieve a reliable design, the junction temperature of the device must remain under the absolute maximum specified limit during both transient (start-up) and steady-state operation. Dynamic power dissipation during start-up is typically an order of magnitude higher than under static conditions, making it critical to calculate the optimal start-up time and inrush current limit relative to the system capacitance to prevent thermal shutdown during initialization.

The required slew rate (SR) to obtain the target output rise time is determined by the formula:

$$SR(V/ms) = \frac{V_{IN}(V)}{t_R(ms)} = \frac{12V}{20ms} = 0.6V/ms \quad (8)$$

The value of C_{SS} required to attain the specified slew rate is derived from the following formula:

$$C_{SS}(pF) = \frac{2200}{SR(V/ms)} = \frac{2200}{0.6} = 3666pF \quad (9)$$

Choose the nearest standard capacitor value as 3600pF.

Based on the specified slew rate, the corresponding inrush current can be determined using the formula:

$$I_{INRUSH}(mA) = SR(V/ms) \times C_{OUT}(\mu F) = 0.6 \times 470 = 282mA \quad (10)$$

The average power dissipated within the component during inrush conditions is determined by the following equation:

$$PD_{INRUSH}(W) = \frac{I_{INRUSH}(A) \times V_{IN}(V)}{2} = \frac{0.282 \times 12}{2} = 1.69W \quad (11)$$

To ensure reliable start-up, the thermal shutdown time of the device must surpass the ramp-up time t_R under the specified power dissipation conditions. According to *Time to T_{SD} vs. Power Dissipation (Inrush State)*, which outlines the thermal shutdown limit, the shutdown time exceeds 10 seconds for a power of 1.69W, significantly longer than the t_R value of 20ms. Consequently, a start-up time of 20ms is considered safe for this application.

Setting Power-Good Assertion Threshold

The resistors R4 and R5 connected to the PGTH pin determine the Power-Good assertion threshold, with their values derived from the formula:

$$V_{PG} = \frac{V_{PGTH\_R} \times (R4 + R5)}{R5} \quad (12)$$

To minimize leakage current from the output rail VOUT, resistors R4 and R5 must be carefully selected, as they draw current from the supply. The current through these resistors is defined as $I_{R45} = V_{OUT}$ / (R4 + R5). Note that external active components attached to this network may introduce additional leakage, potentially affecting calculation accuracy. Therefore, to ensure precision, the current through the resistor string (I_{R45}) should be set to a value at least 20 times larger than the anticipated leakage current at the PGTH pin.

Based on the device specs, the PGTH leakage current is 1.5μA (max), with a rising threshold voltage (V_{PGTH_R}) of 1.21V. The design requires V_{PG} = 11.4V. To compute the values, begin by setting R4 to 47kΩ, which yields R5 = 5.58kΩ. The nearest 1% standard value is R5 = 5.6kΩ.

APPLICATION INFORMATION (continued)

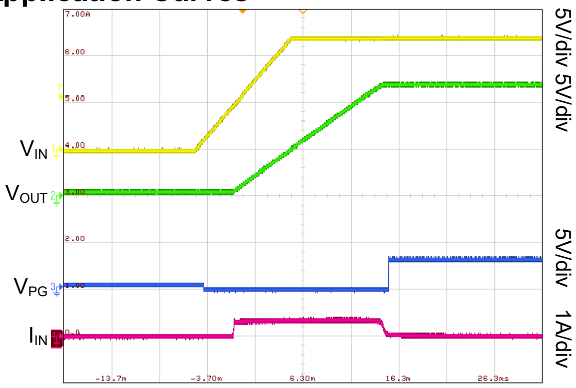
Setting Analog Current Monitor Voltage (IMON) Range

The analog current monitor voltage range can be set using the R_{IMON} resistor is determined by the formula:

$$R_{IMON}(\Omega) = \frac{V_{IMON\_MAX}(V) \times 10^{-6}}{I_{OUT\_MAX}(A) \times G_{IMON}(\mu A/A)} = \frac{0.5 \times 10^{-6}}{5 \times 182} = 549.5\Omega \quad (13)$$

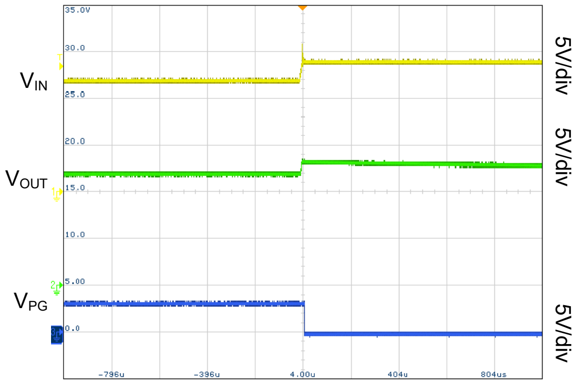
Choose nearest 1% standard resistor value as 549Ω.

Application Curves



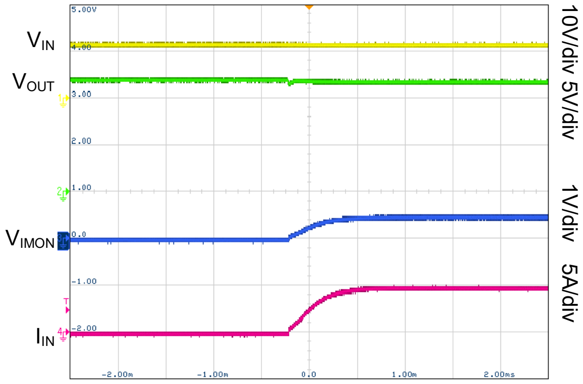
Time (5ms/div)

Figure 15. Power Up



Time (200μs/div)

Figure 16. Over-Voltage Protection



Time (500μs/div)

Figure 17. Analog Load Current Monitor Output

Active ORing

A typical redundant power supply topology is illustrated in Figure 18. Historically, Schottky ORing diodes have been the go-to solution for connecting parallel power sources, for example, pairing a wall adapter with a battery or a backup energy storage capacitor. This ORing requirement is also common in end-user equipment like PCs, notebooks, docking stations, and monitors, which often draw power from multiple USB ports and/or dedicated power adapters. However, ORing diodes suffer from a critical drawback: their inherent forward voltage drop leads to significant power dissipation and efficiency loss. The SGM2548, which integrates low-on-resistance back-to-back FETs, offers a streamlined, high-efficiency alternative. The figure below demonstrates how this device enables an active ORing implementation to address these limitations.

APPLICATION INFORMATION (continued)

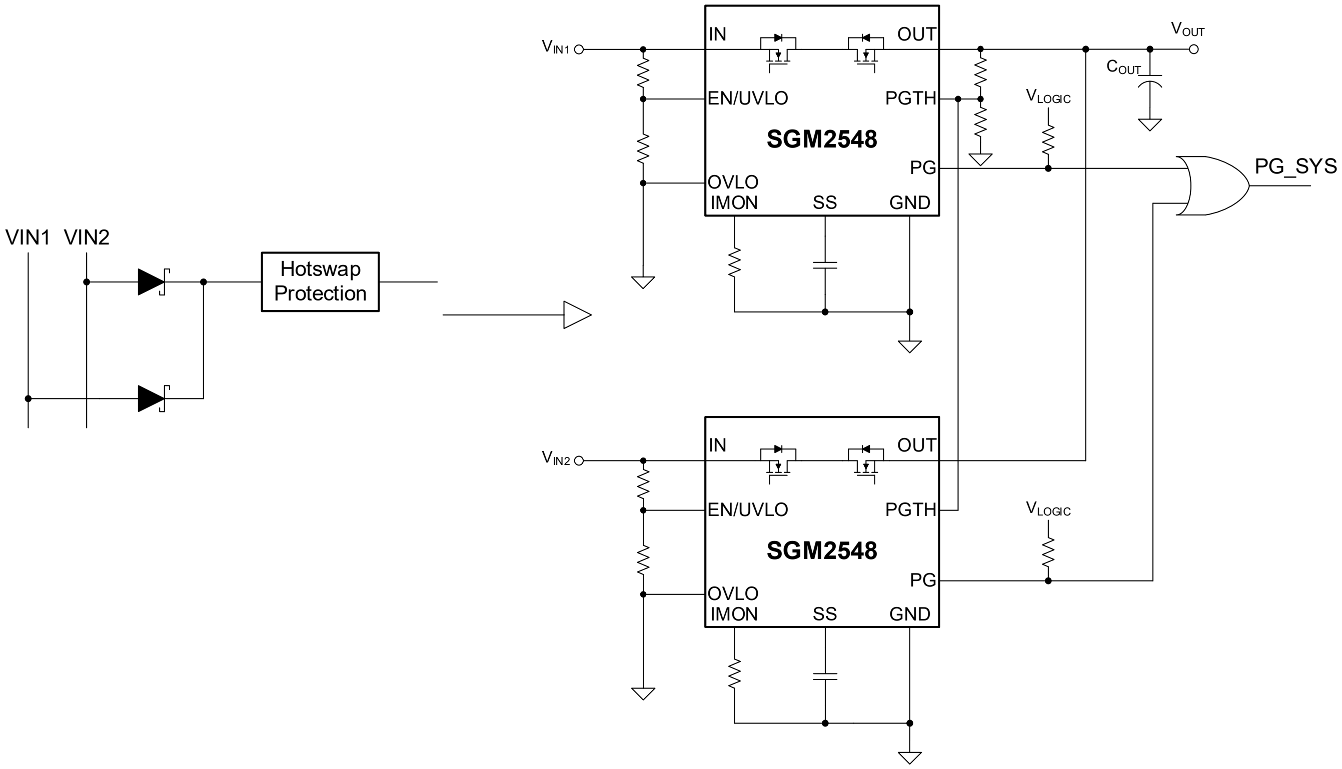


Figure 18. Two Devices, Active ORing Configuration

The linear ORing functionality in the SGM2548 prevents reverse current from transferring between power sources, regardless of whether the supply voltage ramps up quickly or slowly.

The subsequent waveform demonstrates the operation of active ORing during the sequential voltage increase of the supply rails.

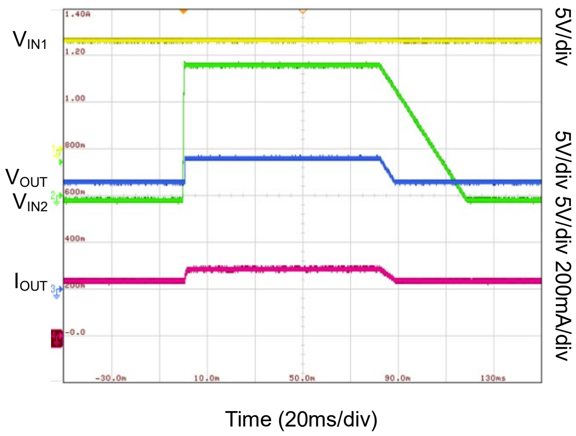


Figure 19. Active ORing Response

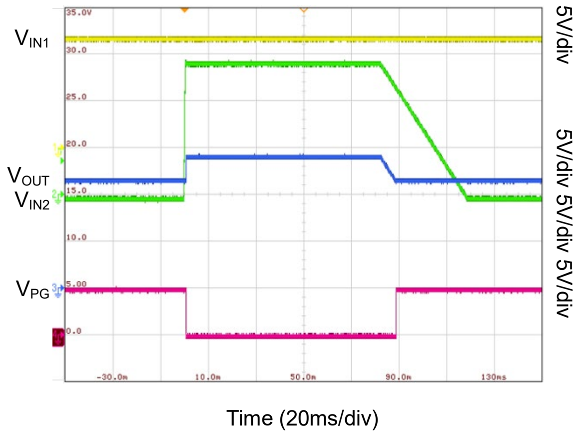


Figure 20. Active ORing Response

When the bus voltages (IN1 and IN2) are equal, the components in each pathway become forward-biased and conduct, supplying current to the load. Current distribution between the rails during this operation is proportional to the voltage differential present across each respective component.

Beyond performing supply ORing functions, these components continuously safeguard the system against over-voltage conditions, high inrush currents, overload situations, and short-circuit failures under all operating conditions.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The operational input voltage range for the SGM2548 devices is specified between 2.7V and 23V. A ceramic input bypass capacitor with a value exceeding 0.1μF is recommended if the supply is positioned more than a few inches away. The power supply must be specified to deliver currents beyond the set current limit to avoid droops under overcurrent or short-circuit events.

The device's input must not exceed a minimum negative voltage of -15V or V_{OUT} - 21V, whichever is greater. For low-voltage signals derived from the input supply (such as EN/UVLO, OVLO, and PGTH), a sufficiently large pull-up resistor must be used to ensure that the current through these pins remains below 10μA under reverse polarity conditions. For further information, please consult the Absolute Maximum Ratings table.

Transient Protection

During a short-circuit or overload current interruption event, the input inductance produces a positive voltage spike at the input, while the output inductance creates a negative voltage spike at the output. The magnitude of these voltage transients is determined by the amount of inductance in series with the device's input or output. Without adequate mitigation, such transients may exceed the absolute maximum ratings of the device. Common methods used to suppress these transients include:

- Keep all lead lengths into and out of the device as short as possible to minimize inductance.
- Implement an extensive ground plane on the PCB.
- Attach a Schottky diode between the OUT pin and ground to suppress negative voltage transients.
- Place a low-ESR capacitor with a value greater than 1μF adjacent to the OUT pin.
- Utilize a ceramic input capacitor (C_{IN} = 1μF) with low equivalent series resistance to absorb energy and dampen transients. Ensure its voltage rating is at least twice the input supply voltage to endure positive voltage overshoot during inductive ringing.

The required input capacitance can be approximated using Equation 14

$$V_{SPIKE\_ABS} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (14)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input

- In certain applications, adding a Transient Voltage Suppressor (TVS) may be necessary to keep voltage transients within the device's absolute maximum ratings. Even when transient amplitudes remain below these limits, a TVS can help absorb excess energy, preventing very fast transient voltages from developing at the IC's supply input. Such transients could otherwise couple into internal control circuitry and lead to erratic operation.

NOTE: If reverse polarity conditions may occur at the input, it suggests employing either a bidirectional TVS or a unidirectional TVS paired with a series reverse-blocking diode for enhanced protection.

- In systems such as USB-C where a powered cable connects to the device output, overvoltage stress from OUT to IN may surpass the absolute maximum rating of the device. It recommends placing a TVS diode across OUT and IN to clamp the transient voltage within a safe operating range.

The circuit implementation with optional protection components is shown in Figure 27.

APPLICATION INFORMATION (continued)

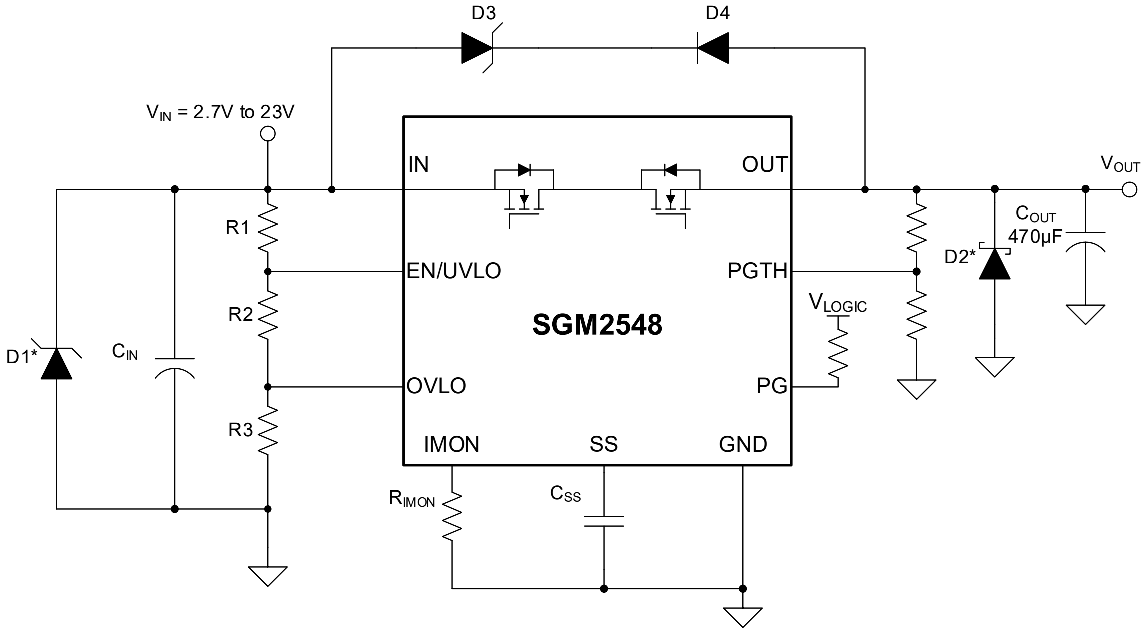


Figure 21. Circuit Implementation with Optional Protection Components

Output Short-Circuit Measurements

Achieving consistent and reproducible short-circuit test results can be challenging due to multiple factors introducing variability. Key contributors to result discrepancies include:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The physical shorting process itself involves inherent randomness—microscopic bouncing and arcing effects occur during contact. It is important to employ a well-defined configuration and methodology to achieve representative results. Note that actual waveforms are likely to differ from those shown in this datasheet, as each test setup varies.

APPLICATION INFORMATION (continued)

Layout Guidelines

- To ensure stable operation in all designs, SGMICRO advises placing a ceramic decoupling capacitor with a capacitance of at least 0.1μF between the input (IN) and ground (GND) terminals.
- The decoupling capacitor should be positioned as near as possible to the IN and GND pins of the device. Critical attention is required to reduce the loop area generated by the bypass capacitor's trace connections, the input (IN) terminal, and the ground (GND) node of the device.
- For power transmission lines handling significant currents, conductor lengths should be minimized to reduce resistance, with their cross-sectional dimensions engineered to safely accommodate currents exceeding twice the system's maximum operational load capacity.
- The GND terminal must be connected to the PCB ground plane of the IC's terminals via the shortest possible trace adjacent. The PCB ground layer should be constructed as a continuous copper plane or an isolated island on the board. SGMICRO strongly advises implementing a dedicated ground plane for the eFuse, which is designed exclusively as a low-current pathway to serve as a noise-free reference potential for all critical analog signals of the device. This isolated ground plane must be interfaced with the system's power ground layer using a star-configured single-point interconnection to eliminate ground loops and ensure signal integrity.
- The IN and OUT pins are used for heat dissipation. Connect as much copper area as possible to the top and bottom layers of the PCB, using thermal vias for connection. The vias below the device also help to reduce the voltage gradient between the IN and OUT pins and ensure that the current flows uniformly through the device, which is crucial for achieving the best conduction resistance and current detection accuracy.
- Place the following components as close as possible to their connection pins:
  1. R_{ILIM}
  2. C_{SS}
  3. C_{ITIMER}
  4. Resistors for the EN/UVLO, OVLO/OVCSEL, and PGTH pins
- Use the shortest trace to connect the other end of the above component to the GND pin of IC. In order to minimize the parasitic effects on the current limit, over-current blanking interval and soft start timing, the trace from the R_{ILIM}, C_{ITIMER} and C_{SS} components to the IC must be as short as possible. To maintain stable system performance, the parasitic capacitance at the ILIM pin should not exceed 50pF. Additionally, ensure these traces are fully isolated from any switching signals on the PCB to avoid unintended coupling or noise interference.
- The ILIM pin's bias current dictates the device's over-current protection (OCP) threshold. To ensure reliable OCP operation, its PCB traces must be rigorously isolated from switching noise sources (e.g., power switching) to prevent false triggering due to coupled interference.
- Place TVS diodes, snubbers, bypass capacitors, and protective diodes adjacent to the device they protect. Route connections with short, wide traces to minimize parasitic inductance. For example, it recommends to use a protection Schottky diode for suppressing negative voltage transients from inductive load switching. It also recommends to install a ≥ 1μF ceramic capacitor directly between the OUT pin and GND. These components must be physically close to the OUT pins. Optimize the layout of the Schottky diode → OUT pin → GND path to form the smallest possible loop.

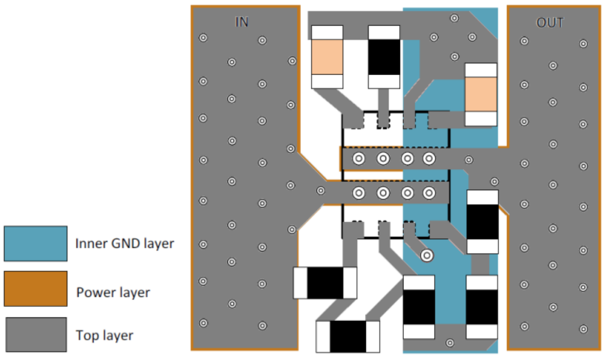


Figure 22. Layout Example

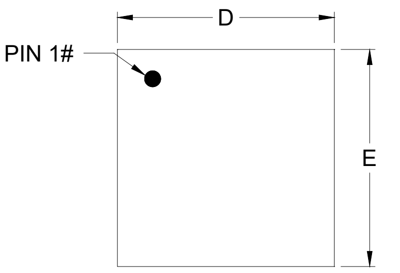
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

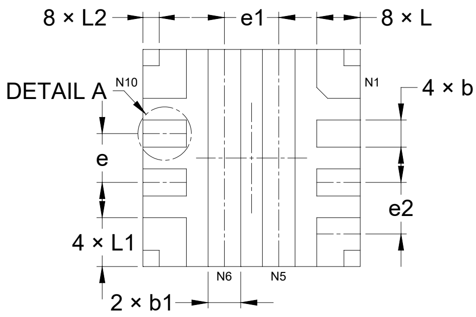
Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

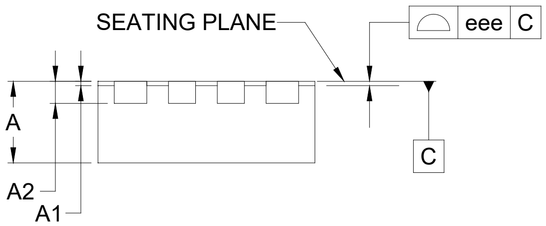
TQFN-2×2-10L



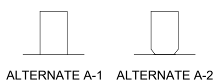
TOP VIEW



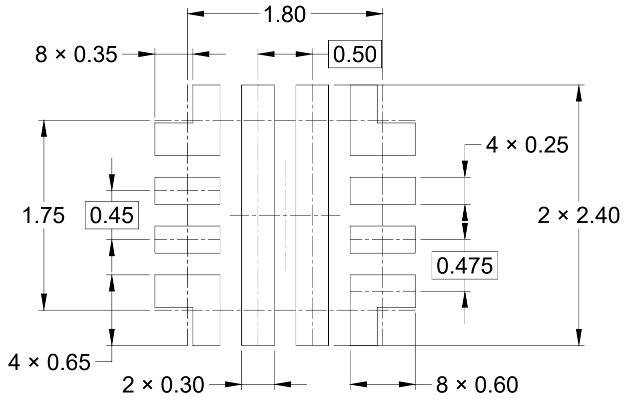
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



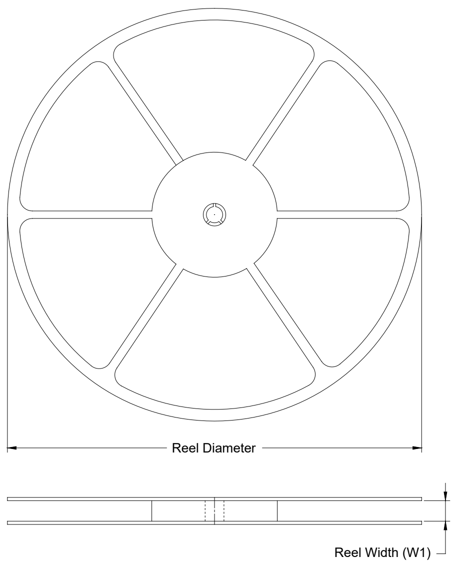
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.250	-	0.350
D	1.900	-	2.100
E	1.900	-	2.100
e	0.450 BSC		
e1	0.500 BSC		
e2	0.475 BSC		
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.150 REF		
eee	0.080		

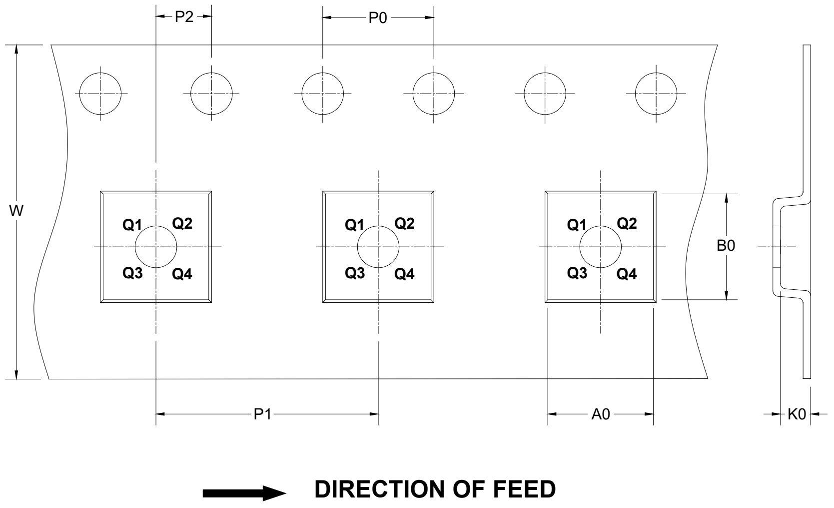
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



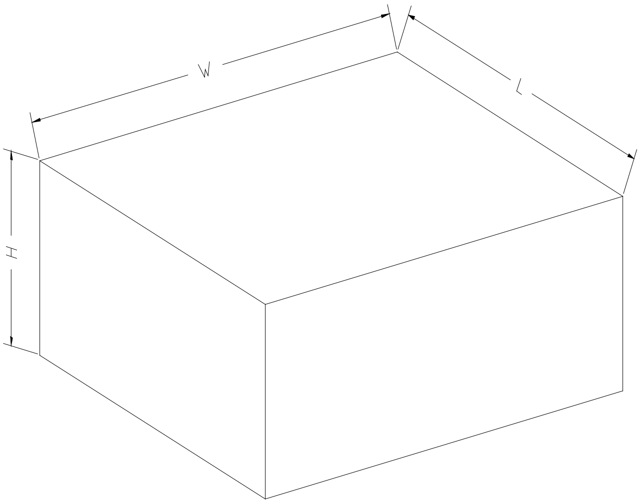
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002