



SGM7300AN

3.3V, Differential 2-Channel, 2:1 Multiplexer/Demultiplexer Switch

GENERAL DESCRIPTION

The SGM7300AN is a differential 2-channel switch which can be used for both multiplexer (MUX) and demultiplexer (DEMUX) configurations. The device can be used for PCI Express Generation 3, USB 3.1 and other high-speed serial interface applications.

The product can switch dual differential signals to 1 of 2 locations. The SGM7300AN minimizes the impedance of the switch so that the attenuation observed through the switch can be ignored and minimizes the inter-channel skew and inter-channel crosstalk required for high-speed serial interfaces. The SGM7300AN can achieve extremely low power consumption by extending existing high-speed ports. In order to achieve high ESD tolerance, the ESD protection circuits are integrated into ICs.

The SGM7300AN optimizes the pins to match the product to different application layouts. It is suitable for edge connectors with different signal sources on the motherboard, with input and output pins on opposite sides of the package. The impedances of all Ports are Hi-Z relative to GND pin.

No external DC blocking capacitors are required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM7300AN is available in a Green TLGA-2.5×4.5-20L package.

FEATURES

- High Bandwidth: 9GHz
- Support 10Gbps Signal Transmission
- Support USB 3.1 Gen1 and Gen2 Data Rates
- Low Insertion Loss:
 - ♦ -0.36dB at 0.1GHz
 - ♦ -0.71dB at 4.0GHz
- Low Off-State Isolation: -21dB at 4.0GHz
- Low Return Loss: -20dB at 4.0GHz
- Available in a Green TLGA-2.5×4.5-20L Package

APPLICATIONS

USB 3.1

PCI Express Generation 3

DisplayPort 1.2

SATA 6Gbit/s

High-Speed Differential Signals Routing

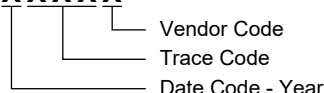
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7300AN	TLGA-2.5×4.5-20L	-40°C to +85°C	SGM7300ANYTLN20G/TR	1TY TLN20 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	-0.3V to 3.7V
Package Thermal Resistance	
TLGA-2.5×4.5-20L, θ_{JA}	105.6°C/W
TLGA-2.5×4.5-20L, θ_{JB}	78.3°C/W
TLGA-2.5×4.5-20L, θ_{JC}	100.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM	±1000V
CDM	±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD}	3.0V to 3.6V
Control Voltage, V_{XSD} , V_{SEL}	0V to 3.6V
Operating Temperature Range	-40°C to +85°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

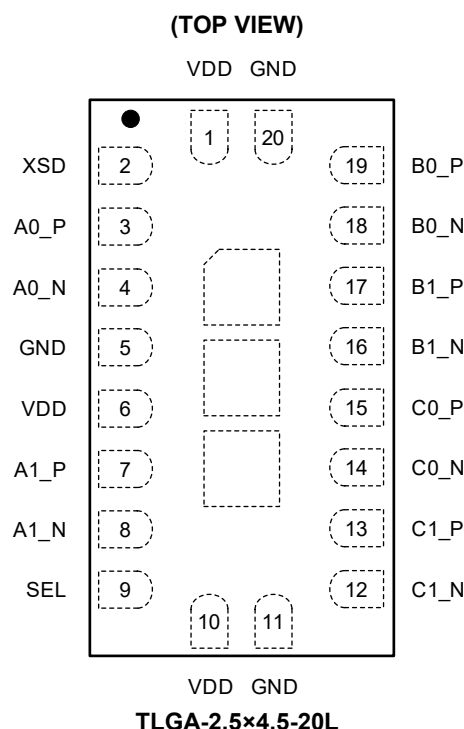
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
3	A0_P	I/O	Channel 0, Port A, Positive/Negative Signal.
4	A0_N	I/O	
7	A1_P	I/O	Channel 1, Port A, Positive/Negative Signal.
8	A1_N	I/O	
19	B0_P	I/O	Channel 0, Port B, Positive/Negative Signal.
18	B0_N	I/O	
17	B1_P	I/O	Channel 1, Port B, Positive/Negative Signal.
16	B1_N	I/O	
15	C0_P	I/O	Channel 0, Port C, Positive/Negative Signal.
14	C0_N	I/O	
13	C1_P	I/O	Channel 1, Port C, Positive/Negative Signal.
12	C1_N	I/O	
9	SEL	CMOS Single-Ended Input	Operation Mode Select Pin. SEL = Low: A ↔ B SEL = High: A ↔ C
2	XSD	CMOS Single-Ended Input	XSD = Low: Normal Operation XSD = High: Hi-Z Operation
1, 6, 10	VDD	Power	Positive Supply Voltage.
5, 11, 20	GND	Power	Ground.
Exposed Pad	—	Power	Exposed pad must be connected to ground.

FUNCTIONAL BLOCK DIAGRAM

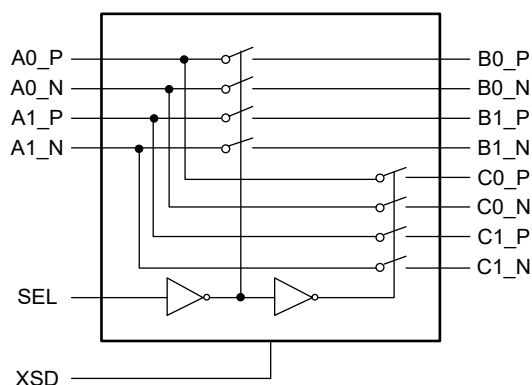


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION

XSD	SEL	FUNCTION
High	X	All channel off
Low	Low	Channel on An to Bn
Low	High	Channel on An to Cn

X = Don't care.

ELECTRICAL CHARACTERISTICS(T_A = +25°C, V_{DD} = 3.3V ± 0.3V, typical values are at V_{DD} = 3.3V and maximum loading, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Characteristics						
Supply Current	I _{VDD}	Normal mode, V _{DD} = max, XSD = low		80	100	μA
		Hi-Z mode, V _{DD} = max, XSD = high		80	100	
High-Level Input Current	I _{IH}	V _{DD} = max, V _I = V _{DD}			±30	μA
Low-Level Input Current	I _{IL}	V _{DD} = max, V _I = GND			±30	μA
High-Level Input Voltage	V _{IH}	SEL, XSD pins	1.4		V _{DD}	V
Low-Level Input Voltage	V _{IL}	SEL, XSD pins			0.45	V
Input Voltage	V _{IN}	Differential pins			2.4	V
		SEL, XSD pins			V _{DD}	
Common-Mode Input Voltage	V _{IC}		0		2	V
Differential Input Voltage	V _{ID}	Peak to peak			1.6	V
Dynamic Characteristics						
Differential Insertion Loss	DDIL	Channel is off	f ₀ = 0.1GHz		-47	dB
			f ₀ = 4.0GHz		-21	
		Channel is on	f ₀ = 0.1GHz		-0.36	
			f ₀ = 4.0GHz		-0.71	
Differential Near-End Crosstalk	DDNEXT	Adjacent channels are on	f ₀ = 0.1GHz		-60	dB
			f ₀ = 4.0GHz		-36	
-3dB Bandwidth	BW			9		GHz
Differential Return Loss	DDRRL	f ₀ = 0.1GHz		-31		dB
		f ₀ = 4.0GHz		-20		
On-State Resistance	R _{ON}	V _{DD} = 3.3V, V _{IN} = 2V, I _{IN} = 19mA		5.5	9	Ω
On-State Input/Output Capacitance	C _{IO_ON}			2.0		pF
Propagation Delay	t _{PD}	An to Bn or An to Cn, frequency = 4.0GHz			100 ⁽¹⁾	ps
Switching Characteristics						
Start-Up Time	t _{STARTUP}	V _{DD} = 3.3V and XSD is turning to low			1000	ns
Turn-On Time	t _{ON}				150	ns
Turn-Off Time	t _{OFF}				150	ns
Differential Skew Time	t _{SK_DIF}	Intra-pair			15 ⁽¹⁾	ps
Skew Time	t _{SK}	Inter-pair			25 ⁽¹⁾	ps

NOTE:

1. Guaranteed by design, not tested in production.

VOLTAGE WAVEFORMS

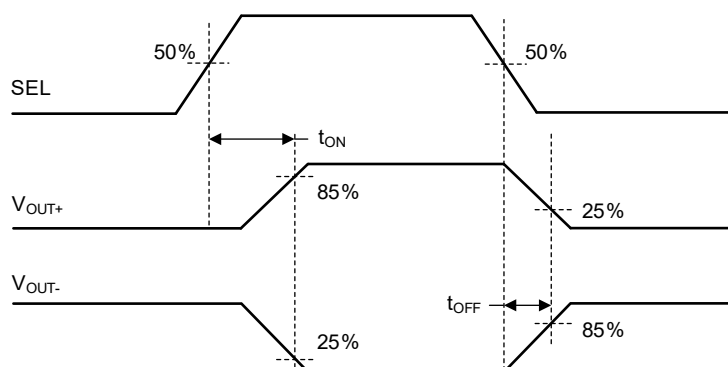


Figure 2. Voltage Waveforms for Enable and Disable Times

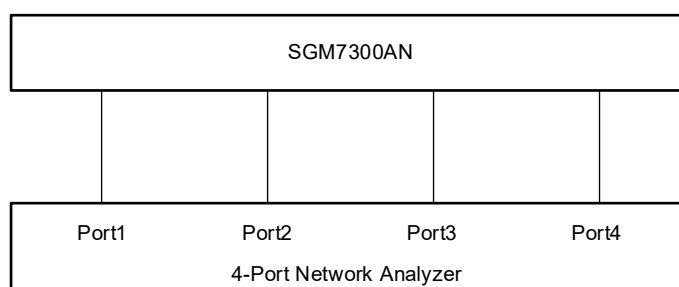


Figure 3. Test Circuit

DETAILED DESCRIPTION

The SGM7300AN is a 4-channel, high-speed bidirectional passive switch. The device provides switching on differential channels between A port and B port or C port according to the control pin SEL. The SGM7300AN has a common voltage range from 0V to 2V and differential signaling amplitude up to 1600mV_{pp}. It can be flexibly applied in many interface applications. Besides, the impedances of all Ports are Hi-Z relative to GND pin. For more detailed descriptions, please refer to Table 1 and Table 2.

Table 1. Port Impedance at V_{DD} Power-Off

XSD	SEL	Port Impedance State		
		A Port	B Port	C Port
High	X	Hi-Z	Hi-Z	Hi-Z
Low	Low			
Low	High			

Table 2. Port Impedance at V_{DD} Power-On

XSD	SEL	Port Impedance State		
		A Port	B Port	C Port
High	X	Hi-Z	Hi-Z	Hi-Z
Low	Low	Hi-Z	Hi-Z	Hi-Z
Low	High	Hi-Z	Hi-Z	Hi-Z

X = Don't care.

APPLICATION INFORMATION

The SGM7300AN is a generic analog differential passive switch that can work for both multiplexer (MUX) and demultiplexer (DEMUX) configurations for any high-speed interface application, such as PCI Express Generation 3, USB 3.1. This device allows high-speed switching with minimum attenuation to the signal eye diagram with very little added jitter due to its excellent dynamic characteristics. The typical application diagram of SGM7300AN is shown in the Figure 4.

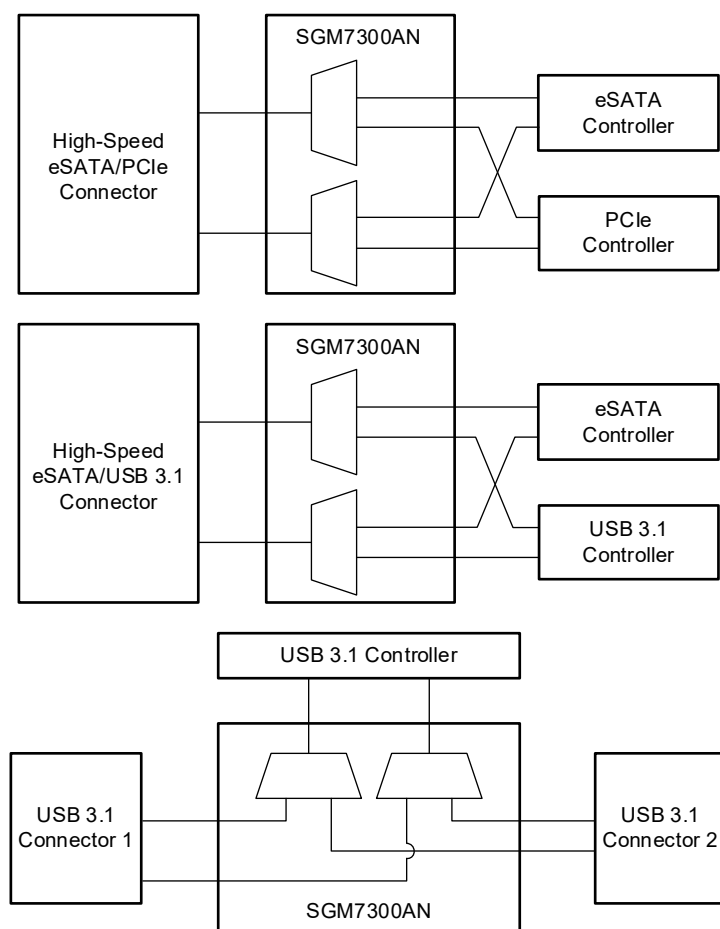


Figure 4. Typical Application Scenario

Most interfaces require AC coupling between the transmitter and receiver. The recommended providing AC coupling packaging is 0402. The 0805 size capacitors may be avoided. The AC coupling capacitors should be symmetrically placed and the value should match for the lane pair. The SGM7300AN can be used with the USB Type-C connector to support the connector's flip. Figure 5 provides the generic location for the AC coupling capacitors for this application.

APPLICATION INFORMATION (continued)

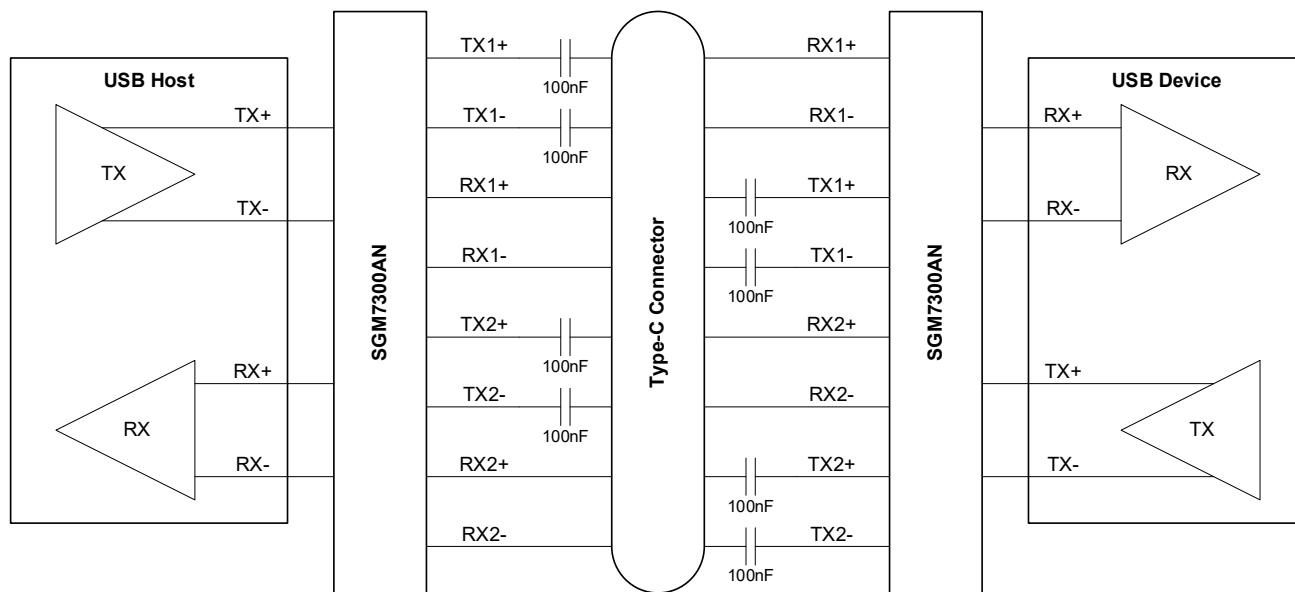


Figure 5. AC Coupling Capacitors for USB Type-C

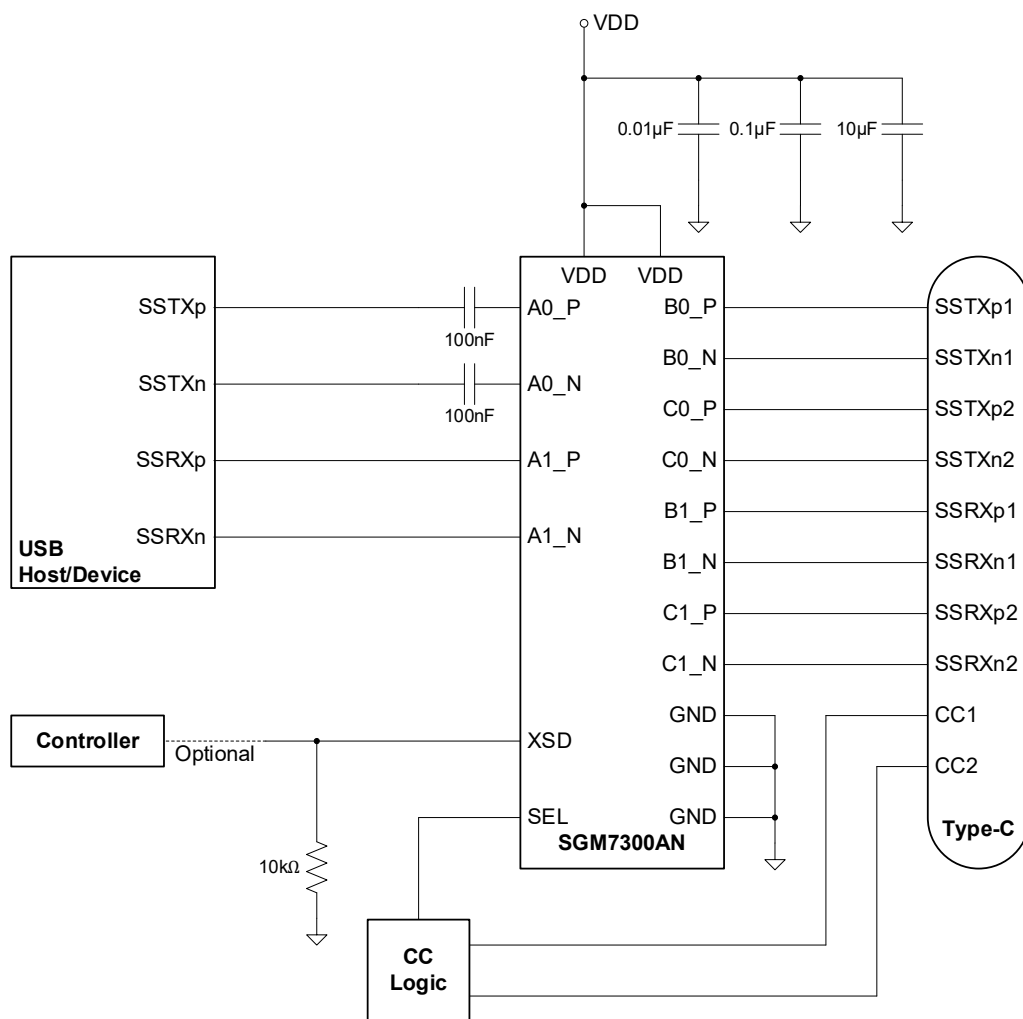


Figure 6. USB 3.1 Type-C Connector

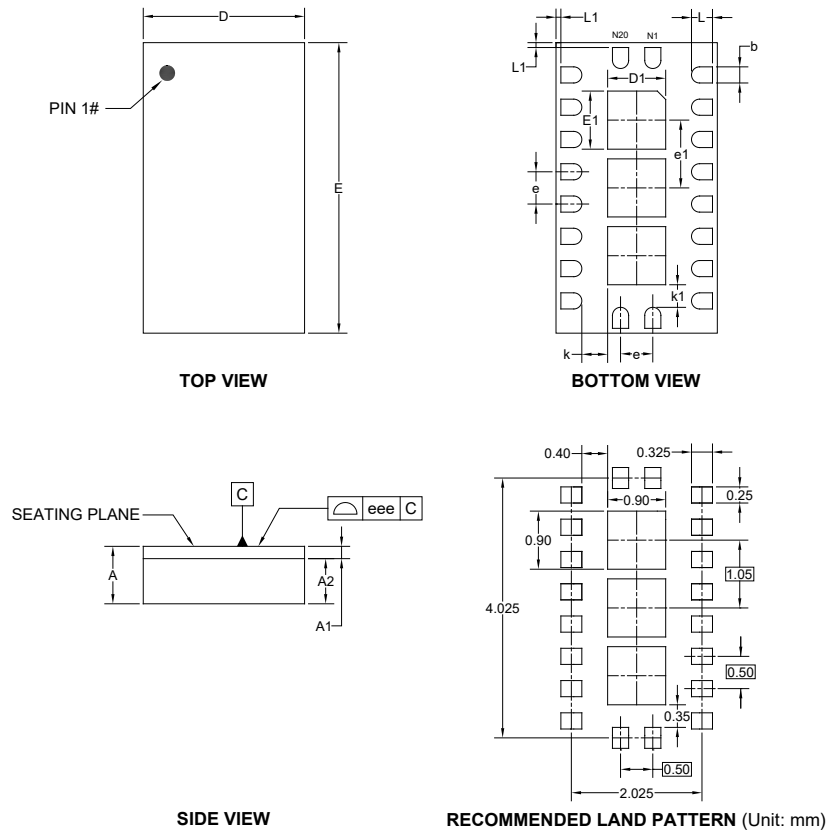
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JULY 2025)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

TLGA-2.5×4.5-20L



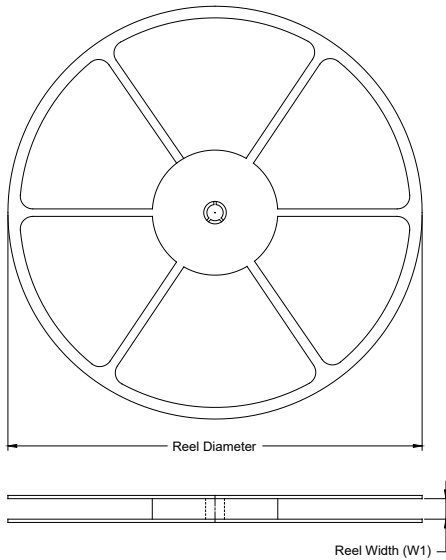
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.840	-	0.940
A1	0.160	-	0.220
A2	0.700 REF		
b	0.200	-	0.300
D	2.400	-	2.600
E	4.400	-	4.600
D1	0.800	0.900	1.000
E1	0.800	0.900	1.000
e	0.500 BSC		
e1	1.050 BSC		
L	0.275	-	0.375
L1	0.025	-	0.125
k	0.400 REF		
k1	0.350 REF		
eee	0.100		

NOTE: This drawing is subject to change without notice.

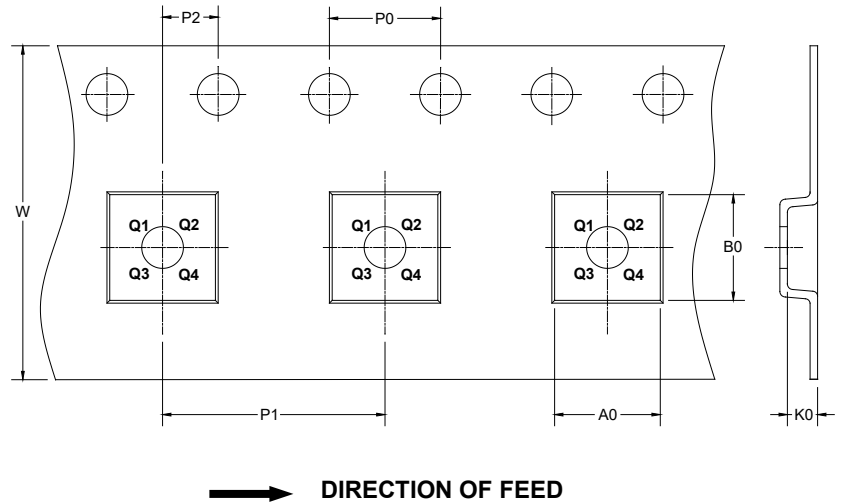
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

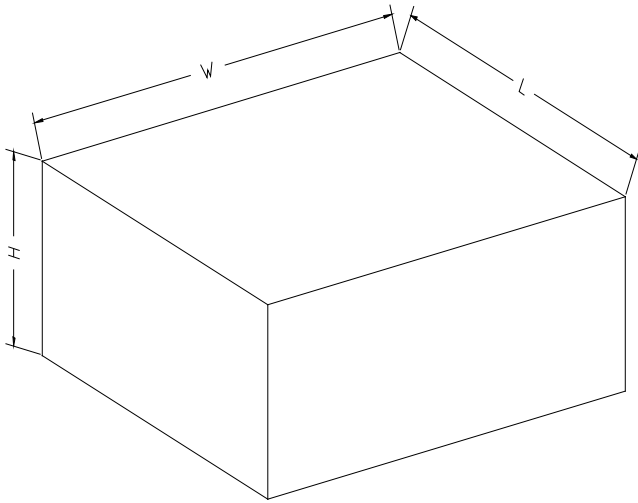
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TLGA-2.5×4.5-20L	13"	12.4	2.8	4.8	1.15	4	8	2	12	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002