SGM8250-1/SGM8250-2
High Voltage, Micro-Power, Zero-Drift, CMOS Operational Amplifiers

GENERAL DESCRIPTION

The single SGM8250-1 and dual SGM8250-2 are micro-power, high voltage, high precision CMOS operational amplifiers. These devices can operate from 3V to 24V single supply or from ±1.5V to ±12V dual power supplies, and consume only 50μA quiescent current per amplifier. The SGM8250-1/2 support rail-to-rail input and output operation. The input common mode voltage range is from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V, and the output range is from ($-V_S$) + 0.037V to ($+V_S$) - 0.065V.

The SGM8250-1/2 have high impedance inputs and zero-drift 50μV (MAX) offset voltage. These specifications make SGM8250-1/2 appropriate for a wide range of applications requiring high precision.

The SGM8250-1 is available in Green SOT-23-5, SC70-5 and SOIC-8 packages. The SGM8250-2 is available in Green TDFN-3×3-8L and SOIC-8 packages. They are specified over -40℃ to +125℃ temperature range.

FEATURES

- **Low Input Offset Voltage: 50μV (MAX)**
- **Low Noise: 0.85μV_{P-P} at 0.1Hz to 10Hz**
- **Quiescent Current: 50μA/Amplifier (TYP)**
- **Rail-to-Rail Input and Output**
- **Support Single or Dual Power Supplies:**
  3V to 24V or ±1.5V to ±12V
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8250-1 Available in Green SOT-23-5, SC70-5 and SOIC-8 Packages
  SGM8250-2 Available in Green TDFN-3×3-8L and SOIC-8 Packages

APPLICATIONS

Industrial Equipment
Battery-Powered Equipment
Sensor Signal Conditioning

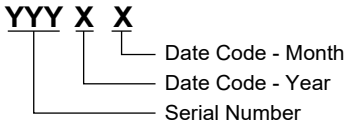
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8250-1	SOT-23-5	-40℃ to +125℃	SGM8250-1XN5G/TR	GSCXX	Tape and Reel, 3000
	SC70-5	-40℃ to +125℃	SGM8250-1XC5G/TR	GS3XX	Tape and Reel, 3000
	SOIC-8	-40℃ to +125℃	SGM8250-1XS8G/TR	SGM 82501XS8 XXXXX	Tape and Reel, 4000
SGM8250-2	TDFN-3×3-8L	-40℃ to +125℃	SGM8250-2XTDB8G/TR	SGM 82502DB XXXXX	Tape and Reel, 4000
	SOIC-8	-40℃ to +125℃	SGM8250-2XS8G/TR	SGM 82502XS8 XXXXX	Tape and Reel, 4000

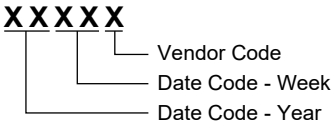
MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code and Vendor Code.

SOT-23-5/SC70-5



SOIC-8/TDFN-3×3-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 26.4V
Input Common Mode Voltage Range
..... ($-V_S$) - 0.3V to ($+V_S$) + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
MM 250V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Specified Voltage Range ..... 3V to 24V
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

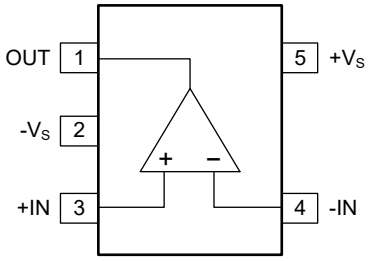
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

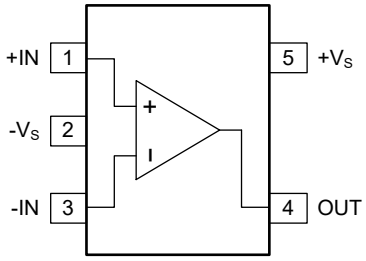
PIN CONFIGURATIONS

SGM8250-1 (TOP VIEW)



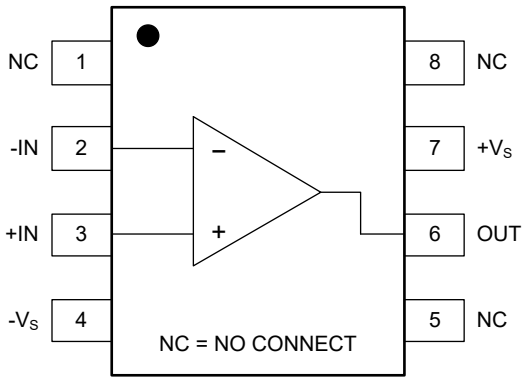
SOT-23-5

SGM8250-1 (TOP VIEW)



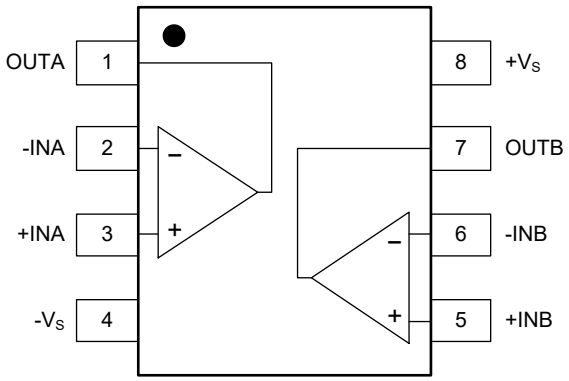
SC70-5

SGM8250-1 (TOP VIEW)



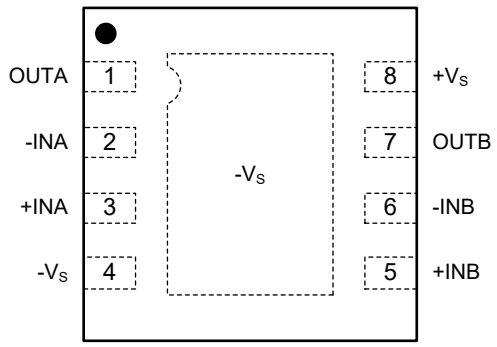
SOIC-8

SGM8250-2 (TOP VIEW)



SOIC-8

SGM8250-2 (TOP VIEW)



TDFN-3×3-8L

ELECTRICAL CHARACTERISTICS

(+V_S = 5V, -V_S = 0V, V_{CM} = +V_S/2, V_{OUT} = +V_S/2 and R_L = 10kΩ to +V_S/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}		+25℃		10	50	μV
			Full			90	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.11		μV/℃
Input Bias Current	I_B		+25℃		60		pA
Input Common Mode Voltage Range	V_{CM}		Full	(-V_S) - 0.1		(+V_S) + 0.1	V
Common Mode Rejection Ratio	CMRR	(-V_S) - 0.1V < V_{CM} < (+V_S) + 0.1V	+25℃	95	112		dB
			Full	92			
Open-Loop Voltage Gain	A_{OL}	(-V_S) + 0.1V < V_{OUT} < (+V_S) - 0.1V	+25℃	108	131		dB
			Full	105			
Output Characteristics							
Output Voltage Swing from Rail	V_{OH}		+25℃		14	25	mV
			Full			30	
	V_{OL}		+25℃		8	16	
			Full			20	
Output Short-Circuit Current	I_{SC}		+25℃		±17		mA
Power Supply							
Operating Voltage Range	V_S		Full	3		24	V
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0mA	+25℃		45	60	μA
			Full			80	
Power Supply Rejection Ratio	PSRR	V_S = 3V to 24V	+25℃	116	142		dB
			Full	113			
Dynamic Performance							
Gain-Bandwidth Product	GBP	G = +100, C_L = 100pF	+25℃		350		kHz
Slew Rate	SR	G = +1, V_{OUT} = $2V_{P-P}$, C_L = 100pF	+25℃		0.1		V/μs
Turn-On Time			+25℃		0.75		ms
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		0.85		μV_{P-P}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		40		$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS (continued)

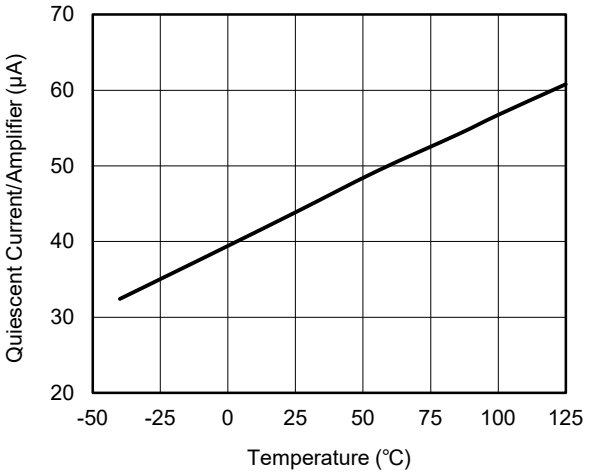
($+V_S$ = 24V, $-V_S$ = 0V, V_{CM} = $+V_S$/2, V_{OUT} = $+V_S$/2 and R_L = 10kΩ to $+V_S$/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}		+25℃		10	50	μV
			Full			90	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.11		μV/℃
Input Bias Current	I_B		+25℃		80	850	pA
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio	CMRR	$(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V	+25℃	112	130		dB
			Full	107			
Open-Loop Voltage Gain	A_{OL}	$(-V_S)$ + 0.1V < V_{OUT} < $(+V_S)$ - 0.1V	+25℃	120	145		dB
			Full	110			
Output Characteristics							
Output Voltage Swing from Rail	V_{OH}		+25℃		65	95	mV
			Full			130	
	V_{OL}		+25℃		37	60	
			Full			85	
Output Short-Circuit Current	I_{SC}		+25℃		±17		mA
Power Supply							
Operating Voltage Range	V_S		Full	3		24	V
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0mA	+25℃		50	64	μA
			Full			84	
Power Supply Rejection Ratio	PSRR	V_S = 3V to 24V	+25℃	116	142		dB
			Full	113			
Dynamic Performance							
Gain-Bandwidth Product	GBP	G = +100, C_L = 100pF	+25℃		350		kHz
Slew Rate	SR	G = +1, V_{OUT} = $2V_{P-P}$, C_L = 100pF	+25℃		0.09		V/μs
Turn-On Time			+25℃		1.5		ms
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		0.85		μV_{P-P}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		40		$nV/\sqrt{Hz}$

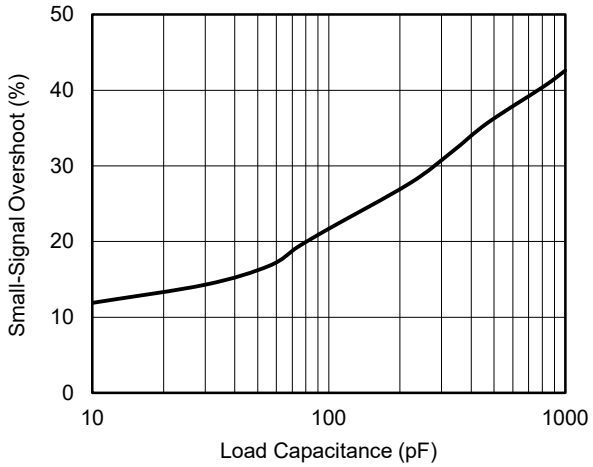
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, $+V_S$ = 5V, $-V_S$ = 0V, R_L = 10kΩ and C_L = 0pF, unless otherwise noted.

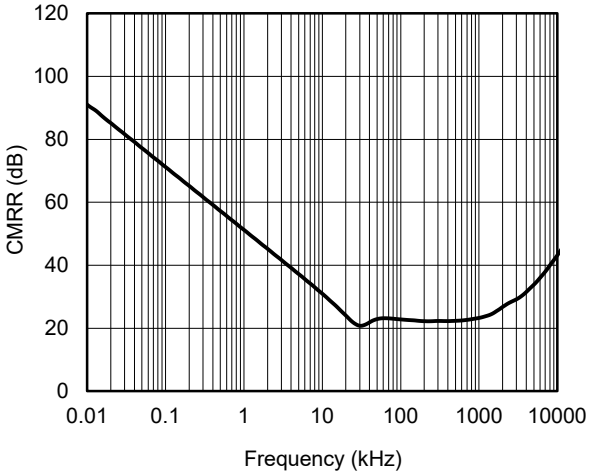
Quiescent Current vs. Temperature



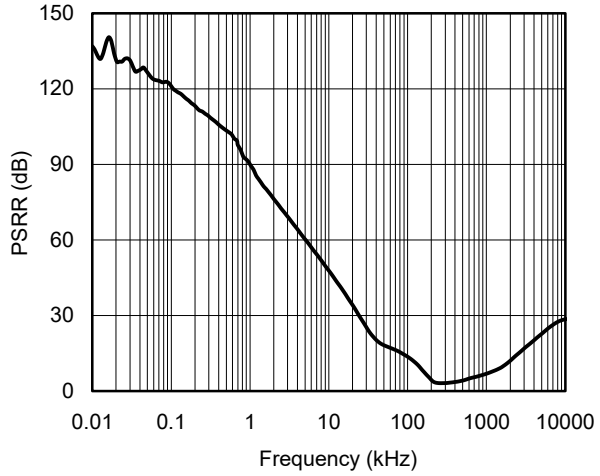
Small-Signal Overshoot vs. Load Capacitance



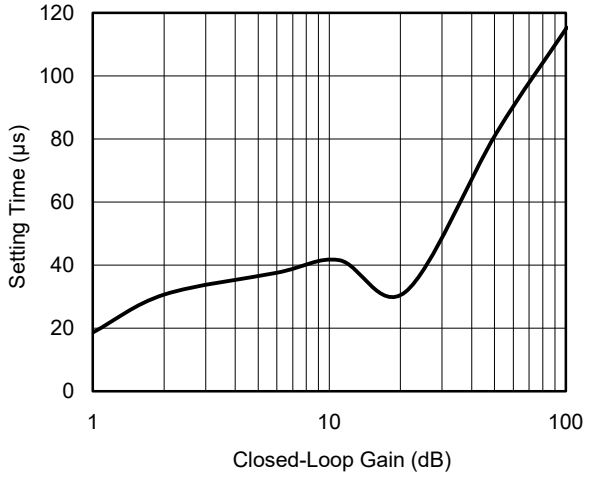
Common Mode Rejection Ratio vs. Frequency



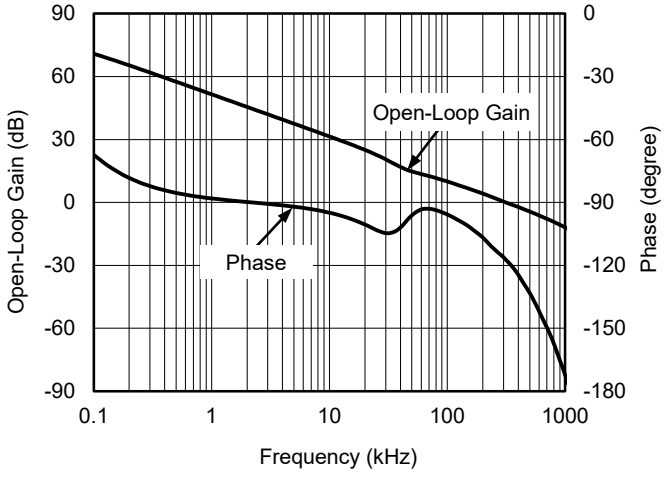
Power Supply Rejection Ratio vs. Frequency



Settling Time vs. Closed-Loop Gain



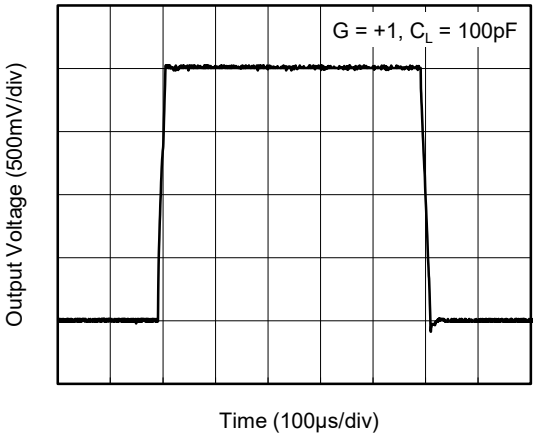
Open-Loop Gain and Phase vs. Frequency



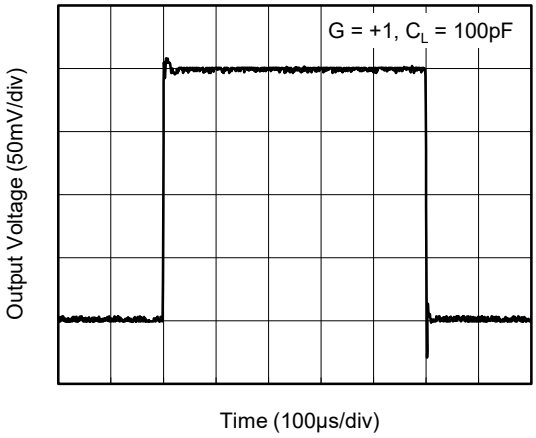
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, $+V_S$ = 5V, $-V_S$ = 0V, R_L = 10kΩ and C_L = 0pF, unless otherwise noted.

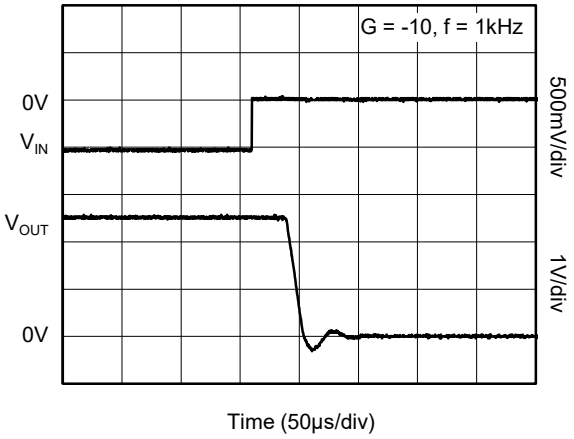
Large-Signal Step Response



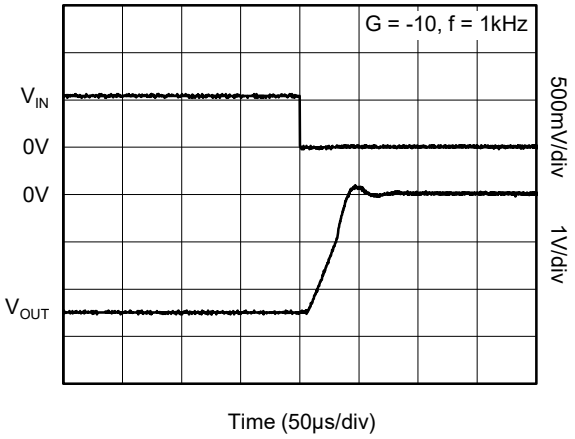
Small-Signal Step Response



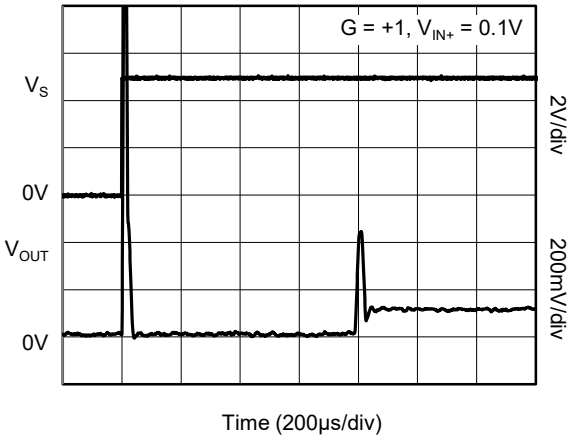
Positive Overload Recovery



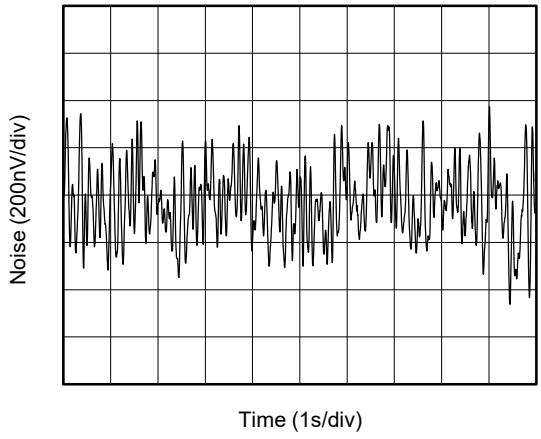
Negative Overload Recovery



Turn-On Time



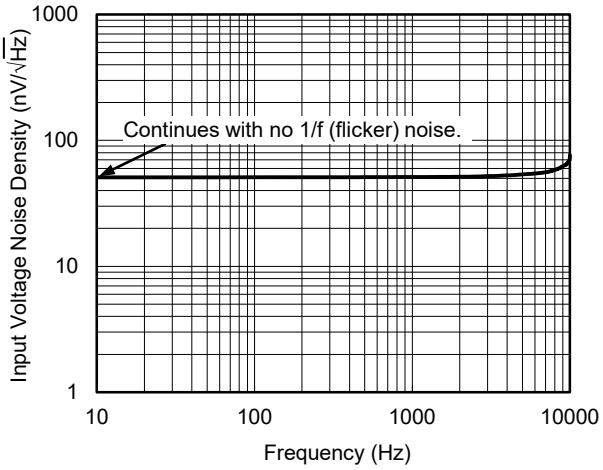
0.1Hz to 10Hz Noise



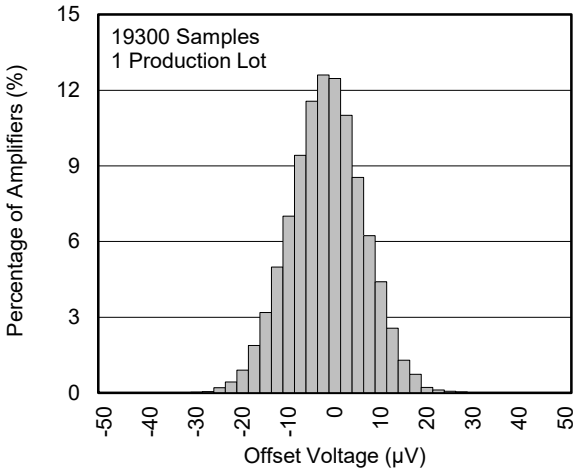
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, $+V_S$ = 5V, $-V_S$ = 0V, R_L = 10kΩ and C_L = 0pF, unless otherwise noted.

Input Voltage Noise Density vs. Frequency



Offset Voltage Production Distribution



APPLICATION INFORMATION

Rail-to-Rail Input

When SGM8250-1/2 work at the power supply between 3V and 24V, the input common mode voltage range is from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage not to exceed the rails.

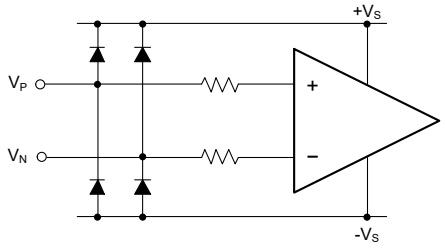


Figure 1. Input Equivalent Circuit

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

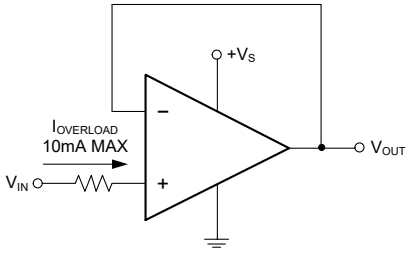


Figure 2. Input Current-Limit Protection

Rail-to-Rail Output

The SGM8250-1/2 support rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 24V, $-V_S$ = GND, 10kΩ load resistor is tied from OUT pin to $+V_S/2$, the typical output swing range is from 0.037V to 23.935V.

Driving Capacitive Loads

The SGM8250-1/2 are designed for driving capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

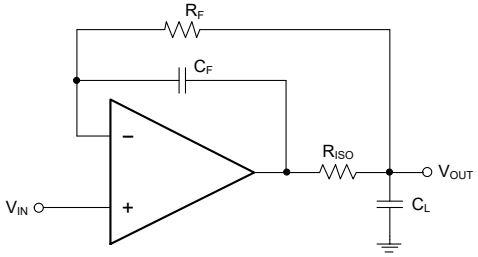


Figure 3. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifiers through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

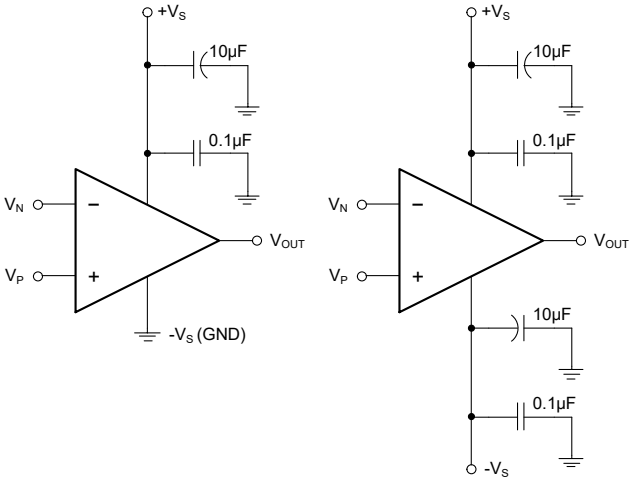


Figure 4. Amplifier Power Supply Bypassing

APPLICATION INFORMATION (continued)

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

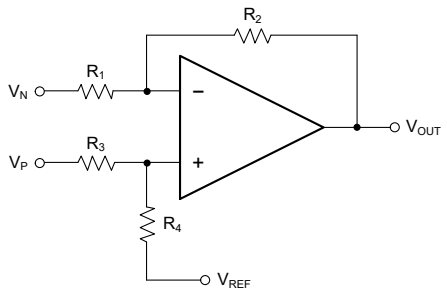


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier, the added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

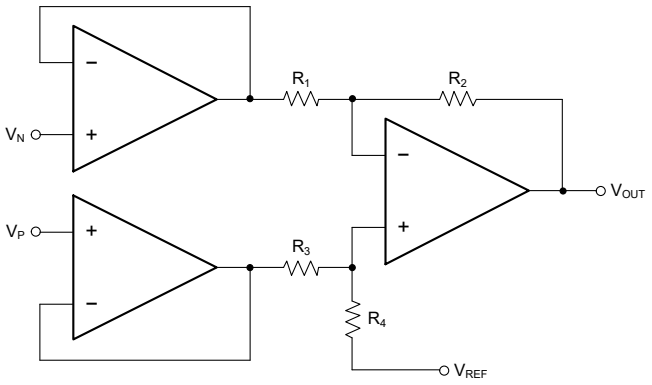


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/2\pi R_2 C$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

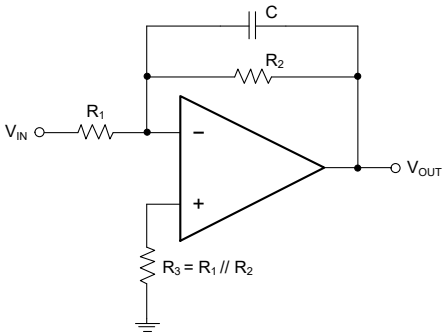


Figure 7. Active Low-Pass Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JULY 2023 – REV.A to REV.A.1	Page
Updated Package Outline Dimensions section	13

Changes from Original (DECEMBER 2017) to REV.A	Page
Changed from product preview to production data	All