GENERAL DESCRIPTION

The SGM825 is a complete microprocessor supervisory device which combines reset and manual reset functions in a SOT-23-5 package. System reliability is significantly improved by such integration compared to the designs with individual ICs or discrete components. The SGM825 also features an excellent transient immunity to ignore fast V_{CC} transients.

This device has an active-low push-pull reset output (nRESET) that is activated by a logic low on the manual reset input (nMR) or due to a low V_{CC} voltage. The nRESET output can still be in the correct logic state even if V_{CC} is 1V. The SGM825 is offered in four fixed V_{CC} reset threshold voltages.

The SGM825 is available in a Green SOT-23-5 package. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Ultra-Low Supply Current: < 1µA (TYP)**
- **Precision Supply-Voltage Monitor**
  - **4.63V for SGM825-L**
  - **3.08V for SGM825-T**
  - **2.93V for SGM825-S**
  - **2.63V for SGM825-R**
- **Guaranteed Reset Valid at V_{CC} = 1V**
- **Two Reset Output Options**
  - **Push-Pull nRESET**
  - **Push-Pull RESET**
- **Reset Pulse Width: 200ms (TYP)**
- **Debounced TTL/CMOS-Compatible**
- **Manual Reset Input**
- **Fully Specified over Temperature**
- **Power-Supply Transient Immunity**
- **Without External Components**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Computers

Portable Equipment

Automotive Equipment

Intelligent Instruments
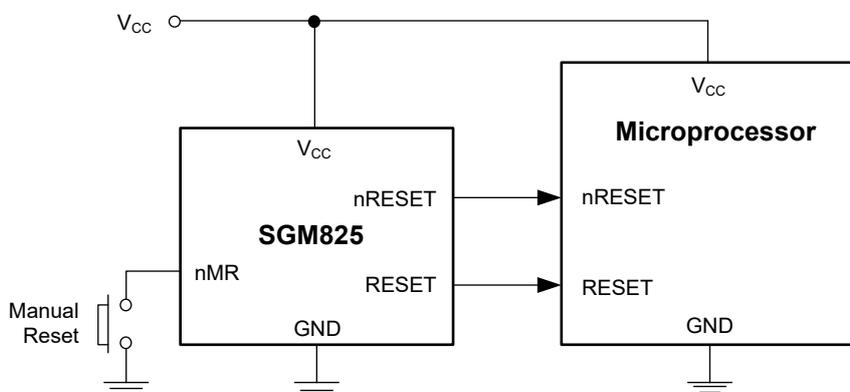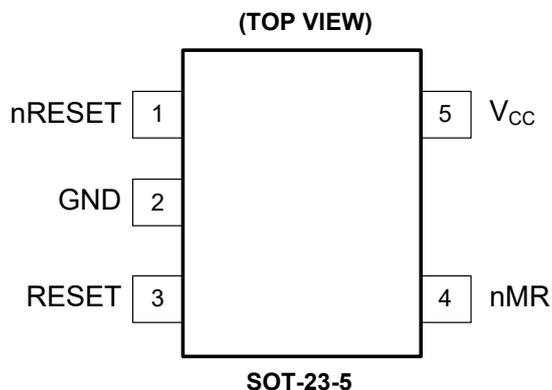
Critical µP Power Monitoring

TYPICAL APPLICATION

Figure 1. Typical Application Circuit Example

PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM825	4.63	SOT-23-5	SGM825-LXN5G/TR	MZ2XX	Tape and Reel, 3000
	3.08	SOT-23-5	SGM825-TXN5G/TR	MGCXX	Tape and Reel, 3000
	2.93	SOT-23-5	SGM825-SXN5G/TR	MGDXX	Tape and Reel, 3000
	2.63	SOT-23-5	SGM825-RXN5G/TR	MGEXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.

YYY X   X
- └── Date Code - Week
- └── Date Code - Year
- └── Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (With Respect to GND)

V_{CC} .... -0.3V to 6.0V

All Other Inputs ....-0.3V to V_{CC} + 0.3V

Input Current

V_{CC} 20mA

GND 20mA

Output Current

All outputs 20mA

Package Thermal Resistance

SOT-23-5, θ_{JA} .... 234℃/W

Junction Temperature .... +150℃

Storage Temperature Range......................... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ....+260℃

ESD Susceptibility

HBM... 4000V

MM.. 400V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)

nRESET	1		5	V$_{CC}$
GND	2			
RESET	3		4	nMR

SOT-23-5

PIN DESCRIPTION

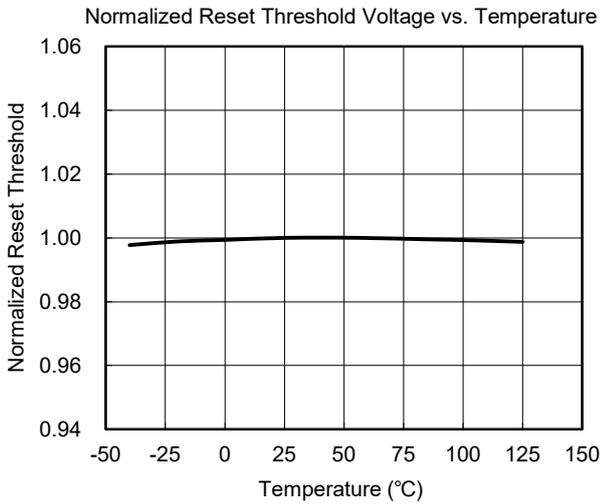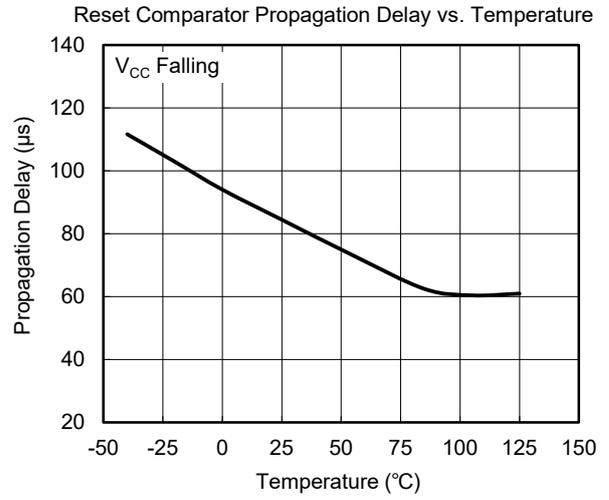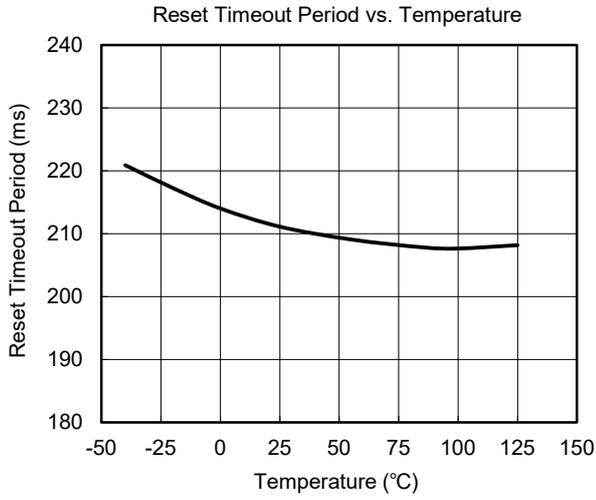| PIN	NAME	FUNCTION
1	nRESET	Active-Low Reset Output Pin. It delivers a 200ms (TYP) low pulse when activated. nRESET remains low if V$_{CC}$ is below the reset threshold or nMR is logic low. It remains low for 200ms after any of the following events: V$_{CC}$ rises above the reset threshold or the nMR input goes from low to high.
2	GND	Ground.
3	RESET	Active-High Reset Output. Inverse of nRESET.
4	nMR	Manual Reset Input Pin. nRESET keeps low when nMR is low. When nMR is high, nRESET becomes high after a 200ms timeout period. It is an active-low reset input with an internal 59kΩ pull-up resistor. nMR can be driven by a CMOS/TTL logic or by a switch shorting to GND. If not used, leave it open or connect it to V$_{CC}$.
5	V$_{CC}$	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{CC} = 4.73V to 5.5V for SGM825-L, V_{CC} = 3.14V to 5.5V for SGM825-T, V_{CC} = 2.99V to 5.5V for SGM825-S, V_{CC} = 2.68V to 5.5V for SGM825-R, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Operating Voltage Range (V_{CC})			Full	1		5.5	V
Supply Current (I_{SUPPLY})		V_{CC} = 3.6V	Full		0.5	1.2	μA
		V_{CC} = 5.5V	Full		0.7	1.4	
Reset Threshold (V_{RST})		SGM825-L	+25℃	4.55	4.63	4.70	V
			Full	4.54	4.63	4.73	
		SGM825-T	+25℃	3.03	3.08	3.13	
			Full	3.02	3.08	3.14	
		SGM825-S	+25℃	2.88	2.93	2.98	
			Full	2.87	2.93	2.99	
		SGM825-R	+25℃	2.59	2.63	2.67	
			Full	2.58	2.63	2.68	
Reset Threshold Hysteresis (V_{HYS})		SGM825-L	+25℃		20		mV
		SGM825-T	+25℃		14		
		SGM825-S	+25℃		13		
		SGM825-R	+25℃		12		
Reset Threshold Temperature Coefficient			Full		20		ppm/℃
Reset Pulse Width (t_{RP})			Full	140	200	290	ms
nRESET Output Voltage	V_{OH}	SGM825-L, V_{CC} = $V_{RST(MAX)}$, I_{SOURCE} = 120μA	Full	V_{CC} - 1.5			V
		SGM825-T/S/R, V_{CC} = $V_{RST(MAX)}$, I_{SOURCE} = 30μA	Full	0.8 × V_{CC}			
	V_{OL}	SGM825-L, V_{CC} = $V_{RST(MIN)}$, I_{SINK} = 3.2mA	Full			0.4	
		SGM825-T/S/R, V_{CC} = $V_{RST(MIN)}$, I_{SINK} = 1.2mA	Full			0.3	
		V_{CC} = 1V, V_{CC} falling, I_{SINK} = 50μA	Full			0.3	
nRESET Output Short-Circuit Current (I_{SOURCE})		SGM825-L, nRESET = 0V, V_{CC} = 5.5V	Full			460	μA
		SGM825-T/S/R, nRESET = 0V, V_{CC} = 3.6V	Full			430	
RESET Output Voltage	V_{OH}	V_{CC} > 1.8V, I_{SOURCE} = 150μA	Full	0.8 × V_{CC}			V
	V_{OL}	SGM825-L, V_{CC} = $V_{RST(MAX)}$, I_{SINK} = 3.2mA	Full			0.4	
		SGM825-T/S/R, V_{CC} = $V_{RST(MAX)}$, I_{SINK} = 1.2mA	Full			0.3	
V_{CC} to Reset Delay (t_{RD})		V_{RST} - V_{CC} = 100mV	+25℃		84		μs
nMR Input Voltage	V_{IL}		Full			0.8	V
	V_{IH}		Full	2			
nMR Pulse Width (t_{MR})			Full	300			ns
nMR Noise Immunity (Pulse width with no reset)			+25℃		130		ns
nMR to Reset Out Delay (t_{MD})			Full			470	ns
nMR Pull-Up Resistance (Internal)			Full	44	59	78	kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

Reset Timeout Period vs. Temperature

Reset Comparator Propagation Delay vs. Temperature

Normalized Reset Threshold Voltage vs. Temperature
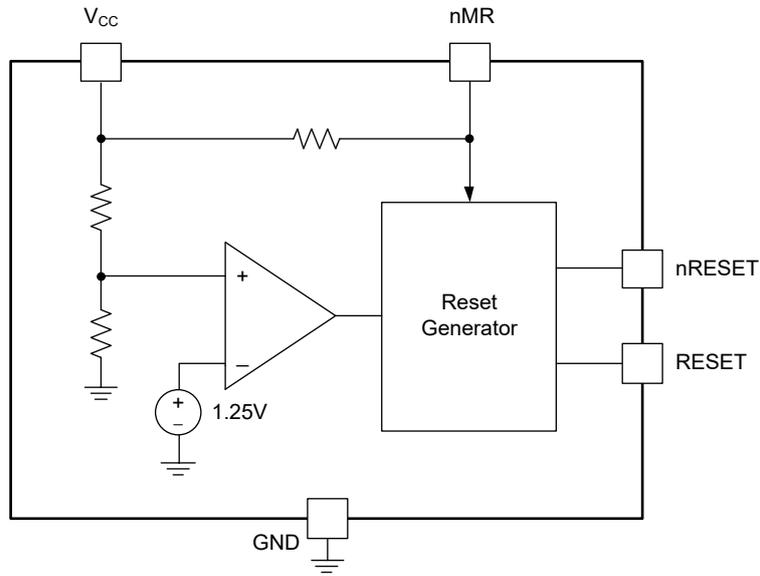
FUNCTIONAL BLOCK DIAGRAM

Figure 2. Block Diagram

DETAILED DESCRIPTION

Reset Output

The reset input of a microprocessor (µP) initiates it to a known state. The SGM825 supervisory circuit asserts a reset to the supervised µP to prevent the code-execution errors that may occur due to power-up, power-down, brownout conditions or other transients. The reset output is still in the correct logic state even if V_{CC} is lower than 1V. During power-up, when V_{CC} exceeds the rising threshold voltage ($V_{RST} + V_{HYS}$), an internal timer keeps nRESET in low state for the reset timeout period (t_{RP}) before nRESET returns to the high state (Figure 3).

If V_{CC} drops below the falling threshold voltage (V_{RST}) (a brownout condition occurs), a reset is asserted and nRESET goes low. In general, nRESET remains low for the t_{RP} (200ms, TYP) period every time after the last event. So, if during the low period of nRESET, V_{CC} goes up and dips below V_{nRST} again, the internal timer will restart for a new t_{RP} period. The nRESET output can source and sink current. RESET on the SGM825 is the inverse of nRESET.
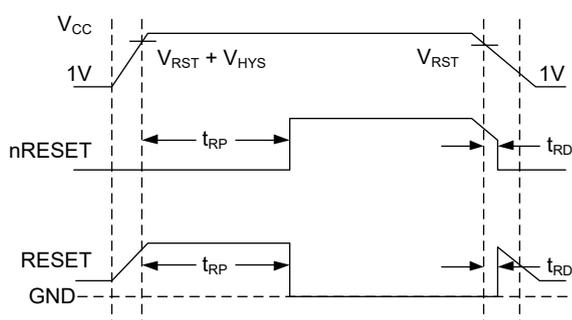
Figure 3. Reset Timing Diagram

Manual Reset Input

Many µP-based products need manual-reset capability to let the operator or an external logic reset the µP. For the SGM825, applying a logic low to the nMR input, asserts a reset (nRESET = low). nRESET remains low while nMR is low, and will stay low for the t_{RP} (200ms, TYP) period after nMR returns to high state. The nMR input is internally pulled up by a 59kΩ resistor and can be left floating if not used. It can be driven by a CMOS/TTL logic or by a switch shorting to GND. A

normally open momentary switch connected between nMR and GND pins can be used as a manual reset. Switch debouncing is not needed. However, if long cables are used to drive the nMR input or if the environment is noisy, connect a 0.1µF capacitor between nMR and GND to immune the additional noise.

Using SGM825 with Microprocessors with Bidirectional Reset Pins

Some microprocessors can internally force their reset pins low to assert a reset (bidirectional reset pins). The low pull-up current of the SGM825 allows using of them along with the microprocessors with bidirectional resets like the 68HC11. The microprocessor can force nRESET low when nRESET is pulled high by the SGM825 with no issues (Figure 4).
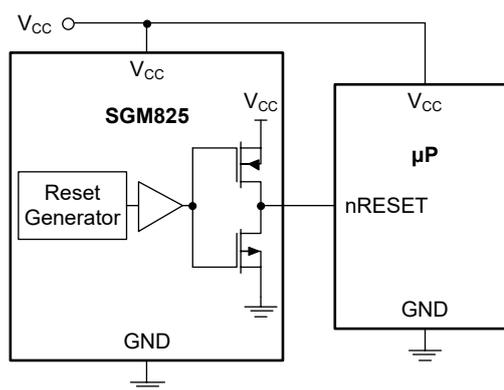

Figure 4. Interfacing to µP with Bidirectional Resets

Negative-Going V_{CC} Transient Immunity

The SGM825 has the ability to immune short time and negative V_{CC} transients or even glitches. It does not need to shut down the entire system. Resets are applied to the microprocessor during power-up, power-down and brownout conditions and not when an insignificant V_{CC} transient occurs.

A 0.1µF ceramic capacitor is recommended between the V_{CC} and GND pin to reduce the input supply noise.
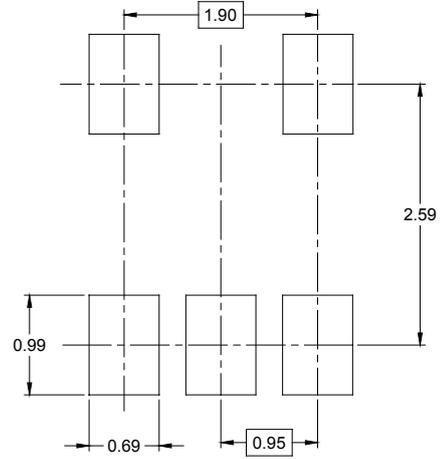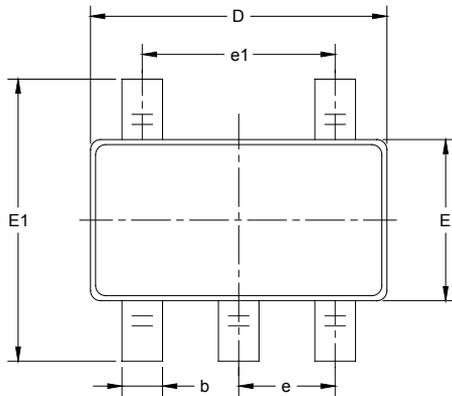
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
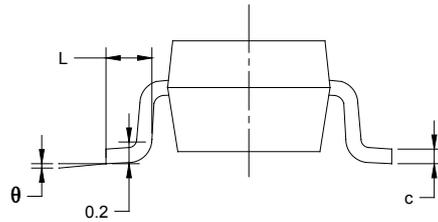
PACKAGE OUTLINE DIMENSIONS

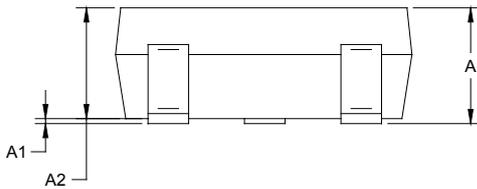## SOT-23-5

RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
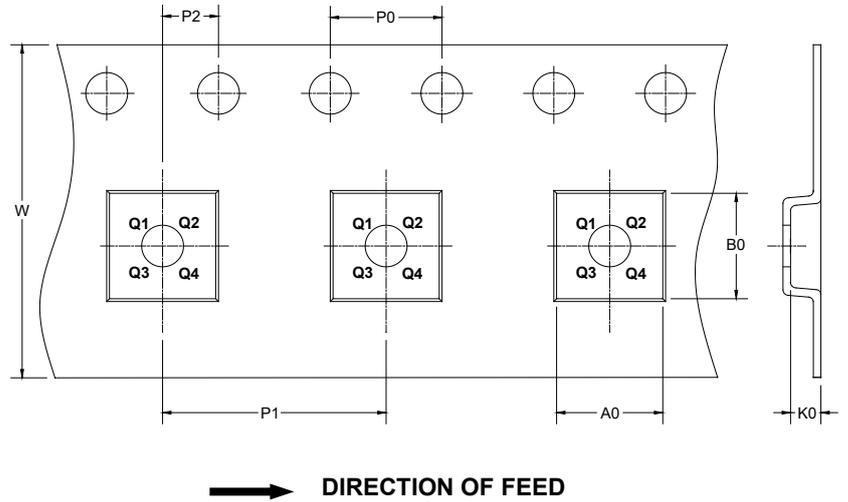
DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.
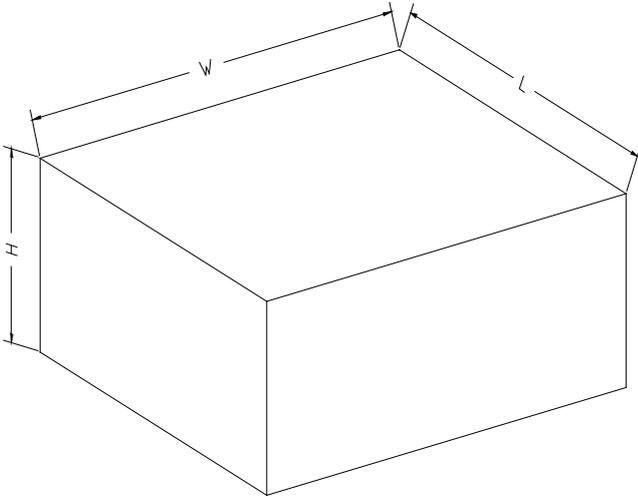
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002