VCE2765
18-Bit Magnetic Encoder for Off-Axis Application

GENERAL DESCRIPTION

The VCE2765 is a magnetic encoder based on Anisotropic Magnetic Resistance (AMR) technology, primarily designed for off-axis mounting applications. The SAR-based ADC enables an angular resolution of 18 bits for off-axis angle detection with absolute angle accuracy (INL) of <±0.3°, extremely low angle output latency of <4μs, and supports rotational speeds up to 120000rpm. The device offers various angle signal output modes, including SPI, SSI, ABZ, UVW and PWM. Users can make selections based on their specific requirements.

Due to AMR's insensitivity to the changes in magnetic field strength under saturation mode, it exhibits excellent vibration resistance and low temperature drift characteristics, making it suitable for applications in harsh environmental conditions. The built-in calibration algorithm can compensate for the zero offset, amplitude and temperature effects in real time. For users' convenience, the VCE2765 provides one-touch auto-calibration and one-touch zero-position controlled by external pins, the calibration results are stored in the MTP memory.

The VCE2765 is not only suitable for off-axis mounting applications, but also for on-axis mounting applications, in which case the output angle accuracy is ±0.2°.

FEATURES

- **For Off-Axis Shaft Mounting**
- **Automatic Calibration without External References**
- **One Touch Auto-Calibration and Zero-Position**
- **18-Bit Angular Signal**
- **Accuracy: ±0.3°**
- **Interfaces: SPI, SSI, PWM, ABZ, UVW**
- **3-Wire/4-Wire SPI Communication**
- **Maximum Tracking Speed: 120000rpm**
- **Output Latency: <4μs**
- **ABZ: 1~4096 ppr Configurable**
- **UVW: 1~64 Pairs Configurable**
- **12-Bit Angle Output in PWM Mode**
- **Wide Operating Temperature Range: -40℃ to +125℃**
- **Weak Magnetic Field Threshold Alarm, Low Voltage Threshold Alarm**
- **Built-in MTP for Multiple Programming without High Voltage Programming Port**
- **Built-in Temperature Compensation**

APPLICATIONS

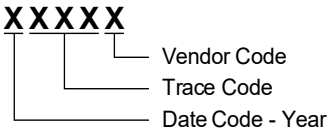
Drive Control for Drum Motors, Hub Motors, and External Rotor Motors
Stepping Servo Motors, General Purpose Servo Motors
Motion Control and Feedback for Industrial Robot Arm Joints

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	CONFIGURATION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
VCE2765	TQFN-3.5×3.5-16BL	-40℃ to +125℃	4-Wire SPI, AB = 1024, Z = 4LSB, PWM = 971.1Hz, CW	VCE2765-000XTYZ16G/TR	2765 TYZ16 XXXXX	Tape and Reel, 4000
			4-Wire SPI, AB = 1024, Z = 4LSB, PWM = 971.1Hz, CCW, HYST = 0.132°	VCE2765-002XTYZ16G/TR		
			4-Wire SPI, AB = 4096, Z = 4LSB, PWM = 971.1Hz, CW, HYST = 0.011°	VCE2765-003XTYZ16G/TR		
			3-Wire SPI, AB = 1024, Z = 4LSB, PWM = 971.1Hz, CW	VCE2765-211XTYZ16G/TR		
			3-Wire SPI, AB = 2500, Z = 4LSB, PWM = 971.1Hz, CW	VCE2765-221XTYZ16G/TR		
			3-Wire SPI, AB = 4096, Z = 4LSB, PWM = 971.1Hz, CW	VCE2765-241XTYZ16G/TR		

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 6V
All Digital Port Pin Voltage ..... -0.3V to V_{DD} + 0.3V
Package Thermal Resistance
TQFN-3.5×3.5-16BL, θ_{JA} ..... 46.8℃/W
TQFN-3.5×3.5-16BL, θ_{JB} ..... 21.8℃/W
TQFN-3.5×3.5-16BL, $\theta_{JC\ (TOP)}$ ..... 28℃/W
TQFN-3.5×3.5-16BL, $\theta_{JC\ (BOT)}$ ..... 12.4℃/W
Junction Temperature ..... +125℃
Storage Temperature Range ..... -50℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
Latch-Up ..... -200mA to 200mA
ESD Susceptibility (1) (2)
HBM ..... ±8000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} ..... 3.0V to 5.5V
All Digital Port Pin Voltage Range ..... -0.3V to V_{DD}
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

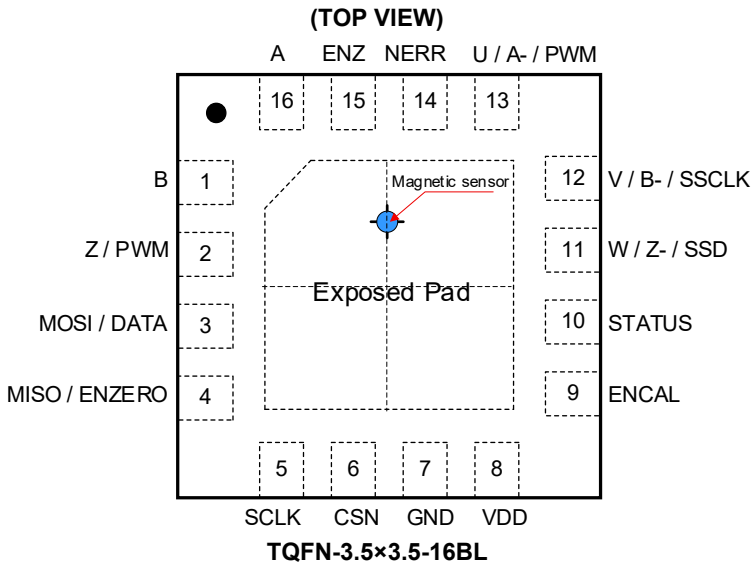
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-3.5×3.5-16BL

PIN DESCRIPTION

PIN	PIN NAME				TYPE (1)	FUNCTION
	MODE 1	MODE 2	MODE 3	MODE 4		
1	B	B+	-	B	DO	Incremental Output B/B+.
2	Z	Z+	PWM (2)	Z	DO	Incremental Output Z/Z+, PWM Output.
3	MOSI (DATA)				DI/O	MOSI Pin for 4-Wire SPI, DATA Pin for 3-Wire SPI.
4	MISO (ENZERO)				DI/O	MISO in 4-Wire SPI Mode, NC or ENZERO (External Write-Zero with Internal Pull-Up) in 3-Wire SPI Mode.
5	SCLK				DI	SPI Clock Signal, Internal Pull-Up.
6	CSN				DI	SPI Chip Select Signal, Internal Pull-Up.
7	GND				G	Ground.
8	VDD				P	Power.
9	ENCAL				DI	External Calibration Function Enable with Internal Pull-Down.
10	STATUS				DO	Status Indication Output.
11	W	Z-	W	SSD	DO	W/Z- Output; SSI Data Output (SSD).
12	V	B-	V	SSCLK	DI/O	V/B- Output / SSI Clock Input (SSCLK, Internal Pull-Down).
13	U	A-	U	PWM (2)	DO	U/A- Output / PWM Output.
14	NERR				DO	Alarm Indication Output.
15	ENZ				DI	External Control Z Signal Output Enable with Internal Pull-Up.
16	A	A+	-	A	DO	Incremental Signal A/A+ Output.
-	Exposed Pad				-	Floating or Grounded.

NOTES:

1. DI: Digital Input, DO: Digital Output, DI/O: Digital Inputs and Outputs, G: Ground, P: Power.
2. Multiplexing mode 3 and multiplexing mode 4 both contain PWM, but the pin is different, no special requirements, PWM mode factory default mode 4.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 3.0V to 5.5V, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Power Supply Voltage	V_{DD}	-40℃ ≤ T_A ≤ +125℃	3.0	3.3/5.0	5.5	V
Active Supply Current	I_{DD}			13.6	18.5	mA
DC Characteristics						
Integral Non-Linearity	INL	+25℃, operating magnetic field > 300Gs, off-axis		±0.3		°
		+25℃, operating magnetic field > 300Gs , on-axis		±0.2		°
Maximum Tracking Speed	Speed	1-pole pair			120000	rpm
Transient Noise[1]	TN	+25℃, BW0, RMS		0.007		°
Window Hysteresis	HYST	Register configurable@ HYST[2:0] = 010		0.022		°
System Delay	t_{DELAY}	Actual latency without compensation		4		μs
Power-On Reset	POR	T_A = +25℃	2.4	2.65	2.85	V
POR Hysteresis	POR_{HYST}			0.15		V
System Power-Up Time	$t_{POWER-UP}$			7.5		ms
Operational Temperature	T_A		-40		125	℃
Angle Range	α		0		360	°
Digital I/O Characteristics						
Output Rising Time	t_{RO}	C_{LOAD} = 15pF			20	ns
Output Falling Time	t_{FO}	C_{LOAD} = 15pF			20	ns
Digital I/O Output Logic High Level	V_{HSO}	I_{OUT} = 2mA	V_{DD} - 0.5			V
Digital I/O Output Logic Low Level	V_{LSO}	I_{OUT} = 2mA			0.5	V
Digital I/O Input Logic High Level	V_{HSI}		0.75 × V_{DD}			V
Digital I/O Input Logic Low Level	V_{LSI}				0.2 × V_{DD}	V

NOTE: 1. The transient noise and system delay are configurable according to the condition of system filtering.

DYNAMIC CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 3.0V to 5.5V, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ABZ/PWM/UVW Output Mode Parameters						
AB Pulse per Turn	R_{AB}	Configurable	1		4096	ppr
UVW Pair of Poles per Turn	R_{UVW}	Configurable	1		64	Pair
Frequency in PWM Mode	f_{PWM}	Configurable to 121.4Hz, 242.8Hz, 485.6Hz, 971.1Hz, 1942.2Hz, 3884.4Hz, 7768.8Hz	121.4		7768.8	Hz
MTP Characteristics						
Read/Write Voltage	V_{MTP}		3.0		5.5	V
Erasable/Write Cycles	Memory Endurance			1000		Cycle
Data Retention	-	@150℃		10		Year

TYPICAL PERFORMANCE CHARACTERISTICS

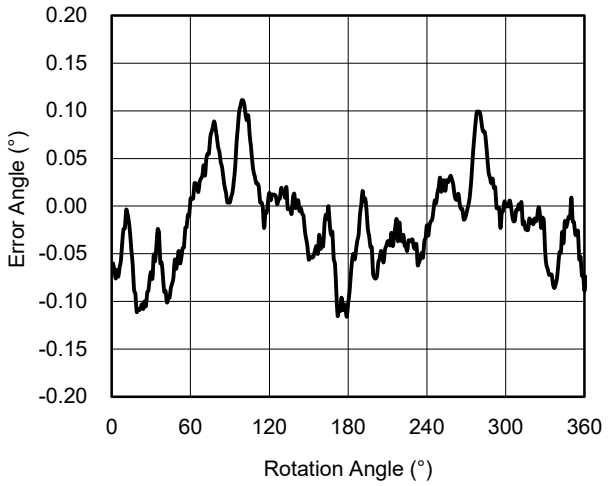


Figure 1. Accuracy (INL) in Full Range for Off-Axis Mounting (Magnetic Field > 300Gs, +25℃)

TYPICAL APPLICATION CIRCUITS

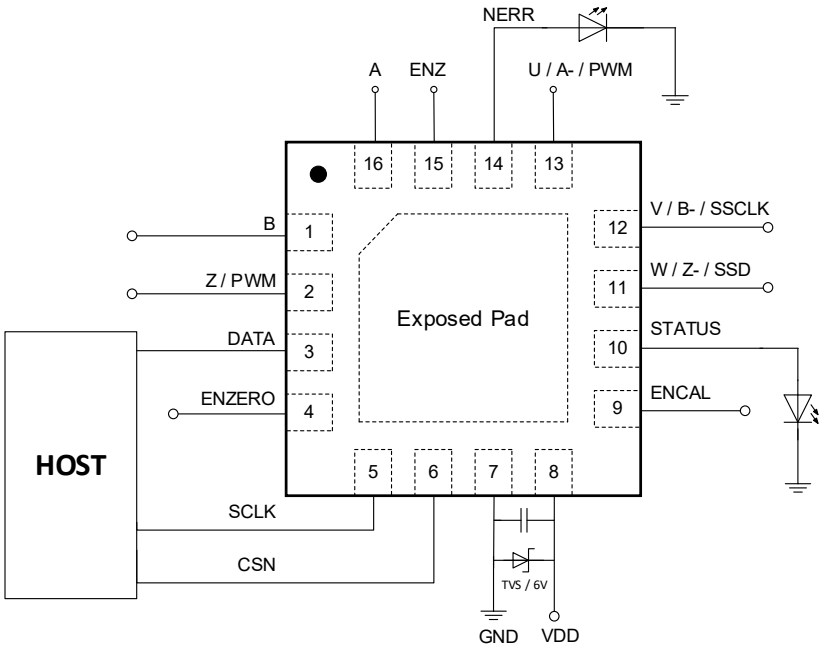


Figure 2. Application Circuit for the 3-Wire SPI

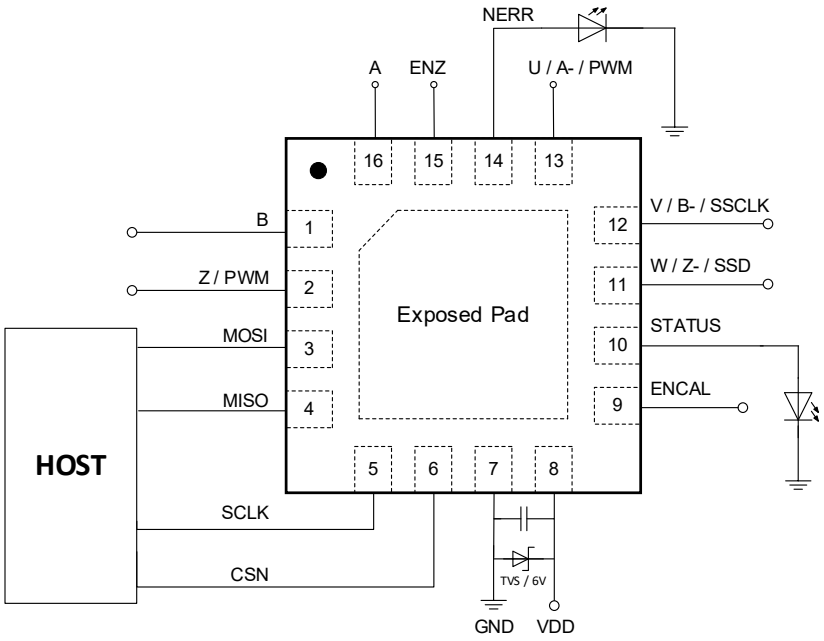


Figure 3. Application Circuit for the 4-Wire SPI

FUNCTIONAL BLOCK DIAGRAM

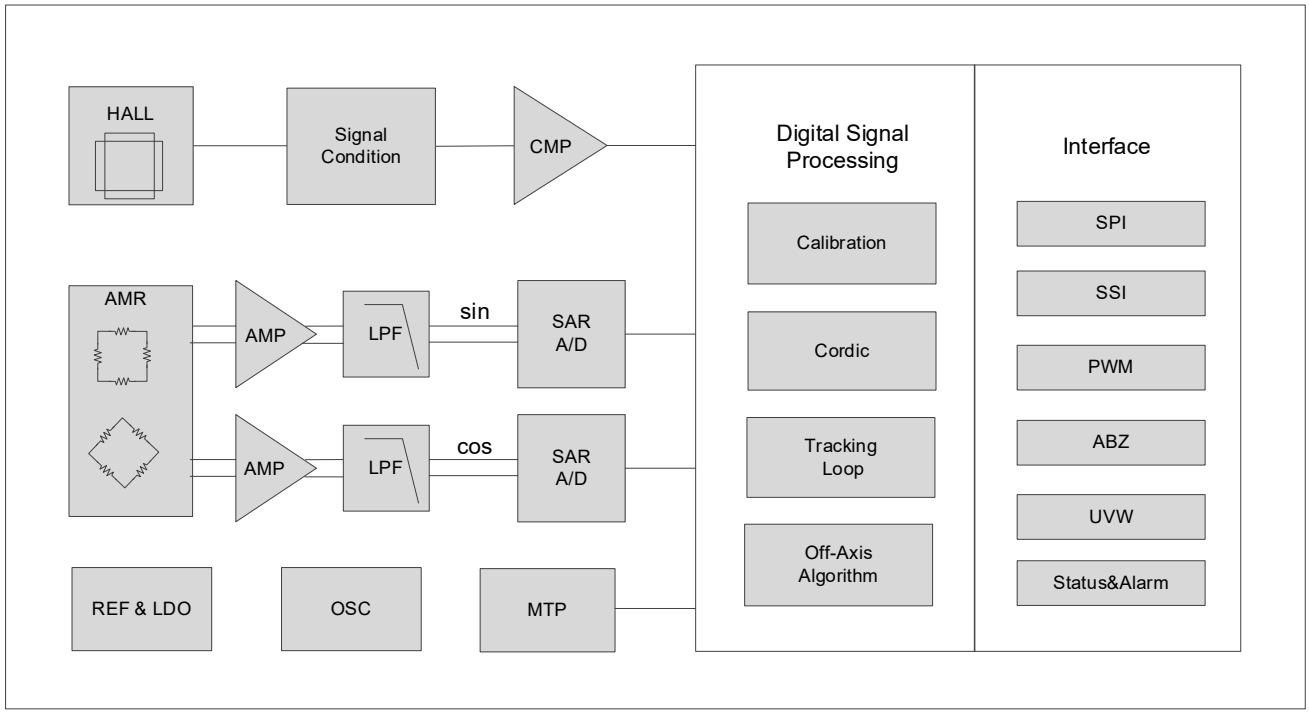


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The VCE2765 contains two AMR magnetic sensors that provide sine and cosine outputs that vary with the angle of the magnetic field. The signals are amplified and digitally converted, and together with the hall signals are processed by an algorithm to obtain angle signals from 0 to 360°, which are then output through various interfaces. The SAR structure of the ADC together with the Tracking Loop filtering guarantees a very low signal delay. The MTP stores the configuration of the various modes, compensation parameters and the zero-position of the external motor, which can be rewritten multiple times.

By enabling ENCAL and ENZERO pins, VCE2765 can realize auto-calibration and zero write for off-axis encoder. The NERR and STATUS pins indicate operation status and abnormality alarms for users' conveniences.

Rotation Direction and Output Signals

The device is mounted on one side of the magnetic ring. Figure 5 shows the clockwise rotation of the magnetic ring and the corresponding angle output curve in CW mode. Figure 6 shows the counterclockwise rotation of the magnetic ring and the corresponding angle output curve in CW mode.

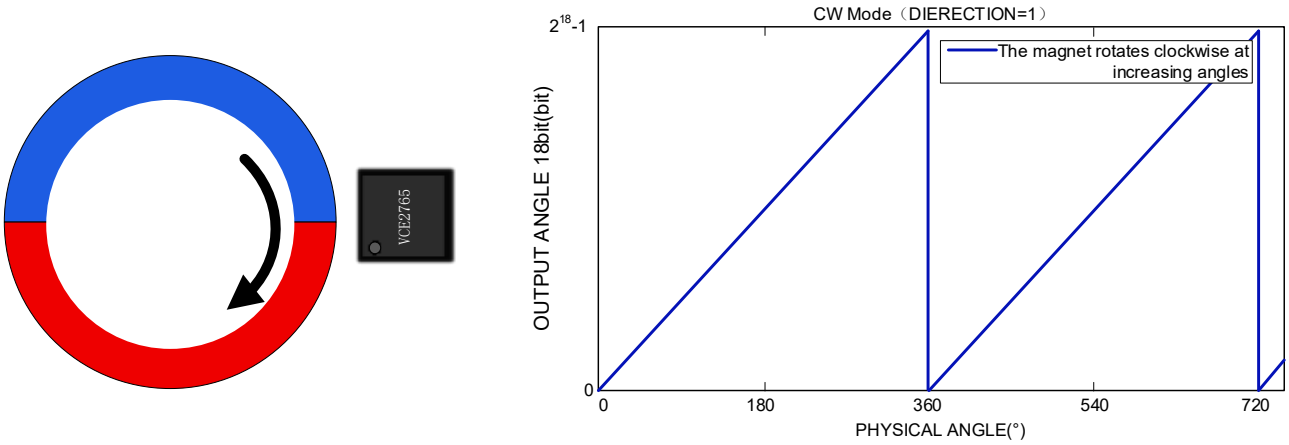


Figure 5. Clockwise Rotation of the Magnetic Ring and Angle Output in CW Mode

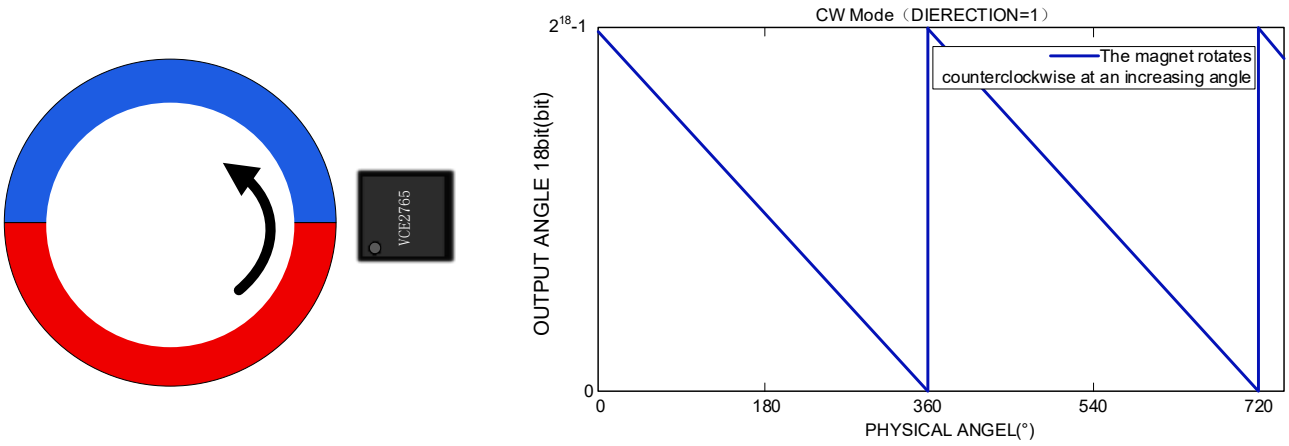


Figure 6. Magnetic Ring Rotating Counterclockwise and Angle Output in CW Mode

DETAILED DESCRIPTION (continued)

ABZ Output Mode

Figure 7 illustrates the output signals of A, B, and Z during clockwise (CW)/counterclockwise (CCW) magnet rotation in CW mode. For CW rotation (refer to Figure 5), the A signal lags the B signal by a quarter-period. For CCW rotation (refer to Figure 6), the A signal leads the B signal by a quarter-period. The Z signal indicates the 0° angular position, generating one pulse per 360° magnet rotation. The Z-signal high-level pulse width is user-programmable via register Z_WIDTH[2:0] to achieve specific duty cycle requirements. Alternatively, the Z high-level width can be set to 180°, where one complete Z pulse cycle (high + low states) constitutes a 360° signal output.

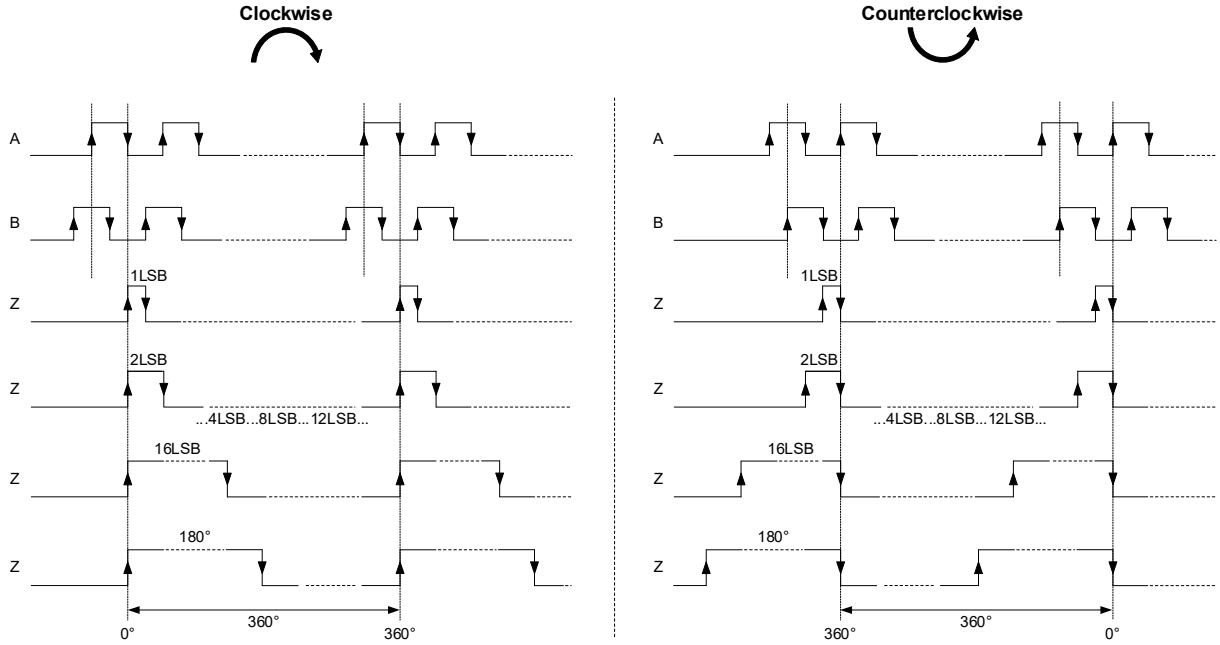


Figure 7. ABZ Signal Output Diagram (Z pulse width Optional: 1/2/4/8/12/16LSBs/180°)

The ABZ output resolution (PPR) is configurable via register ABZ_RES[11:0], supporting 1~4096 pulses per revolution (PPR). As shown in Figure 8, when configured for 1024 PPR, the output provides 4096 steps per revolution.

In addition, the polarity of the ABZ output signal can be inverted by configuring the ABZ_INV[0] register.

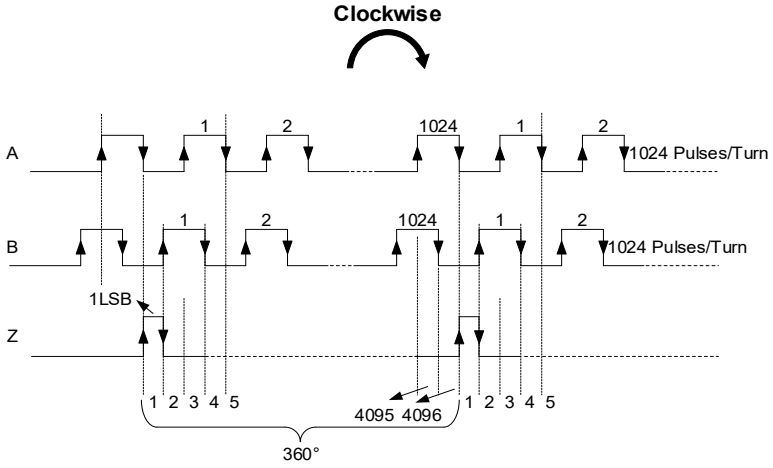


Figure 8. AB Signal Resolution is 1024 Pulses per Revolution in CW Mode during Clockwise Magnet Rotation

DETAILED DESCRIPTION (continued)

Output Pulse Sequences of ABZ Signals during the Power-Up

During the $t_{POWER-UP}$ period in ABZ output mode, the output pulse sequence can be configured via the ABZ_INI_DELAY[1:0] register. There are six selectable options. The factory default is pulse sequences 1.

Pulse sequence 1: Standard output, the ABZ output will first assert a low-level signal for approximately 7.5ms before entering normal operation, as shown in Figure 9.

Pulse sequences 2~5: The angle pulse output at power-up with configured 25/50/200/1000ms delay, as shown in Figure 10.

Pulse sequence 6: Angle pulse output at power-up delayed with the Z-pulse generating a dedicated pulse sequences, as shown in Figure 11.

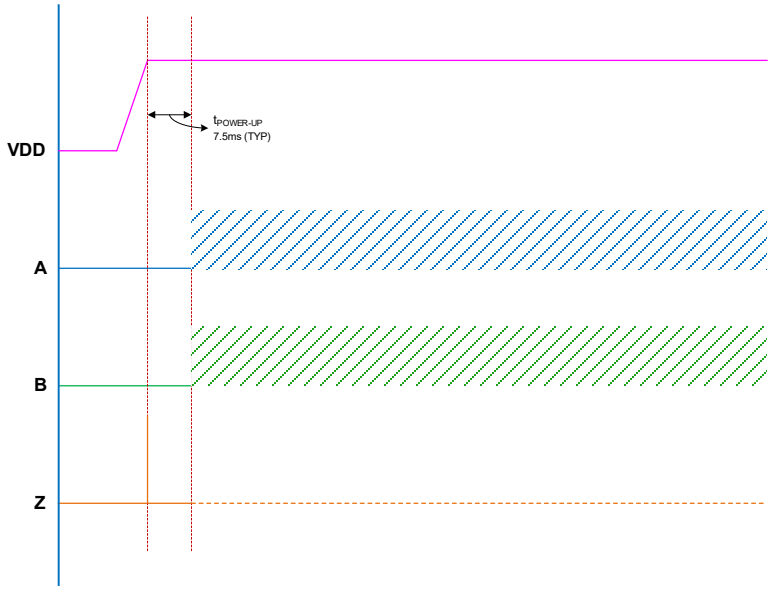


Figure 9. Pulse Sequence 1 after Power-Up

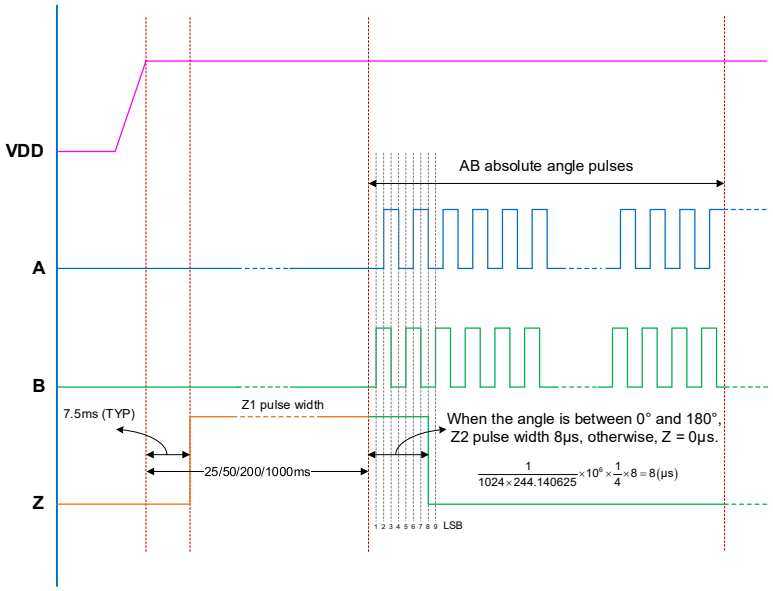


Figure 10. Pulse Sequences 2~5 after Power-Up

DETAILED DESCRIPTION (continued)

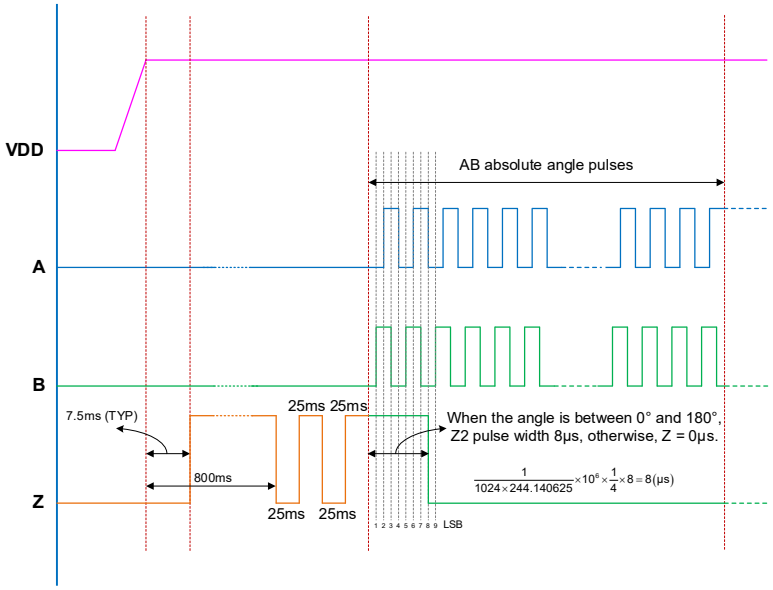


Figure 11. Pulse Sequence 6 after Power-Up

When power-up pulse sequences 2~6 are selected, the absolute angle at power-up is calculated based on the AB pulse count, with the calculation determined by the resolution (PPR) and the number of AB pulses (refer to Table 1). Moreover, the frequency of the AB pulse output is determined by the resolution (PPR), calculated as: Frequency ≈ PPR × 244.14 (Hz).

Table 1. ABZ Output Power-Up Pulse Sequences Configuration Description

Impulse	Angular Range	Formula
B leads A	0°~180°	ANGLE (°) = $\frac{360}{PPR}$ × Number Of Pulses Read
A leads B	180°~360°	ANGLE (°) = 360 - $\frac{360}{PPR}$ ×Number Of Pulses Read

Example: When PPR = 1024, the number of A (B) pulses at power-up is 415, and since A leads B, the power-up absolute ANGLE (°) = 360 - $\frac{360}{1024}$ ×415 ≈ 214.10°.

DETAILED DESCRIPTION (continued)

UVW Output Mode

The U, V, and W phases are electrically spaced 120 degrees apart, with the corresponding mechanical angle determined by the motor's pole pair count. Users can configure the UVW pole pairs per revolution via register UVW_RES[5:0] according to the motor design. Figure 12 illustrates the UVW output signals for 1-pole pair and 2-pole pair configurations when the magnet rotates clockwise in CW mode. Figure 13 illustrates the ABZ and UVW output pulse sequences for a configuration with AB resolution PPR = 9, Z pulse width of 1LSB, and UVW at 3-pole pair during clockwise rotation in CW mode.

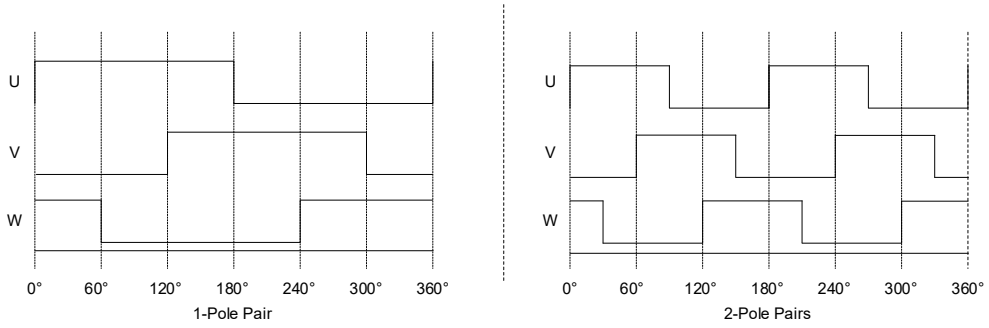


Figure 12. UVW Pulse Sequences for 1-Pole Pair and 2-Pole Pair in CW Mode with Clockwise Magnet Rotation

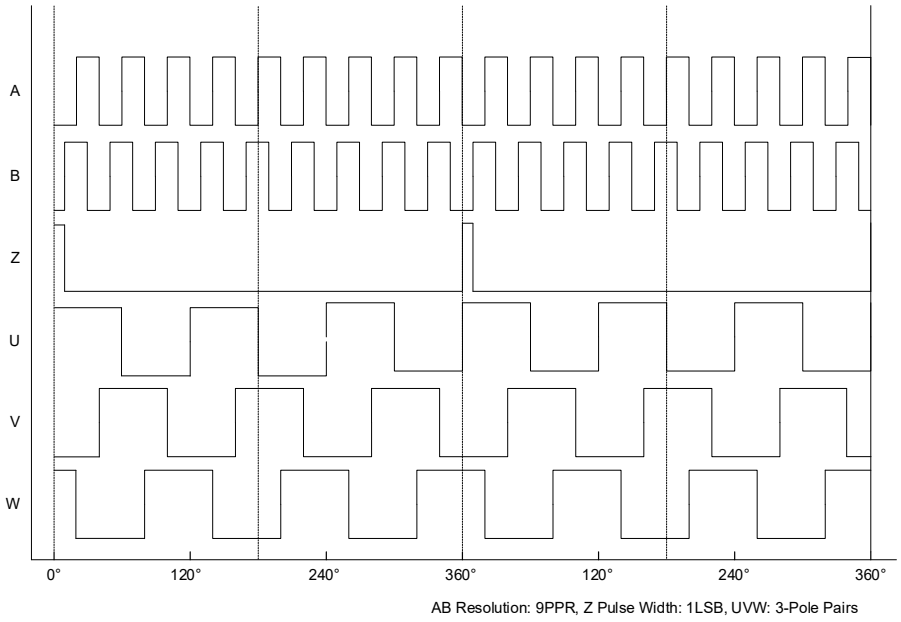


Figure 13. ABZ and UVW Output Pulse Sequences in CW Mode with Clockwise Magnet Rotation

DETAILED DESCRIPTION (continued)

PWM Output Mode

The PWM output resolution is 12-bit. The entire PWM signal period consists of 4119 minimum pulse widths t_U, where the each t_U depends on the PWM output frequency. The default PWM output frequency is 971.1Hz, corresponding to a minimum unit t_U of 250ns. Via registers PWM_FREQ[2:0], the PWM output frequency can also be set to 121.4Hz, 242.8Hz, 485.6Hz, 1942.2Hz, 3884.4Hz and 7768.8Hz corresponding to minimum units t_U of 2000ns, 1000ns, 500ns, 125ns, 62.5ns, 32ns respectively.

As shown in Figure 14, the PWM signal begins with a start signal t_{START} consisting of 16 consecutive high-level pulse width t_U, and ends with a stop signal t_{END} consisting of 8 consecutive low-level pulse width t_U. The middle section contains 0 to 4095 minimum pulse width representing absolute angles from 0° to 360°. The PWM output frequency shown in the Figure 14 is 971.1Hz, where each minimum pulse width t_U of 250ns represents an absolute angle of 0.088°.

PWM angle calculation formula: $ANGLE(°) = [4119 \times (\frac{t_{ON}}{t_{PWM}}) - 16] \times \frac{360}{4096}$ (t_{ON}: Duration of high level, $t_{ON} = n \times t_U + t_{START}$)

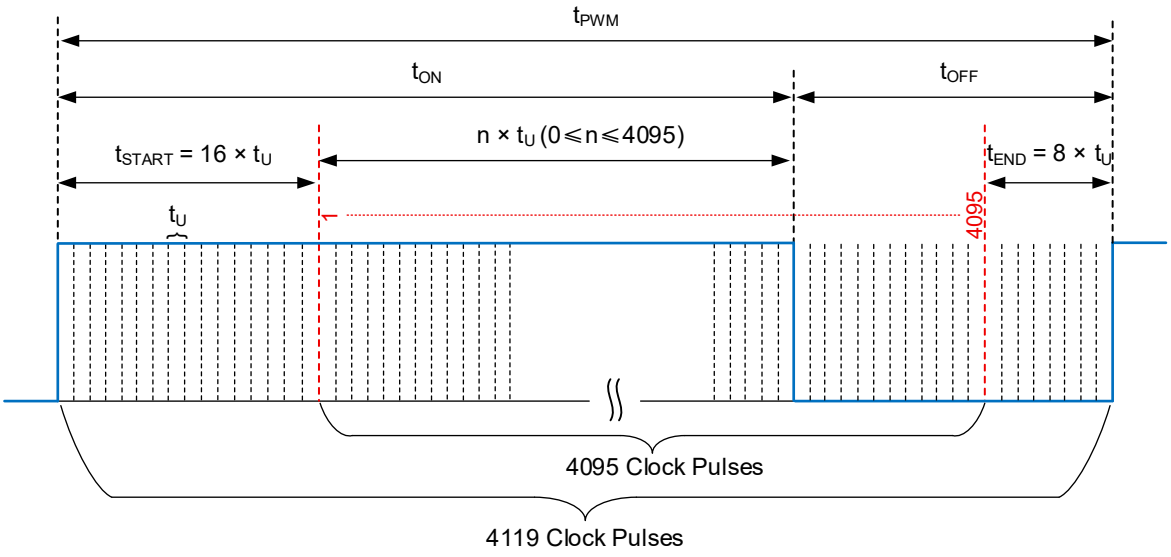


Figure 14. PWM Signal Output

DETAILED DESCRIPTION (continued)

SPI Interface

The VCE2765 supports a 3-wire SPI synchronous serial communication interface. The transfer protocol uses mode 3, specifically CPOL = 1, CPHA = 1, where SCLK idles at high level, the first clock edge is falling edge, the second clock edge is rising edge, and data is sampled on the rising edge. The SPI timing is shown in Figure 15.

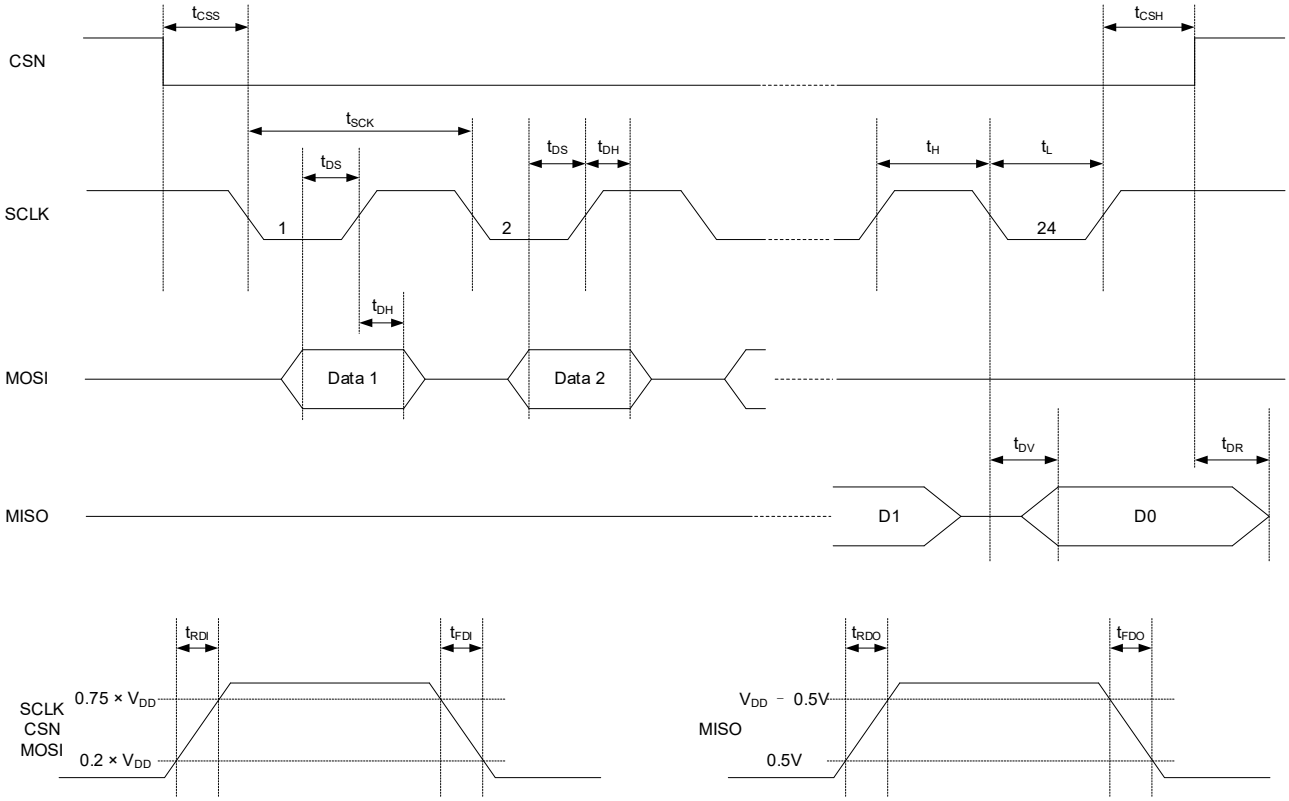


Figure 15. SPI Timing Sequence

Table 2. SPI Timing Requirement

PARAMETE	SYMBOL	MIN	TYP	MAX	UNITS
CSN Setup Time	t_{CSS}	100	-	-	ns
CSN Hold Time	t_{CSH}	0.5 × t_{SCK}	-	-	ns
SCLK High Time	t_H	30	-	-	ns
SCLK Low Time	t_L	30	-	-	ns
SCLK Cycle Time	t_{SCK}	60	-	-	ns
Input Rise Time	t_{RDI}	-	10	-	ns
Input Fall Time	t_{FDI}	-	10	-	ns
Data Output Rise Time	t_{RDO}	-	10	-	ns
Data Output Fall Time	t_{FDO}	-	10	-	ns
Data Setup Time	t_{DS}	10	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Data Valid Time	t_{DV}	-	-	25	ns
Data Release Time	t_{DR}	-	-	30	ns

DETAILED DESCRIPTION (continued)

SPI Register Read/Write

SPI communication is triggered by the falling edge of the chip select signal (CSN) and terminated by its rising edge. Data is sampled on the rising edge of the SCLK clock signal. In 3-wire SPI applications, the DATA line serves as both the data input and output for the device. The R/W signal indicates the SPI read/write operation mode, where R/W = 0 denotes a write operation and R/W = 1 denotes a read operation.

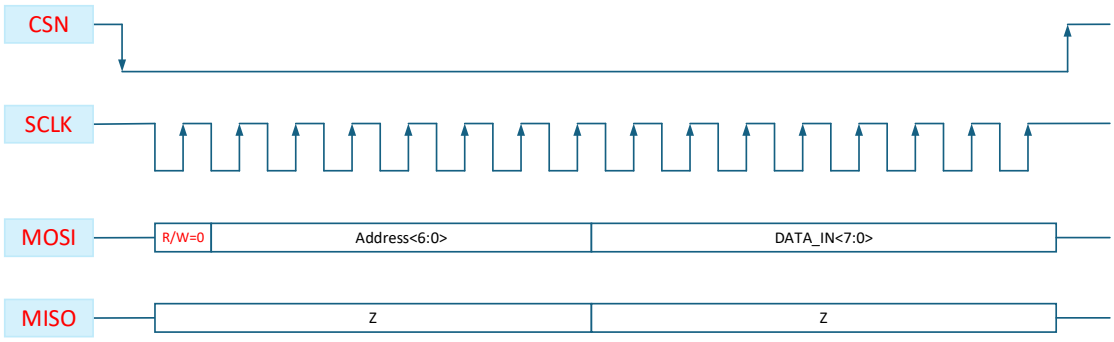


Figure 16. 4-Wire SPI Write Timing Diagram

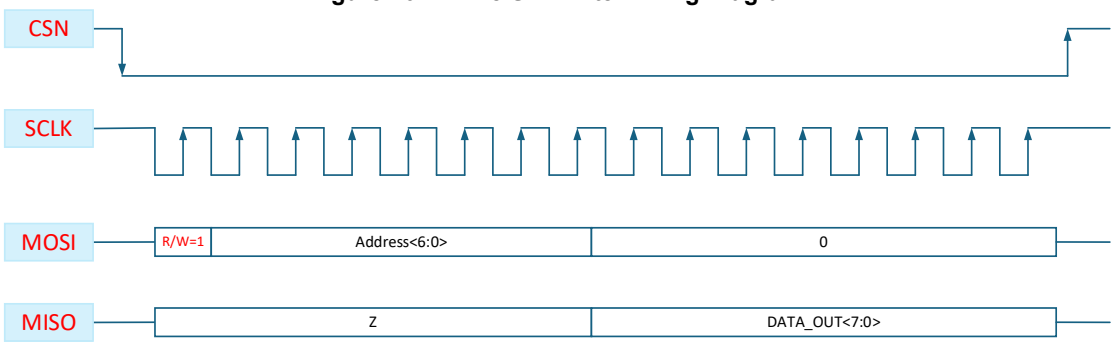


Figure 17. 4-Wire SPI Read Timing Diagram

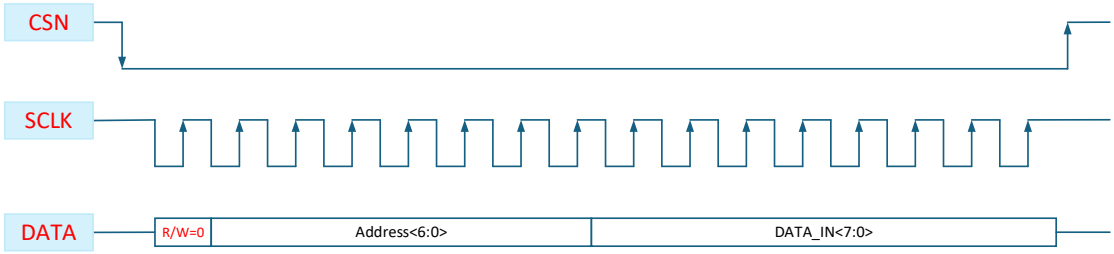


Figure 18. 3-Wire SPI Write Timing Diagram

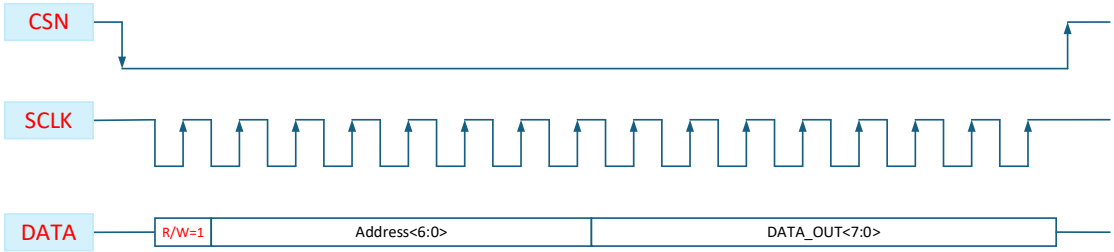


Figure 19. 3-Wire SPI Read Timing Diagram

DETAILED DESCRIPTION (continued)

SPI Single and Continuous Angle Reading

In single-read mode, one complete set of angle data is read out with each operation. After CSN is pulled down, a read command 0xC3 (R/W=1b, Address[6:0] = 100 0011b) must be sent, and the register group 0x43, 0x44 and 0x45 are read. After the data group is retrieved, CSN is pulled high. To read the next group of data, CSN must be pulled down again, and the read command must be sent. The 4-wire SPI is shown in Figure 20 and the 3-wire SPI is shown in Figure 22.

To improve the efficiency of reading angle data, the continuous-read mode can be adopted. As shown in Figure 21 for the 4-wire SPI and the 3-wire SPI is shown in Figure 23, after pulling down CSN, a read command 0xC3 (R/W = 1b, Address[6:0] = 100 0011b) is sent once. Without pulling CSN high, data will be cyclically read in units of 0x43, 0x44, and 0x45 until CSN is pulled high to end the continuous reading. In this mode, while reading the CRC of the Nth group of data, the $(N+1)^{th}$ group of angle data is latched.

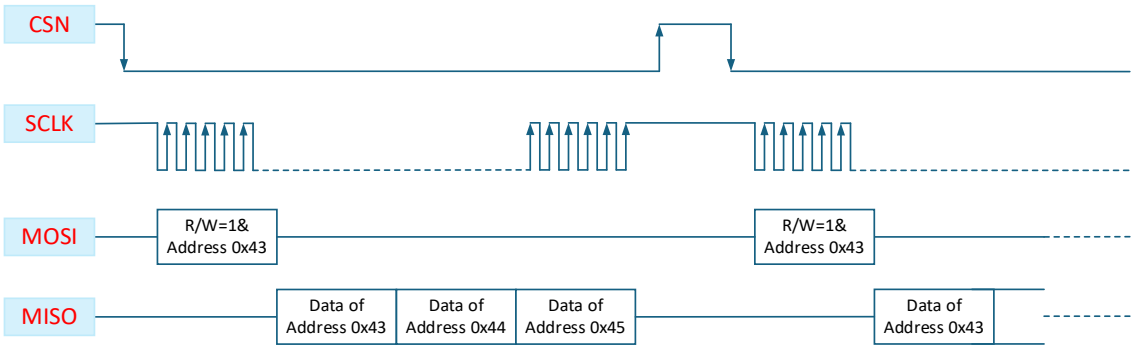


Figure 20. 4-Wire SPI Single Read Angle Timing Diagram

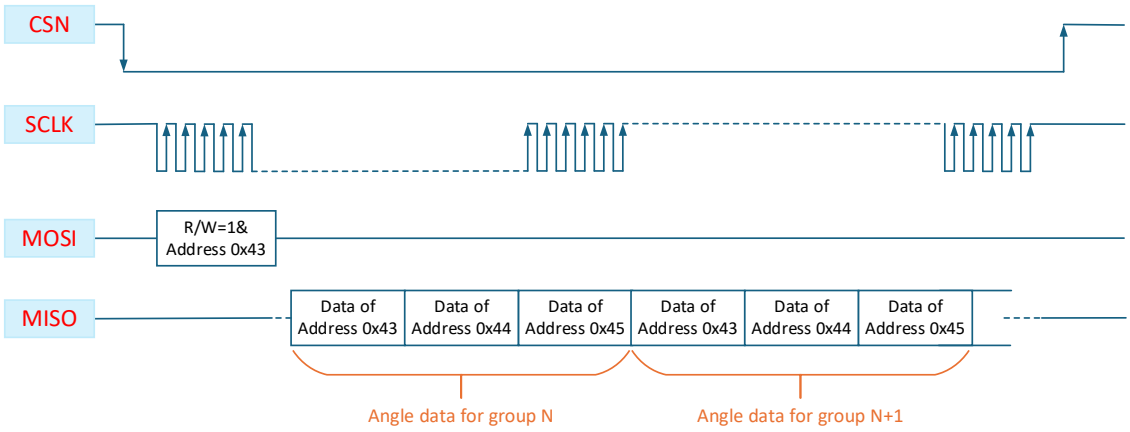


Figure 21. 4-Wire SPI Continuous Read Angle Timing Diagram

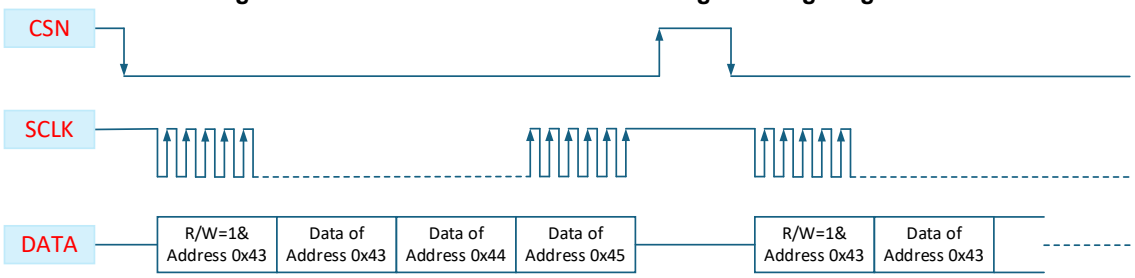


Figure 22. 3-Wire SPI Single Read Angle Timing Diagram

DETAILED DESCRIPTION (continued)

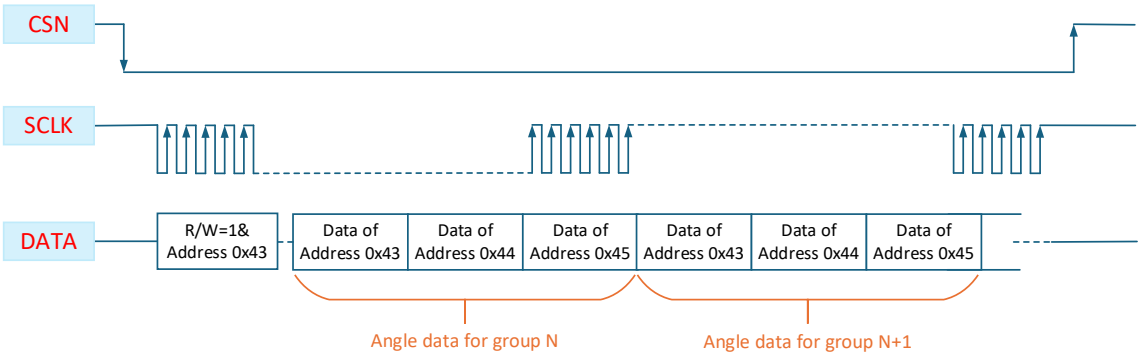


Figure 23. 3-Wire SPI Continuous Read Angle Timing Diagram

SPI Angle Output

Registers 0x43, 0x44, and 0x45 store 18-bit angle data, where the effective number of bits for the angle data is 13 bits in off-axis application. Users can obtain higher-resolution data through filtering based on the acquired 18-bit angle data. The read angle data is based on the zero-position angle defined by the application. The current 18-bit angle output ANGLE equals the internally generated original 18-bit angle (filter output) minus the 18-bit offset angle (the high 12 bits are the zero-position register ZERO_POS[11:0], and the low 6 bits are padded with zeros).

Angle Calculation Formula: $\text{ANGLE}\,(°) = \text{ANGLE}\,(°)\,(\text{18-bit}) \times \frac{360}{2^{18}}$

SSI Interface

Figure 24 shows the SSI timing diagram and Table 3 shows the SSI timing parameters.

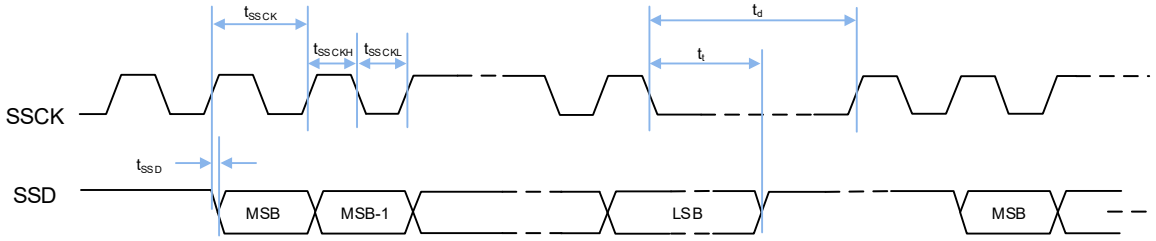


Figure 24. SSI Timing Diagram

Table 3. SSI Timing Requirement

PARAMETER	SYMBOL	MIN	MAX	UNITS
	t_{SSD}	-	25	ns
SSCK Period	t_{SSCK}	0.05	16	μs
SSCK Low Level	t_{SSCKL}	0.02	8	μs
SSCK High Level	t_{SSCKH}	0.02	8	μs
Transfer Timeout (Monoflop Time)	t_T	25		μs
Interval Time (Wait Time for Next Data Reading)	t_D	40		μs

DETAILED DESCRIPTION (continued)

As shown in Figure 25, SSI communication uses 25 clock cycles per data frame. The first clock serves as the start signal, with data transmission beginning from the second clock. Data is sampled on the falling edge of the clock. The SSCK remains low when idle, and the interval between two data frames is ≥40μs.

One data frame consists of 24 bits, including 16-bit angle data, 2-bit detection bits, and 6-bit CRC check bits, as follows:

- D15 ~ D0: 16-bit angle data.
- S1: Low magnetic field (SMF) alarm flag. SMF = 1 indicates an alarm; SMF = 0 indicates normal operation.
- S0: Low voltage (LOW_VOL) alarm flag. LOW_VOL = 1 indicates an alarm; LOW_VOL = 0 indicates normal operation. The alarm is triggered when the supply voltage drops below 2.9V.
- CRC5 ~ CRC0: 6-bit CRC checksum calculated over the 18-bit data (D15 ~ D0 angle data and S1 ~ S0 status bits). The corresponding CRC generator polynomial is $X^6 + X + 1$ with an initial value of 6'b000000. Input and output data are not inverted.

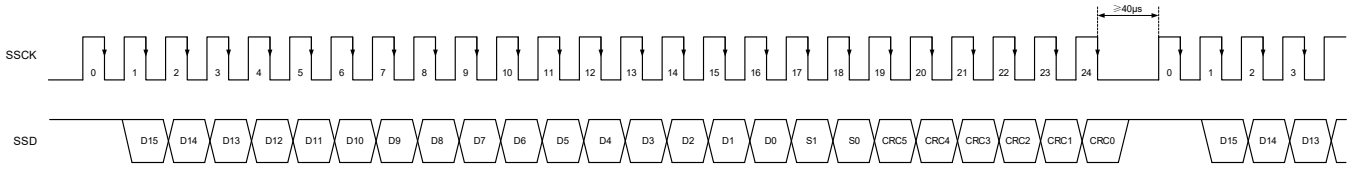


Figure 25. SSI Timing Diagram and Data Structure

Calibration and Compensation

The VCE2765 features enabled-by-default automatic calibration. It must be performed after installation with a magnet attached to a motor. When the motor has a stable rotating speed, initiated either through pin (ENCAL) enable (one-touch calibration) or SPI command triggering, the device collects the data of the spinning magnet and automatically calculates compensation parameters, the whole calibration process takes a few seconds to complete. STATUS pin indicates the results.

The device auto-calibration function can be triggered by connecting the ENCAL pin to a high level, but it is necessary to keep ENCAL high until the calibration is successful, and it is necessary to release ENCAL to low after the calibration is successful.

The SPI calibration code starts the process by writing "AA'h" to register 0x70, stops the process by writing "55'h" to register 0x70, the process can be terminated after the calibration is successful or in the middle of the calibration. The calibration status can be determined by reading the lower two bits of 0x70 (bit[0] and bit[1]) during calibration.

The motor should be kept at a constant speed during calibration, (the smaller the speed fluctuation, the higher the calibration accuracy), and the speed should be ≥50RPM.

The STATUS pin can also observe the calibration state, via the configuration register LED_DRIV_EN, two output modes can be configured, one for PWM output, the other for LED driver, detailed description as shown in Table 4.

Table 4. STATUS Output Status during Calibration

Calibration State	PWM Output（LED_DRIV_EN = 0）	LED Driver Output (1)（LED_DRIV_EN = 1）
Calibrating	1kHz, 50% Duty Cycle	LED Flashing (1Hz, 50% Duty Cycle)
Successful Calibration	High Level	LED Stays On (High Level)

NOTE: 1. LED driver output is 10mA constant current output, NERR pin should be connected to LED positive terminal.

DETAILED DESCRIPTION (continued)

Angle Hysteresis

To prevent angle transient jitter, different levels of angle hysteresis can be selected by configuring register HYST[2:0] to suppress jitter.

Abnormal Operation Alarm

VCE2765 controls the output of NERR and STATUS pins via the configuration register LED_DRIV_EN, which can observe the weak magnetic alarm, low voltage alarm, AB Pulse High Frequency Alarm, and MTP calibration abnormality alarm function, NERR and STATUS pin outputs can be PWM pulses or LED drivers, as shown in Table 5.

Table 5. NERR, STATUS Pin Output Status during Abnormal Operation

Pin	Status	PWM Output (LED_DRIV_EN = 0)	LED Driver Output (1) (LED_DRIV_EN = 1)
NERR	Operating Normally	High Level	LED Stays On (High Level)
	Operating Abnormally (2)	1khz, 50% Duty Cycle	LED Flashing (1Hz, 50% Duty Cycle)
STATUS	Field Weakening Alarm (3)	250Hz, 75% Duty Cycle	LED Flashing (1Hz, 50% Duty Cycle)
	Under-Voltage Alarm (4)	250Hz, 50% Duty Cycle	LED Flashing (0.25Hz, 50% Duty Cycle)

NOTES:

1. LED driver output is 10mA constant current output, NERR pin should be connected to LED positive terminal.
2. When any bit of register ERROR FLAG 0x42[3:0] is set to "1", then it is a "working abnormality".
3. The weak magnetic alarm is triggered when the magnetic field detected by the device falls below the weak magnetic alarm threshold, which can be configured via register WEAK_MAG_LVL[1:0] as required.
4. Low voltage alarm triggered when voltage falls below 2.9V.

When a device fault alarm is triggered, the specific fault type can be determined by reading the ERROR_FLAG register value at address 0x42[3:0].

Off-Axis Mounting Instructions and Magnet Recommendations

It is recommended to use a 1-pole pair, radially magnetized ring magnet with the VCE2765, three key considerations should be taken into account.

- Coaxially deviation between the magnetic ring axis and the rotation axis (marked as e in Figure 26) will introduce angular measurement errors. Please make efforts to ensure the alignment. This effect becomes more pronounced with smaller inner/outer diameter rings, so larger rings are preferred when mounting space permits, to minimize alignment-induced errors.
- The line between the center of magnet ring and the center of device should be perpendicular to the device edge, as non-perpendicular alignment (marked as α in Figure 26) will also cause angular errors.
- The Pin13~Pin16 side should be placed close to the magnetic ring, as the magnetic field strength at the sensor location is stronger.

DETAILED DESCRIPTION (continued)

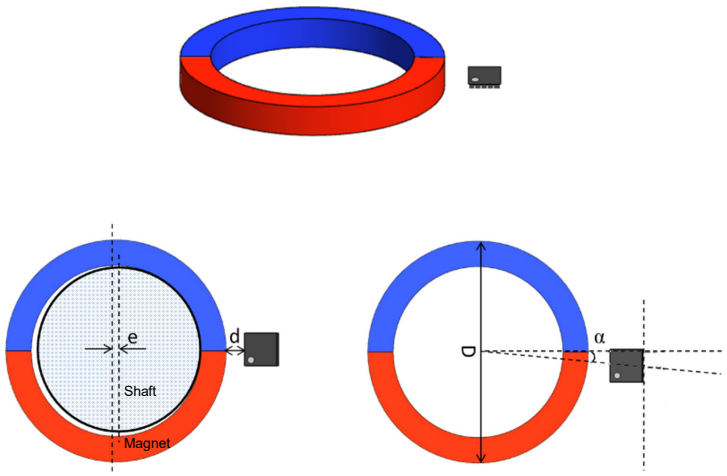


Figure 26. Off-Axis Magnet Installation Diagram

The basic magnet and device mounting parameters are shown in Table 6.

Table 6. External Magnet Parameters of Off-Axis

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Outer Diameter	D	Single pole magnet ring, radially magnetized, inner diameter determined by the rotating shaft.		15	30	mm
Magnet Ring Thickness	T	-	2	3		mm
Airgap	d	Spacing between the outer diameter and the edge of the device.		2	3	mm
Offset Angle	α	Deviation of the perpendicularity. The line between center of the ring and the device to the edge of the device.			2	°
Coaxial Deviation	e	Distance between the center of Magnet and the center of the shaft.			0.3	mm
Operating Magnetic Field	H	Parallel Magnetic field on surfaces of the device.	300			Gs

On-Axis Mounting Instructions and Magnet Recommendations

The VCE2765 can be mounted on-axis and paired with a rotating magnet parallel to it to measure the rotation angle, speed and direction. It is recommended to use a 1-pole pair, radially magnetized cylindrical magnet. Note that since the center of the sensing point of the VCE2765 does not coincide with the center of the chip, in on-axis applications the center of the magnet should be aligned with the center of the sensing point of the chip.

The AMR magnetoresistive sensor requires a certain magnetic field during operation to keep it in saturation. The closer the magnet is to the surface of the chip, the higher the magnetic field; therefore, it is recommended to keep the chip as close to the magnet as possible to ensure measurement accuracy. Due to mounting tolerances, an offset between the center of the magnet and the sensing point of the chip will introduce angular errors in the measurement results. For magnets with a smaller diameter, the angular error caused by the mounting offset becomes more pronounced. Therefore, when mounting space permits, a magnet with a larger diameter should be selected to reduce the angular error caused by the mounting offset.

DETAILED DESCRIPTION (continued)

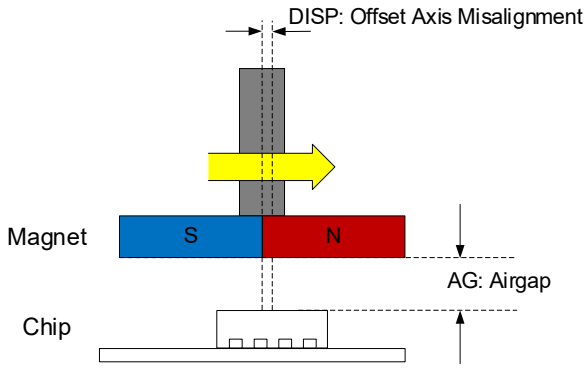


Figure 27. Magnet Installation Diagram

This product uses cylindrical magnets, radial magnetization, with a pair of N/S poles, the parameters are as follows:

Table 7. External Magnetic Field Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Airgap	Airgap	The distance between the magnet and the chip surface			3	mm
Offset	Offset	The offset between the magnet center and the Sensor Element Center Point			0.3	mm
Magnet Diameter	Diameter	1-pole magnet, radial magnetization		10		mm
Magnet Thickness	Thickness			2.5		mm
Working Magnetic	H	Parallel magnetic field between two surfaces of the chip	300			Gauss

Zero-Position Setting

In motor drive control application, it is necessary to align the mechanical zero point of the motor with the encoder's zero-position. After locating and locking the motor's mechanical zero point, user can achieve zero-position alignment by writing the current encoder angle to the zero-position register. The VCE2765 supports zero-position setting through either external pin or zero-position register programming. The STATUS output status is shown in Figure 28.

When using the external pin zero-writing function, configure the SPI to 3-wire mode and set register ZERO_POS_PROG=1. This changes the function of pin4 from MISO to ENZERO, enabling automatic zero-writing control. Holding the ENZERO pin low for 1 second triggers the ASIC to calculate the offset and write it to the zero-position register ZERO_POS[11:0], making the encoder's angle output 0°.

Upon successful zero-writing, the STATUS pin outputs a 5Hz square wave for 1 second before returning to its pre-operation state. During this process, ENZERO must remain low. If zero-writing fails, the STATUS pin maintains the 5Hz square wave output until ENZERO goes high.

DETAILED DESCRIPTION (continued)

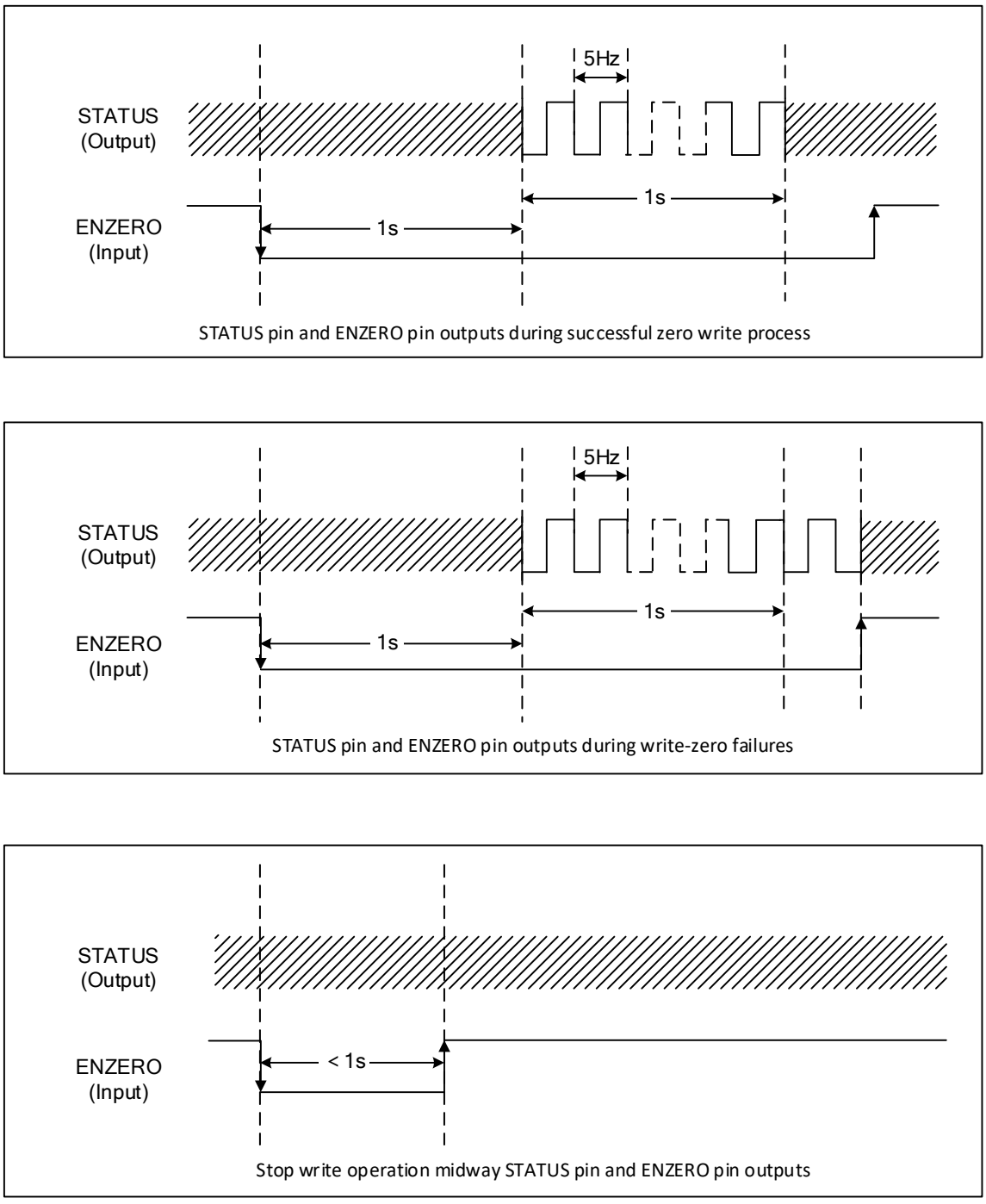


Figure 28. External Pin Enable Write Zero Timing Chart

Digital Filtering

To suppress signal noise for enhanced accuracy, configurable digital filtering offers four selectable strength levels, programmable via register BANDWIDTH[7:0]. Smaller bandwidth provides higher angular resolution but reduces system dynamic performance. Users should make comprehensive considerations based on their specific requirements for both resolution and dynamic response.

REGISTER MAP

ADDR	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT	MTP
0x02	ZERO_POS_PROG	PWM_FREQ[2:0]			PWM_SEL[1:0]		Reserved	PWM_POL	/(1)	√
0x03	WEAK_MAG_LVL[1:0]		IO_MUX[1:0]		Reserved	IO_DS	SPI_3W	DIRECTION	/(1)	√
0x05	Reserved		UVW_RES[5:0]						/(1)	√
0x06	Reserved					HYST[2:0]			/(1)	√
0x07	BANDWIDTH[7:0]								/(1)	√
0x08	ZERO_POS[7:0]								/(1)	√
0x09	Reserved				ZERO_POS[11:8]				/(1)	√
0x0F	ABZ_RSE[7:0]								/(1)	√
0x10	ABZ_INV	Z_WIDTH[2:0]			ABZ_RES[11:8]				/(1)	√
0x11	ABZ_INV_USR	Reserved	CAL_OK	Reserved	LED_DRIV_EN	ABZ_INI_DELAY[2:0]			/(1)	√
0x18	Chip ID[7:0]								65'h	√
0x1C	Reserved							NERR_DEFAULT	/(1)	√
0x42	LOW_VOL_FLAG	OVER_SPEED_FLAG	WMF_FLAG	Reserved	CRC_MTP_ERR_FLAG	LOW_VOL_STA	OVER_SPEED_STA	WMF_STA	/(1)	×
0x43	ANG_RB[17:10]								/(1)	×
0x44	ANG_RB[9:2]								/(1)	×
0x45	ANG_RB[1:0]		WMF	LOW_VOL	CRC[3:0]				/(1)	×
0x5F	REG_KEY[7:0]								00'h	×
0x64	SOFT_RST[7:0]								00'h	×
0x70	CAL_SPI_REQ[7:0]								00'h	×

NOTE: 1. "/" indicates the default value is determined by the **Ordering Number** or specific user requirements. Before use, please verify the configuration according to the OPN. These bits are writable and can be re-configured via the MTP memory if needed.

0x02: User Configure0 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	ZERO_POS_PROG	R/W	External Pin ENZERO Write Zero Control Enable Register 0 = Disable external pin ENZERO control to write zero 1 = Allows external pin ENZERO to control write zeros
D[6:4]	PWM_FREQ[2:0]	R/W	Frequency Configuration of PWM Output Pulses 000 = 121.4Hz, unit pulse width (tu) = 2000ns 001 = 242.8Hz, unit pulse width (tu) = 1000ns 010 = 485.6Hz, unit pulse width (tu) = 500ns 011 = 971.1Hz, unit pulse width (tu) = 250ns 100 = 1942.2Hz, unit pulse width (tu) = 125ns 101 = 3884.4Hz, unit pulse width (tu) = 62.5ns 110 = 7768.8Hz, unit pulse width (tu) = 32ns 111 = 7768.8Hz, unit pulse width (tu) = 32ns
D[3:2]	PWM_SEL[1:0]	R/W	PWM Output Selection 00 = Angle calculation by duty cycle 01 = Angle calculation by pulse count
D[1]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[0]	PWM_POL	R/W	Polarity Configuration of PWM Output Pulses 0 = PWM pulses polarity remains unchanged (default) 1 = PWM pulses polarity reversal

REGISTER MAP (continued)

0x03: User Configure1 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:6]	WEAK_MAG_LVL[1:0]	R/W	Weak Magnetic Alarm Threshold Configuration 00 = 1/8 01 = 1/4 10 = 3/8 11 = 1/2 The ratio of the ADC output signal range to the full scale. When the ratio is less than the set threshold, the system outputs a field weakening alarm.
D[5:4]	IO_MUX[1:0]	R/W	Multiplexed Output Mode Configuration 00 = Output mode 1 (ABZ/UVW/SPI) 01 = Output mode 2 (Differential ABZ/SPI) 10 = Output mode 3 (PWM/UVW/SPI) 11 = Output mode 4 (PWM/ABZ/SSI/SPI)
D[3]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[2]	IO_DS	R/W	I/O Output Drive Capability Configuration 0 = I/O drive capability 2mA 1 = I/O drive capability 4mA
D[1]	SPI_3W	R/W	SPI Operating Mode Configuration 0 = 4-wire SPI 1 = 3-wire SPI
D[0]	DIRECTION	R/W	Configuration for Identifying the Direction of Magnetic Field Rotation 0 = CCW: The sensor is installed beside the magnetic ring (top view perspective): Rotate the magnetic ring counterclockwise, Signal B leads Signal A by 1/4 cycle, Angular position increments (See Figure 5). Rotate the magnetic ring clockwise, Signal B lags Signal A by 1/4 cycle, Angular position decrements (See Figure 6). 1 = CW: The sensor is installed beside the magnetic ring (top view perspective): Rotate the magnetic ring clockwise, Signal B leads Signal A by 1/4 cycle, Angular position increments (See Figure 5). Rotate the magnetic ring counterclockwise, Signal B lags Signal A by 1/4 cycle, Angular position decrements (See Figure 6).

0x05: User Configure2 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:6]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[5:0]	UVW_RES[5:0]	R/W	Resolution of UVW Mode 00 0000 = 1 polarity 00 0001 = 2 polarity 00 0010 = 3 polarity ….. 11 1111 = 64 polarity

0x06: User Configure3 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:3]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[2:0]	HYST[2:0]	R/W	Angle Hysteresis Configuration 000 = 0° 001 = 0.011° 010 = 0.022° ….. 110 = 0.154° 111 = 0.176°

REGISTER MAP (continued)

0x07: User Configure4 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	BANDWIDTH[7:0]	R/W	Filter Bandwidth Configuration 0x9F = BW0 0x8D = BW0 × 2 0x7B = BW0 × 4 0x69 = BW0 × 8

0x08 to 0x09: User Configure5 Register Address

ADDR	BITS	BIT NAME	TYPE	DESCRIPTION
0x09	D[7:4]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
0x09	D[3:0]	ZERO_POS[11:8]	R/W	Zero-Position Configuration, 12-Bit Angle Data, Internal Raw Angle Offset 0000 0000 0000 = 0° 0000 0000 0001 = -0.088° 0000 0000 0010 = -0.176° ..... 1111 1111 1111 = -360°
0x08	D[7:0]	ZERO_POS[7:0]	R/W	

0x0F to 0x10: User Configure6 Register Address

ADDR	BITS	BIT NAME	TYPE	DESCRIPTION
0x10	D[7]	ABZ_INV	R/W	ABZ Polarity Configuration 0 = ABZ signal polarity remains unchanged 1 = ABZ Signal polarity reversed
0x10	D[6:4]	Z_WIDTH[2:0]	R/W	ABZ Mode Z Pulse Width Configuration 000 = 1LSB 001 = 2LSB 010 = 4LSB 011 = 8LSB 100 = 12LSB 101 = 16LSB 110 = 180° 111 = 1LSB
0x10	D[3:0]	ABZ_RES[11:8]	R/W	ABZ Mode Resolution Configuration. PPR=ABZ_RES[11:0]+1 0000 0000 0000 = 1ppr 0000 0000 0001 = 2ppr 0000 0000 0010 = 3ppr ..... 1111 1111 1111 = 4096ppr
0x0F	D[7:0]	ABZ_RES[7:0]		

REGISTER MAP (continued)

0x11: User Configure7 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	ABZ_INV_USR	R/W	Pulse Sequences Configuration for Power-On Output in ABZ Mode. Registers ABZ_INV_USR and ABZ_INI_DELAY must be used together. 0000 = ABZ both output about 7.5ms low level, then enter the normal operating state 0001 = Absolute angle pulse output on power-up, power-up delay 25ms 0011 = Absolute angle pulse output on power-up, power-up delay 50ms 0101 = Absolute angle pulse output on power-up, power-up delay 200ms 0111 = Absolute angle pulse output on power-up, power-up delay 1000ms 1001 = Absolute angle pulse output on power-on, power-up delay 900ms (Z pulse is a specific pulse sequences, see Figure 11)
D[2:0]	ABZ_INI_DELAY[2:0]	R/W	
D[6]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[5]	CAL_OK	R/W	Calibration Success Indicator Bit 0 = Calibration not initiated or calibration failed 1 = Calibration successful
D[4]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[3]	LED_DRIV_EN	R/W	Output Configuration of NERR and STATUS Pins 0 = PWM output 1 = LED driver output The LED driver is a 10mA constant current output, and the pin should be connected to the positive terminal of the LED.

0x18: Chip Configure0 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	Chip ID	R	Device ID (8-bit, factory-programmed)

0x1C: User Configure8 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:1]	Reserved	R/W	This register value is factory-calibrated. For internal system use only. User write access is prohibited, otherwise normal system operation may be affected.
D[0]	NERR_DEFAULT	R/W	NERR Pin State when No System Alarm is Present 0 = NERR Pin output low level state 1 = NERR Pin output high level state

REGISTER MAP (continued)

0x42: Error Flag Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	LOW_VOL_FLAG	R	Low-Voltage Alarm Flag, when the VDD voltage falls below 2.9V, LOW_VOL_FLAG is set to "1". After the alarm condition is resolved, it does not automatically clear to "0" and requires a manual write of "0" or a chip reset.
D[6]	OVER_SPEED_FLAG	R	Magnetic Field Rotation Overshoot Alarm Flag, when the AB output frequency exceeds 7.6MHz, OVER_SPEED_FLAG are set to "1". After the alarm condition is resolved, it does not automatically clear to "0" and requires a manual write of "0" or a chip reset.
D[5]	WMF_FLAG	R	Weak Magnetic Field Alarm Flag, when the magnetic field detected by the device is lower than the set weak magnetic alarm threshold, WMF_FLAG will be set to "1". After the alarm condition is resolved, it does not automatically clear to "0" and requires a manual write of "0" or a chip reset.
D[4]	Reserved	R	For internal system use only.
D[3]	CRC_MTP_ERR_FLAG	R	MTP Calibration Exception Alarm Flag, CRC_MTP_ERR_FLAG is set to "1" in case of device MTP checksum exception.
D[2]	LOW_VOL_STA	R	Low-Voltage Alarm Status, when the VDD voltage falls below 2.9V, LOW_VOL_STA is set to "1". After the alarm condition is resolved, it automatically clears to "0".
D[1]	OVER_SPEED_STA	R	Magnetic Field Rotation Overshoot Alarm Status, when the AB output frequency exceeds 7.6MHz, OVER_SPEED_STA are set to "1". After the alarm condition is resolved, it automatically clears to "0".
D[0]	WMF_STA	R	Weak Magnetic Field Alarm Status, when the magnetic field detected by the device is lower than the set weak magnetic alarm threshold, WMF_STA will be set to "1". After the alarm condition is resolved, it automatically clears to "0".

0x43, 0x44, 0x45: Data Read Back Register Address

ADDR	BITS	BIT NAME	TYPE	DESCRIPTION
0x43	D[7:0]	ANG_RB[17:10]	R	18-Bit Angle Data Effective resolution of 13 bits
0x44	D[7:0]	ANG_RB[9:2]	R	
0x45	D[7:6]	ANG_RB[1:0]	R	
	D[5]	WMF	R	Weak Magnetic Field Alarm Flag, for its function see register 0x42[0]
	D[4]	LOW_VOL	R	Low-Voltage Alarm Flag, for its function see register 0x42[2]
	D[3:0]	CRC[3:0]	R	CRC Checksum Value for 20-Bit Data (18-Bit ANG_RB[17:0] + 2-Bit Flag Bit), CRC polynomial is X^4+X+1, initial value is 0000b, input and output are not inverted.

0x5F: Control1 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	REG_KEY[7:0]	R/W	Register Write Protection Operation 55'h = Disable register write protection and allow write operations to registers 0x00~0x3F AA'h = Enable register write protection to disable write operations to registers 0x00~0x3F Read the value in REG_KEY[7:0] to judge the current register write-protection status, REG_KEY[7:0] = 01'h is allowed to write registers, REG_KEY[7:0] = 00'h is forbidden to write registers.

REGISTER MAP (continued)

0x64: Control2 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	SOFT_RST[7:0]	R/W	Soft Reset Operation 20'h = reset device

0x70: Control3 Register Address

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	CAL_SPI_REQ[7:0]	R/W	Automatic Calibration Command AA'h = Start calibration 55'h = Stop calibration The calibration status is determined by the combination of bit[0] and bit[1] in the current register. When bit[1] = 1 and bit[0] = 1, calibration is in progress. When bit[1] = 0 and bit[0] = 1, the calibration is successful.

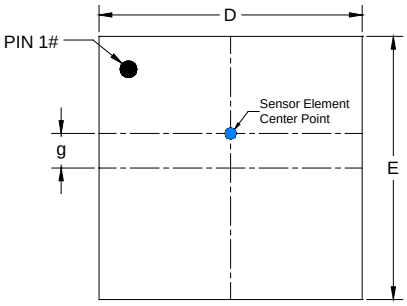
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

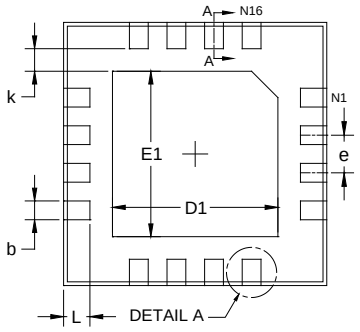
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

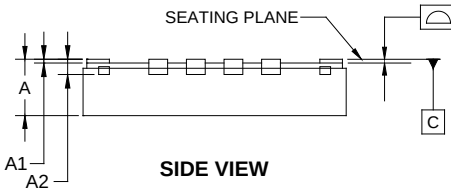
TQFN-3.5×3.5-16BL



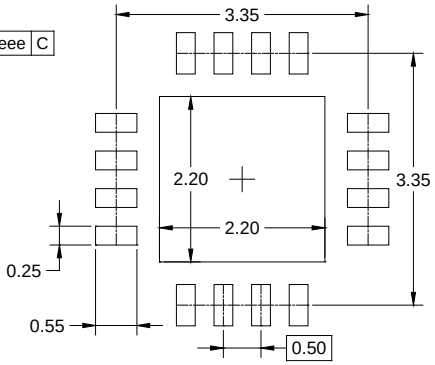
TOP VIEW



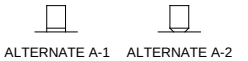
BOTTOM VIEW



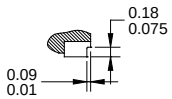
SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



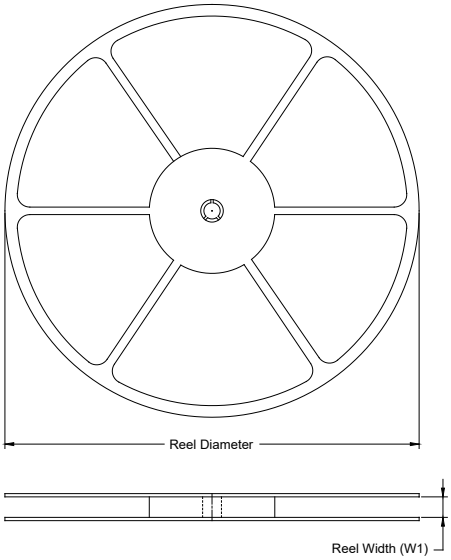
SECTION A-A
TERMINAL CROSS SECTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	3.400	-	3.600
D1	2.100	-	2.300
E	3.400	-	3.600
E1	2.100	-	2.300
e		0.500 BSC	
g	0.455	-	0.465
k		0.300 REF	
L	0.250	-	0.450
eee		0.080	

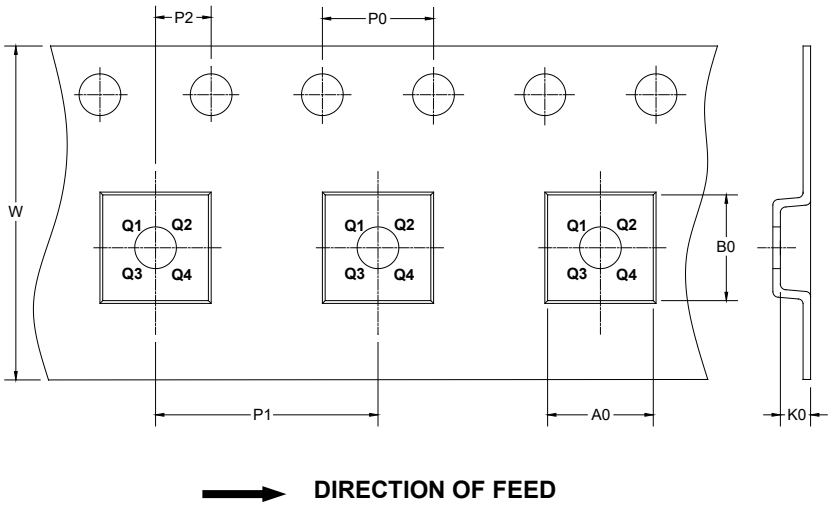
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



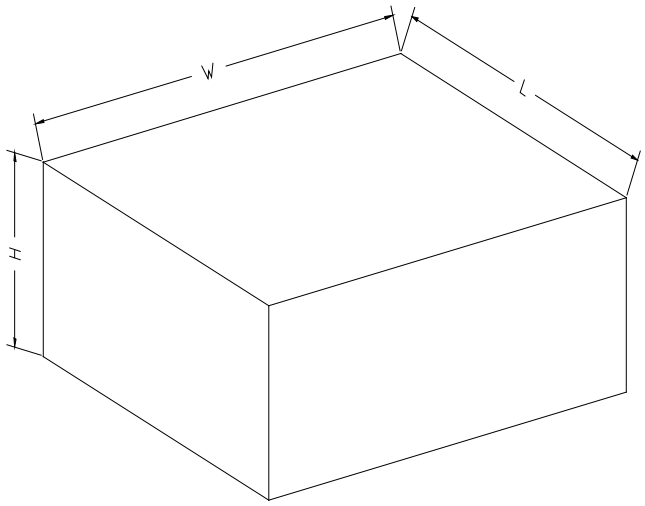
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-16BL	13"	9.5	3.80	3.80	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002