



SGM2037S

500mA, Low Noise, High Accuracy, Very Low Dropout Bias Rail CMOS Voltage Regulator

GENERAL DESCRIPTION

The SGM2037S is a low noise, high accuracy and low dropout voltage linear regulator which is designed using CMOS technology. It provides 500mA output current capability. The operating input voltage range is from 0.8V to 5.5V and bias supply voltage range is from 2.4V to 5.5V. The fixed output voltage range is from 0.9V to 3.3V and adjustable output voltage range is from 0.8V to 3.6V.

Other features include under-voltage lockout, 1.2V logic-controlled shutdown mode, current limit and thermal shutdown protection. The SGM2037S has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2037S is suitable for application which needs low noise, fast transient response and low I_Q consumption, such as battery-powered equipment and smartphones, etc.

The SGM2037S is available in Green SOT-23-5, SOT-23-6 and XTDFN-1.2×1.2-6L packages. It operates over an operating temperature range of -40°C to $+125^{\circ}\text{C}$.

FEATURES

- Input Voltage Range: 0.8V to 5.5V
- Bias Voltage Range: 2.4V to 5.5V
- Enable Pin Accept Voltages Higher than the Supply Voltage and up to 5.5V
- Fixed Output from 0.9V to 3.3V
- Adjustable Output from 0.8V to 3.6V
- 500mA Output Current
- Output Voltage Accuracy: $\pm 0.8\%$ at $+25^{\circ}\text{C}$
- Low Bias Input Current: $38\mu\text{A}$ (TYP)
- Low Dropout Voltage: 140mV (TYP) at 500mA
- Low Noise: $17\mu\text{V}_{\text{RMS}}$ (TYP) at $V_{OUT} = 0.8\text{V}$
- Current Limiting and Thermal Protection
- Excellent Load and Line Transient Responses
- Supports 1.2V Logic Enable Input
- With Output Automatic Discharge
- Stable with Small Case Size Ceramic Capacitors
- -40°C to $+125^{\circ}\text{C}$ Operating Temperature Range
- Available in Green SOT-23-5, SOT-23-6 and XTDFN-1.2×1.2-6L Packages

APPLICATIONS

Portable Equipment
Smartphone
Industrial and Medical Equipment

TYPICAL APPLICATION

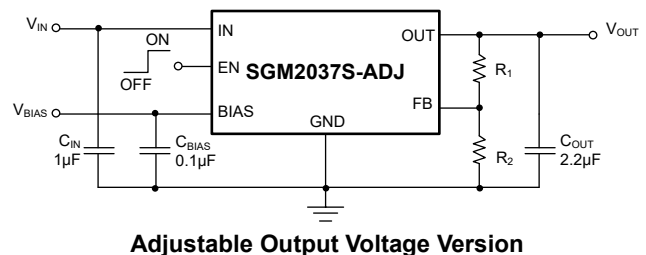
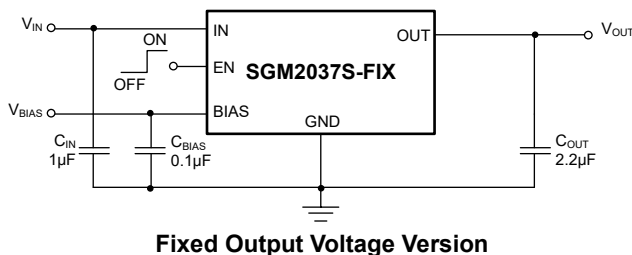


Figure 1. Typical Application Circuits

500mA, Low Noise, High Accuracy, SGM2037S Very Low Dropout Bias Rail CMOS Voltage Regulator

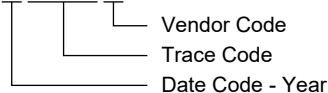
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2037S-1.2	SOT-23-5	-40°C to +125°C	SGM2037S-1.2XN5G/TR	2KY XXXXX	Tape and Reel, 3000
SGM2037S-1.8	SOT-23-5	-40°C to +125°C	SGM2037S-1.8XN5G/TR	2AF XXXXX	Tape and Reel, 3000
SGM2037S-3.3	SOT-23-5	-40°C to +125°C	SGM2037S-3.3XN5G/TR	2KX XXXXX	Tape and Reel, 3000
SGM2037S-ADJ	SOT-23-6	-40°C to +125°C	SGM2037S-ADJXN6G/TR	XXXXX 28U	Tape and Reel, 3000
SGM2037S-0.9	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-0.9XXED6G/TR	0N XX	Tape and Reel, 5000
SGM2037S-1.1	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-1.1XXED6G/TR	0M XX	Tape and Reel, 5000
SGM2037S-1.2	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-1.2XXED6G/TR	0P XX	Tape and Reel, 5000
SGM2037S-1.8	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-1.8XXED6G/TR	0K XX	Tape and Reel, 5000
SGM2037S-3.3	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-3.3XXED6G/TR	0Q XX	Tape and Reel, 5000
SGM2037S-ADJ	XTDFN-1.2×1.2-6L	-40°C to +125°C	SGM2037S-ADJXXED6G/TR	0J XX	Tape and Reel, 5000

MARKING INFORMATION

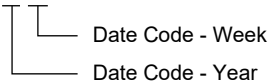
NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX = Date Code.

XXXXX



YY — Serial Number

XX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, BIAS, EN to GND	-0.3V to 6V
OUT, FB to GND	-0.3V to MIN($V_{IN} + 0.3V$, 6V)
Package Thermal Resistance	
SOT-23-5, θ_{JA}	158.6°C/W
SOT-23-5, θ_{JB}	41.3°C/W
SOT-23-5, θ_{JC}	79.3°C/W
SOT-23-6, θ_{JA}	151.4°C/W
SOT-23-6, θ_{JB}	39.9°C/W
SOT-23-6, θ_{JC}	83.6°C/W
XTDFN-1.2×1.2-6L, θ_{JA}	159.4°C/W
XTDFN-1.2×1.2-6L, θ_{JB}	95.4°C/W
XTDFN-1.2×1.2-6L, $\theta_{JC(TOP)}$	99.6°C/W
XTDFN-1.2×1.2-6L, $\theta_{JC(BOT)}$	95.1°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM	±3000V
CDM	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Input Voltage Range, V_{IN}	0.8V to 5.5V
Operating Bias Voltage Range, V_{BIAS}	2.4V to 5.5V
Enable Input Voltage Range	0V to 5.5V
BIAS Effective Capacitance, C_{BIAS}	0.05 μ F (MIN)
Input Effective Capacitance, C_{IN}	0.5 μ F (MIN)
Output Effective Capacitance, C_{OUT}	1 μ F to 100 μ F
Operating Ambient Temperature Range	-40°C to +125°C
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

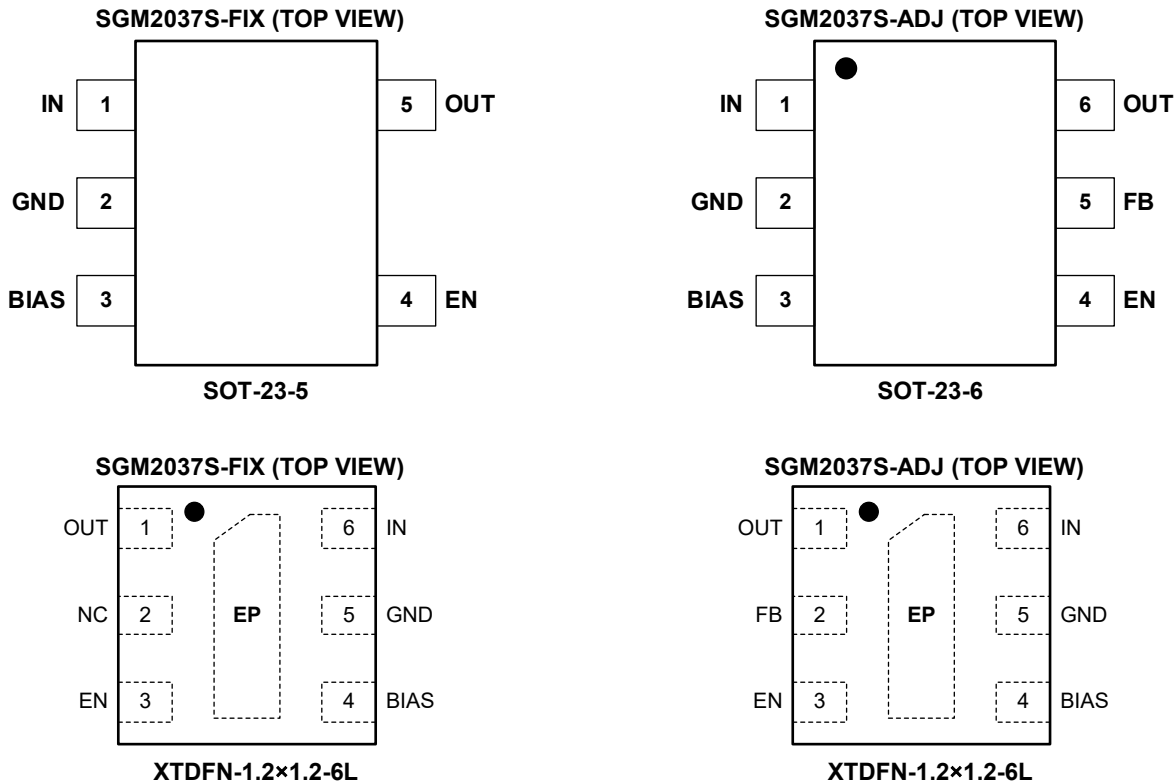
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

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PIN CONFIGURATIONS



PIN DESCRIPTION

PIN			NAME	FUNCTION
SOT-23-5	SOT-23-6	XTDFN-1.2x1.2-6L		
1	1	6	IN	Input Supply Voltage Pin. It is recommended to use a 1μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
2	2	5	GND	Ground.
3	3	4	BIAS	Bias Voltage Supply Pin for Internal Control Circuits. It is recommended to use a 0.1μF or larger ceramic capacitor from BIAS pin to ground and this ceramic capacitor should be placed as close as possible to BIAS pin.
4	4	3	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. The EN pin has an internal pull-down resistance which ensures that the device is turned off when the EN pin is floated.
5	6	1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 100μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
–	5	2	FB	Feedback Voltage Input Pin (adjustable voltage version only). Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
–	–		NC	No Connection (fixed voltage version only).
–	–	Exposed Pad	–	Exposed Pad. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

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FUNCTIONAL BLOCK DIAGRAMS

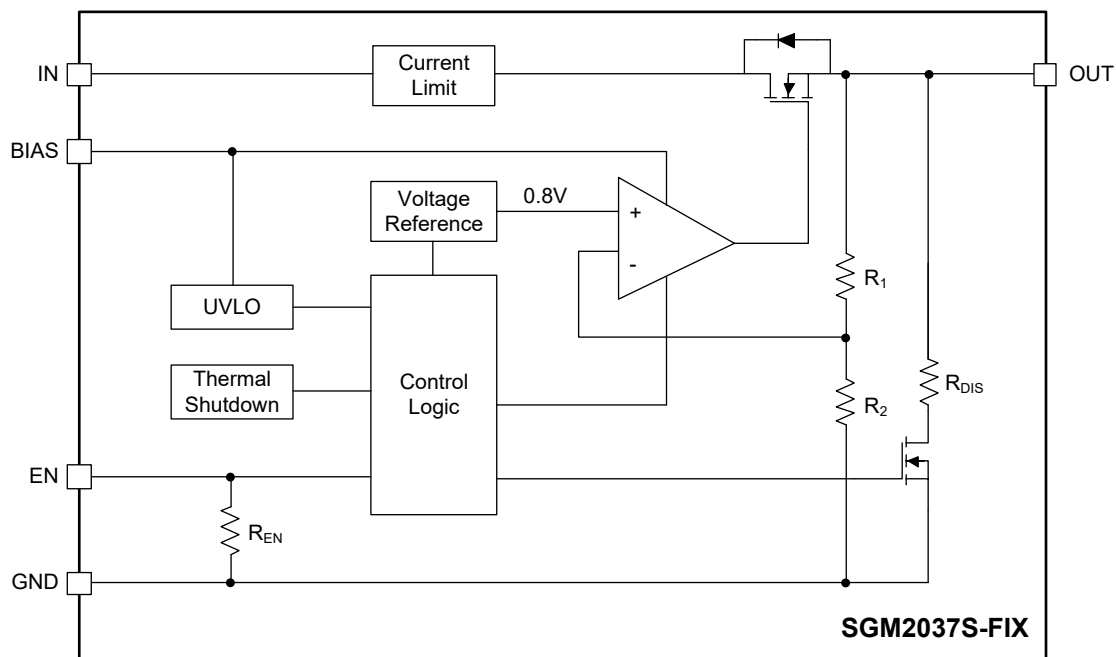


Figure 2. Internal Block Diagram of Fixed Output Voltage

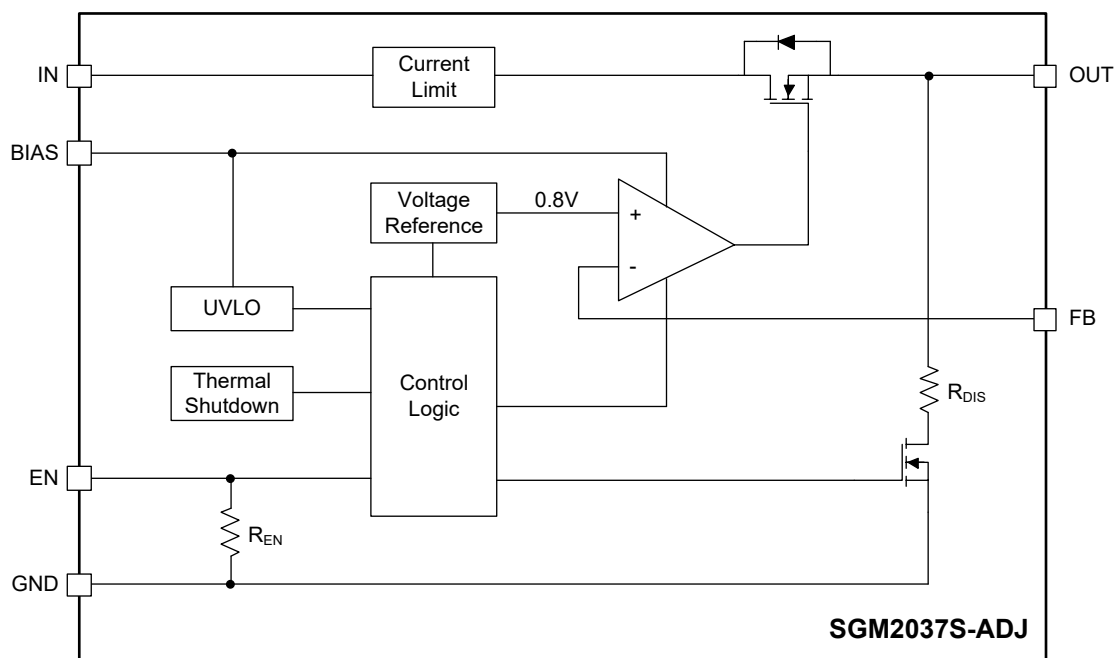


Figure 3. Internal Block Diagram of Adjustable Output Voltage

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ELECTRICAL CHARACTERISTICS

($V_{IN} = V_{OUT(NOM)} + 0.3V$, $V_{BIAS} = 2.4V$ or $(V_{OUT(NOM)} + 1.6V)$ (whichever is greater), $V_{EN} = V_{BIAS}$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{BIAS} = 0.1\mu F$, $C_{OUT} = 2.2\mu F$, $T_J = -40^\circ C$ to $+125^\circ C$, typical values are at $T_J = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Input Voltage Range	V_{IN}		$V_{OUT(NOM)} + V_{DROD_IN}$		5.5	V	
Operating Bias Voltage Range	V_{BIAS}		2.4		5.5	V	
Output Voltage Range	V_{OUT}	SGM2037S-FIX	0.9		3.3	V	
		SGM2037S-ADJ	0.8		3.6		
Under-Voltage Lockout Thresholds	V_{UVLO}	V_{BIAS} rising		2.08	2.35	V	
		Hysteresis		0.42			
Feedback Voltage	V_{FB}	$V_{OUT} = V_{FB}$, $V_{IN} = 1.1V$ to $1.8V$, $V_{BIAS} = 2.4V$ to $5.5V$, $I_{OUT} = 1mA$ to $500mA$	$T_J = +25^\circ C$	0.7936	0.8	0.8064	V
			$T_J = -40^\circ C$ to $+125^\circ C$	0.788		0.812	
FB Pin Input Current	I_{FB}	$V_{FB} = 0.9V$	-50	0.1	50	nA	
Output Voltage Accuracy	V_{OUT}	$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to $(V_{OUT(NOM)} + 1V)$, $V_{BIAS} = 2.4V$ or $(V_{OUT(NOM)} + 1.6V)$ to $5.5V$, $I_{OUT} = 1mA$ to $500mA$	$T_J = +25^\circ C$	-0.8		0.8	%
			$T_J = -40^\circ C$ to $+125^\circ C$	-1.5		+1.5	
V_{IN} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	$V_{IN} = (V_{OUT(NOM)} + 0.3V)$ to $5.5V$		0.001	0.05	%/V	
V_{BIAS} Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{BIAS} \times V_{OUT}}$	$V_{BIAS} = 2.4V$ or $(V_{OUT(NOM)} + 1.6V)$ to $5.5V$		0.003	0.05	%/V	
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT} \times V_{OUT}}$	$I_{OUT} = 1mA$ to $500mA$		0.05	0.35	%/A	
V_{IN} Dropout Voltage ⁽¹⁾	V_{DROD_IN}	$I_{OUT} = 150mA$		40	70	mV	
		$I_{OUT} = 500mA$		140	230		
V_{BIAS} Dropout Voltage ^(1,2)	V_{DROD_BIAS}	$I_{OUT} = 500mA$		1.12	1.4	V	
Output Current Limit	I_{LIMIT}	$V_{OUT} = 90\% \times V_{OUT(NOM)}$	505	690		mA	
Short-Circuit Current Limit	I_{SHORT}	$V_{OUT} = 0V$		390		mA	
BIAS Pin Operating Current	I_{BIAS}	$V_{BIAS} = 5.5V$		38	58	μA	
IN Pin Disable Current	I_{DIS_IN}	$V_{EN} = 0V$		0.01	2	μA	
BIAS Pin Disable Current	I_{DIS_BIAS}	$V_{EN} = 0V$		0.25	1	μA	
EN Pin Threshold Voltage	V_{IH}	EN input voltage high	0.71		5.5	V	
	V_{IL}	EN input voltage low	0		0.46	V	
EN Pin Pull-Down Resistance	R_{EN}		240	500	800	k Ω	
Output Discharge Resistance	R_{DIS}	$V_{BIAS} = 2.4V$, $V_{EN} = 0V$, $V_{OUT} = 0.5V$	50	110	190	Ω	
Turn-On Time	t_{ON}	From assertion of V_{EN} to $V_{OUT} = 90\% \times V_{OUT(NOM)}$		110		μs	
V_{IN} Power Supply Rejection Ratio	PSRR	$V_{IN} = 1.5V$, $V_{BIAS} = 2.4V$, $V_{OUT(NOM)} = 1V$, $I_{OUT} = 150mA$, $f = 1kHz$	V_{IN} to V_{OUT}	77		dB	
V_{BIAS} Power Supply Rejection Ratio			V_{BIAS} to V_{OUT}	85			
Output Voltage Noise	e_n	$V_{IN} = 1.5V$, $V_{BIAS} = 2.4V$, $V_{OUT(NOM)} = 0.8V$, $I_{OUT} = 1mA$, $f = 10Hz$ to $100kHz$		17		μV_{RMS}	
		$V_{IN} = 3.9V$, $V_{BIAS} = 5.5V$, $V_{OUT(NOM)} = 3.6V$, $I_{OUT} = 1mA$, $f = 10Hz$ to $100kHz$		72			
Thermal Shutdown Temperature	T_{SHDN}	T_J rising		168		$^\circ C$	
Thermal Shutdown Hysteresis	ΔT_{SHDN}	Hysteresis		30		$^\circ C$	

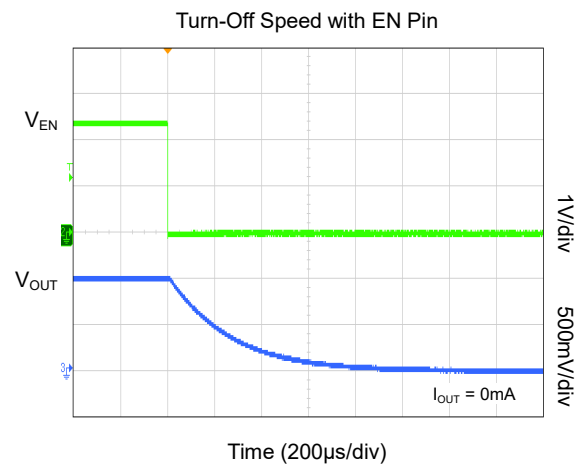
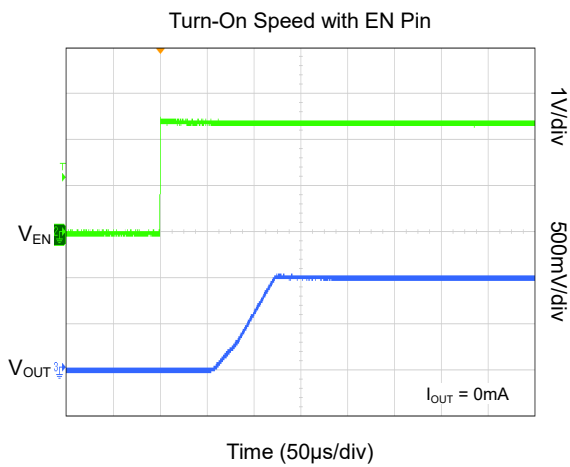
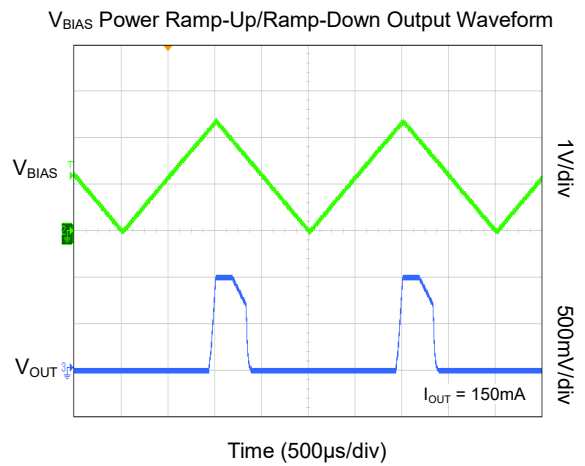
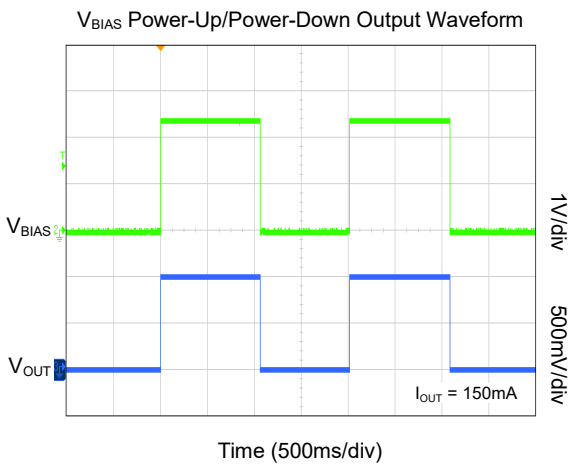
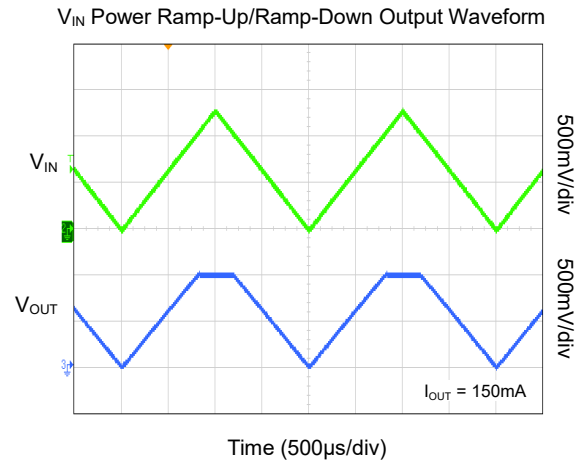
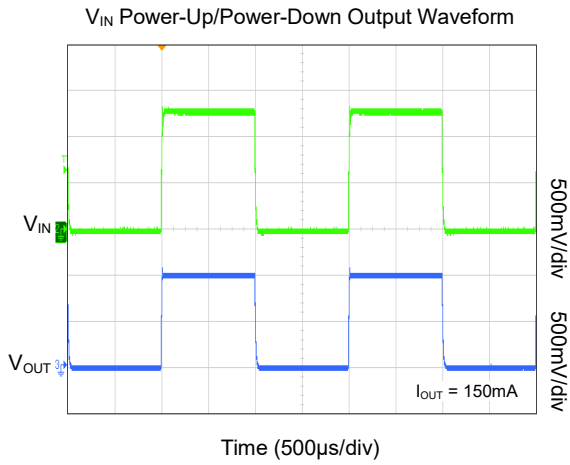
NOTES:

- V_{IN} dropout voltage is defined as the difference between V_{IN} and V_{OUT} when V_{OUT} falls to $95\% \times V_{OUT(NOM)}$.
- V_{BIAS} dropout voltage refers to $V_{BIAS} - V_{OUT}$ when the IN and BIAS pins are connected together and V_{OUT} falls to $95\% \times V_{OUT(NOM)}$.

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TYPICAL PERFORMANCE CHARACTERISTICS

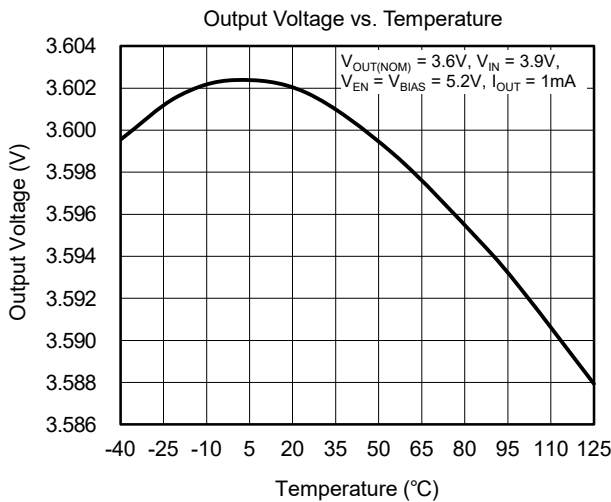
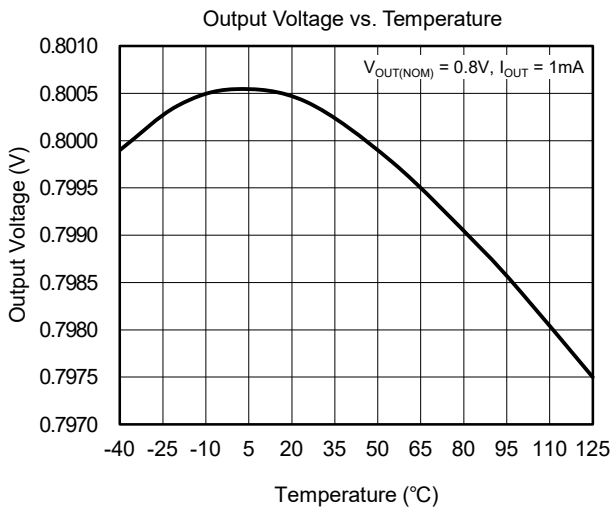
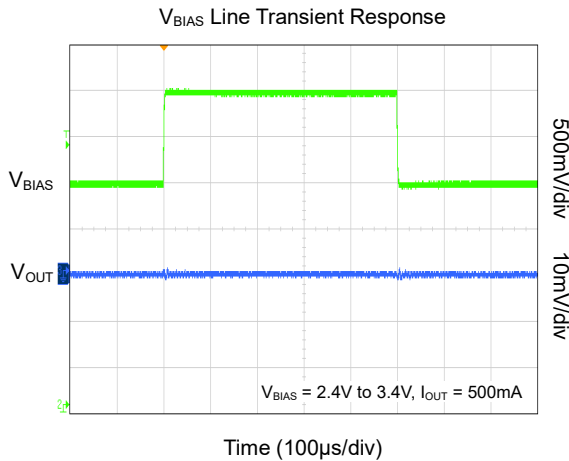
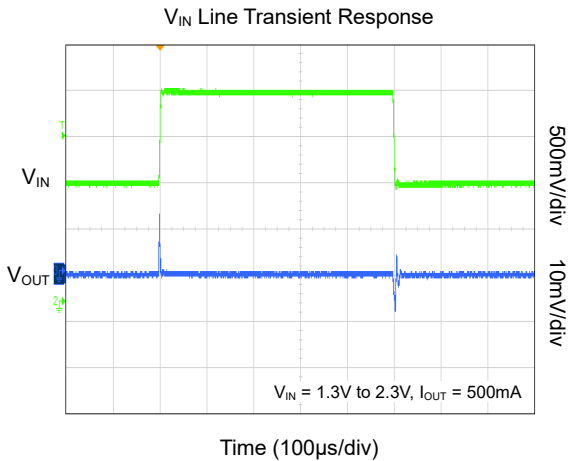
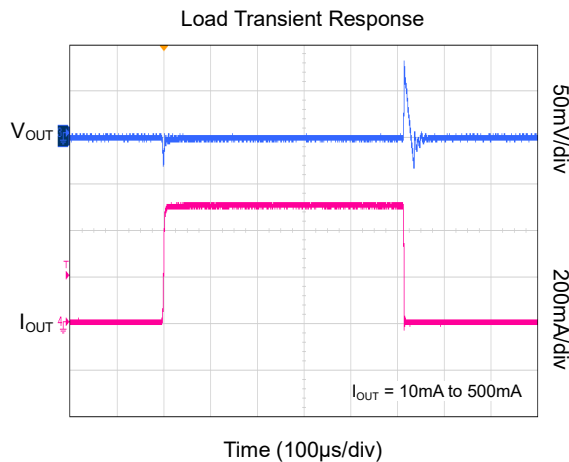
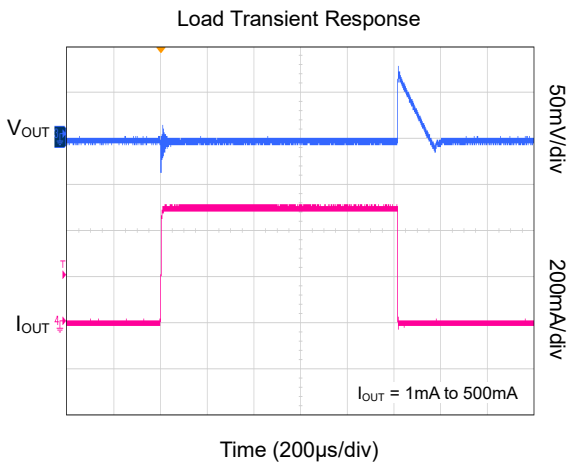
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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

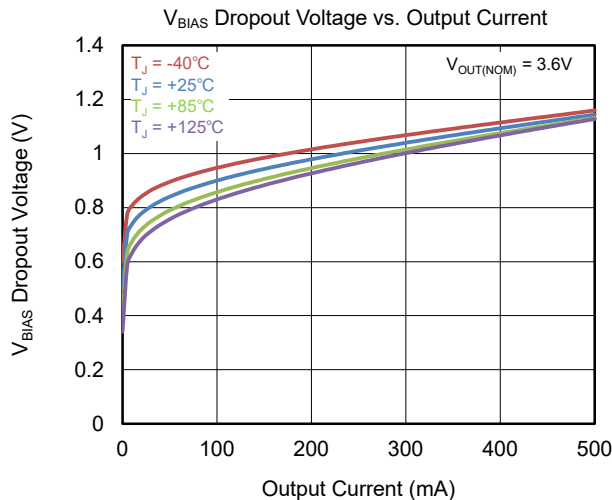
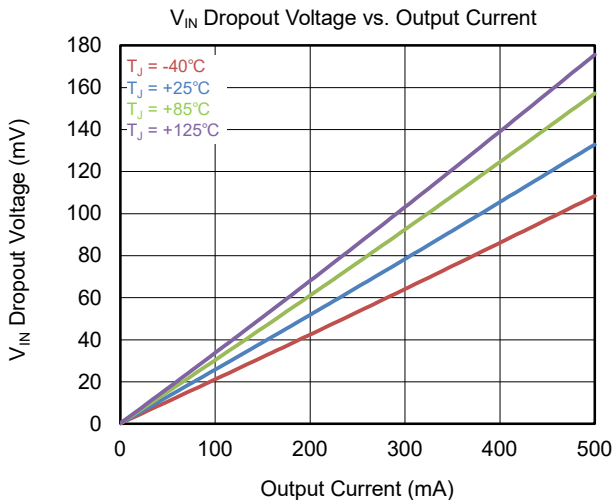
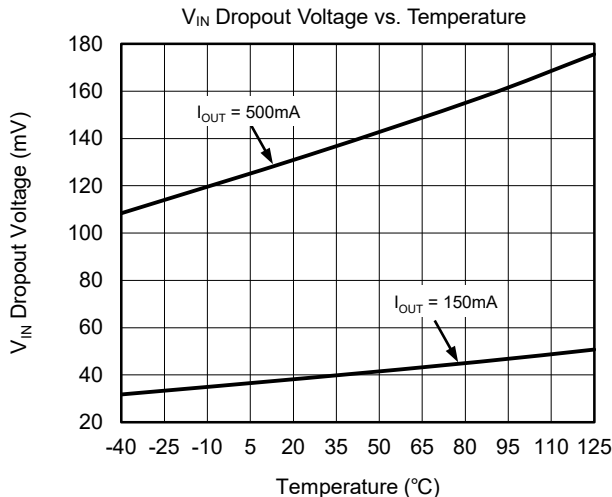
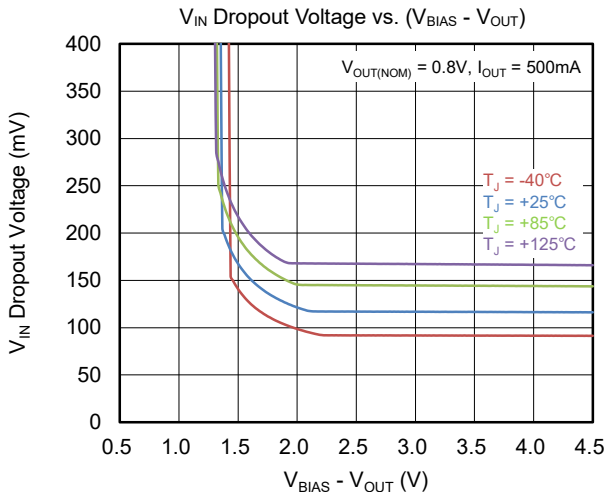
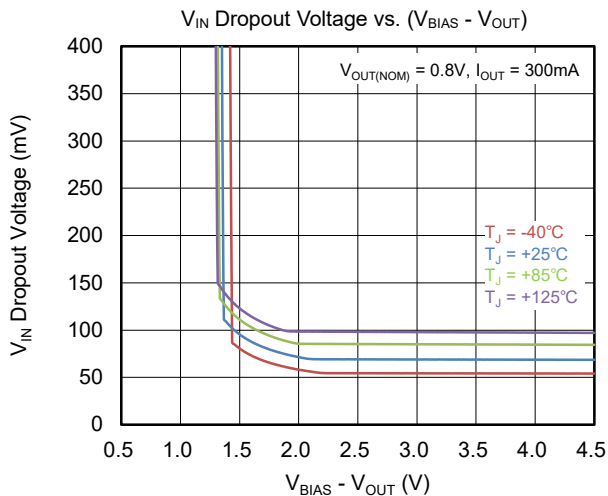
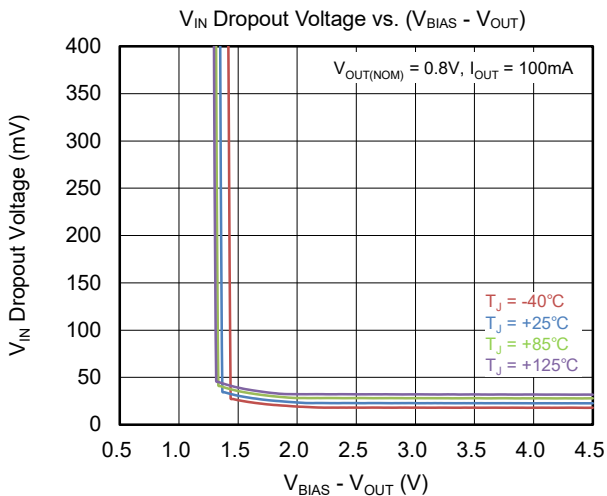
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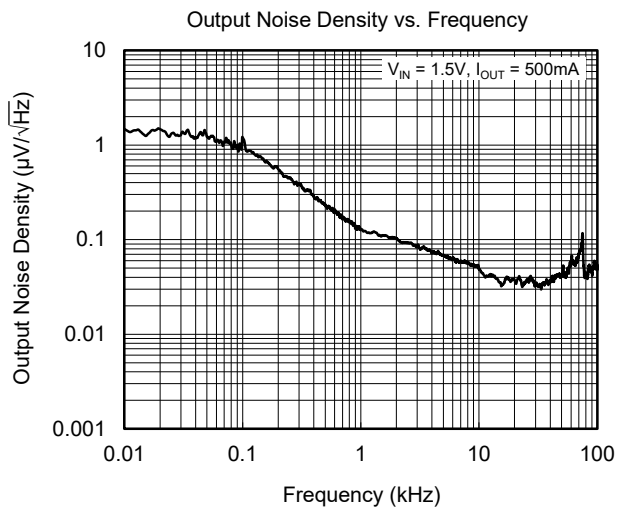
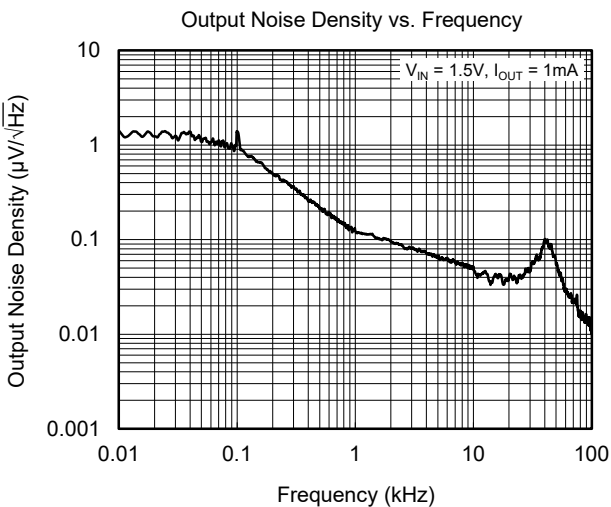
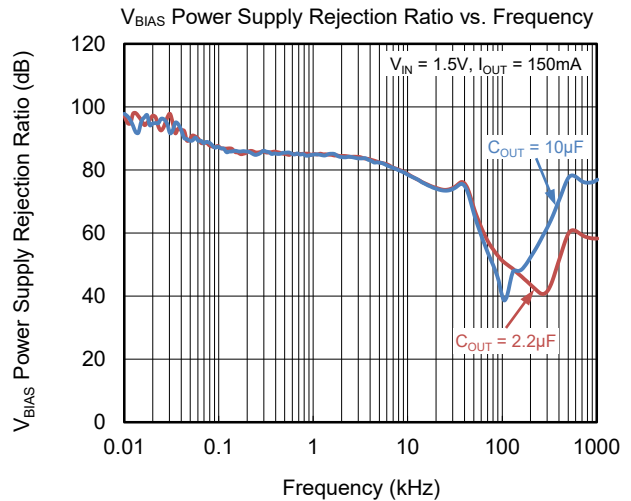
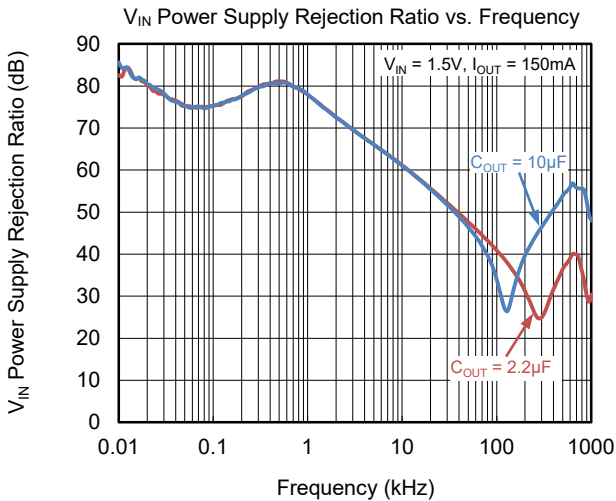
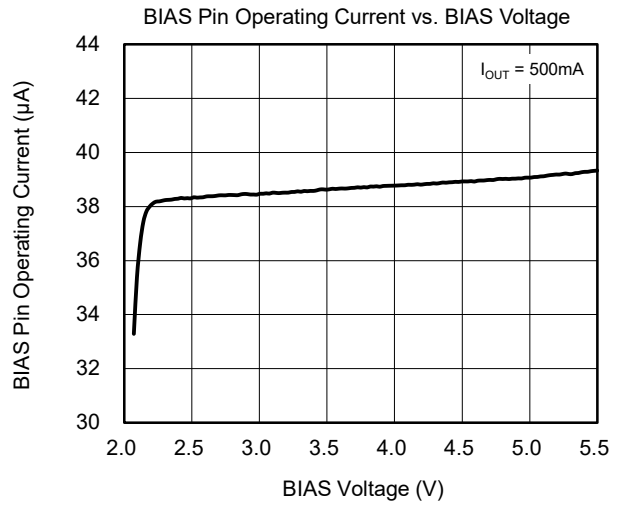
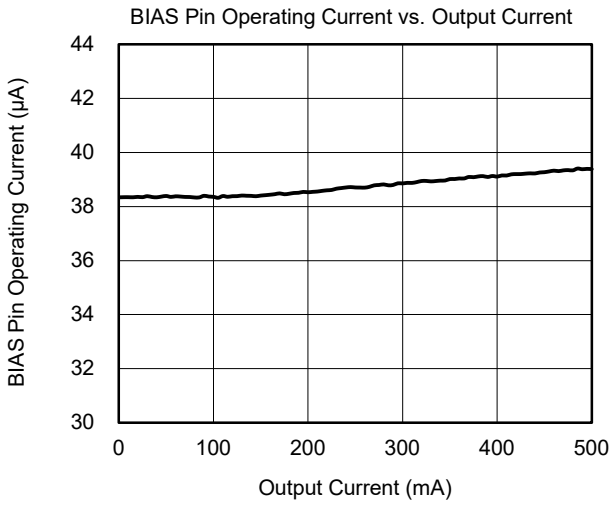
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 1.3V$, $V_{EN} = V_{BIAS} = 2.4V$, $V_{OUT(NOM)} = 1.0V$, $C_{IN} = 1\mu F$, $C_{BIAS} = 0.1\mu F$, $C_{OUT} = 2.2\mu F$, $T_J = +25^\circ C$, unless otherwise noted.



APPLICATION INFORMATION

The SGM2037S is a low noise and very low dropout voltage linear regulator, it consumes only 38 μ A (TYP) quiescent current and provides 500mA output current. The SGM2037S provides the protection function for output overload and overheating.

The SGM2037S is suitable for application which has noise sensitive circuit such as battery-powered equipment and smartphones.

Input Capacitor Selection (C_{IN} and C_{BIAS})

The input decoupling capacitor should be placed as close as possible to the IN pin and BIAS pin to ensure the device stability. $C_{IN} = 1\mu$ F and $C_{BIAS} = 0.1\mu$ F or larger X7R or X5R ceramic capacitors are selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings. For C_{OUT} with larger capacitance, it is recommended to choose the larger capacitance C_{IN} .

Output Capacitor Selection (C_{OUT})

One or more output capacitors are required to maintain the stability of the LDO, and the output capacitors should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R and X5R ceramic capacitors as output capacitors. Ceramic capacitors have low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitors is affected by temperature, DC bias and package size.

For example, Figure 4 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10 μ F \pm 10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of

the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

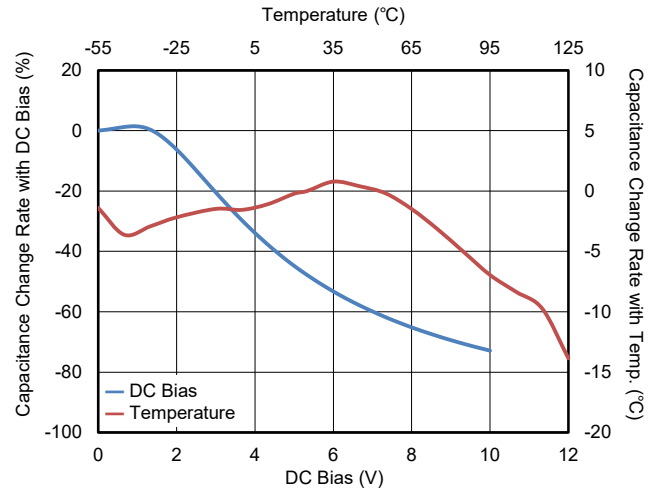


Figure 4. Capacitance vs. DC Bias and Temperature Characteristics

The SGM2037S requires a minimum effective capacitance of 1 μ F for C_{OUT} to ensure stability. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Dropout Voltage

The SGM2037S specifies two dropout voltages because there are two power supplies V_{IN} and V_{BIAS} and one V_{OUT} regulator output. V_{IN} dropout voltage is defined as the difference between V_{IN} and V_{OUT} when V_{OUT} falls 5% below $V_{OUT(NOM)}$.

When V_{OUT} begins to decrease and V_{BIAS} is high enough, the V_{IN} dropout voltage equals to $V_{IN} - V_{OUT}$. V_{BIAS} dropout voltage refers to $V_{BIAS} - V_{OUT}$ when the IN and BIAS pins are connected together and V_{OUT} begins to decrease.

SGM2037S 500mA, Low Noise, High Accuracy, Very Low Dropout Bias Rail CMOS Voltage Regulator

APPLICATION INFORMATION (continued)

Adjustable Regulator

The output voltage of the SGM2037S-ADJ can be adjusted from 0.8V to 3.6V. The FB pin will be connected to two external resistors as shown in Figure 5. The output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2} \right) \quad (1)$$

where:

V_{OUT} is output voltage and V_{FB} is the internal voltage reference, $V_{FB} = 0.8V$. Choose $R_2 = 40k\Omega$ to maintain a $20\mu A$ minimum load.

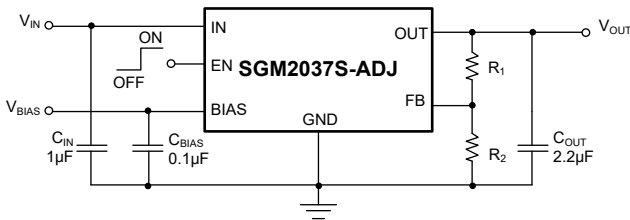


Figure 5. Adjustable Output Voltage Application

Enable Operation

The SGM2037S uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.46V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through an 110Ω (TYP) resistor.

When the EN pin voltage is higher than 0.71V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

Reverse Current Protection

The NMOS power transistor has an inherent body diode. This body diode will be forward biased when $V_{OUT} > V_{IN}$. When $V_{OUT} > V_{IN}$, the reverse current flowing from the OUT pin to the IN pin will damage the SGM2037S. If reverse current protection function is needed in application, the circuit in Figure 6 is good solution to provide reverse current protection.

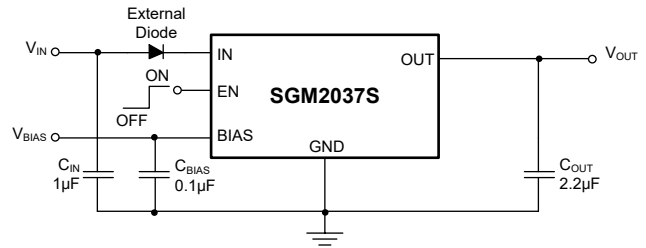


Figure 6. Reverse Protection Reference Design

Negatively Biased Output

When the output voltage is negative, the chip may not start up due to parasitic effects. Ensure that the output is greater than $-0.3V$ under all conditions. If negatively biased output is excessive and expected in the application, a Schottky diode can be added between the OUT pin and GND pin.

Output Current-Limit Protection

When overload events happen, the output current is internally limited to 690mA (TYP). When the OUT pin is shorted to ground, the output current is internally limited to 390mA (TYP).

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2037S will be in shutdown state and it will remain in this state until the die temperature decreases to $+138^{\circ}C$.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2037S can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2037S is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN/BIAS pin and OUT pin separately.

SGM2037S 500mA, Low Noise, High Accuracy, Very Low Dropout Bias Rail CMOS Voltage Regulator

REVISION HISTORY

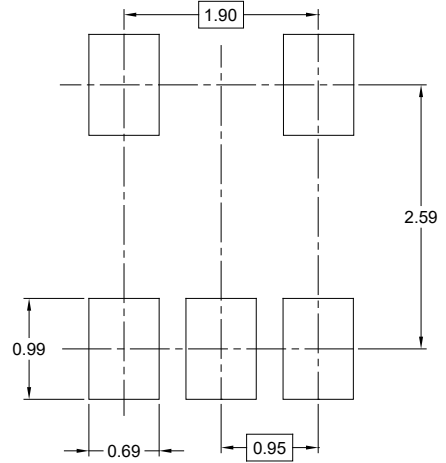
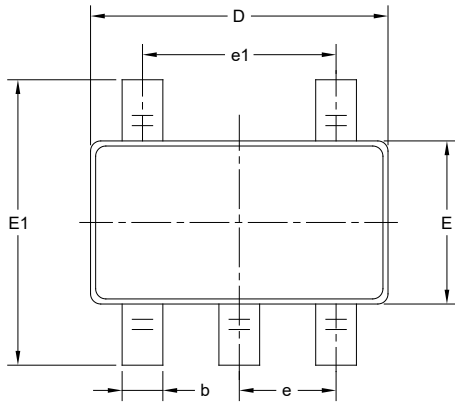
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2026 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	6

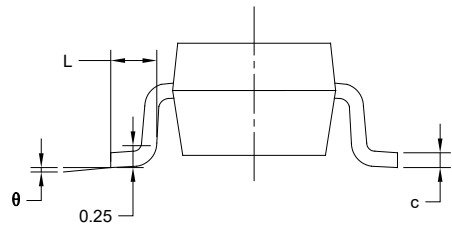
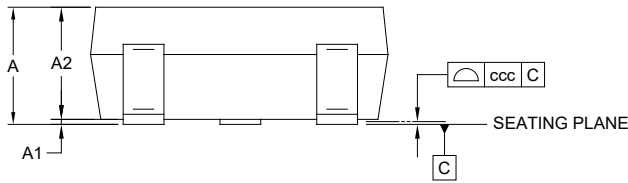
Changes from Original to REV.A (FEBRUARY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

SOT-23-5



RECOMMENDED LAND PATTERN (Unit: mm)



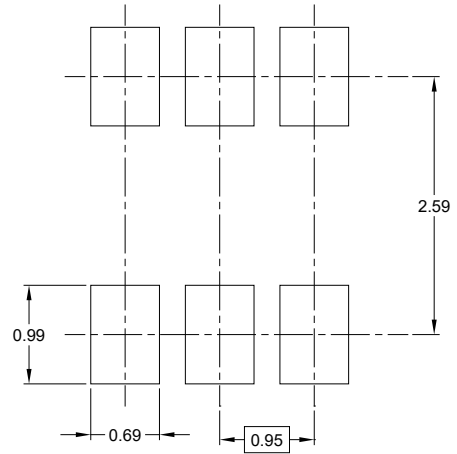
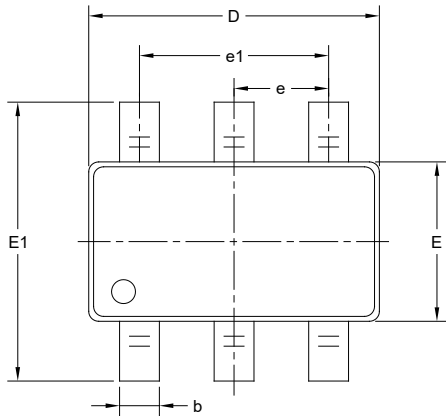
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:

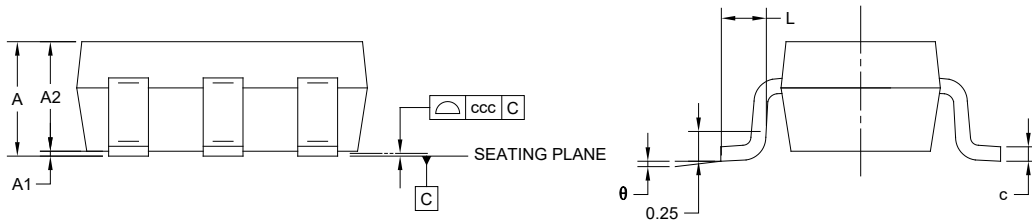
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

SOT-23-6



RECOMMENDED LAND PATTERN (Unit: mm)



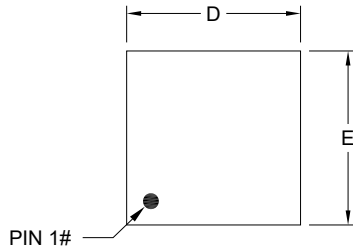
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:

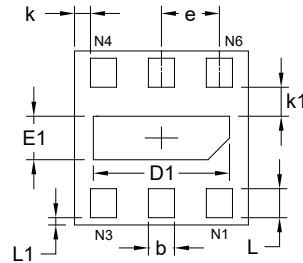
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

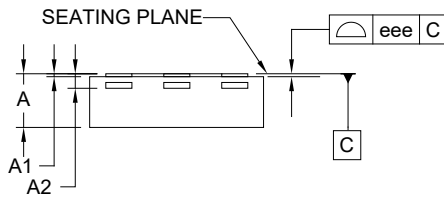
XTDFN-1.2×1.2-6L



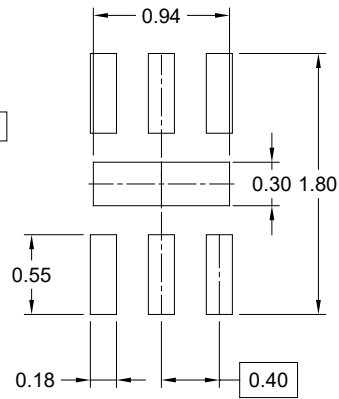
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

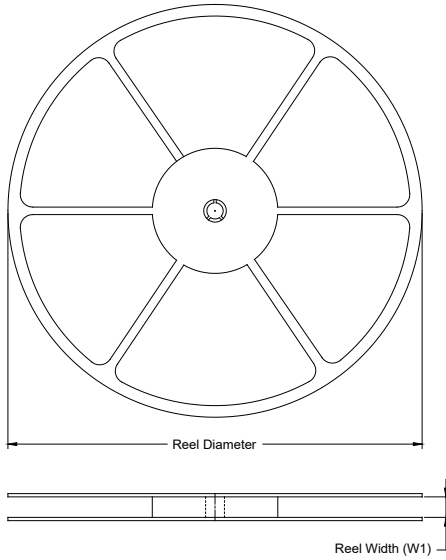
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.340	0.370	0.400
A1	0.000	-	0.050
A2	0.100 REF		
b	0.130	0.180	0.230
D	1.100	1.200	1.300
E	1.100	1.200	1.300
D1	0.890	0.940	0.990
E1	0.250	0.300	0.350
e	0.300	0.400	0.500
k	0.110 REF		
k1	0.150	0.200	0.250
L	0.150	0.200	0.250
L1	0.000	0.050	0.100
eee	0.080		

NOTE: This drawing is subject to change without notice.

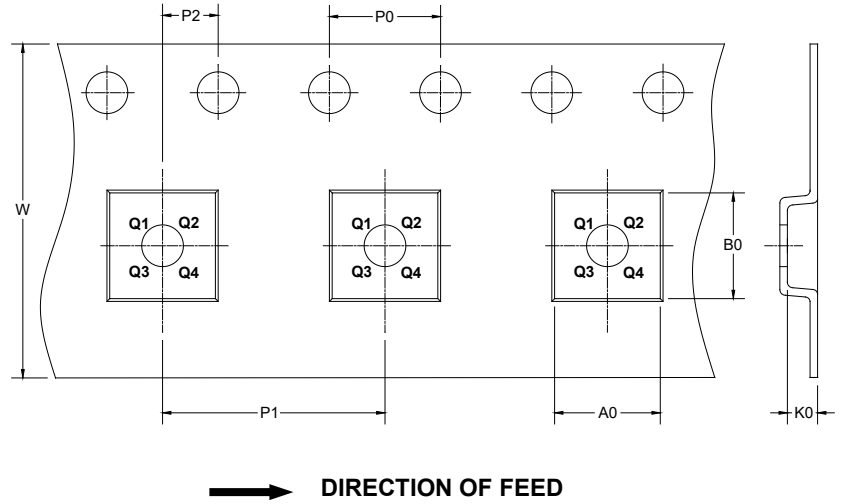
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

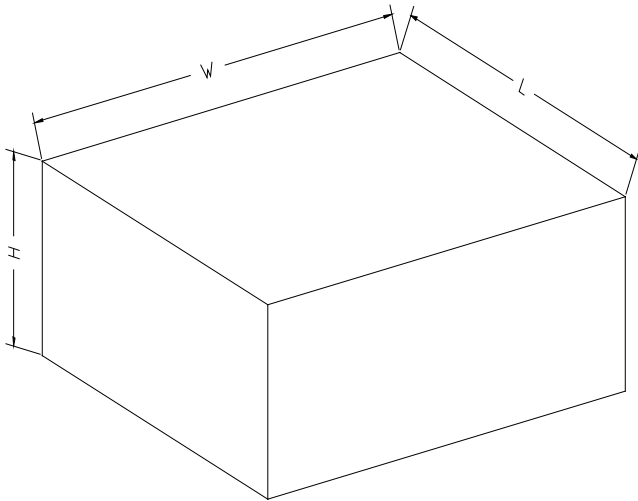
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3
XTDFN-1.2×1.2-6L	7"	9.5	1.37	1.37	0.55	4.0	4.0	2.0	8.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

D00002