SGM37461Q
Automotive 6-CH Display LED Backlight Driver with 200mA per Channel

GENERAL DESCRIPTION

The SGM37461Q is a 6-channel high-efficiency LED driver with configurable Boost controller for automotive infotainment, HUD and other automotive LED backlight applications.

The SGM37461Q applies an external PMOS gate control for load disconnection. The device integrates 6 high-precision current sinks to control the LED brightness with 200mA (MAX) each channel. The Boost controller dynamically adjusts the output voltage based on the minimum headroom voltage of the working LED current sinks, which provides improved efficiency. The Boost switching frequency can be configured among a wide range or controlled by external synchronization signal. And the spread spectrum function helps to reduce the peak EMI emissions.

The SGM37461Q adjusts the LED current flexibly through the I^2C interface or PWM input. The SGM37461Q supports the phase shift function for less Boost output ripple. And it also supports the hybrid PWM dimming and analog current dimming, which has a better performance at EMI and total efficiency.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM37461Q is available in Green TSSOP-38 (Exposed Pad) and TQFN-5×5-32KL packages.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Input Voltage Range: 3V to 48V (Conditional)**

Boost Controller:

- **Up to 48V Output Voltage Boost or SEPIC DC/DC Controller**
- **100kHz (TYP) to 2.222MHz (TYP) Switching Frequency**
- **Low EMI Frequency Spread Spectrum**
- **External Frequency Synchronization**
- **Output Voltage Automatically Discharged when EN is Disabled**

LED Sinks:

- **6 High-Precision Current Sinks**
- **200mA (MAX) per Channel**
- **3.5% (MAX) Current Matching**
- **8 Configurable LED Strings Configuration**
- **Programmable Dimming Options:**
  - **Direct PWM Dimming**
  - **Phase Shift PWM Dimming**
  - **Current Dimming**
  - **Hybrid Dimming**
  - **Up to 16-Bit LED Dimming Resolution with I^2C or PWM Input**
- **32000:1 Dim Ratio in PWM Dim at f_{PWM} ≤ 152Hz**
- **Extensive Fault Diagnostics**
- **Available in Green TSSOP-38 (Exposed Pad) and TQFN-5×5-32KL Packages**

APPLICATIONS

Automotive Applications
Automotive Infotainment Backlights
Automotive Instrument Clusters
Heads-Up Displays (HUD)
Smart Mirrors

SIMPLIFIED SCHEMATIC

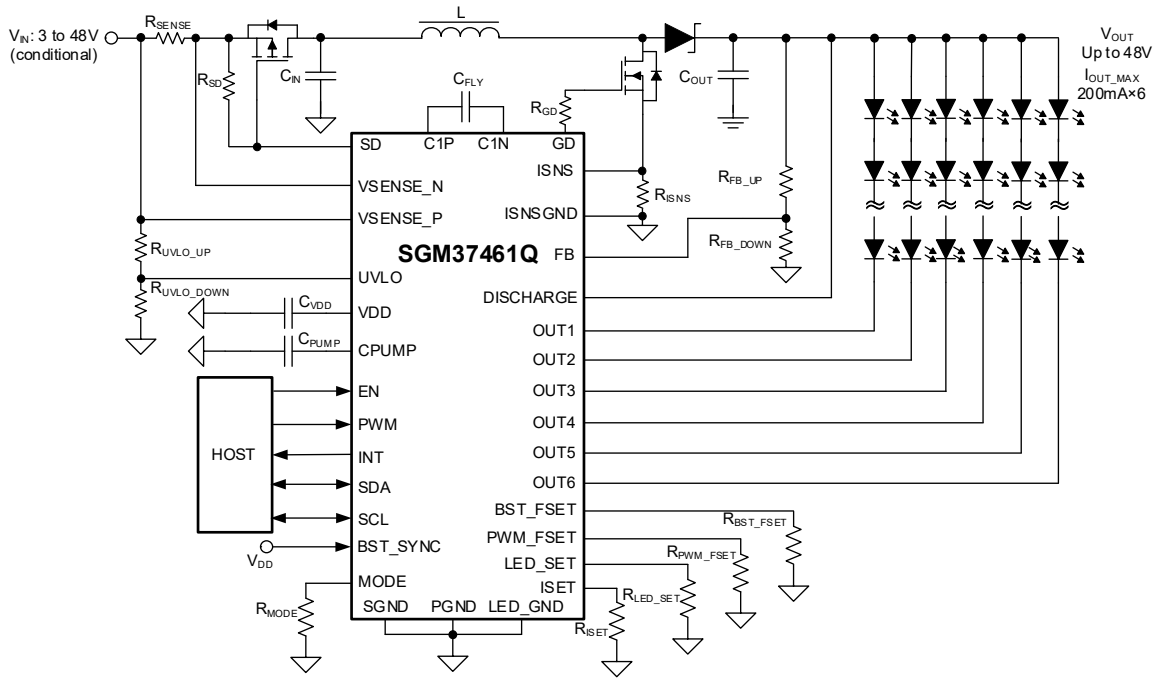


Figure 1. Simplified Schematic

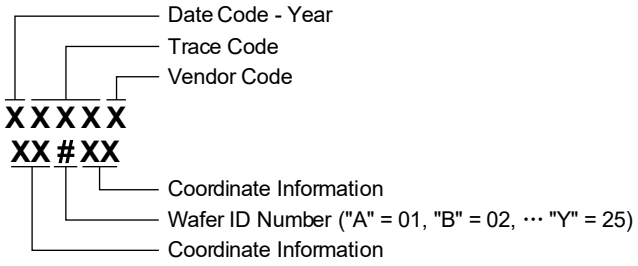
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37461Q	TSSOP-38 (Exposed Pad)	-40℃ to +125℃	SGM37461QPTS38G/TR	2F3PTS38 XXXXX XX#XX	Tape and Reel, 4000
	TQFN-5×5-32KL	-40℃ to +125℃	SGM37461QTXP32G/TR	2F4TXP32 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TSSOP-38 (Exposed Pad)/TQFN-5×5-32KL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage on Pins (1)

VSENSE_N, SD, UVLO ..... -0.3V to V_{SENSE_P} + 0.3V

VSENSE_P, FB, DISCHARGE, OUT1 to OUT6 ..... -0.3V to 52V

C1N, C1P, VDD, EN, ISNS, ISNSGND, INT, MODE, PWM_FSET, BST_FSET, LED_SET, ISET, GD and CPUMP ..... -0.3V to 6V

PWM, BST_SYNC, SDA, SCL ..... -0.3V to V_{DD} + 0.3V

Continuous Power Dissipation ..... Internally Limited

Package Thermal Resistance

TSSOP-38 (Exposed Pad), θ_{JA} ..... 33.3℃/W

TSSOP-38 (Exposed Pad), θ_{JB} ..... 14℃/W

TSSOP-38 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 22℃/W

TSSOP-38 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 9.2℃/W

TQFN-5×5-32KL, θ_{JA} ..... 28℃/W

TQFN-5×5-32KL, θ_{JB} ..... 7.9℃/W

TQFN-5×5-32KL, $\theta_{JC\ (TOP)}$ ..... 18.6℃/W

TQFN-5×5-32KL, $\theta_{JC\ (BOT)}$ ..... 1.6℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (2) (3)

HBM ..... ±3000V

CDM ..... ±1000V

RECOMMENDED OPERATING CONDITIONS

Voltage on Pins (1)

VSENSE_P, VSENSE_N, SD, UVLO ..... 3V to 48V

FB, DISCHARGE, OUT1 to OUT6 ..... 0V to 48V

ISNS, ISNSGND ..... 0V to 5.5V

EN, PWM, INT, SDA, SCL, BST_SYNC ..... 0V to 5.5V

VDD ..... 3V to 5.5V

C1N, C1P, CPUMP, GD ..... 0V to 5.5V

Operating Ambient Temperature Range ..... -40℃ to +125℃

NOTES:

1. All voltages are referenced to the potential at the GND pins.

2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

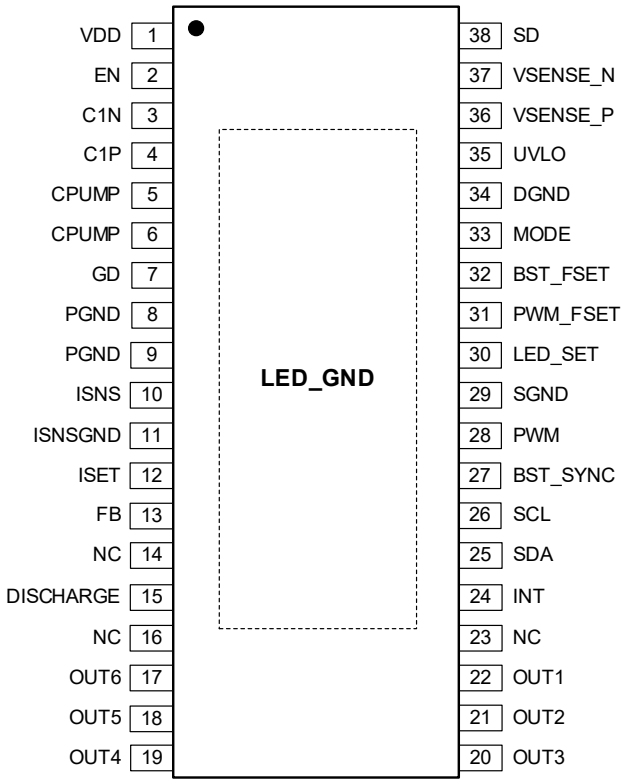
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

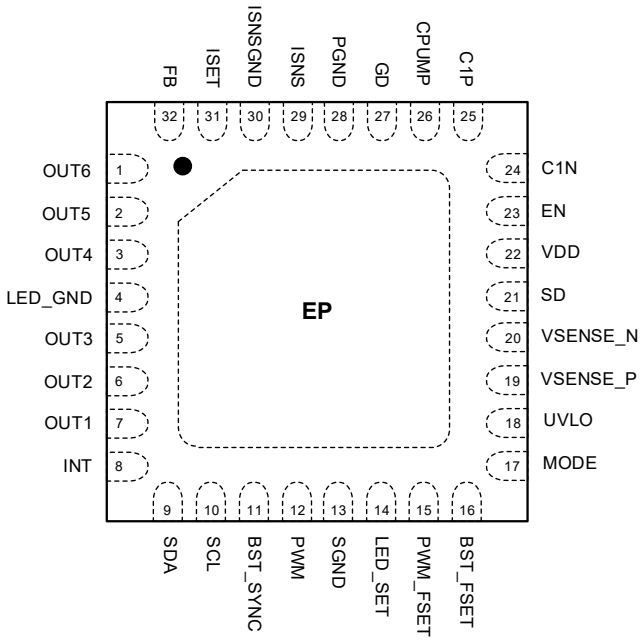
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-38 (Exposed Pad)

(TOP VIEW)



TQFN-5×5-32KL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TSSOP-38 (Exposed Pad)	TQFN-5×5-32KL			
1	22	VDD	P	Power Supply Input for Internal Analog and Digital Circuit. A 10μF bypass capacitor is recommended.
2	23	EN	DI	Enable Input. IC is enabled when EN is high and disabled when EN is low. Internal 1MΩ pull-down.
3	24	C1N	AI	Negative Input for Charge Pump Flying Capacitor. If charge pump is not used, leave it floating.
4	25	C1P	AI	Positive Input for Charge Pump Flying Capacitor. If charge pump is not used, leave it floating.
5, 6	26	CPUMP	P	Charge Pump Output Pin. Please connect Pin 6 to Pin 5 of TSSOP-38 (Exposed Pad) package. Don't power other loads from this power rail. A 4.7μF bypass capacitor is recommended. If charge pump is not used, connect it to VDD.
7	27	GD	AO	Gate Driver Pin for Boost External Power FET.
8, 9	28	PGND	G	Power Ground.
10,	29	ISNS	AI	Boost Current Sense Pin. Connect a sense resistor from this pin to ISNSGND. A 15mΩ to 50mΩ sense resistor is recommended.
11	30	ISNSGND	G	Boost Current Sense Resistor GND. A Kelvin connection is recommended between this pin and the ISNS pin.
12	31	ISET	AI	Full Scale LED Sink Current Configuration Pin. Connect an external resistor between this pin and ground for configuration.
13	32	FB	AI	Boost Output Feedback Pin. Configure Boost output voltage adjustable range through a resistor divider between this pin and Boost output.
14	—	NC	—	No Connect. Do not connect to this pin.
15	—	DISCHARGE	P	Boost Output Voltage Discharge Pin. Connect it to Boost output for discharge function.
16	—	NC	—	No Connect. Do not connect to this pin.
17 - 22	1 – 3, 5 - 7	OUT6 - OUT1	P	LED Current Sink Regulation Input. If not used, tie it to ground.
—	4	LED_GND	G	LED Ground Connection.
23	—	NC	—	No Connect. Do not connect to this pin.
24	8	INT	DO	Device Fault Interrupt Pin. Open-drain output.
25	9	SDA	DI/DO	I^2C Interface Data Input Pin. Connect SDA to the logic high rail via a pull-up resistor (typically 10kΩ). A small capacitor (e.g. 100pF) to AGND is recommended at direct PWM mode. The I^2C communication block is automatically reset if a STOP condition is not received within 500ms during a single transaction.
26	10	SCL	DI	I^2C Interface Clock Input Pin. Connect SCL to the logic high rail via a pull-up resistor (typically 10kΩ). A small capacitor (e.g. 100pF) to AGND is recommended at direct PWM mode.
27	11	BST_SYNC	DI	External Boost Frequency Synchronization Pin. If synchronization is not used, tie it to the ground. Or tie it to VDD for spread spectrum function.
28	12	PWM	DI	PWM Signal Input Pin for Brightness Control. If not used, tie it to ground.
29	13	SGND	G	Signal Ground Pin.
30	14	LED_SET	AI	LED String Configuration Pin. Connect an external resistor between this pin and ground for configuration.
31	15	PWM_FSET	AI	LED Dimming Frequency Configuration Pin. Connect an external resistor between this pin and ground for configuration.
32	16	BST_FSET	AI	Boost Switching Frequency Configuration Pin. Connect an external resistor between this pin and ground for configuration.
33	17	MODE	AI	Dimming Mode Configuration Pin. Connect an external resistor between this pin and ground for configuration.
34	—	DGND	G	Digital Ground Pin.
35	18	UVLO	AI	Input Voltage Sense Pin for Input UVLO Threshold. Configure UVLO threshold through a resistor divider between this pin and input. If input UVLO detection is not used, connect UVLO to VSENSE_P pin.
36	19	VSENSE_P	P	Input Voltage Sense Pin for OVP and Positive Input Current Sense Pin. If input current sense is used, connect a sense resistor (20mΩ for 11A) between this pin and VSENSE_N pin. If not used, tie it to VSENSE_N pin.
37	20	VSENSE_N	P	Negative Input Current Sense Pin. If not used, tie it to VSENSE_P pin.
38	21	SD	AO	Gate Connection Pin for External Load Disconnection PMOS. If not used, leave it floating.
—	—	EP	—	Exposed Pad. LED ground connection.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground, A = Analog, D = Digital.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = 3.3V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
Shutdown Mode Current, VDD Pin	I_Q	EN = L		0.1	1.5	μA
Active Mode Current, VDD Pin (1)		f_{SW} = 303kHz, PWM = H, C_{GD_LOAD} = 1nF, charge pump disabled, V_{DD} = V_{CPUMP} = 5V		13	21	mA
		f_{SW} = 2200kHz, PWM = H, C_{GD_LOAD} = 1nF, charge pump disabled, V_{DD} = V_{CPUMP} = 5V		31	46	
		f_{SW} = 303kHz, PWM = H, C_{GD_LOAD} = 1nF, charge pump enabled		16	26	
		f_{SW} = 2200kHz, PWM = H, C_{GD_LOAD} = 1nF, charge pump enabled		50	76	
CPUMP and LDO						
Voltage Accuracy	V_{CPUMP}	V_{DD} = 3.3V, I_{LOAD} = 0 to 20mA, initial accuracy	4.5	4.9	5.3	V
CP Switching Frequency	f_{CP}		370	420	460	kHz
VCPUMP UVLO Threshold	V_{CPUMP_UVLO}	V_{CPUMP} falling edge	3.9	4.1	4.3	V
		V_{CPUMP} rising edge	4.1	4.3	4.5	
VCPUMP UVLO Hysteresis	V_{CPUMP_HYS}		0.1	0.2		V
Charge Pump Start-up Time	T_{START_UP}	C_{CPUMP} = 10μF		1000	2000	μs
Protection						
VDD UVLO Threshold	VDD_{UVLO_F}	V_{DD} falling	2.63	2.75	2.87	V
	VDD_{UVLO_R}	V_{DD} rising			3.0	
VDD UVLO Hysteresis	VDD_{UVLO_H}			0.1		V
UVLO Pin Threshold	VIN_{UVLO_TH}	V_{UVLO} falling	0.74	0.775	0.815	V
UVLO Pin Bias Current	I_{UVLO}	V_{UVLO} = V_{UVLO_TH} + 50mV		-4		μA
OVP Threshold	VIN_{OVP_TH}	VSENSE_P rising	40.1	42.3	44.7	V
OVP Hysteresis	VIN_{OVP_HYS}			1.7		V
Input OCP Threshold	VIN_{OCP_TH}	R_{SENSE} = 20mΩ	197	220	253	mV
Thermal Shutdown Threshold (1)	T_{SD}	Temperature rising	150	165	180	℃
Thermal Shutdown Hysteresis (1)	T_{SD_HYS}			20		
SD Leakage Current	I_{SD_LKG}	V_{SD} = 48V		0.1		μA
SD Pull-Down Current	I_{SD}	R_{SD} = 20kΩ	255	330	405	μA
FB Pin - Boost OVP Low Threshold	V_{FB_OVPL}			1.4		V
FB Pin - Boost OVP High Threshold	V_{FB_OVPH}			1.74		V
FB Pin - Boost OCP Threshold	V_{FB_UVP}			0.87		V
Discharge Pin - Boost OVP High Threshold	V_{BST_OVPH}		45.7	48.7	51.9	V
PWM Input						
PWM Leakage Current	$I_{PWM_LEAKAGE}$	V_{PWM} = 5V		1		μA
PWM Input Frequency	f_{PWM_IN}		100		20000	Hz
PWM Input Minimum On-Time	$t_{PWM_MIN_ON}$	Direct PWM mode			200	ns
		Phase shift PWM mode, hybrid mode, current Dimming mode		200	220	
PWM Input Resolution	PWM_IN_{RES}	f_{PWM_IN} = 100Hz		16		bit
		f_{PWM_IN} = 20kHz		10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = 3.3V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Current Sink and LED PWM						
Leakage Current on OUTx	I_{LKG}	OUTx = V_{OUT} = 45V, EN = L		0.1	0.5	μA
ISET Voltage	V_{ISET}		1.17	1.21	1.25	V
Maximum LED Sink Current	I_{MAX}	OUTx		200		mA
ISET Pin Under-Voltage Lockout	V_{ISET_UVLO}		0.95	1	1.05	V
ISET Resistor Range	R_{ISET}	I_{OUT} = 30mA to 200mA	15.6		104	kΩ
LED Current Limit when ISET Pin Short-to-GND	I_{LED_LIMIT}			280		mA
LED Sink Current Accuracy	I_{ACC}	R_{ISET} = 15.6kΩ, I_{OUT} = 200mA, PWM = 100%	-4		4	%
LED Sink Current Matching	I_{MATCH}	R_{ISET} = 15.6kΩ, I_{OUT} = 200mA, PWM = 100%		0	3.5	%
LED Dimming Frequency	f_{DIM}	R_{PWM_FSET} = 3.92kΩ	136	152	168	Hz
		R_{PWM_FSET} = 4.75kΩ	274	305	336	
		R_{PWM_FSET} = 5.76kΩ	549	610	671	
		R_{PWM_FSET} = 7.87kΩ	1098	1221	1344	
		R_{PWM_FSET} = 11kΩ	2196	2441	2686	
		R_{PWM_FSET} = 17.8kΩ	4394	4883	5372	
		R_{PWM_FSET} = 42.2kΩ	8789	9766	10743	
		R_{PWM_FSET} = 124kΩ	17577	19531	21485	
Dimming Ratio	DIM	f_{PWM_OUT} = 152Hz		32000:1		
		f_{PWM_OUT} = 4.88kHz		1000:1		
LED Sink Headroom	$V_{HEADROOM}$			0.7		V
LED Sink Normal Threshold	V_{NORMAL_THD}			1.5		V
LED Internal Short Threshold	V_{LED_SHORT}			5.4		V
LED Short-to-Ground Threshold	V_{SHORT_GND}			0.24		V
LED Output Minimum Pulse	t_{PWM_OUT}			200		ns
Boost Controller						
Switching Frequency	f_{SW}	R_{BST_FSET} = 7.87kΩ	90	100	110	kHz
		R_{BST_FSET} = 4.75kΩ	180	200	220	
		R_{BST_FSET} = 5.76kΩ	272	303	334	
		R_{BST_FSET} = 3.92kΩ	360	400	440	
		R_{BST_FSET} = 11kΩ	450	500	550	
		R_{BST_FSET} = 17.8kΩ	1636	1818	2000	
		R_{BST_FSET} = 42.2kΩ	1800	2000	2200	
		R_{BST_FSET} = 124kΩ	1999	2222	2445	
External FET Current Limit	V_{ISNS}	V_{ISNS} threshold, R_{SENSE} = 15mΩ to 50mΩ	180	200	220	mV
IBSTFB Maximum Current	I_{IBSTFB_MAX}	V_{DD} = 3.3V	36.7	38.7	40.7	μA
R_{DSON} of High-side FET to Gate Driver	R_{DSON_H}	V_{GD}/(R_{DSON} + total resistance to gate input of SW FET) must not be higher than 2.5A		0.8		Ω
R_{DSON} of Low-side FET to Gate Driver	R_{DSON_L}	V_{GD}/(R_{DSON} + total resistance to gate input of SW FET) must not be higher than 2.5A		0.52		Ω
Start-up Time	$t_{START-UP}$	Delay from beginning of Boost soft-start to when LED drivers can begin		50		ms
Minimum Switch On-Time	t_{ON}			150		ns
Minimum Switch Off-Time	t_{OFF}			150		ns

NOTE: 1.Guaranteed by design, not production tested.

LOGIC INTERFACE CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = 5V, V_{EN} = 3.3V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input EN						
EN Logic Low Threshold	VEN_{IL}				0.4	V
EN Logic High Threshold	VEN_{IH}		1.2			V
EN Pin Internal Pull-Down Resistance	R_{ENPD}			1		MΩ
Logic Input SDA, SCL, BST_SYNC and PWM						
Logic Low Threshold	V_{IL}	V_{DD} = 3.3V and 5V			0.4	V
Logic High Threshold	V_{IH}	V_{DD} = 3.3V and 5V	1.2			V
Logic Output SDA, INT						
Output Low Level	V_{OL}	I = 3mA		0.2	0.4	V
Output Leakage Current	I_{LKG_OUT}	V = 3.3V			0.5	μA

TIMING REQUIREMENTS for I²C Interface

(V_{IN} = 12V, V_{DD} = 5V, V_{EN} = 3.3V, T_A = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency	f_{SCLK}				400	kHz
Hold Time (Repeated) START Condition	t_1		0.6			μs
Clock Low Time	t_2		1.3			μs
Clock High Time	t_3		600			ns
Set-up Time for a Repeated START Condition	t_4		600			ns
Data Hold Time	t_5		50			ns
Data Setup Time	t_6					ns
Rise Time of SDA and SCL	t_7				300	ns
Fall Time of SDA and SCL	t_8				300	ns
Set-up Time for STOP Condition	t_9		600			ns
Bus Free Time between a STOP and a START Condition	t_{10}		1.3			μs

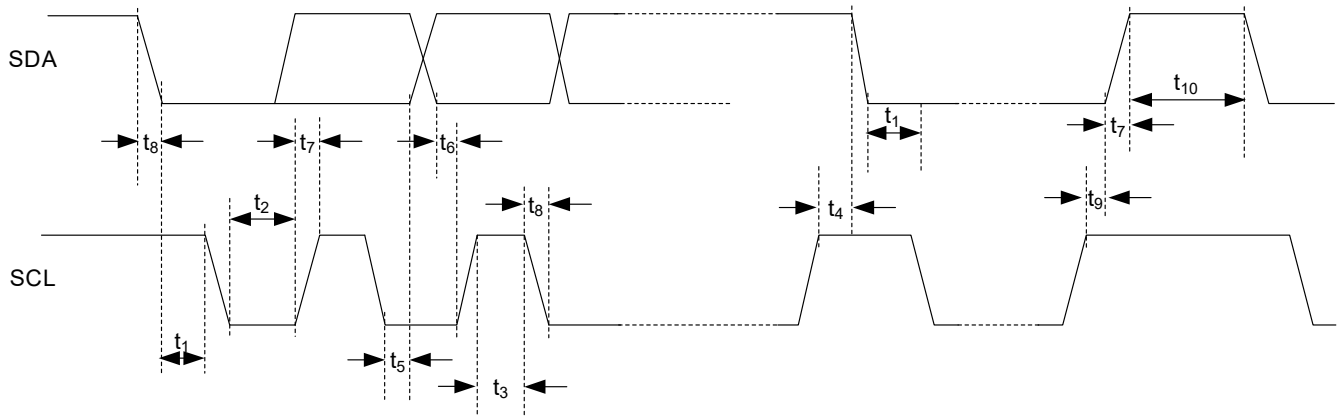
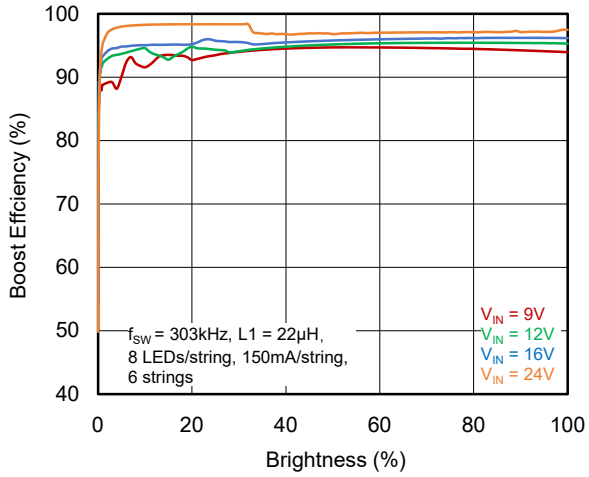


Figure 2. I²C Timing Diagram

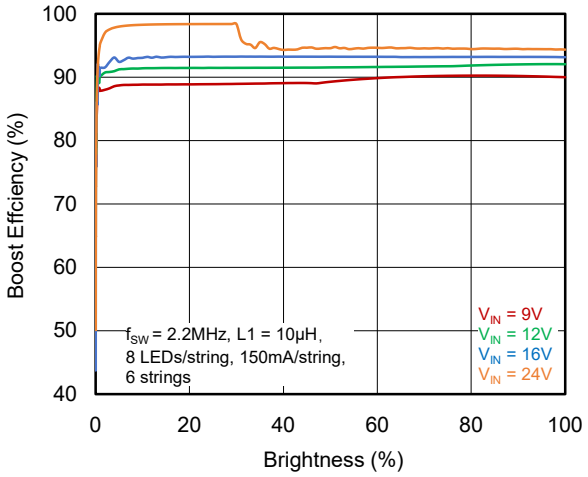
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, C_{IN} = C_{OUT} = 2 × 10μF ceramic and 2 × 33μF electrolytic, V_{DD} = 3.3V, charge pump enabled, unless otherwise noted.

Boost Efficiency



Boost Efficiency



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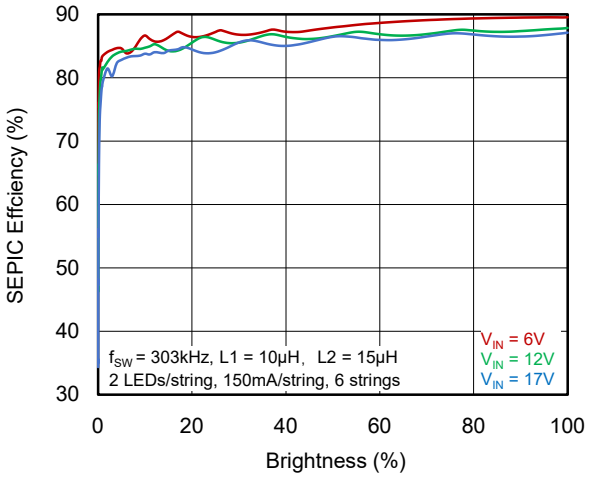
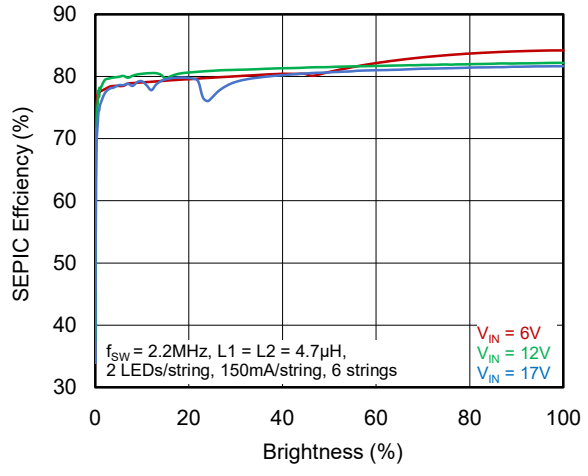
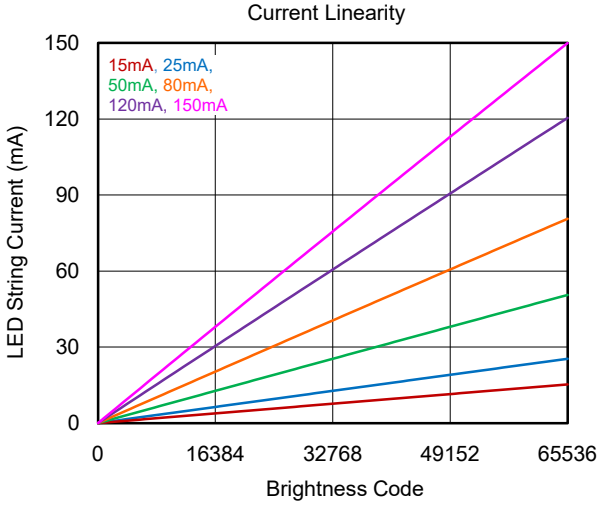


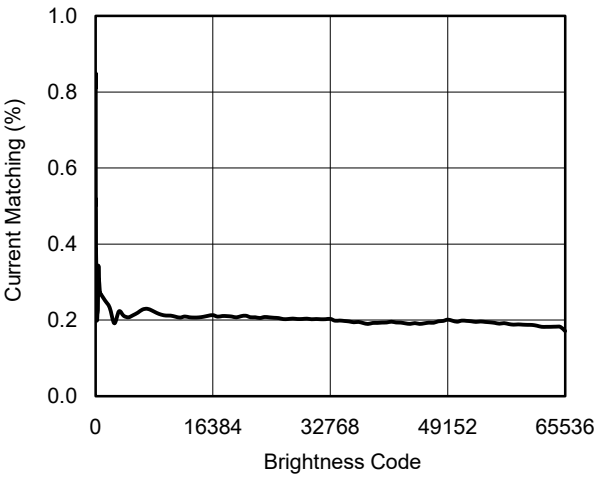
SEPIC Efficiency



Current Linearity



Current Matching



FUNCTIONAL BLOCK DIAGRAM

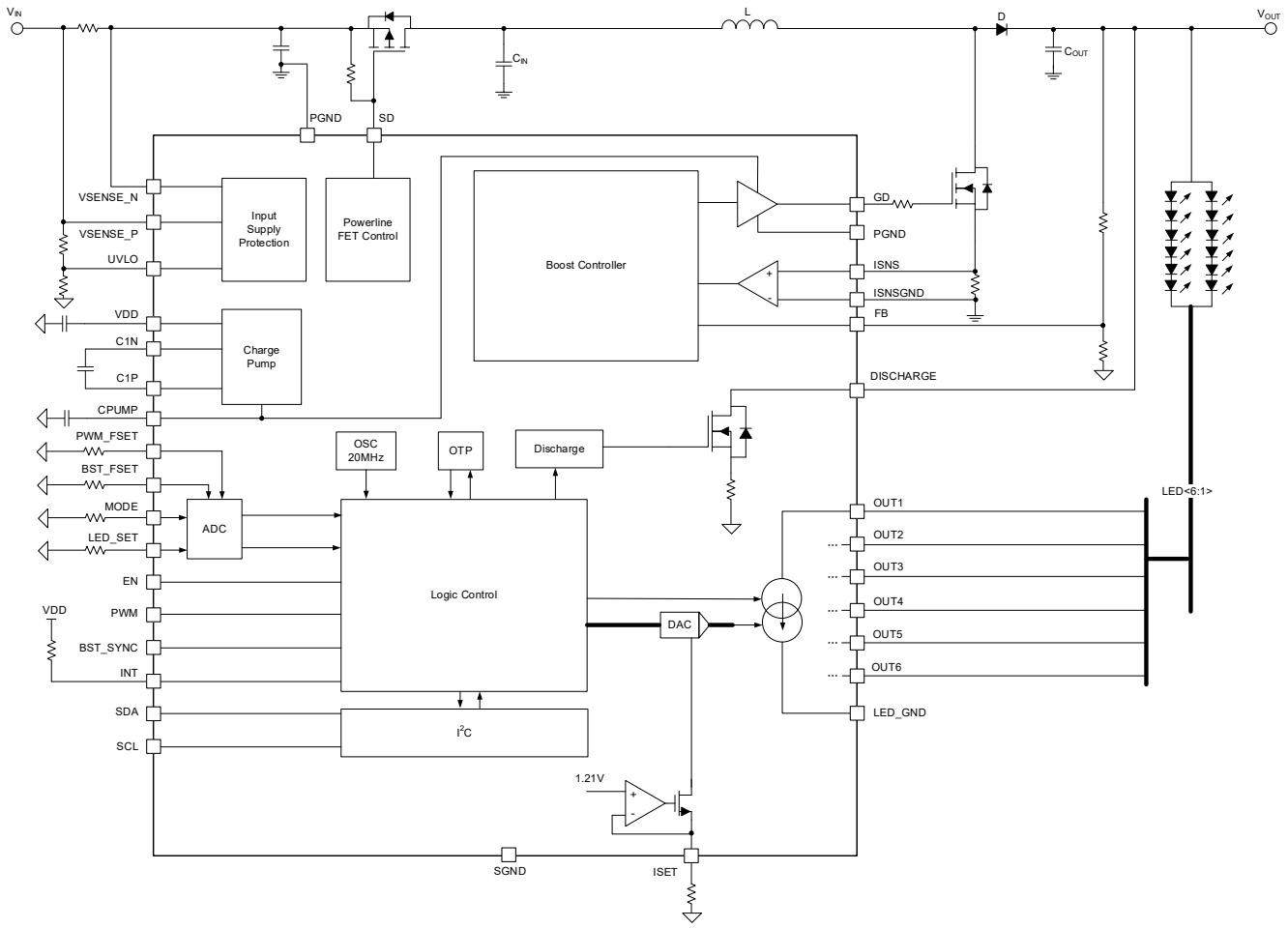


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

SGM37461Q is a high-voltage automotive LED driver designed for infotainment displays, instrument clusters, HUD and other automotive backlight display applications. Brightness control defaults to external PWM input, and can also be set via I^2C interface.

Boost switching frequency, LED dimming mode, LED PWM frequency, LED string configuration and LED string current are configured through external resistors on BST_FSET, MODE, PWM_FSET, LED_SET and ISET pins. The INT pin reports fault conditions, and interrupt flags can be cleared via I^2C or by EN falling edge.

Boost switching frequency is adjustable from 100kHz (TYP) to 2.222MHz (TYP) configured by BST_FSET resistor. The device offers a soft-start function to limit inrush current during start-up. The device can also drive an external power-line FET for system isolation and leakage reduction during shutdown or fault conditions. The Boost controller can be synchronized to an external clock through the BST_SYNC pin. When external synchronization is not used, connect BST_SYNC to GND to disable spread spectrum or to VDD pin to enable spread spectrum. The system adopts adaptive Boost voltage control. During operation, the Boost output is adaptively adjusted to the minimum required level by monitoring LED headroom, improving system efficiency.

The SGM37461Q provides phase shift PWM mode, hybrid mode, current dimming mode and direct PWM mode, determined by the MODE resistor. It integrates 6 well-matched constant current sinks to control the brightness of LED string, and each channel can provide up to 200mA constant current. The outputs can be paralleled for higher current capability, like HUD application. Maximum LED current is set by ISET resistor and can be fine-tuned via the LED_CURRENT[11:0] register.

LED string configuration is set by the LED_SET resistor. The device automatically determines the phase shift operation according to the number of active LED strings (e.g., 4-string mode corresponds to 90° phase shift). Unused LED outputs must be connected to GND.

The SGM37461Q provides various protections for supply circuit, Boost controller and LED driver. The protections help prevent thermal stress, LED damage, and system-level faults in automotive lighting applications. Fault protection includes: LED open/short detection, LED short-to-GND detection, ISET/ BST_FSET/PWM_FSET/LED_SET/MODE resistor range check, Boost over-current protection (OCP), Boost over-voltage protection (OVP), V_{DD} under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP, VSENSE_P pin), V_{IN} under-voltage protection (UVLO, UVLO pin), V_{IN} over-current protection (OCP, VSENSE pins), and thermal shutdown (T_{SD}).

Device Control Interface

The device provides multiple interfaces for device control and monitoring:

• EN Pin: Input enable pin of the device, used to turn the device on or off.
• PWM Pin: The default input to control the brightness of all current sinks. PWM frequency from 100Hz to 20kHz is recommended.
• SCL and SDA Pins: Provide bidirectional communication for device configuration, internal LED current sink brightness control, and fault status monitoring.
• BST_SYNC Pin: External SYNC signal input pin, connected to GND to disable spread spectrum or to VDD to enable spread spectrum.
• INT Pin: An open-drain fault output indicating fault detection.

DETAILED DESCRIPTION (continued)

External Function Setting

The device provides multiple parameter settings for different functions:

- MODE Pin: Configure the dimming mode, set through a resistor to GND.
- PWM_FSET Pin: Configure the LED output dimming frequency, set through a resistor to GND.
- BST_FSET Pin: Configure Boost switching frequency, set through a resistor to GND.
- LED_SET Pin: Determine the LED channels configuration, set through a resistor to GND.
- ISET Pin: Configure the maximum LED output current of all the active channels.
- SD Pin: The gate of power line MOSFET, used to provide input power protection by disconnecting the input supply from the Boost controller.
- VSENSE_P and VSENSE_N Pins: Set the input current limit through a resistor between VSENSE_P and VSENSE_N pins.
- UVLO Pin: Set the input voltage UVLO threshold through a voltage divider between V_{IN} and UVLO.
- ISNS Pin: Set the Boost cycle-by-cycle current limit through a resistor to ISNSGND.
- DISCHARGE Pin: Discharge the Boost output when EN is pulled down.

Device Supply (V_{DD})

All internal analog and digital blocks of SGM37461Q are powered from the external VDD supply. V_{DD} is typically provided by a 5V or 3.3V power rail through an LDO or DC/DC converter, with at least 200mA current capability.

Enable (EN)

SGM37461Q is enabled when the V_{EN} exceeds the V_{EN_ON} threshold, and is disabled when V_{EN} falls below V_{EN_OFF}. When EN powers up, all analog and digital blocks are activated. When EN powers off, the device is in shutdown state: SD pin is floating, and both I^2C interface and fault monitoring are not active.

Charge Pump

An integrated regulated charge pump provides voltage supply for the driver of external Boost switching FET. Charge pump operation is automatically selected based on the connection between VDD and CPUMP. When V_{DD} is below 4.5V during the IC initialization, the charge pump is enabled to generate a 5V gate drive for the external FET. A 2.2μF capacitor is required between C1P and C1N for charge pump. If the charge pump is not used, C1P and C1N are left unconnected, and C_{PUMP} is tied to VDD. In this case, a 5V V_{DD} is recommended. In both configurations, a 4.7μF pump capacitor must be placed on CPUMP to support gate drive energy storage, and it should be placed close to the CPUMP pins.

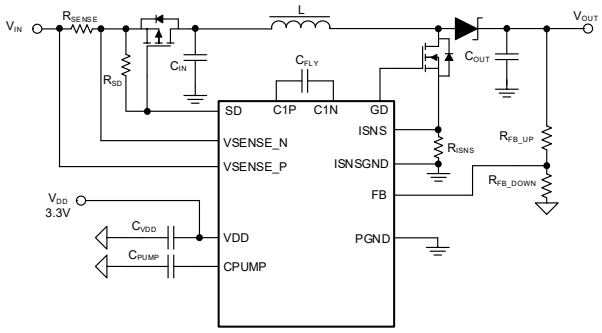


Figure 4. Charge Pump Enabled Circuit

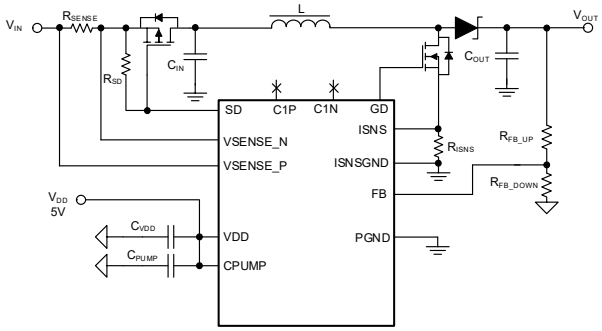


Figure 5. Charge Pump Disabled Circuit

When the charge pump is enabled, CPCAP_STATUS indicates detection of the flying capacitor and CP_STATUS indicates the status of charge pump. If the charge pump fault happens, INT pin is pulled down. The CP_INT_EN[1:0] and CPCAP_INT_EN[1:0] bits mask charge pump and flying capacitor faults respectively and prevent IC from triggering an interrupt on the INT pin.

DETAILED DESCRIPTION (continued)

Boost Controller

The SGM37461Q integrates a current-mode Boost DC/DC controller to generate the LED anode supply voltage. The Boost controller employs cycle-by-cycle peak current limit by monitoring the voltage across an external current-sense resistor connected between the ISNS and ISNSGND pins. The cycle-by-cycle current limit is determined by the value of the external sense resistor. Typically a 20mΩ sense resistor sets the current limit to approximately 10A. Depending on the application requirements, the sense resistor value is recommended to be selected from 15mΩ to 50mΩ. The maximum Boost output voltage is programmed using an external resistor divider connected between VOUT and the FB pins. The total configuration and connection of Boost controller are described in Figure 6.

The Boost switching frequency is programmable from 100kHz (TYP) to 2.222MHz (TYP) using an external resistor connected to the BST_FSET pin (see Table 1). To ensure accurate switching frequency and proper device operation, a resistor with 1% tolerance or better is recommended.

Table 1. Boost Frequency Configuration

R_{BST_FSET} (kΩ)	Typical Boost Frequency (kHz)
7.87	100
4.75	200
5.76	303
3.92	400
11	500
17.8	1818
42.2	2000
124	2222

Boost Cycle-by-Cycle Current Limit

The voltage difference between ISNS and ISNSGND provides current feedback for the Boost controller and the voltage is also monitored for cycle-by-cycle current limit. If the current exceeds the limit, IC stops the switching until the next switching cycle. This cycle-by-cycle current limiting ensures rapid protection for critical power-stage components, such as the inductor, Schottky diode and switching MOSFET. It prevents current stress from exceeding their absolute maximum ratings. The cycle-by-cycle current limit can be calculated as follow:

$$I_{CBC_LIMIT} = \frac{V_{ISNS}}{R_{ISNS}} \quad (1)$$

where, V_{ISNS} = 200mV, R_{ISNS} represents the resistor between ISNS and ISNSGND pins.

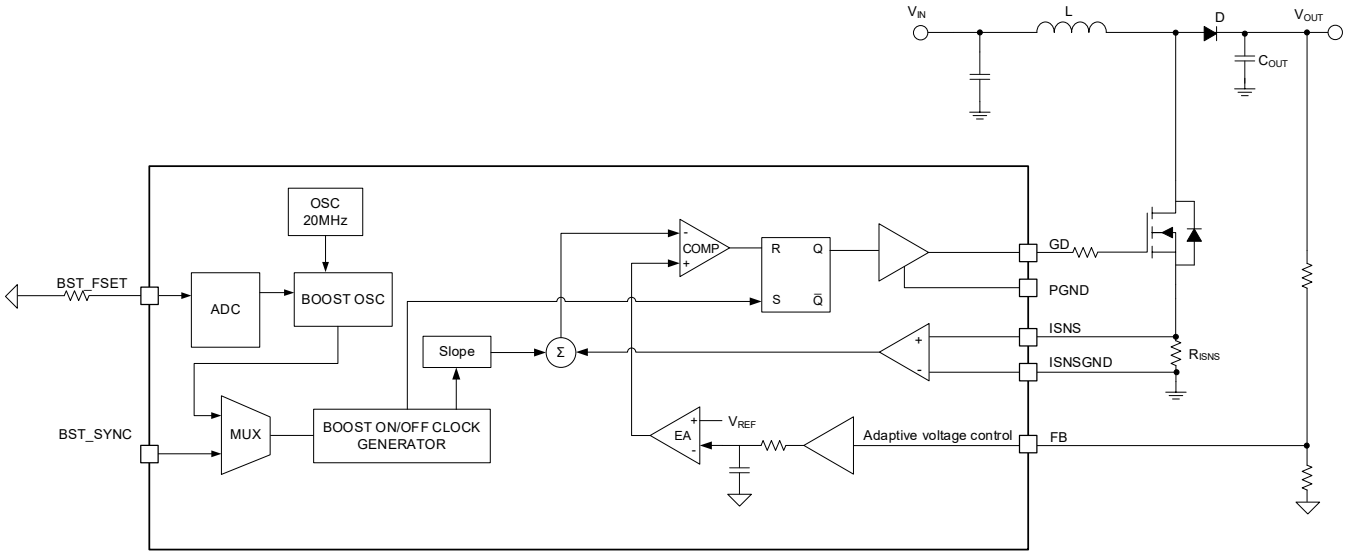


Figure 6. Boost Controller Block Diagram

DETAILED DESCRIPTION (continued)

Minimum ON-/OFF-Time of Boost Controller

The device Boost DC/DC controller features internally defined minimum on-time and minimum off-time, as listed in the Electrical Characteristics table. The system design must ensure that the minimum off-time requirement is satisfied. In particular, the rising time of SW node shall be smaller than the specified minimum off-time.

Table 2. Minimum ON-Time and OFF-Time Characteristic

Frequency (kHz)	Minimum Switch OFF Time (ns)	Minimum Switch ON Time (ns)
100 to 500	150	150
1818 to 2222	40	110

Boost Adaptive Voltage Control

The SGM37461Q Boost DC/DC controller provides the anode supply voltage for the LED strings. During normal operation, the Boost output voltage is automatically regulated according to the minimum LED current sink headroom voltage, which is called adaptive voltage control. Only enabled LED channels are included in the adaptive Boost regulation loop. LED channels detected as open-circuit or short-circuit faults are excluded from the control loop.

The IC continuously monitors the OUTx pin voltages of the active LED channels. If any monitored channel voltage falls below the $V_{HEADROOM}$ threshold, the Boost output voltage is increased to restore sufficient headroom. Conversely, the Boost voltage is gradually reduced until one of the OUTx voltages reaches the $V_{HEADROOM}$ level. The regulation process of Boost adaptive voltage control is shown in Figure 7.

The resistor divider (R_{FB_UP}, R_{FB_DOWN}) defines the adjustable Boost output voltage range. The maximum Boost output is determined by the designed LED string voltage. It is recommended to set the maximum Boost output at least 2V higher than the maximum LED string voltage to reach the expected LED current and maintain the system stability. The minimum Boost output of adjustable range should be lower than the minimum LED string voltage. At the Boost soft-start operation, the Boost output is regulated to the 88% of the Boost output's adjustable range.

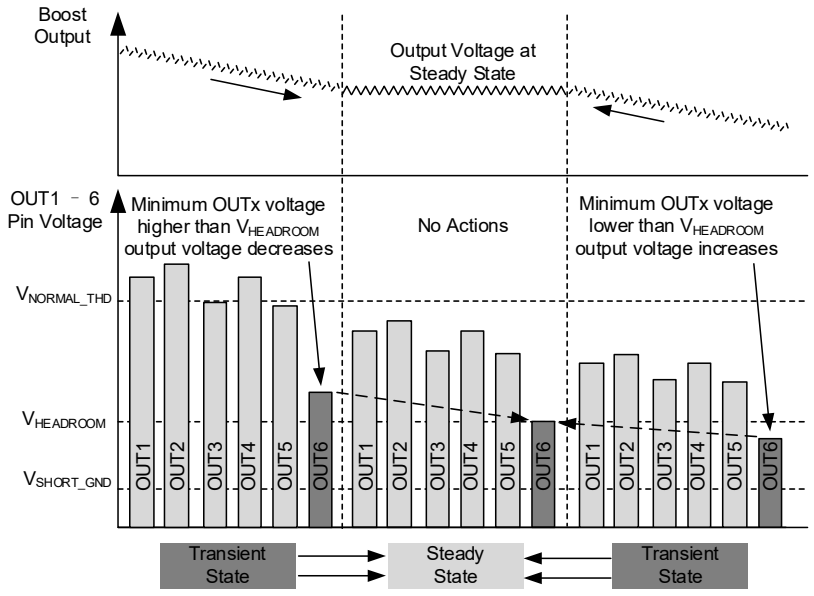


Figure 7. Adaptive Boost Voltage Control Regulating the Minimum OUTx Voltage

DETAILED DESCRIPTION (continued)

Boost Output Voltage Adjustment Using Two-Resistor Divider

Figure 8 shows the Boost output voltage adjustment using two-resistor divider.

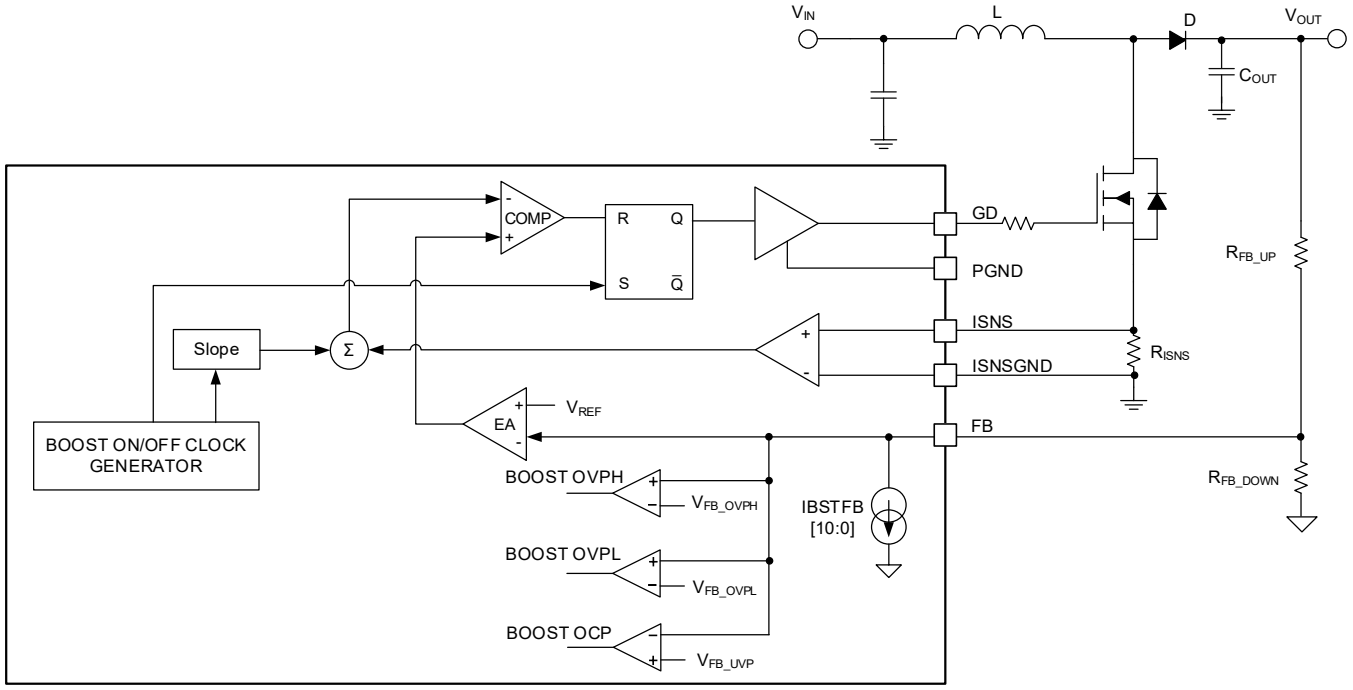


Figure 8. FB Setting Circuit for Two-Resistor Divider

The maximum Boost voltage is calculated as below:

$$V_{BOOST_MAX} = I_{BSTFB_MAX} \times R_{FB_UP} + \left(\frac{R_{FB_UP}}{R_{FB_DOWN}} + 1 \right) \times V_{REF} \quad (2)$$

where, V_{REF} = 1.21V and I_{BSTFB_MAX} = 38.7μA, a typical range of R_{FB_UP}/R_{FB_DOWN} ratio is from 7 to 15.

The minimum Boost voltage is calculated as below:

$$V_{BOOST_MIN} = \left(\frac{R_{FB_UP}}{R_{FB_DOWN}} + 1 \right) \times V_{REF} \quad (3)$$

where, V_{REF} = 1.21V.

DETAILED DESCRIPTION (continued)

Boost Output Voltage Adjustment Using Three-Resistor Divider

Figure 9 shows the Boost output voltage adjustment using three-resistor divider.

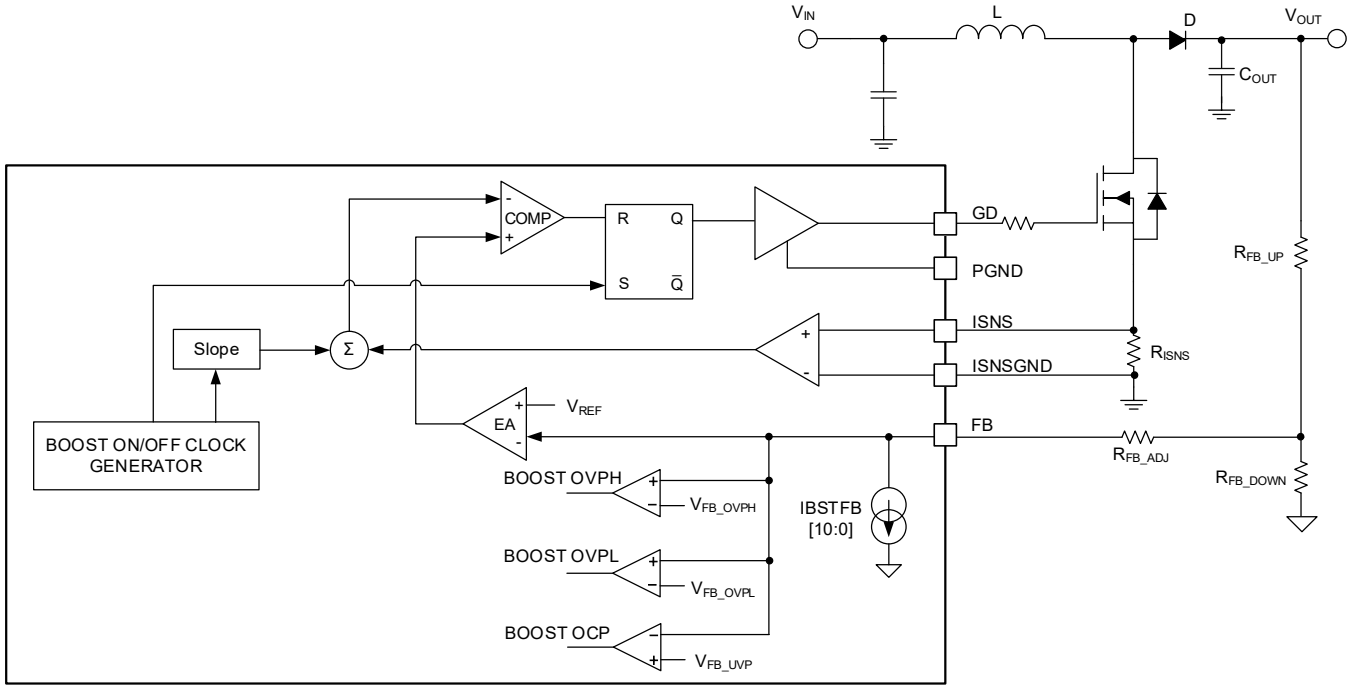


Figure 9. FB Setting Circuit for Three-Resistor Divider

The maximum Boost voltage is calculated as below:

$$V_{BOOST_MAX} = \left(\frac{R_{FB_UP} \times R_{FB_ADJ}}{R_{FB_DOWN}} + R_{FB_UP} + R_{FB_ADJ} \right) \times I_{BSTFB_MAX} + \left(\frac{R_{FB_UP}}{R_{FB_DOWN}} + 1 \right) \times V_{REF} \quad (4)$$

where, V_{REF} = 1.21V and I_{BSTFB_MAX} = 38.7μA, a typical range of R_{FB_UP}/R_{FB_DOWN} ratio is from 7 to 15.

The minimum Boost voltage is calculated as below:

$$V_{BOOST_MIN} = \left(\frac{R_{FB_UP}}{R_{FB_DOWN}} + 1 \right) \times V_{REF} \quad (5)$$

DETAILED DESCRIPTION (continued)

Boost Synchronization and Spread Spectrum

The spread spectrum function is enabled when the BST_SYNC pin is held high and disabled when the BST_SYNC pin is held low. The spread spectrum configuration is sampled and latched during the IC initialization.

The Boost controller can also be synchronized to an external clock applied to the BST_SYNC pin. When an external clock is present, the Boost switching frequency is determined by the external clock signal. If the external clock is removed, the controller automatically resumes operation at the switching frequency programmed by the resistor connected to the BST_FSET pin.

The spread spectrum function reduces EMI peaks by modulating the switching frequency and spreading the energy across a wider frequency range. It achieves this by modulating the Boost switching frequency around the nominal center frequency within a range of ±3.3% to ±7.2%, with a modulation frequency between 200Hz and 22kHz. The Boost switching frequency spread range is set through SPREAD_RANGE[1:0] bits. The spread spectrum modulation frequency is set through SPREAD_MOD_FREQ1[1:0] and SPREAD_MOD_FREQ2[1:0] bits. The spread spectrum function is disabled when an external synchronization clock is applied.

Table 3. Spread Spectrum Frequency Range Selection

SPREAD_RANGE[1:0] (Binary)	Switching Frequency Variation
00	±3.3%
01	±4.3%
10 (Default)	±5.3%
11	±7.2%

Table 4. Modulation Frequency Selection

SPREAD_MOD_FREQ1[1:0]/ SPREAD_MOD_FREQ2[1:0]	Modulation Frequency
SPREAD_MOD_FREQ1[1:0] = 00 (default), SPREAD_MOD_FREQ2[1:0] = 00 (default)	200Hz
SPREAD_MOD_FREQ1[1:0] = 01, SPREAD_MOD_FREQ2[1:0] = 00 (default)	500Hz
SPREAD_MOD_FREQ1[1:0] = 10, SPREAD_MOD_FREQ2[1:0] = 00 (default)	800Hz
SPREAD_MOD_FREQ1[1:0] = 11, SPREAD_MOD_FREQ2[1:0] = 00 (default)	1200Hz
SPREAD_MOD_FREQ2[1:0] = 01	10kHz
SPREAD_MOD_FREQ2[1:0] = 10	20kHz
SPREAD_MOD_FREQ2[1:0] = 11	22kHz

Boost Output Discharge

When EN is pulled low, the Boost controller, LED current sinks and power-line FET are disabled. The Boost output is actively discharged. The DISCHARGE pin typically sinks 30mA for 400ms, after which the device fully shuts down. An internal comparator monitors DISCHARGE voltage. If it exceeds V_{BST_OVPH}, the device enters Fault Recovery mode and sets the BST_OVPH fault, providing protection against uncontrolled Boost output over-voltage.

The discharge function is supported only in the TSSOP-38 (Exposed Pad) package and is not available in the TQFN-5×5-32KL package.

LED Current Sinks

LED Current Configuration

The maximum LED output current is programmed by an external resistor connected between ISET pin and GND. The maximum current is determined by the R_{ISET}, when the LED_CURRENT[11:0] bits remain unchanged. Equation 6 shows the current setting across all LED channels:

$$I_{SET} = \left(\frac{1.21V}{R_{ISET}} \times 2580\right) \times \left(\frac{LED_CURRENT[11:0]}{4095}\right) \quad (6)$$

The default value of LED_CURRENT[11:0] is the maximum setting, 0xFFF (4095). The LED_CURRENT[11:0] can be used to achieve a lower maximum LED output current.

It is recommended to configure the LED current within a range of 30mA to 200mA. Therefore, the R_{ISET} value is typically in the range of 15.6kΩ (corresponding to 200mA) to 104kΩ (corresponding to 30mA).

DETAILED DESCRIPTION (continued)

LED String Configuration

The LED string configuration is set by the LED_SET resistor. The channels can be grouped as 1, 2, or 3 strings, enabling configurations such as three 400mA strings, two 600mA strings or a single 1200mA string.

Channel phase shift function is automatically assigned according to the selected string configuration, which is shown in Table 5. It reduces Boost output ripple, allows smaller output capacitors, and helps reduce audible noise from capacitors. The increased effective load frequency can shift switching-related noise above the audible range while maintaining low PWM frequency for high dimming resolution.

When IC powers up, the LED_SET resistor is sampled to determine the string configuration and channel phase assignment. The configuration must not be changed during operation. IC follows the configuration though the LED_SET resistor missing or invalid after initialization. For reliable active string detection during initialization, the unused OUTx pins must be connected to GND.

Table 5. LED Output String Configuration

R_{LED_SET} (kΩ)	LED Strings	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	Automatic Phase Shift
3.92	6 Channels	200mA	200mA	200mA	200mA	200mA	200mA	60°
4.75	5 Channels	200mA	200mA	200mA	200mA	200mA	(Tied to GND)	72°
5.76	4 Channels	200mA	200mA	200mA	200mA	(Tied to GND)	(Tied to GND)	90°
7.87	3 Channels	200mA	200mA	200mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	120°
11	2 Channels	200mA	200mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	(Tied to GND)	180°
17.8	3 Channels	400mA		400mA		400mA		120°
42.2	2 Channels	600mA			600mA			180°
124	1 Channel	1200mA						-

DETAILED DESCRIPTION (continued)

Brightness Control

The SGM37461Q offers flexible dimming solutions with multiple dimming modes, including phase shift PWM mode, hybrid mode, current dimming mode and direct PWM mode. Each mode provides its own advantages in terms of brightness performance, EMI performance and efficiency. Brightness control can be configured through either external PWM input or I^2C commands. An LED current sloper function is also available to achieve smooth LED current transitions.

Dimming Mode

Dimming mode is configured via an external resistor on the MODE pin. The MODE pin also selects the I^2C address of SGM37461Q, which can be either 0x2A or 0x2B. The different I^2C addresses allow two SGM37461Q devices to be connected on the same I^2C bus in a single LED driver system.

Table 6. Dimming Mode Configuration

R_{MODE} (kΩ)	Mode	I^2C Address
3.92	Phase Shift PWM Mode	0x2B
4.75	Hybrid Mode	0x2B
5.76	Current Dimming Mode	0x2B
7.87	Direct PWM Mode	0x2B
11	Phase Shift PWM Mode	0x2A
17.8	Hybrid Mode	0x2A
42.2	Current Dimming Mode	0x2A
124	Direct PWM Mode	0x2A

LED Dimming Frequency

The LED dimming frequency is asynchronous to the input PWM in phase shift PWM mode and hybrid dimming mode. It is derived from an internal 20MHz oscillator and can be programmed to eight discrete frequencies ranging from 152Hz to 19.531kHz.

The PWM_FSET resistor selects the LED PWM frequency according to Table 7. Lower PWM frequency provides higher dimming resolution. The PWM resolution shown in Table 7 applies when PWM dither is disabled.

Table 7. LED PWM Frequency Selection

R_{PWM_FSET} (kΩ)	Typical LED PWM Frequency (Hz)	PWM Dimming Resolution (bits)
3.92	152	16
4.75	305	16
5.76	610	15
7.87	1221	14
11	2441	13
17.8	4883	12
42.2	9766	11
124	19531	10

DETAILED DESCRIPTION (continued)

Phase Shift PWM Mode

Phase shift PWM mode reduces the instantaneous current variation, which reduces output current ripple and improves EMI performance. The brightness control path is shown in Figure 10.

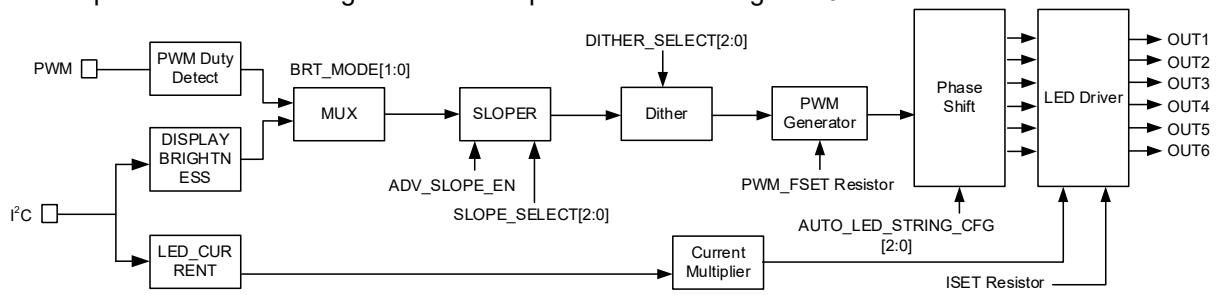


Figure 10. Brightness Control Path of Phase Shift PWM Mode

In phase shift PWM mode, all active channels are switched on and off at the LED dimming frequency with a fixed delay. The phase delay between adjacent channels is determined by the number of active channels or channel groups, as shown in Figure 11.

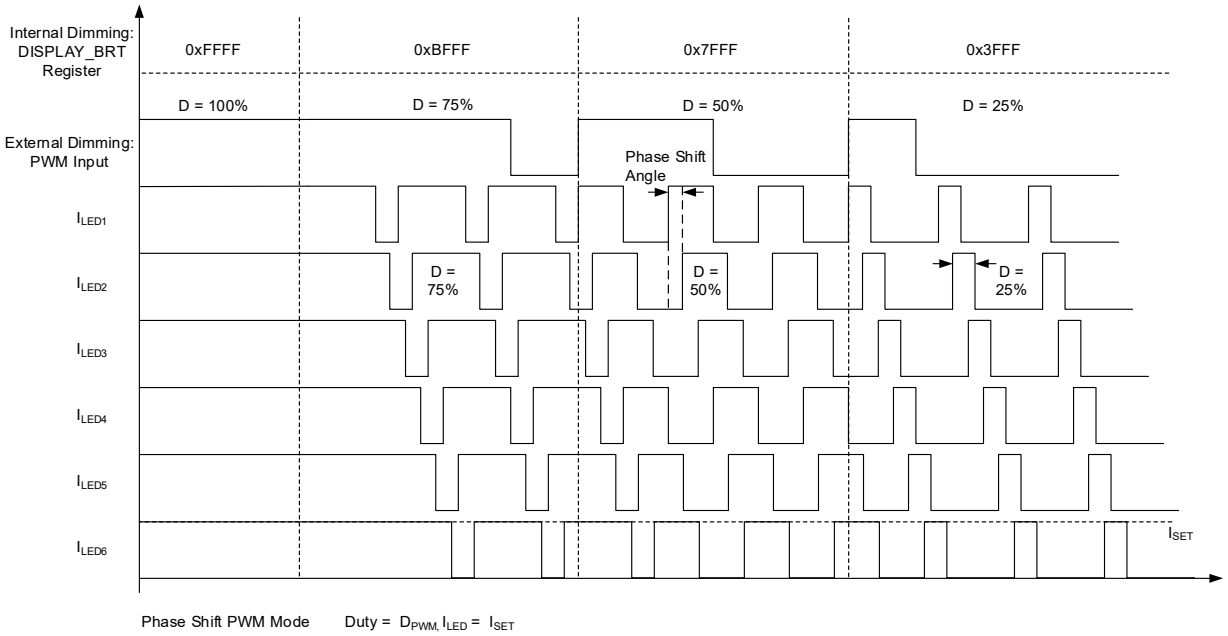


Figure 11. Phase Shift Dimming Diagram

DETAILED DESCRIPTION (continued)

Hybrid Mode

SGM37461Q supports hybrid mode, which combines PWM and current control for the display brightness path. The brightness control path is shown in Figure 13 below.

Hybrid mode is selected via the MODE pin resistor. When operating in hybrid dimming mode with a PWM signal applied to the PWM pin, the system behaves as follows:

• Above 12.5% PWM duty cycle, current dimming is adopted, with the LED current amplitude directly proportional to the PWM duty.

• Below 12.5% PWM duty cycle, the system adopts PWM dimming, fixing the LED current at 12.5% of its maximum. The output dimming duty is then 8 times the input PWM duty.

Current dimming improves optical efficiency and has a better EMC performance at high brightness, while PWM dimming ensures linear and accurate control at low brightness. The transition threshold between PWM and current dimming can be configured at 12.5% or 0%. Selecting 0% enables pure current dimming mode.

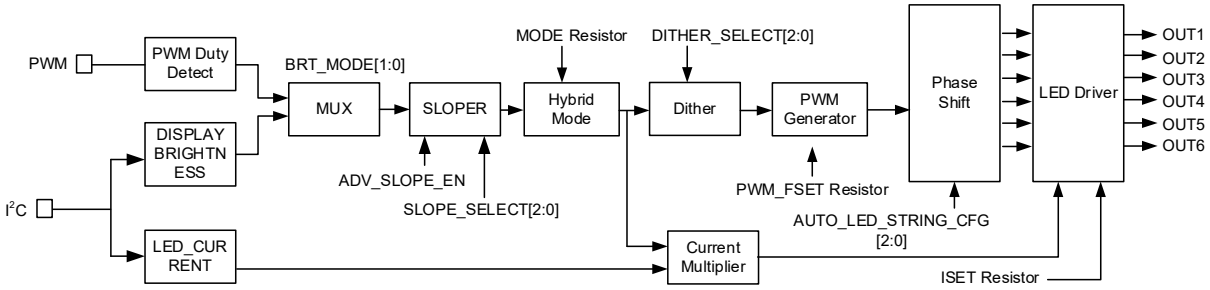


Figure 12. Brightness Control Path of Hybrid Mode

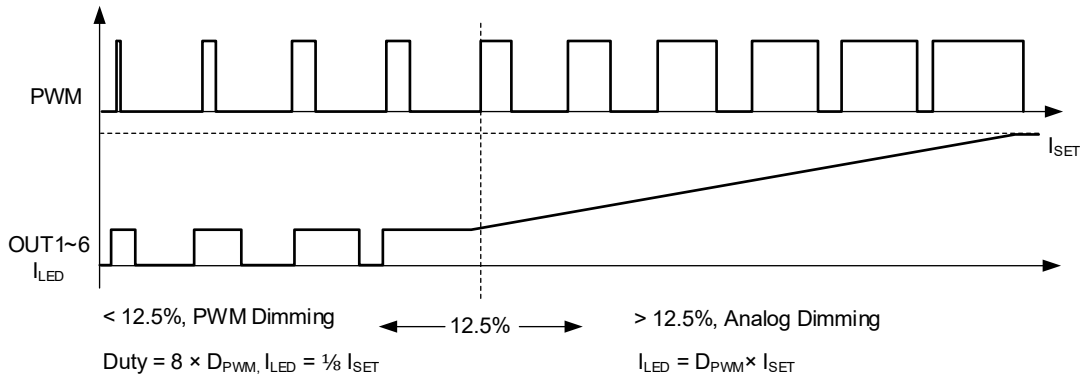


Figure 13. Hybrid Dimming Diagram

DETAILED DESCRIPTION (continued)

Current Dimming Mode

Analog mode provides smooth LED current regulation without PWM switching, reducing conducted and radiated EMI. The brightness control path is shown in Figure 14.

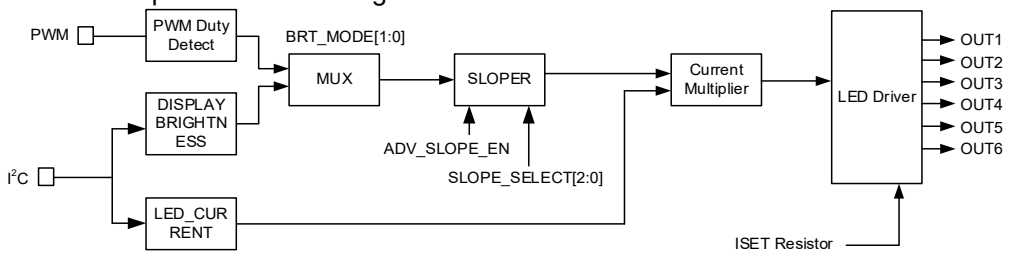


Figure 14. Brightness Control Path of Current Dimming Mode

In current dimming mode, the LED current remains stable and continuous, with the current amplitude proportional to the input PWM duty cycle.

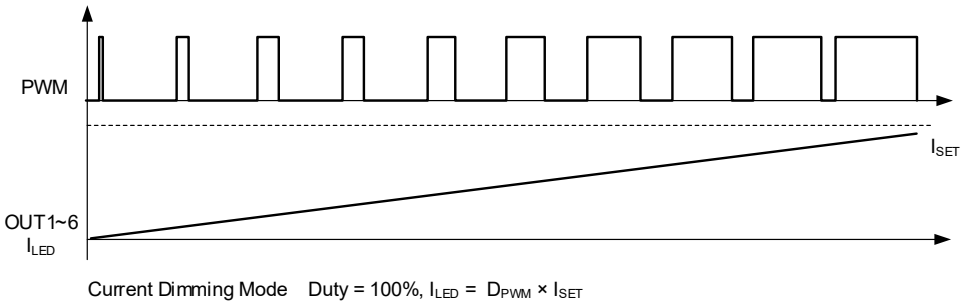


Figure 15. Current Dimming Diagram

Direct PWM Mode

SGM37461Q supports direct PWM mode, the brightness control path is shown in Figure 16.

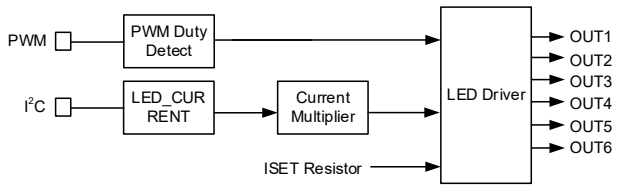


Figure 16. Brightness Control Path of Direct PWM Mode

In direct PWM mode, the LED current is directly chopped by the input PWM signal applied to the PWM pin, with the LED current frequency and duty mirroring that of the input PWM signal.

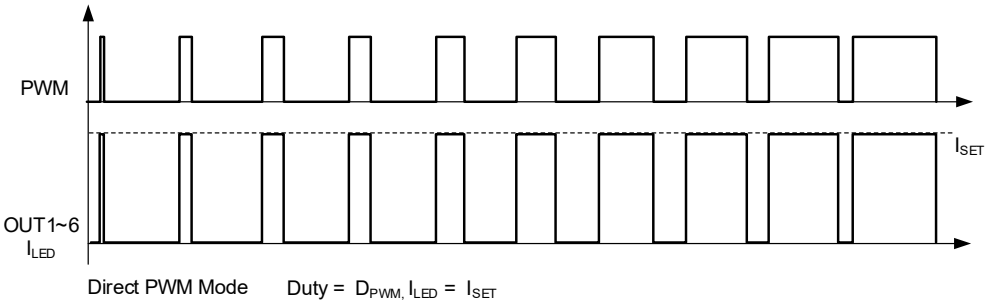


Figure 17. Direct PWM Dimming Diagram

DETAILED DESCRIPTION (continued)

Sloper

The optional sloper function enables smooth optical transitions between brightness levels. By default, the advanced sloper is enabled with a 200ms slope transition.

The transition time can be configured via SLOPE_SELECT[2:0], setting to 000 disables the sloper function. With ADV_SLOPE_ENABLE set to 1, brightness transitions are further smoothed.

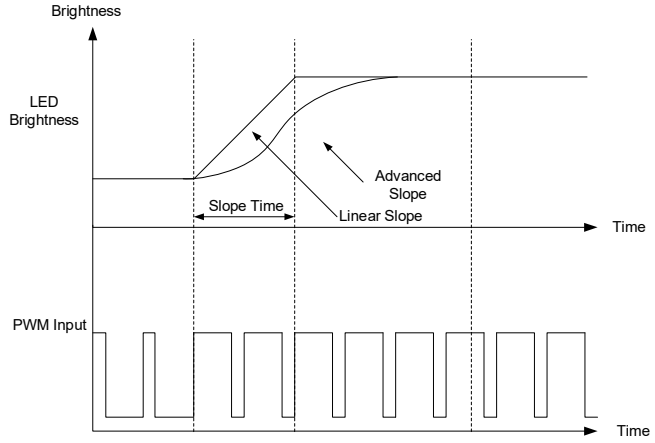


Figure 18. Brightness Sloper

PWM Detector Hysteresis

The PWM detector adopts an internal hysteresis to prevent duty cycle sampling errors caused by the onboard PWM signal's rising/falling time or other abnormal jitter of duty cycle. Except in direct PWM mode, the PWM output duty cycle updates only when the PWM input duty cycle variation exceeds 0.19% in the opposite direction.

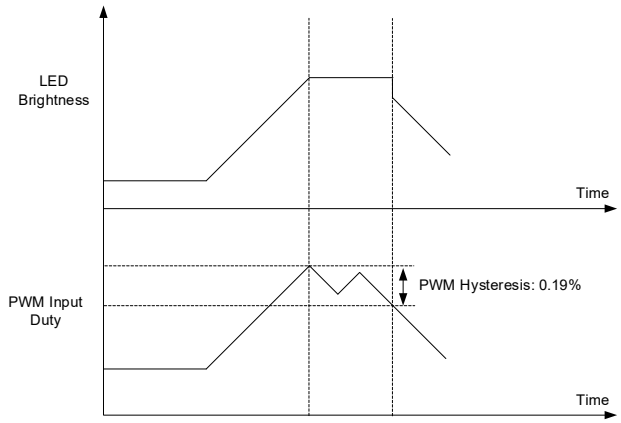


Figure 19. PWM Detector Hysteresis

DETAILED DESCRIPTION (continued)

Dither for PWM Duty Cycle

The LED PWM dimming resolution is limited by the ratio of the internal 20MHz oscillator frequency to the LED PWM frequency configured by the PWM_FSET resistor. To achieve higher-resolution brightness adjustment beyond the inherent clock resolution, the SGM37461Q integrates a PWM duty cycle dither function. This function periodically adjusts the PWM pulse width to generate additional duty cycles. The additional duty cycle is determined by the minimum step size of the 20MHz clock period (50ns).

The dither function can be set through DITHER_SELECT[2:0] bits. The SGM37461Q offers five programmable dither levels, including disabled, 1-bit, 2-bit, 3-bit and 4-bit. Dither function is disabled by default.

The additional duty cycle is evenly distributed across multiple PWM cycles according to the selected dither resolution: 2 cycles for 1-bit dither, 4 cycles for 2-bit dither, 8 cycles for 3-bit dither and 16 cycles for 4-bit dither.

Take 3-bit for example, code 001 represents one additional duty cycle that is evenly added at every 8 duty cycles, code 010 represents two additional duty cycles that are evenly added at every 8 duty cycles and code 100 represents four additional duty cycles that are evenly added at every 8 duty cycles. A timing example of the PWM output 3-bit dither is illustrated in Figure 20.

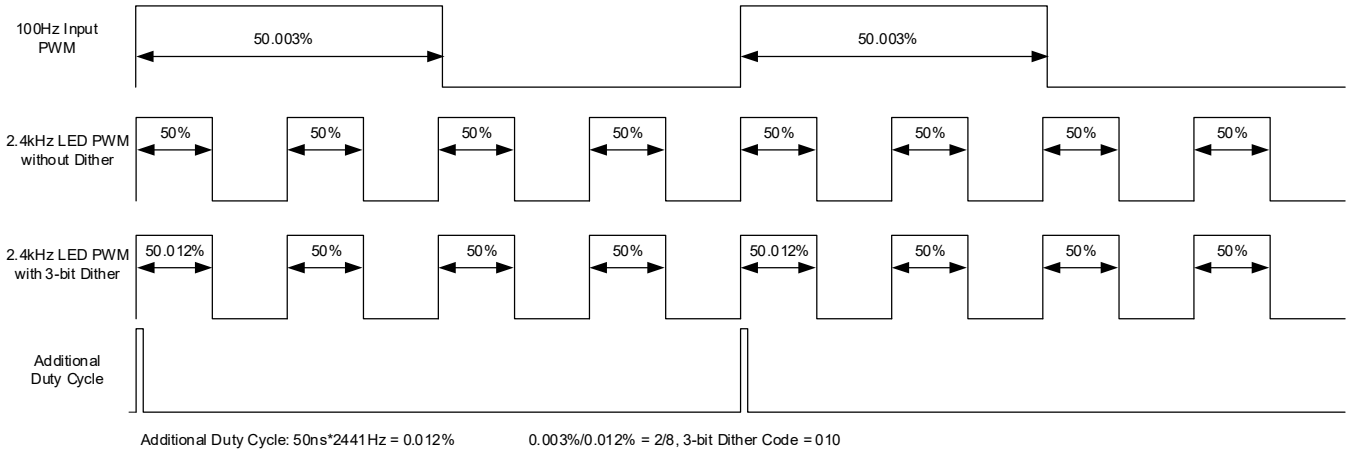


Figure 20. PWM Dither Example

DETAILED DESCRIPTION (continued)

Dither for Ultra-Short LED Pulse Width

To ensure stable and accurate LED current during PWM dimming except direct PWM dimming, the minimum LED current pulse width is limited to 200ns. When the expected LED current pulse width is less than 200ns, the SGM37461Q offers a dither function to skip the LED pulse. It further reduces the minimum brightness limitation caused by the LED output settling time. At a fixed PWM frequency, pulse skipping reduces the effective LED PWM frequency by periodically removing PWM pulses. So the effective PWM frequency of dither function remains ≥ 152Hz to prevent the visual flicker. A timing example of the dither for ultra-short LED pulse width is illustrated in Figure 21.

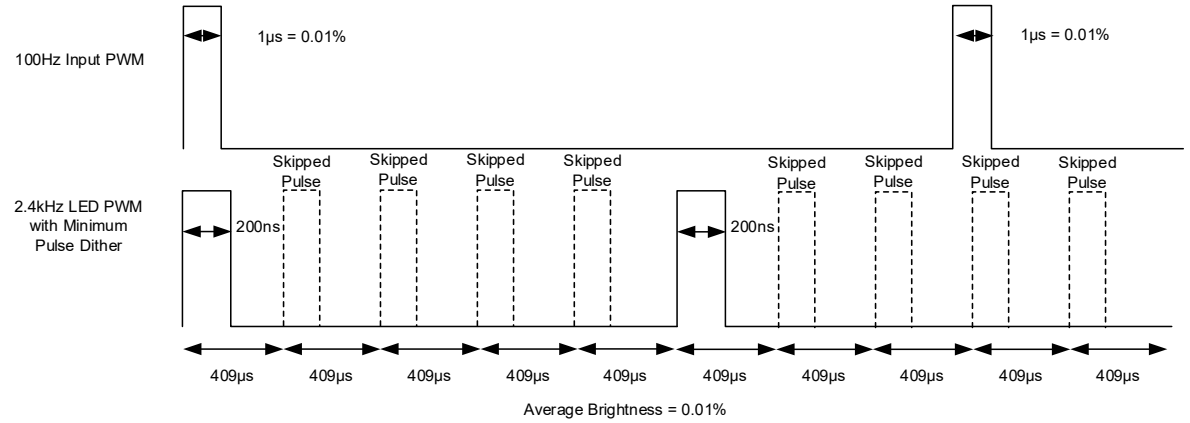


Figure 21. Minimum Brightness Dither Example

Protection and Fault Detections

The SGM37461Q integrates fault detections and corresponding protections for supply state, such as: V_{IN} under-voltage, over-voltage and over-current, V_{DD} under-voltage, charge pump voltage fault and component missing fault. For the Boost controller, fault detections and corresponding protections includes Boost over-current, Boost over-voltage and thermal shutdown. For LED channels, the device provides protections against LED open, LED short and LED short-to-GND conditions. The above fault conditions can be monitored through the SUPPLY_STATUS, BOOST_STATUS, and LED_STATUS registers.

Supply Faults

V_{IN} Under-Voltage Faults

The SGM37461Q provides V_{IN} under-voltage protection. The UVLO threshold is set via an external resistor divider at the UVLO pin. When the UVLO pin voltage falls below the falling threshold (0.775V, TYP), the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. The device transitions to Standby mode after entering Fault Recovery. The VINUVLO_STATUS bit in the SUPPLY_STATUS register is set to 1, and the INT pin is pulled low. When the UVLO pin voltage exceeds the rising threshold, the device exits Standby mode and restarts the start-up procedure.

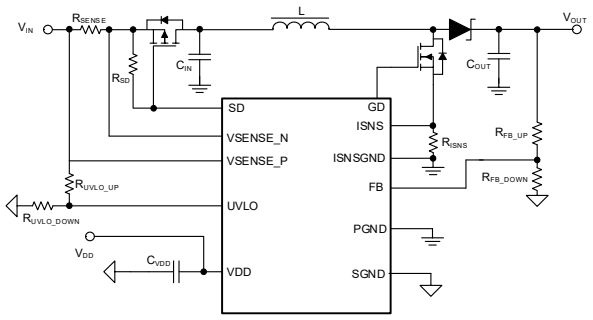


Figure 22. V_{IN} UVLO Setting Circuit

The V_{IN} UVLO rising threshold can be calculated as follows:

$$VIN_{UVLO_RISING} = \left(\frac{R_{UVLO_UP}}{R_{UVLO_DOWN}} + 1 \right) \times VIN_{UVLO_TH} \quad (7)$$

where, VIN_{UVLO_TH} = 0.775V (TYP).

The UVLO hysteresis is calculated using the following equation:

$$VIN_{HYS} = R_{UVLO_UP} \times I_{UVLO} \quad (8)$$

where, I_{UVLO} = 4μA (default) or 1μA.

DETAILED DESCRIPTION (continued)

V_{IN} Over-Voltage Faults

The V_{IN} over-voltage rising threshold is internally fixed at a typical value of 42.3V (TYP). If the V_{SENSE_P} pin voltage exceeds the OVP rising threshold, the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. The device transitions to Standby mode after entering Fault Recovery. The VINOVP_STATUS bit in the SUPPLY_STATUS register is set to 1 and the INT pin is pulled down. When the VSENSE_P voltage falls below the OVP falling threshold, the device exits Standby mode and restarts the start-up procedure.

V_{DD} Under-Voltage Faults

If V_{DD} drops below the V_{DD} UVLO falling threshold, the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. The device transitions to Standby mode after entering Fault Recovery. The VDDUVLO_STATUS bit in the SUPPLY_STATUS register is set to 1 and the INT pin is pulled down. When V_{DD} rises above the V_{DD} UVLO rising threshold, the device exits Standby mode and restarts the start-up procedure.

V_{IN} OCP Faults

If the voltage across the R_{SENSE} resistor exceeds 220mV, the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. The device transitions to Fault Recovery. The device attempts an automatic restart after a 100ms delay. The VINOCP_STATUS bit in the SUPPLY_STATUS register is set to 1 and the INT pin is pulled down. The V_{IN} OCP threshold can be calculated as follow:

$$I_{VIN_OCP} = \frac{VIN_{OCP_TH}}{R_{SENSE}} \quad (9)$$

where, VIN_{OCP_TH} = 220mV.

V_{IN} OCP Current Limit vs. Boost Cycle-by-Cycle Current Limit

The V_{IN} OCP current limit and Boost cycle-by-cycle current limit provide different levels of protection. The Boost cycle-by-cycle limit protects DC/DC components during normal transient events without triggering a device fault. The V_{IN} OCP limit protects against critical system faults, such as inductor or switching MOSFET shorts which force the device to enter fault recovery. The V_{IN} OCP threshold must be higher than the Boost cycle-by-cycle limit, requiring $R_{ISNS} \geq R_{SENSE}$.

Charge Pump Faults

If the CPUMP pin voltage drops below the typical 4.1V (TYP) during normal operation, the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. The device automatically attempts to restart with a 100ms delay after entering Fault Recovery. The CP_STATUS bit in the SUPPLY_STATUS register is set to 1 and the INT pin is pulled down.

During device initialization, if the charge pump flying capacitor is detected as open or short, the charge pump is disabled. The Boost controller and power-line FET are disabled. The LED current sinks are also turned off. The device automatically attempts to restart with a 100ms delay after entering Fault Recovery. In this case, both CPCAP_STATUS and CP_STATUS bits in the SUPPLY_STATUS register are set to 1. The INT pin is pulled down.

CRC Error Faults

During device initialization, if the factory default configuration (including registers, options and trim bits) is not correctly loaded from internal memory, the CRCERR_STATUS bit in the SUPPLY_STATUS register is set to 1. The INT pin is pulled down. The CRC error does not affect the normal operation of SGM37461Q.

DETAILED DESCRIPTION (continued)

Boost Faults

Boost Over-Voltage Faults (OVPL)

Boost over-voltage fault is triggered when the FB pin voltage exceeds the V_{FB_OVPL} threshold. In this condition, the BSTOVPL_STATUS bit in the BOOST_STATUS register is set to 1. The Boost switching FET is disabled to limit the output voltage. Boost OVPL monitoring is active during both Boost soft-start and normal operation.

Boost Over-Voltage Faults (OVPH)

A higher-level Boost over-voltage fault is triggered when the FB pin voltage exceeds the V_{FB_OVPH} threshold or the DISCHARGE pin voltage exceeds V_{BST_OVPH}. In this case, the BSTOVPH_STATUS bit in the BOOST_STATUS register is set to 1. The INT pin is pulled down and the device enters Fault Recovery mode. The device automatically attempts to restart after 100ms. Boost OVPH monitoring is active during Boost soft-start and normal operation.

Boost Over-Current Faults

Boost over-current fault is triggered when the FB pin voltage remains below the V_{FB_UVP} threshold for a deglitch time of 110ms. In this condition, the BSTOCP_STATUS bit in the BOOST_STATUS register is set to 1. The INT pin is pulled down and the device enters Fault Recovery mode. The device automatically attempts to restart after 100ms. Boost over-current monitoring is active during Boost soft-start and normal operation.

LED_SET Resistor Missing Faults

If the LED_SET resistor is missing or has an invalid value during initialization, it is detected at start-up phase and the device defaults to a 6-channel, 200mA configuration. The LEDSET_STATUS bit in the BOOST_STATUS register is set to 1. This condition is only checked during initialization and is not monitored during normal operation. After start-up, the device operates according to the configuration determined at initialization, even if the LED_SET resistor is subsequently missing or invalid.

MODE Resistor Missing Faults

If the MODE resistor is missing or has an invalid value during initialization, it is detected at start-up phase. The device defaults to phase shift PWM mode and the I^2C address defaults to 0x2A. The MODESEL_STATUS bit in the BOOST_STATUS register is set to 1. This condition is only checked during initialization and is not monitored during normal operation. After start-up, the device continues to operate in the mode determined at initialization, even if the MODE resistor is subsequently missing or invalid.

FSET Resistor Missing Faults

If either the BST_FSET or PWM_FSET resistor is missing or has an invalid value during initialization, it is detected at start-up phase. In this case, the Boost switching frequency defaults to 400kHz when the BST_FSET resistor is missing or has an invalid value, and the PWM dimming frequency defaults to 305Hz when the PWM_FSET resistor is missing or has an invalid value. The FSET_STATUS bit in the BOOST_STATUS register is set to 1. This condition is only checked during initialization and is not monitored during normal operation. After start-up, the device operates according to the configuration determined at initialization, even if the FSET resistor is subsequently missing or invalid.

ISET Resistor Out of Range Faults

During normal operation, if ISET pin resistor is shorted to GND, the maximum LED current is determined as calculated in Equation 10:

$$I_{ISET_FAULT} = I_{LED_LIMIT} \times \left(\frac{LED_CURRENT[11:0]}{4095} \right) \quad (10)$$

where, I_{LED_LIMIT} = 280mA (TYP).

When the ISET pin is detected as fault condition, the LED_CURRENT[11:0] register is automatically reduced to one quarter of the most recently programmed value. For example, if no programming has been performed after device enabled, the default value of LED_CURRENT[11:0] is 0xFFF and it will be reduced to 0x3FF upon fault detection. The ISET_STATUS bit in the BOOST_STATUS register is set to 1. The INT pin is pulled down. If the fault recovers and the ISET pin voltage recovers above 1V (TYP), the LED_CURRENT [11:0] register automatically returns to the last programmed value.

Thermal Shutdown Faults

When the die temperature reaches the thermal shutdown threshold, the SGM37461Q disables the Boost controller, power-line FET and LED outputs to prevent device damage. The TSD_STATUS bit is set to 1 and the INT pin is pulled down. Normal operation resumes automatically when the die temperature falls by the T_{SD} hysteresis level.

DETAILED DESCRIPTION (continued)

LED Faults

Open LED Faults

During normal operation, the Boost output voltage is increased when any active LED output falls below the $V_{HEADROOM}$ threshold. An open LED condition is triggered when the Boost output reaches its maximum limit while at least one LED output remains below $V_{HEADROOM}$. The output of the fault LED string is disabled and it will be removed from the adaptive Boost control.

The LED_STATUS bit is set to 1 if LED fault is triggered. The INT pin is pulled down unless LED interrupt reporting is disabled. Detailed fault information is available via the OPEN_LED and LEDx_FAULT status bits, which remain latched until the device powers off. The LED_STATUS bit can be cleared by the host. However, it will be reasserted and a new interrupt generated if a new LED fault is triggered.

Short LED Faults

A short LED fault is triggered when one or more LED outputs exceed the V_{LED_SHORT} threshold (5.4V, TYP), while at least one other LED output remains within the normal operating range. The output of the fault LED string is disabled and it will be removed from the adaptive Boost control. The LED_STATUS bit is set to 1 and the INT pin is pulled down. Detailed fault information is available via the SHORT_LED and LEDx_FAULT bits in the LED_STATUS register.

In HUD applications, LED channels may be connected together as one or two groups. In this condition, when the Boost adaptive voltage reaches the V_{BOOST_MIN} and at least one LED channel voltage remains higher than V_{NORMAL_THD}, the short LED fault is triggered. The corresponding output will be disabled and removed from the adaptive Boost control.

LED Short-to-GND Faults

If an OUTx voltage remains below the V_{SHORT_GND} threshold for 5ms, an abnormal condition is detected. The corresponding output is temporarily disabled and a 3mA test current is applied for 300μs. If the OUTx voltage is still below $V_{HEADROOM}$ after this check, a LED short-to-GND fault is reported.

When an LED short-to-GND fault is detected, the Boost controller and power-line FET are disabled, and the LED current sinks are also turned off. The device automatically attempts to restart with a 100ms delay after entering Fault Recovery. The LED_STATUS bit is set to 1 and the INT pin is pulled down. Fault details are available via the LED_GND and LEDx_FAULT bits in the LED_STATUS register. These bits are latched until the device powers off. The LED_STATUS bit can be cleared.

Invalid LED String Faults

During device initialization, unused LED outputs are checked whether connected to GND. If an unused output is not correctly grounded, an invalid string fault is detected. The device attempts to continue normal operation if possible. The INVSTRING_STATUS bit in the LED_STATUS register is set to 1 and the INT pin is pulled down. This condition is only evaluated during initialization and is not monitored during normal operation. After start-up, the device continues to operate based on the configuration determined at start-up, even if the LED_SET resistor is subsequently missing or invalid.

I^2C Timeout Faults

If an I^2C transaction is not terminated with a STOP condition within 500ms, the I^2C communication block is automatically reset and returns to an idle state, waiting for the next valid command. The I2C_ERROR_ STATUS bit in the LED_STATUS register is set to 1 and the INT pin is pulled down.

DETAILED DESCRIPTION (continued)

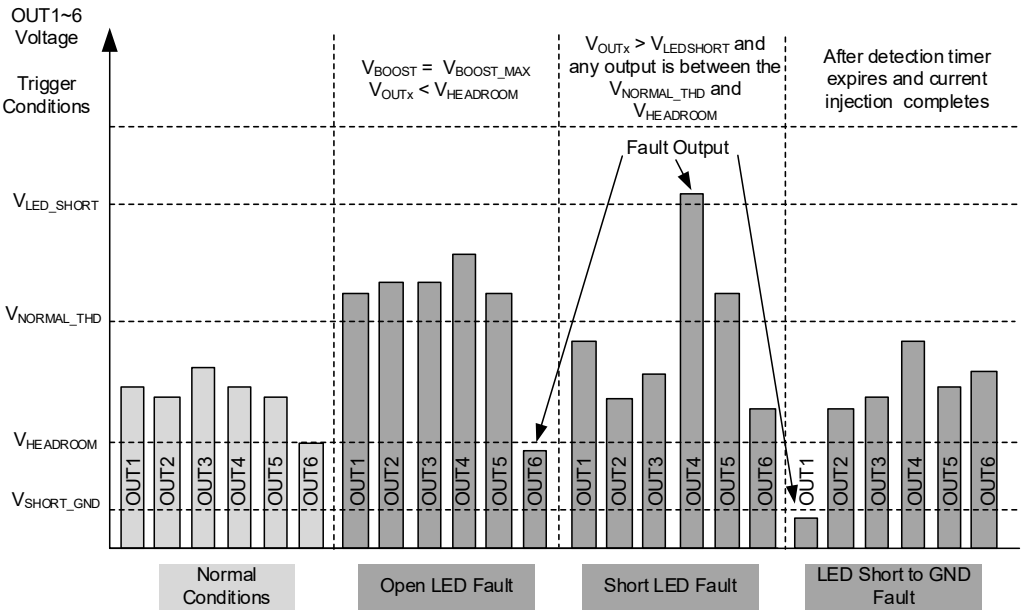


Figure 23. LED Fault Trigger Conditions

Device State

State Diagram

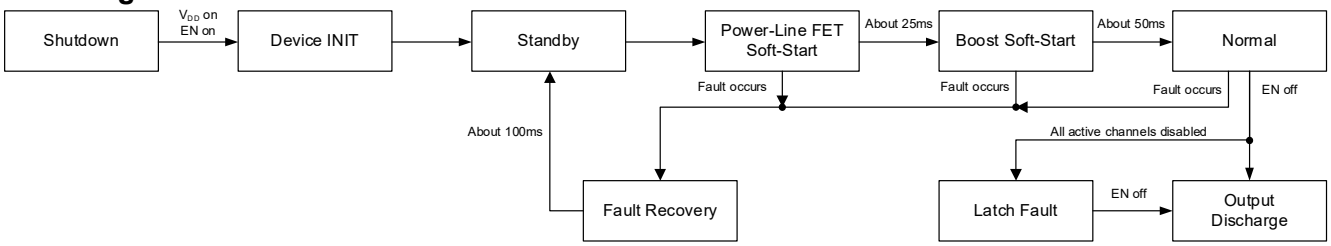


Figure 24. State Machine Diagram

DETAILED DESCRIPTION (continued)

Shutdown

When EN is pulled low, the Boost controller and power-line FET are disabled, and the LED current sinks are turned off. The device discharges the Boost output for 400ms. After this period, the device is fully powered off.

Device Initialization

Device starts the initialization. The device loads default and trim settings from EEPROM. The configurations of Boost and LED current sinks set by external resistors are detected.

Standby Mode

From this mode, the device can change any configuration registers via I^2C. The device will stop in this mode, if some faults are triggered.

Power-Line FET Soft-Start

The power-line FET is gradually enabled through SD pin to prevent the inrush current. This state lasts about 25ms. As the power-line FET is fully turned on, the Boost input and output voltages are equalized to V_{IN} level. The supply protections and LED short-to-GND protection are enabled from this mode.

Boost Soft-Start

During the Boost soft-start, the Boost output voltage is charged to the initial setting voltage. The soft-start phase lasts approximately 50ms, with the current limit typically set to 1A. The Boost protections are enabled from this mode.

Normal Operation

All the active LED outputs are turned on and the LED current ramps up to the setting value depending on the sloper configuration. All LED protections are active.

Fault Recovery

Certain critical faults trigger a fault recovery state. In this state, the Boost controller and power-line FET are disabled, and the LED current sinks are also turned off for 100ms. If EN remains high and brightness is non-zero, the device automatically attempts to restart from Standby mode after the delay.

Latch Fault

If all LED strings are disabled due to faults, the SGM37461Q enters a latched fault state. In this state, the Boost controller and power-line FET are disabled, the LED current sinks are also turned off. This condition is cleared only when the EN pin is pulled low.

Start-up Sequence

For optimal start-up performance, the recommended power-up sequence is as follows: Apply V_{IN} → Apply V_{DD} → Enable EN → Configure via I^2C (if required) → Send PWM dimming signal.

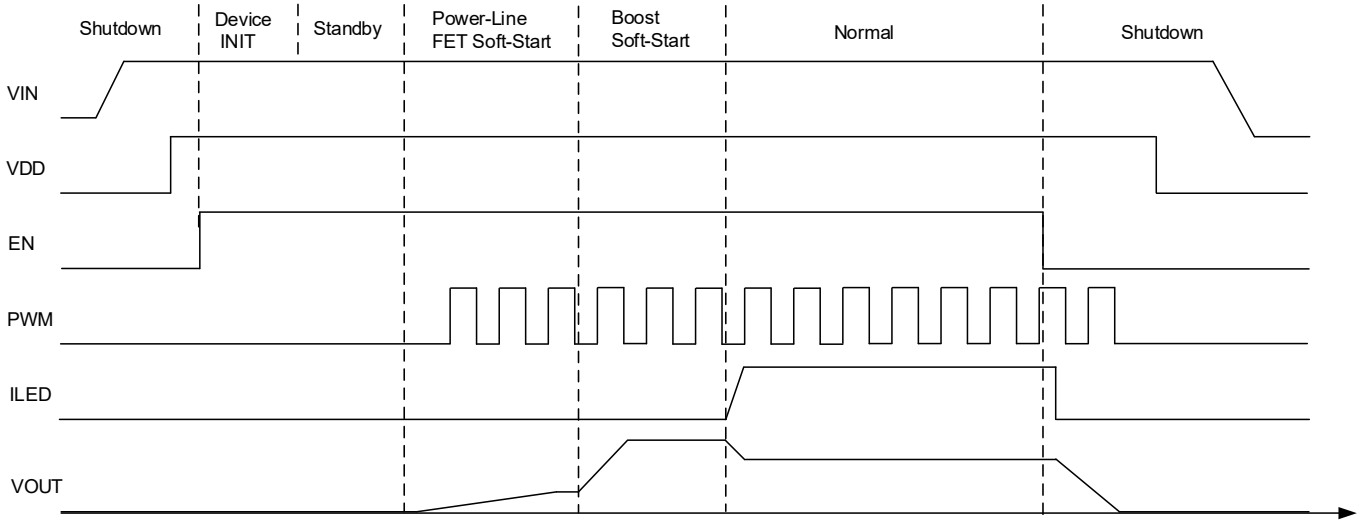


Figure 25. Start-up Sequence Diagram

DETAILED DESCRIPTION (continued)

Programming

I²C-Compatible Interface

The SGM37461Q device supports I²C interface to access and change the configuration. The 7-bit base slave address is 0x2A or 0x2B. The address could be configured through the resistor settings of MODE pin.

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 26. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

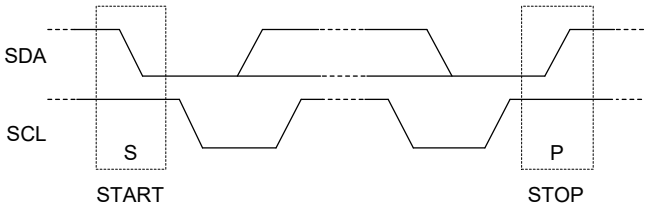


Figure 26. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 27.

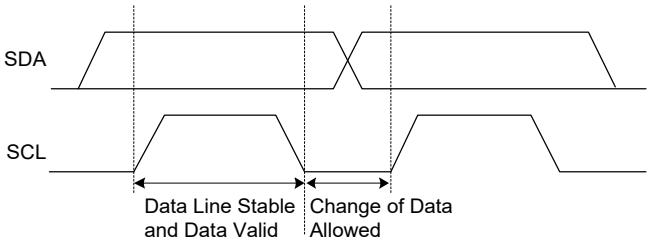


Figure 27. I²C Bus Bit Transfer

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start).

Write

An I²C write transaction consists of four bytes. The first byte includes the 7-bit slave address and Write bit. The second byte defines the register address. The third byte provides the 8-bit LSB. The fourth byte provides the 8-bit MSB of the 16-bit register data.

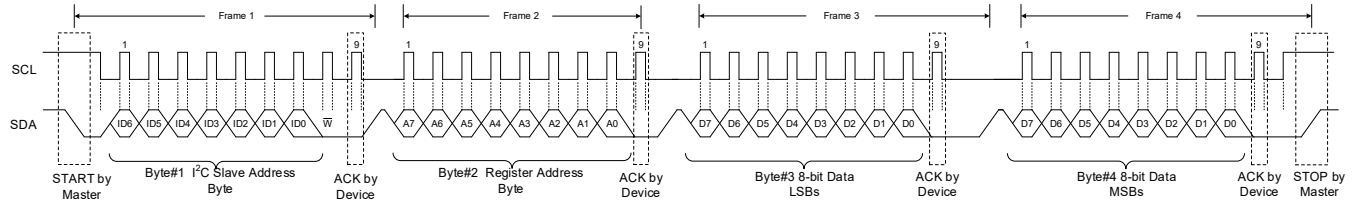


Figure 28. Write Transaction

DETAILED DESCRIPTION (continued)

Read

A read transaction consists of five bytes. The first byte contains the 7-bit slave address and the Write bit. The second byte specifies the 8-bit register address to be read. The third byte contains the 7-bit slave address and the Read bit. The fourth byte returns the lower 8 bits (LSB) of the 16-bit register data, and the fifth byte returns the upper 8 bits (MSB) of the register data.

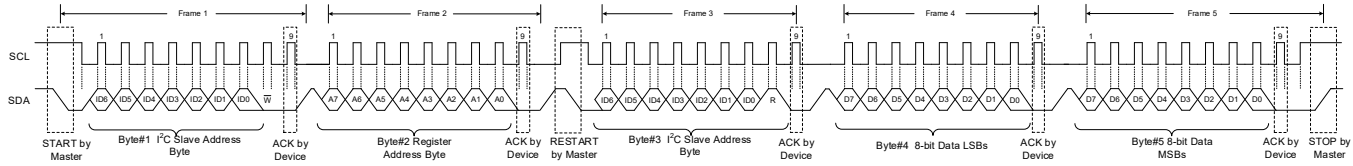


Figure 29. Read Transaction

Configuration Examples through I²C

The SGM37461Q does not require any serial interface configuration. It can be simply controlled with the EN pin and PWM pin. Most of the device configuration is accomplished using external resistor values. If I²C interface is available, then extended configuration is possible. The configuration registers can be written from Standby state to Normal state as shown in Table 8.

Table 8. Configuration Registers

Register Bits Name	Function
BRT_MODE[1:0] & DISPLAY_BRT[15:0]	Select DISPLAY_BRT[15:0] register or PWM input for brightness control. BRT_MODE[1:0] = 2h for internal I²C brightness control.
LED_CURRENT[11:0]	Control the maximum LED current for LED outputs.
SPREAD_PSEUDO_EN & SPREAD_MOD_FREQ1[1:0] & SPREAD_MOD_FREQ2[1:0] SPREAD_RANGE[1:0]	Configure the spread spectrum function of Boost.
SLOPE_SELECT[2:0] & ADV_SLOPE_ENABLE	Configure the slope mode and duration for LED current.
DITHER_SELECT[2:0]	Select PWM dither mode for added dimming resolution.
EN_LED_GND_DETECT	Configure the LED short to ground detection.
LEDx_SHORT_DISABLE	Configure the LED internal short detection.

Fault Interrupts Status and Clearing

The SGM37461Q provides an INT pin to notify the host when a fault event occurs. When the I²C interface is available, the detected fault information can be read through the interrupt fault status registers. The fault status bits are located in the SUPPLY_STATUS, BOOST_STATUS, and LED_STATUS registers.

Each fault interrupt contains a STATUS bit and a CLEAR bit. The STATUS bit indicates the detected fault, while the CLEAR bit is used to clear the latched interrupt status. To clear a fault interrupt, write "1" to both the STATUS bit and CLEAR bit in the same write operation. After the fault status is cleared, the corresponding INT pin status is pulled high.

Fault Interrupt Configuration

Most of the SGM37461Q fault events are enabled to generate an interrupt through the INT pin. Each fault interrupt is controlled by a 2-bit INT_EN setting located in the SUPPLY_INT_EN, BOOST_INT_EN, and LED_INT_EN registers. When the INT_EN setting reads 0b10, the corresponding fault event will assert the INT pin.

To make the interrupt enable, write 0b11 to interrupt enable bits. To make the interrupt disable, write 0b01 to interrupt enable bits. A global interrupt enable control is also provided to disable all fault interrupts from asserting the INT pin.

REGISTER MAPS

Registers Map

The register map defines the memory-mapped registers used for device configuration, control and status monitoring. The table below lists all supported registers and their corresponding addresses. Reserved register addresses and bits must not be modified.

All registers are 16-bit and individual bits are named from D[0] (LSB) to D[15] (MSB).

I^2C Slave Address of SGM37461Q: 0x2A (0b0101010 + R/W)/0x2B (0b0101011 + R/W)

REG	DEFAULT VALUE	REGISTER NAME	DESCRIPTION
0x00	0x0000	BRT_CONTROL	Internal Brightness Control
0x02	0x0FFF	LED_CURR_CONFIG	LED Current Setting
0x04	0x08A3	USER_CONFIG1	User Configuration Register 1
0x06	0x0100	USER_CONFIG2	User Configuration Register 2
0x08	0x2AAA	SUPPLY_INT_EN	Supply Interrupt Control
0x0A	0xA028	BOOST_INT_EN	Boost Interrupt Control
0x0C	0x00AA	LED_INT_EN	LED Interrupt Control
0x0E	0x0000	SUPPLY_STATUS	Supply Fault Status
0x10	0x0000	BOOST_STATUS	Boost Fault Status
0x12	0x0000	LED_STATUS	LED Fault Status
0x14	0x0000	FSM_DIAGNOSTICS	Device State Diagnostics
0x16	0x0000	PWM_INPUT_DIAGNOSTICS	PWM Input Duty Cycle Diagnostics
0x18	0x0000	PWM_OUTPUT_DIAGNOSTICS	PWM Output Duty Cycle Diagnostics
0x1A	0x0000	LED_CURR_DIAGNOSTICS	Actual LED Current Diagnostics
0x1C	0x0000	ADAPT_BOOST_DIAGNOSTICS	Adaptive Boost Control Diagnostics
0x1E	0x0000	AUTO_DETECT_DIAGNOSTICS	Device Configuration Diagnostics
0x20	0xFF00	USER_CONFIG3	User Configuration Register 3

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Read clears the bit
R/WC: Read/Write bit(s). Writing a ‘1’ clears the bit. Writing a ‘0’ has no effect.

REGISTER MAPS (continued)

REG0x00: BRT_CONTROL Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:0]	DISPLAY_BRT[15:0]	R/W	0h	16-bit Internal Display Brightness Control Register	POR-Reset

REG0x02: LED_CURR_CONFIG Register [Reset = 0x0FFF]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:12]	RESERVED	R/W	0h	Reserved bits	
D[11:0]	LED_CURRENT[11:0]	R/W	FFFh	LED current control for all LED outputs	POR-Reset

REG0x04: USER_CONFIG1 Register [Reset = 0x08A3]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15]	RESERVED	R/W	0h	Reversed bit	
D[14]	SPREAD_PSEUDO_EN	R/W	0h	Pseudo-Random Spread Spectrum Enable Bit 0h = Pseudo random SS disabled (default) 1h = Pseudo random SS enabled	POR-Reset
D[13:12]	SPREAD_MOD_FREQ1[1:0]	R/W	0h	Boost Spread Spectrum Modulation Frequency Setting Bits. Determine the modulation frequency together with SPREAD_MOD_FREQ2[1:0] 0h = 200Hz (default) 1h = 500Hz 2h = 800Hz 3h = 1.2kHz	POR-Reset
D[11:10]	SPREAD_RANGE[1:0]	R/W	2h	Boost Spread Spectrum Range Setting Bits 0h = 3.3% 1h = 4.3% 2h = 5.3% (default) 3h = 7.2%	POR-Reset
D[9:8]	BRT_MODE[1:0]	R/W	0h	LED Brightness Control Bits 0h = Brightness controlled by PWM input (default) 1h = Reserved 2h = Brightness controlled by DISPLAY_BRT[15:0] register 3h = Reserved	POR-Reset
D[7:5]	SLOPE_SELECT[2:0]	R/W	5h	Brightness Sloper Duration Select Bits 0h = Disabled 1h = 1ms 2h = 2ms 3h = 50ms 4h = 100ms 5h = 200ms (default) 6h = 300ms 7h = 500ms Times are for linear slope mode. Advanced sloper will increase durations about 50ms while adding additional smoothing to brightness transitions. It is recommended to use 1ms and 2ms sloper times only in linear mode.	POR-Reset
D[4:2]	DITHER_SELECT[2:0]	R/W	0h	Dither Mode Select Bits 0h = Dither Disabled (default) 1h = 1-bit dither 2h = 2-bit dither 3h = 3-bit dither 4h = 4-bit dither	POR-Reset
D[1]	ADV_SLOPE_ENABLE	R/W	1h	Sloper Mode Selection Bit 0h = Linear sloping 1h = Advanced sloping (default)	POR-Reset
D[0]	RESERVED	R/W	1h	Reserved bit	

REGISTER MAPS (continued)

REG0x06: USER_CONFIG2 Register [Reset = 0x0100]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:9]	RESERVED	R/W	0h	Reserved bits	
D[8]	EN_LED_GND_DETECT	R/W	1h	LED Short-to-Ground Detection Enable Bit during Boost Soft-Start and Normal Operation 0h = Disable 1h = Enable (default)	POR-Reset
D[7:6]	RESERVED	R/W	0h	Reserved bits	
D[5]	LED6_SHORT_DISABLE	R/W	0h	LED 6 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset
D[4]	LED5_SHORT_DISABLE	R/W	0h	LED 5 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset
D[3]	LED4_SHORT_DISABLE	R/W	0h	LED 4 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset
D[2]	LED3_SHORT_DISABLE	R/W	0h	LED 3 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset
D[1]	LED2_SHORT_DISABLE	R/W	0h	LED 2 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset
D[0]	LED1_SHORT_DISABLE	R/W	0h	LED 1 Internal Short Fault Disable Bit 0h = Enable (default) 1h = Disable	POR-Reset

REGISTER MAPS (continued)

REG0x08: SUPPLY_INT_EN Register [Reset = 0x2AAA]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:14]	RESERVED	R/W	0h	Reserved bits	
D[13:12]	BSTSYNC_INT_EN[1:0]	R/W	2h	Missing Boost SYNC Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[11:10]	CP_INT_EN[1:0]	R/W	2h	Charge Pump Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[9:8]	CPCAP_INT_EN[1:0]	R/W	2h	Charge Pump Cap Missing Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[7:6]	VINOCP_INT_EN[1:0]	R/W	2h	V_{IN} Over-Current Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[5:4]	VDDUVLO_INT_EN[1:0]	R/W	2h	V_{DD} Under-Voltage Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[3:2]	VINOVP_INT_EN[1:0]	R/W	2h	V_{IN} Over-Voltage Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[1:0]	VINUVLO_INT_EN[1:0]	R/W	2h	V_{IN} Under-Voltage Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset

REGISTER MAPS (continued)

REG0x0A: BOOST_INT_EN Register [Reset = 0xA028]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:14]	TSD_INT_EN[1:0]	R/W	2h	Thermal Shutdown Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[13:12]	ISET_INT_EN[1:0]	R/W	2h	ISET Resistor Short-to-Ground Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[11:10]	LEDSET_INT_EN[1:0]	R/W	0h	Missing LED_SET Resistor Interrupt Enable Read: 0h = Interrupt is currently disabled (default) 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[9:8]	MODE_INT_EN[1:0]	R/W	0h	Missing MODE Resistor Interrupt Enable Read: 0h = Interrupt is currently disabled (default) 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[7:6]	FSET_INT_EN[1:0]	R/W	0h	Missing FSET Resistor Interrupt Enable Read: 0h = Interrupt is currently disabled (default) 2h = Interrupt is currently enabled Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[5:4]	BSTOCP_INT_EN[1:0]	R/W	2h	Boost Over-Current Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[3:2]	BSTOVPH_INT_EN[1:0]	R/W	2h	Boost Over-Voltage High Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[1:0]	Reserved	R/W	0h	Reserved bits	

REGISTER MAPS (continued)

REG0x0C: LED_INT_EN Register [Reset = 0x00AA]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:8]	RESERVED	R/W	0h	Reserved bits	
D[7:6]	GLOBAL_INT_EN[1:0]	R/W	2h	Global Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[5:4]	I2C_ERROR_INT_EN[1:0]	R/W	2h	I²C Time Out Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[3:2]	INVSTRING_INT_EN[1:0]	R/W	2h	Invalid LED String Configuration Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset
D[1:0]	LED_INT_EN[1:0]	R/W	2h	LED Open/Internal Short/Short-to-GND Interrupt Enable Bits Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled (default) Write: 1h = Disable interrupt 3h = Enable interrupt	POR-Reset

REGISTER MAPS (continued)

REG0x0E: SUPPLY_STATUS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15]	CRCERR_STATUS	R/W	0h	CRC Error Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[14]	CRCERR_CLEAR	R/WC	0h	CRC Error Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[13]	BSTSYNC_STATUS	R/W	0h	Missing Boost Sync Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[12]	BSTSYNC_CLEAR	R/WC	0h	Missing Boost Sync Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[11]	CP_STATUS	R/W	0h	Charge Pump Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[10]	CP_CLEAR	R/WC	0h	Charge Pump Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[9]	CPCAP_STATUS	R/W	0h	Missing Charge Pump Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[8]	CPCAP_CLEAR	R/WC	0h	Missing Charge Pump Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[7]	VINOCP_STATUS	R/W	0h	VIN Over-Current Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[[6]	VINOCP_CLEAR	R/WC	0h	V_{IN} Over-Current Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[5]	VDDUVLO_STATUS	R/W	0h	V_{DD} Under-Voltage Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[4]	VDDUVLO_CLEAR	R/WC	0h	V_{DD} Under-Voltage Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[3]	VINOVP_STATUS	R/W	0h	VIN Over-Voltage Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[2]	VINOVP_CLEAR	R/WC	0h	V_{IN} Over-Voltage Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[1]	VINUVLO_STATUS	R/W	0h	V_{IN} Under-Voltage Fault Status 0h = No fault (default) 1h = Fault	POR-Reset
D[0]	VINUVLO_CLEAR	R/WC	0h	V_{IN} Under-Voltage Fault Clear Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset

REGISTER MAPS (continued)

REG0x10: BOOST_STATUS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15]	TSD_STATUS	R/W	0h	Thermal Shutdown Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[14]	TSD_CLEAR	R/WC	0h	Thermal Shutdown Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[13]	ISET_STATUS	R/W	0h	ISET Resistor Short-to-Ground Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[12]	ISET_CLEAR	R/WC	0h	ISET Resistor Short-to-Ground Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[11]	LEDSET_STATUS	R/W	0h	Missing LED Resistor Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[10]	LEDSET_CLEAR	R/WC	0h	Missing LED Resistor Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[9]	MODESEL_STATUS	R/W	0h	Missing MODE SEL Resistor Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[8]	MODESEL_CLEAR	R/WC	0h	Missing MODE SEL Resistor Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[7]	FSET_STATUS	R/W	0h	Missing Boost FSET Resistor Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[6]	FSET_CLEAR	R/WC	0h	Missing Boost FSET Resistor Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[5]	BSTOCP_STATUS	R/W	0h	Boost Over-Current Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[4]	BSTOCP_CLEAR	R/WC	0h	Boost Over-Current Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[3]	BSTOVPH_STATUS	R/W	0h	Boost OVP High Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[2]	BSTOVPH_CLEAR	R/WC	0h	Boost OVP High Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[1]	BSTOVPL_STATUS	R/W	0h	Boost OVP Low Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[0]	BSTOVPL_CLEAR	R/WC	0h	Boost OVP Low Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset

REGISTER MAPS (continued)

REG0x12: LED_STATUS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15]	RESERVED	R/W	0h	Reserved bit	
D[14]	I2C_ERROR_STATUS	R/W	0h	I^2C Time Out Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[13]	I2C_ERROR_CLEAR	R/WC	0h	I^2C Time Out Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[12]	INVSTRING_STATUS	R/W	0h	Invalid String Configuration Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[11]	INVSTRING_CLEAR	R/WC	0h	Invalid String Configuration Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[10]	LED_STATUS	R/W	0h	LED Open/Internal Short/Short-to-GND Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[9]	LED_CLEAR	R/WC	0h	LED Open/Internal Short/Short-to-GND Fault Clear Bit Write "1" to both status indication bit and clear bit in the same write operation to clear corresponding fault status and INT pin status.	POR-Reset
D[8]	GND_LED	R	0h	LED Short-to-GND Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[7]	SHORT_LED	R	0h	LED Internal Short Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[6]	OPEN_LED	R	0h	LED Open Fault Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[5]	LED6_FAULT	R	0h	LED 6 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[4]	LED5_FAULT	R	0h	LED 5 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[3]	LED4_FAULT	R	0h	LED 4 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[2]	LED3_FAULT	R	0h	LED 3 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[1]	LED2_FAULT	R	0h	LED 2 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset
D[0]	LED1_FAULT	R	0h	LED 1 Status Indication Bit 0h = No fault (default) 1h = Fault	POR-Reset

REGISTER MAPS (continued)

REG0x14: FSM_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:5]	RESERVED	R	0h	Reserved bits	
D[4:0]	FSM_LIVE_STATUS[4:0]	R	0h	State Bit that Indicates the Current Status 0h = DISABLED (default) 1h = LDO_STARTUP 2h = OTP_READ 3h = STANDBY 4h - Fh = BOOST_STARTUP 10h = NORMAL 11h = SHUTDOWN 12h = FAULT_RECOVERY 13h = ALL_LED_FAULT	POR-Reset

REG0x16: PWM_INPUT_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:0]	PWM_INPUT_STATUS [15:0]	R	0h	16-bit value for detected duty cycle of PWM input signal	POR-Reset

REG0x18: PWM_OUTPUT_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:0]	PWM_OUTPUT_STATUS [15:0]	R	0h	16-bit code that corresponds to the duty cycle of PWM output	POR-Reset

REG0x1A: LED_CURR_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:12]	RESERVED	R	0h	Reserved bits	
D[11:0]	LED_CURRENT_STATUS [11:0]	R	0h	12-bit current DAC code that corresponds to the actual LED current of all the active outputs	POR-Reset

REG0x1C: ADAPT_BOOST_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:11]	RESERVED	R	0h	Reserved bits	
D[10:0]	IBSTFB_STATUS[10:0]	R	0h	11-bit Boost voltage code that adaptive voltage control loop used to control the Boost output	POR-Reset

REGISTER MAPS (continued)

REG0x1E: AUTO_DETECT_DIAGNOSTICS Register [Reset = 0x0000]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15]	RESERVED	R	0h	Reserved bit	
D[14:12]	AUTO_PWM_ FREQ_SEL[2:0]	R	0h	LED PWM Frequency Configuration Bits by PWM_SEL Pin Resistor 0h = 152Hz (default) 1h = 305Hz 2h = 610Hz 3h = 1221Hz 4h = 2441Hz 5h = 4883Hz 6h = 9766Hz 7h = 19531Hz	POR-Reset
D[11]	RESERVED	R	0h	Reserved bit	
D[10:8]	AUTO_LED_STRING_CFG	R	0h	LED String Configuration Bits by LED_SET Pin Resistor 0h = 6 separate LED strings (default) 1h = 5 separate LED strings 2h = 4 separate LED strings 3h = 3 separate LED strings 4h = 2 separate LED strings 5h = 6 outputs configured as 3 groups to drive 3 LED strings 6h = 6 outputs configured as 2 groups to drive 2 LED strings. 7h = 6 outputs connected together to drive 1 LED string	POR-Reset
D[7:6]	RESERVED	R	0h	Reserved bits	
D[5:3]	AUTO_BOOST_ FREQ_SEL[2:0]	R	0h	Boost Switching Frequency Configuration Bits by PWM_FSET Pin Resistor 0h = 100kHz (default) 1h = 200kHz 2h = 303kHz 3h = 400kHz 4h = 500kHz 5h = 1818kHz 6h = 2000kHz 7h = 2222kHz	POR-Reset
D[2:0]	MODE_SEL[2:0]	R	0h	LED Dimming Mode and I^2C Address Configuration Bits by MODE Pin Resistor 0h = Phase shift PWM mode, I^2C address: 0x2B (default) 1h = Hybrid dimming mode, I^2C address: 0x2B 2h = Current dimming mode, I^2C address: 0x2B 3h = Direct PWM mode, I^2C address: 0x2B 4h = Phase shift PWM mode, I^2C address: 0x2A 5h = Hybrid dimming mode, I^2C address: 0x2A 6h = Current dimming mode, I^2C address: 0x2A 7h = Direct PWM mode, I^2C address: 0x2A	POR-Reset

REGISTER MAPS (continued)

REG0x20: USER_CONFIG3 Register [Reset = 0xFF00]

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION	RESET BY
D[15:6]	RESERVED	R	3FCh	Reserved bits	
D[5:4]	HYBRID_TRANS_TH[1:0]	R/W	0h	Select the hybrid mode transition threshold between PWM dimming and current dimming 0h = 12.5% (default) 1h = 12.5% 2h = 12.5% 3h = 0, pure current dimming	POR-Reset
D[3:2]	SPREAD_MOD_FREQ2[1:0]	R/W	0h	Boost Spread Spectrum Modulation Frequency Setting Bits. Determine the modulation frequency together with SPREAD_MOD_FREQ1[1:0]. 0h = use the configuration of SPREAD_MOD_FREQ1[1:0] (default) 1h = 10kHz 2h = 20kHz 3h = 22kHz	POR-Reset
D[1]	VBOOST_INIT	R/W	0h	Select the Preset Voltage of Boost Output at Boost Soft-Start Operation 0h = 88% of the Boost output's adjustable range (default) 1h = 66% of the Boost output's adjustable range	POR-Reset
D[0]	IUVLO_SELECT	R/W	0h	IUVLO Select Bit 0h = 4μA (default) 1h = 1μA	POR-Reset

APPLICATION INFORMATION

The SGM37461Q is designed for automotive applications like infotainment and center displays. The input of SGM37461Q is connected to the vehicle battery. The SGM37461Q offers the power-line FET control. The device supports both Boost and SEPIC operations depending on the input voltage range. The device offers flexible configuration through external components and I^2C interface. It supports standalone operation without I^2C.

Typical Applications

Full Function Application

Figure 30 shows the full function application circuit when I^2C interface is used. The external P-MOSFET prevents the LED output from being directly connected to the vehicle battery. The integrated charge pump is adopted to provide sufficient gate drive voltage for the external N-MOSFET when the VDD supply is insufficient. The voltage of BST_SYNC pin is pulled up to V_{DD} so the spread spectrum function is enabled. It is recommended to add a small capacitor (e.g. 100pF) from SCL and SDA pins to AGND when direct PWM mode is adopted. For applications where the LEDs are located far from the SGM37461Q, a small capacitor (e.g., 500pF to 1nF) from each OUTx pin to GND is recommended. Typically, the VSENSE_P pin is connected to input. The valid input voltage is limited by the V_{IN} over-voltage (42.3V, TYP) protection. To further extend the input voltage range to 48 V, VSENSE_P and VSENSE_N should be tied to GND. In this case, the V_{IN} over-voltage protection and V_{IN} over-current protection are disabled.

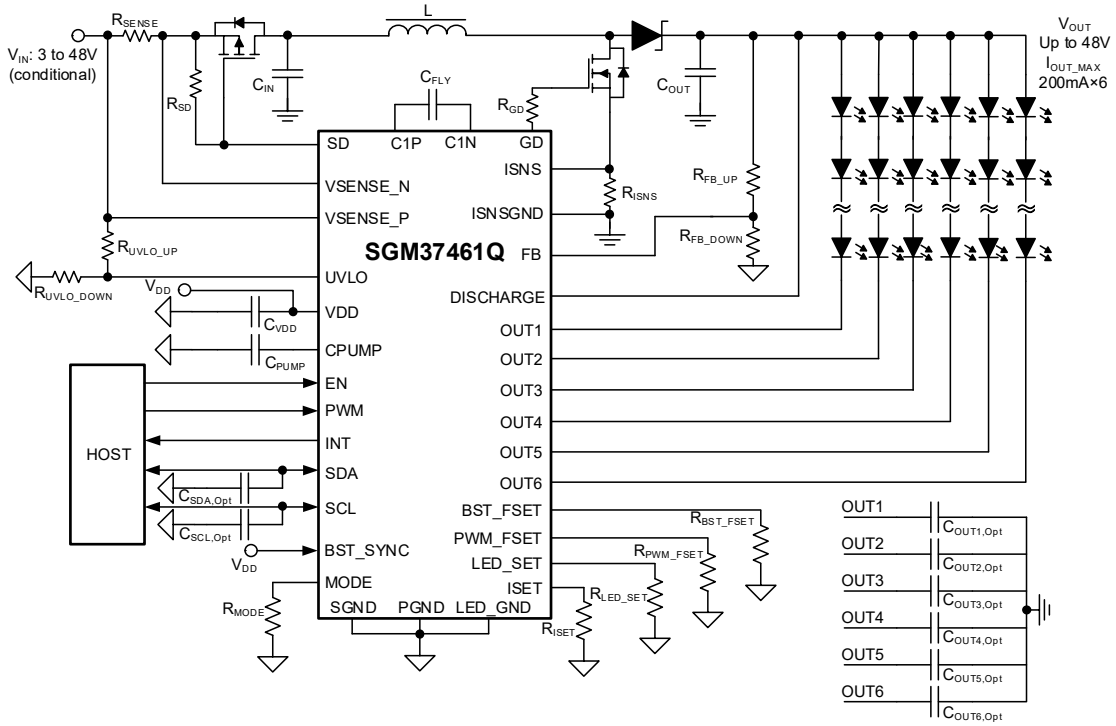


Figure 30. Circuit for Full Function Application

APPLICATION INFORMATION (continued)

Design Consideration

Input Capacitor Selection

The input capacitor is a key component in the minimization of power supply surge currents and the reduction of switching noise. Input capacitance must ensure enough filtering for input power. For optimal performance, ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and stable temperature characteristics. In most cases, a 10μF ceramic capacitor is sufficient. A 33μF damping electrolytic capacitor is recommended at the input to reduce LC resonance and suppress input voltage ringing.

Inductor Selection

There are some considerations for inductor selection, including the rated current, expected output voltage ripple and inductor current ripple. Using a larger inductance value helps to reduce ripple, lower peak inductor current but comes with downsides like bigger size and higher resistance. Select the minimum inductor to ensure the system works in continuous conduction mode in most case. The required inductance value can be determined as below:

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (11)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (12)$$

where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} represents the LED current, and η represents the overall system efficiency.

Table 9 lists the recommended inductor values for different switching frequency. The inductor selection should consider the trade-off between inductor size, cost, and current ripple based on the specific application requirements.

Table 9. Recommended Inductance Values for Different Switching Frequency

Switching Frequency (kHz)	Inductance (μH)
100	22
200	22
303	10
400	10
500	10
1818	10
2000	10
2222	10

A low-DCR inductor is recommended to achieve higher efficiency. For optimum performance, select an inductor with a DC current rating at least 25% greater than the peak input current. The maximum inductor current can be calculated as below:

$$I_{L(PEAK)} = \frac{V_{OUT} \times I_{LOAD}}{\eta \times V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times f_{SW} \times V_{OUT}} \quad (13)$$

where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} represents the LED current, and η represents the overall system efficiency.

Diode Selection

A Schottky diode is required for the Boost output diode. The diode current rating should be at least 25% higher than the maximum output current. A Schottky diode with low forward voltage drop and fast switching capability is recommended to improve efficiency. The reverse breakdown voltage rating should provide sufficient margin above the maximum Boost output voltage, with at least 25% higher voltage rating recommended.

APPLICATION INFORMATION (continued)

Output Capacitor Selection

The output capacitor voltage rating should be at least 50% higher than the maximum output voltage. Capacitance affects voltage ripple and Boost stability, but the DC bias effect can reduce actual capacitance by up to 80%. A target effective capacitance of 50μF is recommended for optimal phase and gain margin. Two 10μF ceramic capacitors in parallel with a 33μF damping electrolytic capacitor are recommended at the output. X5R or X7R ceramic capacitors are recommended for their low ESR characteristics and good temperature performance.

Charge Pump Output Capacitor Selection

A 4.7μF ceramic capacitor with 10V voltage rating is recommended.

Charge Pump Flying Capacitor Selection

A 2.2μF ceramic capacitor with 10V voltage rating is recommended. Connect it between C1P and C1N pins.

Switching FET Selection

The Boost MOSFET should be selected based on voltage rating, current rating, R_{DSON}, switching performance and thermal capability. The voltage rating must provide more than 25% margin above the maximum switch voltage, including voltage spikes. The current rating should be higher than the maximum peak switch current to ensure reliable operation. A low R_{DSON} MOSFET is preferred to reduce conduction loss and improve efficiency. A gate resistor R_{GD} is recommended between the GD pin and MOSFET gate to control the MOSFET turn-on and turn-off slew rate. The gate resistor provides flexibility to optimize the trade-off between switching loss and EMC performance. A higher R_{GD} reduces switching speed and ringing but may increase switching loss, while a lower R_{GD} improves efficiency but may increase EMI and voltage overshoot.

Power-Line FET Selection

The power-line FET provides input power protection by disconnecting the input supply from the Boost controller. It prevents some extreme events like Boost output shorted to GND. A P-MOSFET should be used as the power-line FET in SGM37461Q LED display application. The power-line MOSFET selection should consider voltage rating, current rating and R_{DSON}. Because the power-line MOSFET is continuously turned on during normal operation, low R_{DSON} is critical for reducing conduction loss. The voltage and current ratings should provide 25% margin to ensure reliable operation under maximum input voltage and current conditions. It is recommended to add a 20kΩ resistor between the gate and source of the P-MOSFET.

Input Current Sense Resistor

A sense resistor (R_{SENSE}) is used to monitor the Boost input current. The over-current protection is triggered when the voltage across R_{SENSE} reaches 220mV (TYP). A 20mΩ resistor typically sets the input current limit to 11A. The self-heating effect of the resistor should be considered, as temperature-induced resistance variation may impact current-limit accuracy. A low-TCR sense resistor is recommended for stable operation. The sense resistor package should be selected based on the expected power dissipation.

Boost Sense Resistor

The MOSFET current sense resistor sets the cycle-by-cycle current limit. To minimize sensing loss, the value of R_{ISNS} should not be too high. A R_{ISNS} value ranging from 20mΩ to 50mΩ can satisfy the current-limit requirements for most applications while maintaining a good balance between protection level and sensing power loss. The value of R_{ISNS} can be calculated from the expected cycle-by-cycle current limit.

$$R_{ISNS} = \frac{200mV}{I_{BOOST_OCP}} \quad (14)$$

where, I_{BOOST_OCP} represents the Boost cycle-by-cycle current limit.

APPLICATION INFORMATION (continued)

Basic Function Application

Figure 31 shows the basic function application circuit when I^2C interface is unused. The basic function application minimizes cost and PCB area by eliminating the charge pump and external P-MOSFET. In this configuration, the 5V V_{DD} supply is connected directly to the CPUMP pin. The voltage of BST_SYNC pin is pulled up to VDD so the spread spectrum function is enabled. SCL and SDA pin is also pulled up to V_{DD} to disable I^2C interface. It is recommended to retain the R_{SENSE} and R_{UVLO} to maintain complete protection. For further cost reduction, R_{SENSE} can be eliminated by shorting VSENSE_N and VSENSE_P to V_{IN}. R_{UVLO_UP} and R_{UVLO_DOWN} can be eliminated by connecting UVLO to V_{IN}.

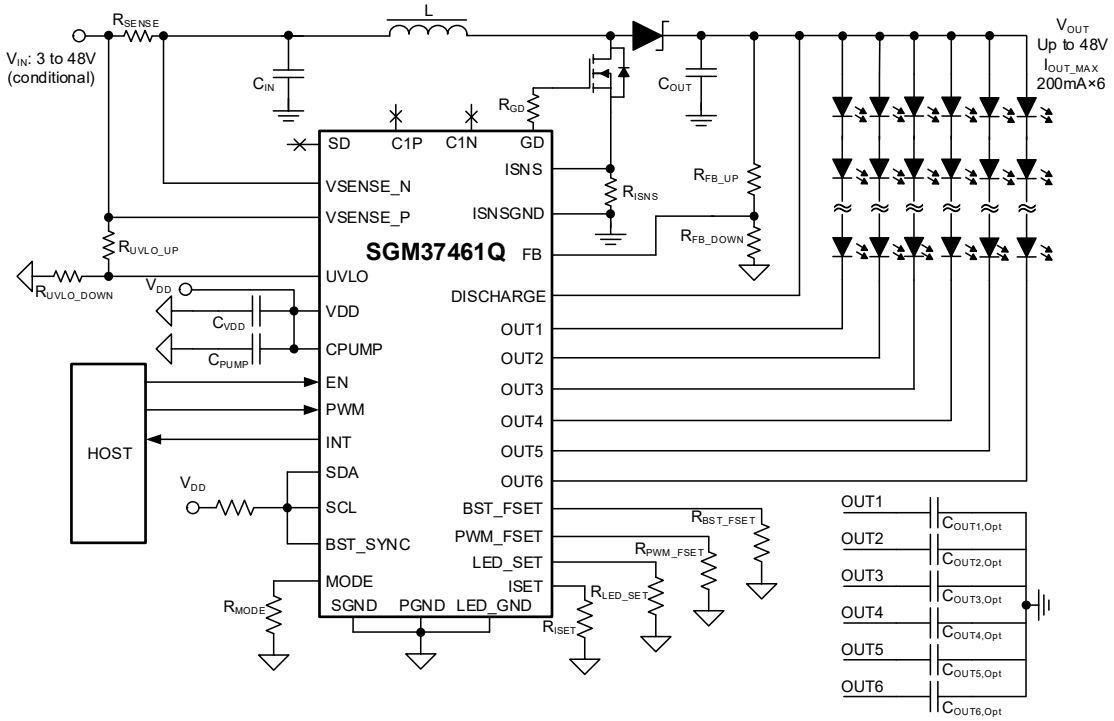


Figure 31. Circuit for Basic Function Application

APPLICATION INFORMATION (continued)

SEPIC Mode Application

SEPIC mode allows the device to regulate the output voltage above or below the input voltage, making it suitable for wide input voltage automotive applications. SEPIC mode is recommended for applications where V_{IN} is close to V_{OUT} and subject to wide voltage variations. It provides stable output regulation under both Boost and Buck conditions.

SEPIC mode has higher switch voltage stress and lower efficiency compared with Boost mode. Higher voltage-rated components are required, and additional components may increase system cost and reduce efficiency.

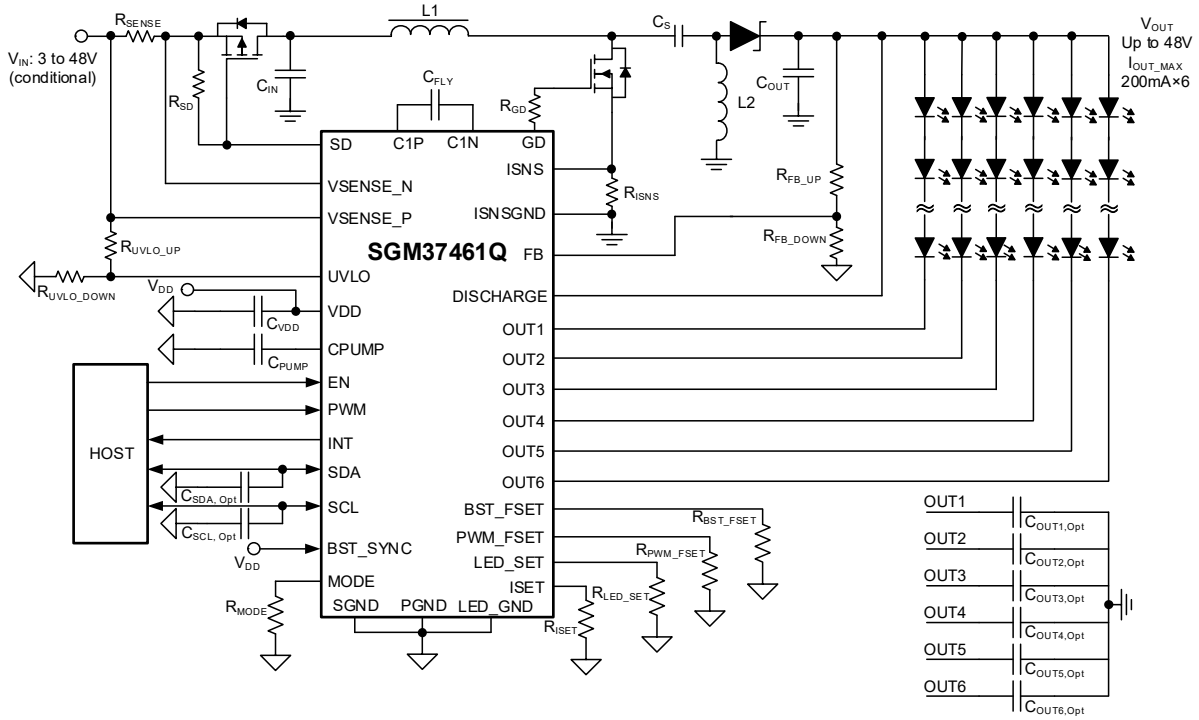


Figure 32. Circuit for SEPIC Mode with Four LEDs in Series

APPLICATION INFORMATION (continued)

Design Consideration

SEPIC Inductor Selection

The inductor value should be selected to achieve an inductor peak-to-peak ripple current of approximately 25% to 40% of the maximum input current at minimum V_{IN}. So the inductor value can be calculated by Equation 15.

$$L_1 = L_2 = L = \frac{V_{IN(MIN)}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (15)$$

$$\Delta I_L = I_{IN} \times 30\% = I_{OUT} \times \frac{V_{OUT}}{V_{IN(MIN)}} \times 30\% \quad (16)$$

where, $V_{IN(MIN)}$ represents the minimum input voltage, ΔI_L represents the peak-to-peak ripple current of inductor, f_{SW} represents the switching frequency, D_{MAX} represents the duty cycle at the $V_{IN(MIN)}$.

Table 10 lists the recommended inductor values for different switching frequency. The inductor selection should consider the trade-off between inductor size, cost and current ripple based on the specific application requirements.

Table 10. Inductance Values for SEPIC Switching Frequencies

Switching Frequency (kHz)	Inductance (μH)
100	22
200	15
303	10
400	10
500	10
1818	4.7
2000	4.7
2222	4.7

The inductor current rating should exceed the maximum inductor peak current by at least 25%. The maximum inductor peak current can be calculated by Equation 17:

$$I_{L1(PEAK)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN(MIN)}} \times \left(1 + \frac{40\%}{2}\right) \quad (17)$$

where, I_{OUT} represents the maximum output current, V_{OUT} represents the output voltage, V_D represents the diode forward voltage, $V_{IN(MIN)}$ represents the minimum input voltage.

$$I_{L2(PEAK)} = I_{OUT} \times \left(1 + \frac{40\%}{2}\right) \quad (18)$$

where, I_{OUT} represents the maximum output current.

SEPIC Coupling Capacitor Selection

The SEPIC coupling capacitor selection requires careful consideration of RMS current capability, voltage rating and capacitance. The capacitor must withstand the high AC current stress in SEPIC operation while maintaining stable controller performance. The capacitor RMS current rating should be at least 25% higher than the calculated RMS current to provide sufficient margin for the maximum operating conditions. The RMS current of coupling capacitor can be calculated as follow:

$$I_{CS(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}} \quad (19)$$

where, I_{OUT} represents the maximum output current, V_{OUT} represents the output voltage, V_D represents the diode forward voltage, $V_{IN(MIN)}$ represents minimum input voltage.

Switching FET Selection

The switching N-MOSFET must withstand a voltage stress of approximately V_{IN} + V_{OUT}. An N-MOSFET with 25% voltage margin above the maximum switch voltage is required. The MOSFET current rating should be higher than the maximum peak switch current, with at least 25% margin recommended to ensure reliable operation.

$$I_{Q1(PEAK)} = I_{L1(PEAK)} + I_{L2(PEAK)} \quad (20)$$

where, $I_{L1(PEAK)}$ represents the peak current for inductor 1, $I_{L2(PEAK)}$ represents the peak current for inductor 2.

Diode Selection

The output diode experiences a reverse voltage stress of approximately $V_{IN(MAX)}$ + V_{OUT}. A diode with a voltage rating at least 25% higher than the maximum reverse voltage is recommended. The average current rating should be 25% higher than the maximum output current, with sufficient margin to handle peak current during transient conditions. Low forward voltage and fast recovery characteristics are preferred to minimize conduction and switching losses. Consequently, a Schottky diode is necessary.

Other Components Selection

Refer to the design consideration of Full Function Application.

APPLICATION INFORMATION (continued)

Layout Guidelines

1. Place a small capacitor (e.g. 10μF) beside the VDD pin to prevent the internal circuit from the noise.

2. Place a charge-pump capacitor beside the PUMP pin and ensure that the bypass capacitors have the close vias to GND. When the charge pump is used, keep the flying capacitor close to the C1N and C1P pin.

3. The Boost input and output capacitors should be close to their respective input and output current loop to minimize the current loop. Put a small high-frequency output capacitor as near as possible to the high-current traces. Keep the inductor – power diode – output capacitors – GND path as short as possible to minimize the high-frequency current loop area and path length.

4. Keep the GND plane intact under high-current Boost traces to minimize return path length and high-frequency current loop area.

5. The external PMOS gate pins should be placed close to the SD pin to minimize the gate trace length and ensure that the gate drive is less susceptible to interference.

6. Place the inductor, N-MOSFET and diode as close as possible. Keep their connecting copper short and wide for minimal power loss and optimal EMI performance. Keep this connecting copper on a single copper layer. Do not use vias to route it across multiple layers.

7. Connect the Boost output voltage to the LED, FB pin and DISCHARGE pins after the output capacitor. Do not route these connections directly from the diode cathode. Place the feedback network as close as possible to the FB pin. A small bypass capacitor can be placed between the FB pin and GND to reduce high-frequency noise. A 47pF capacitor is recommended.

8. The thermal pad of the device must be properly soldered to the PCB for efficient heat dissipation. Use an adequate number of thermal vias beneath the pad to transfer heat to the backside ground plane and improve thermal performance.

9. Use an appropriate number and size of vias in each current path.

10. Connect a 1nF capacitor from OUTx pin to GND if better EMI performance is required.

11. Use ferrite bead at the input and output path to provide high impedance to high-frequency noise for better EMI performance.

12. Put a RC snubber circuit at switch node of Boost to suppress the ringing and overshoot if required.

13. Keep the wires of OUTx as straight as possible at direct PWM mode and phase shift PWM mode.

14. Use narrow traces to “force” the current flow directly through the input filter components. It also prevents the noise coupling and minimizes the parasitic capacitance.

APPLICATION INFORMATION (continued)

Layout Example

Figure 33 shows a layout example for the SGM37461Q to illustrate the recommended layout guidelines. This example can be adapted to the actual application layout where applicable.

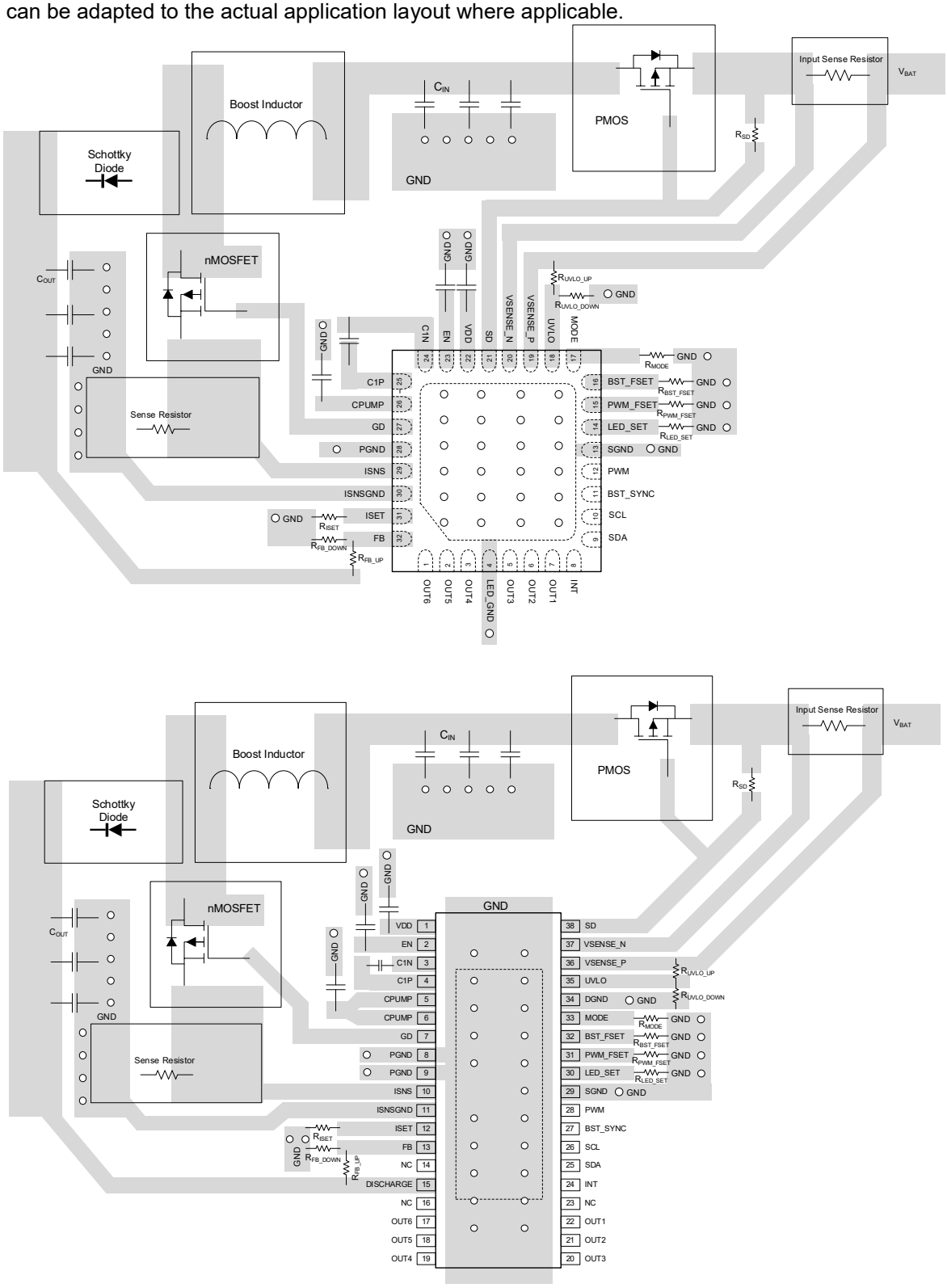


Figure 33. Layout Guidelines

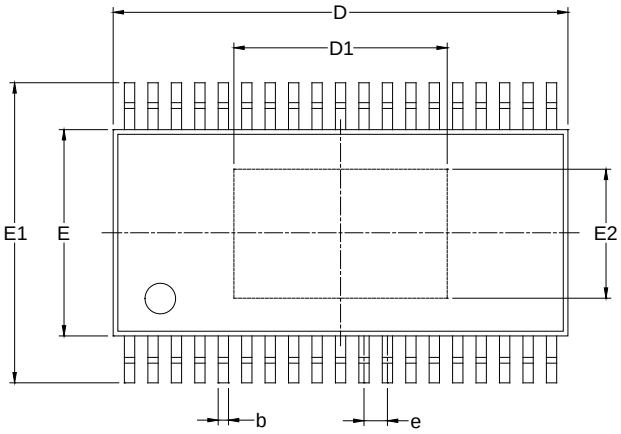
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

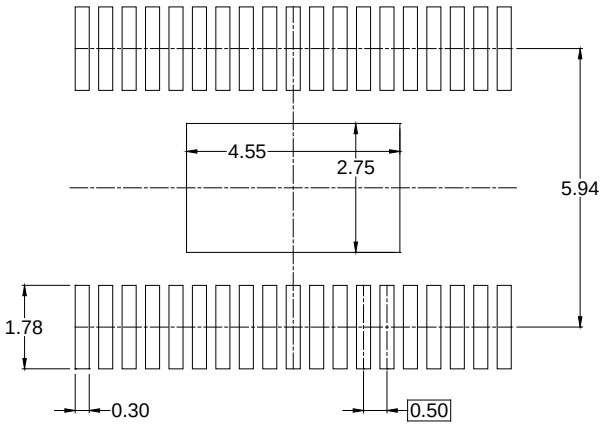
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

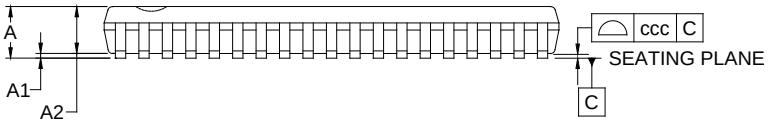
TSSOP-38 (Exposed Pad)

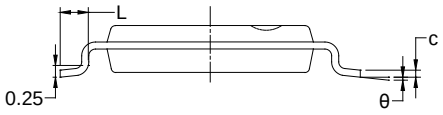


TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



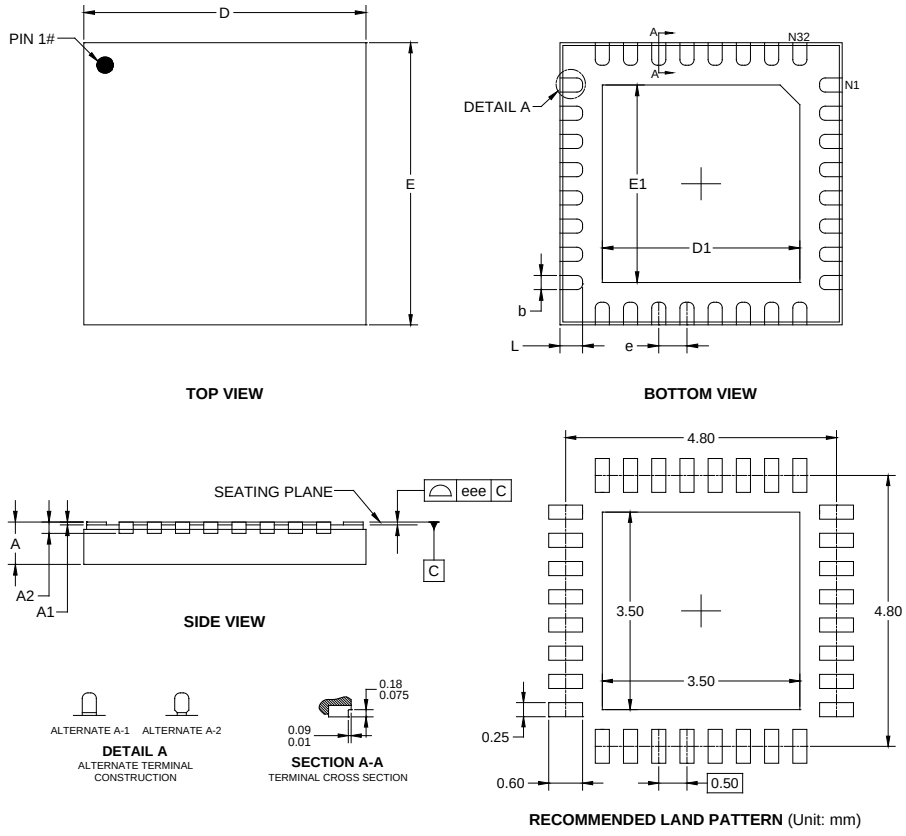


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.050
b	0.170	-	0.270
c	0.090	-	0.200
D	9.600	-	9.800
D1	4.350	-	4.750
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.550	-	2.950
e	0.500 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions, or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

TQFN-5×5-32KL

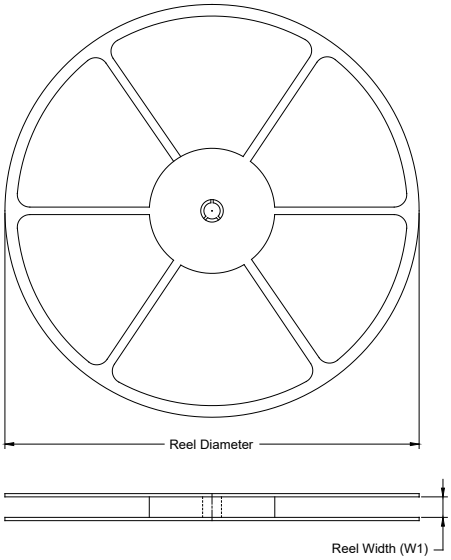


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.200 REF	
b	0.180	-	0.300
D	4.900	-	5.100
D1	3.400	-	3.600
E	4.900	-	5.100
E1	3.400	-	3.600
e		0.500 BSC	
L	0.300	-	0.500
eee		0.080	

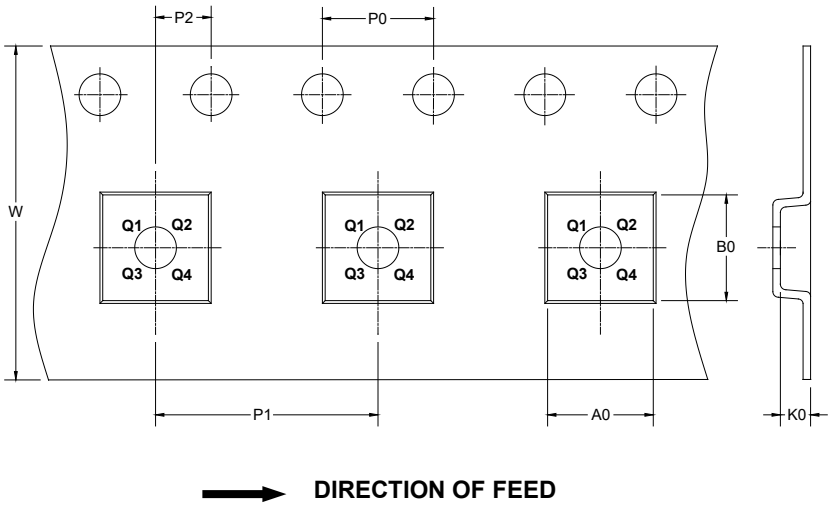
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



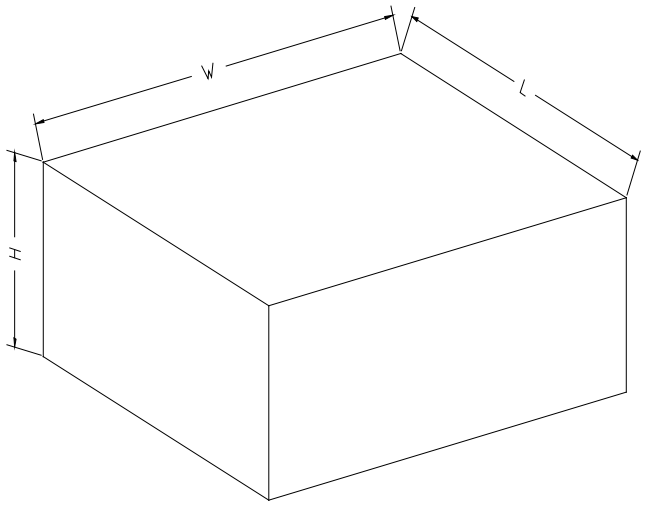
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-38 (Exposed Pad)	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1
TQFN-5×5-32KL	13"	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002