SGM61184
4.5V to 18V Input, 8A, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61184 is an efficient 18V, 8A synchronous Buck DC/DC converter with integrated power MOSFETs and a wide 4.5V to 18V input range. This current mode control device is optimized for high density applications with minimal number of external components. High switching frequency, up to 1600kHz, can be chosen to lessen the solution size by smaller inductor and capacitors.

The peak current mode control with fast transient response makes the loop compensation simple. The high-side MOSFET current and low-side MOSFET sourcing current are cycle-by-cycle limited for overload protection. The hiccup mode limits MOSFET power dissipation if short-circuit or overload keeps appearing.

A power good supervisor circuit monitors the regulator output. When the output voltage is in regulation, the PG open-drain output pin will be in high-impedance state. An internal deglitch time prevents this pin from pulling low unless a fault has occurred. The EN pin can be used to adjust the input UVLO and hysteresis by a resistor divider. The soft-start and tracking pin (SS/TRK) can control the output voltage start-up ramp, which makes the device work as a standalone power supply or work in tracking situations.

The SGM61184 is available in a Green TQFN-3.5×3.5-18AL package.

TYPICAL APPLICATION

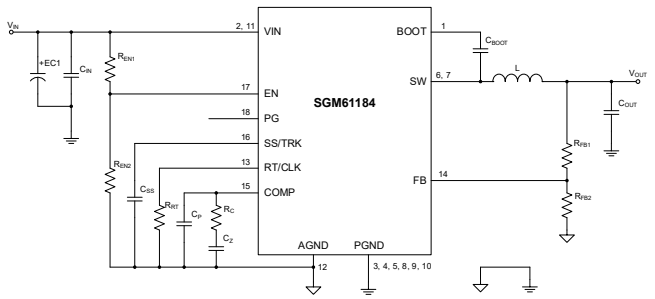


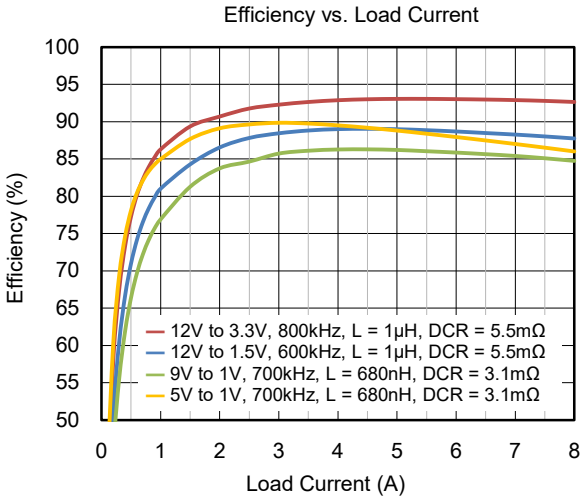
Figure 1. Typical Application Circuit

FEATURES

- **4.5V to 18V Input Voltage Range**
- **0.6V to 12V Output Voltage Range**
- **3.5μA (TYP) Shutdown Current**
- **Integrated R_{DSON} Switches: 8.6mΩ and 4.5mΩ**
- **200kHz to 1600kHz Fixed Switching Frequency**
- **0.6V Internal Voltage Reference**
- **External Clock Synchronization**
- **Peak Current Mode Control with Fast Transient Response**
- **Hiccup Mode Current Limit**
- **Safe Start-Up with Pre-Biased Outputs**
- **Adjustable Soft-Start Time**
- **Power Sequencing Capability**
- **Adjustable Input Under-Voltage Lockout (UVLO)**
- **Power Good Output Monitor for Under-Voltage and Over-Voltage Protections**
- **Non-Latch Thermal Shutdown Protection**
- **Available in a Green TQFN-3.5×3.5-18AL Package**

APPLICATIONS

Test and Measurement Devices
Medical Imaging Equipment
Business Exchange and Server
Wireless Infrastructure
Telecommunications Infrastructure

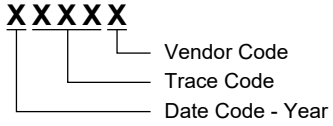


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61184	TQFN-3.5×3.5-18AL	-40℃ to +150℃	SGM61184TTSU18G/TR	SGM057 TTSU18 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN ..... -0.3V to 22V
SW ..... -1V to 22V
SW (10ns Transient) ..... -3V to 23V
EN, SS/TRK, PG, RT/CLK, FB, COMP ..... -0.3V to 6V
BOOT ..... -0.3V to 28V
BOOT to SW ..... -0.3V to 6V
BOOT (10ns Transient) ..... -0.3V to 30V
Package Thermal Resistance
TQFN-3.5×3.5-18AL, θ_{JA} ..... 48℃/W
TQFN-3.5×3.5-18AL, θ_{JB} ..... 7℃/W
TQFN-3.5×3.5-18AL, θ_{JC} ..... 27.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

V_{IN} ..... 4.5V to 18V
V_{OUT} ..... 0.6V to 12V
I_{OUT} ..... 8A (MAX)
f_{SW} ..... 200kHz to 1600kHz
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

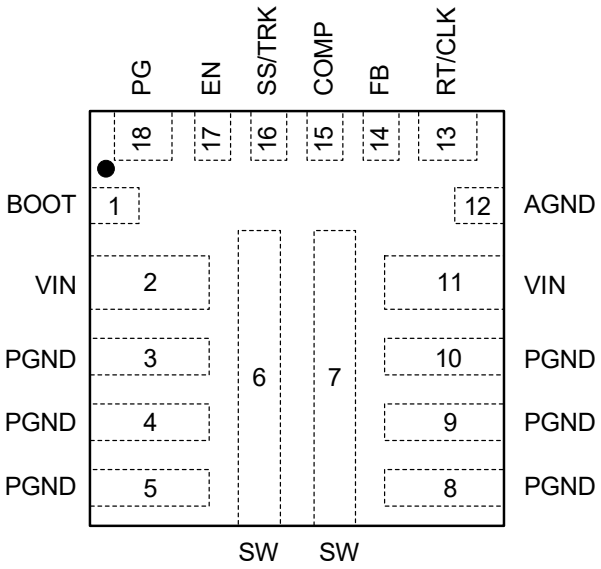
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3.5×3.5-18AL

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	BOOT	I	Bootstrap Input to Supply the High-side Gate Driver. A ceramic capacitor (0.1μF) is required between the BOOT and SW pins.
2, 11	VIN	P	Power Input for the Control Circuitry. The two VIN pins are connected to the input power source with a low-impedance connection. Connect both pins and the adjacent PGND pins.
3, 4, 5, 8, 9, 10	PGND	G	Power Ground. Ground pins return for low-side power MOSFET and its drivers.
6, 7	SW	O	Switching Node. Connect to the source of the high-side MOSFET and drain of the low-side MOSFET.
12	AGND	G	Analog Ground. AGND must be connected to the PGND plane.
13	RT/CLK	I	Frequency Setting Resistor (RT) or External Clock Input (CLK) Pin. In RT mode, an external timing resistor connected between this pin and AGND sets the switching frequency. In CLK mode, an external clock sets the switching frequency.
14	FB	I	Feedback Input. A resistor divider is used to connect to the output.
15	COMP	I	Error Amplifier Output and Input to the PWM Modulator. Connect the frequency compensation circuit between this pin and GND.
16	SS/TRK	I	Soft-Start and Tracking Pin. An external capacitor is used to set the soft-start time. This feature is used for tracking and sequencing functions.
17	EN	I	Enable Pin. When this pin is floated or pulled high, the device is enabled. The EN pin can be used to adjust the input UVLO and hysteresis by a resistor divider.
18	PG	O	Power Good Open-Drain Output Pin. It is pulled low during soft-start, when EN is low or during fault events such as thermal shutdown, dropout or over-voltage.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 18V, typical values are measured at V_{IN} = 12V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage						
VIN Under-Voltage Lockout	V_{UVLO_RISE}	V_{VIN} rising		4.05	4.3	V
	V_{UVLO_FALL}	V_{VIN} falling	3.6	3.85		
VIN Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	Hysteresis VIN voltage		200		mV
VIN Supply Current	I_{VIN}	V_{EN} = 1.35V, V_{FB} = 1.5V, non-switching		950	1250	μA
VIN Shutdown Current	I_{VIN_SD}	V_{EN} = 0V, T_J = -40℃ to +125℃		3.5	13	μA
		V_{EN} = 0V, T_J = -40℃ to +150℃			28	
Enable (EN Pin)						
EN Threshold	$V_{ENRISING}$	V_{EN} rising		1.2	1.35	V
	$V_{ENFALLING}$	V_{EN} falling	1.0	1.15		
EN Threshold Voltage Hysteresis	V_{EN_HYS}			50		mV
EN Sourcing Current	I_P	V_{EN} = 1V		1.2		μA
		V_{EN} = 1.35V		5.2		
EN Hysteresis Current	I_H			4.0		μA
Feedback Voltage						
FB Voltage	V_{FB}	T_J = +25℃	596	600	604	mV
			593	600	607	
Error Amplifier						
Error Amplifier Transconductance (gm)	gm_{EA}	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		1160		μA/V
Error Amplifier DC Gain	A_{DC}			80		dB
Error Amplifier Source Current	I_{COMP_SRC}	V_{FB} = 0.5V		105		μA
Error Amplifier Sink Current	I_{COMP_SNK}	V_{FB} = 0.7V		-105		μA
Power Stage Transconductance	gm_{PS}			17		A/V
Soft-Start						
Soft-Start Current	I_{SS}			4.7		μA
$V_{SS/TRK}$ to V_{FB} Matching	V_{SS_OFFSET}	$V_{SS/TRK}$ = 0.4V		38		mV
MOSFET						
High-side Switch Resistance	R_{DSON_H}	$V_{BOOT-SW}$ = 3V		10	22.5	mΩ
		$V_{BOOT-SW}$ = 5V		8.6	20	
Low-side Switch Resistance	R_{DSON_L}	V_{IN} = 12V		4.5	9.5	mΩ
		V_{IN} = 4.5V		4.7	10	
BOOT						
BOOT UVLO Falling				2.5	2.7	V
Current Limit						
High-side Peak Current Limit	$I_{OC\_HS\_PK}$		11.6	14.5	17.2	A
Low-side Sinking Current Limit	$I_{OC\_LS\_SNK}$			-3.4		A
Low-side Sourcing Current Limit	$I_{OC\_LS\_SRC}$		9.1	11.4	13.6	A
RT/CLK						
Logic High Input Voltage	V_{IH}		2			V
Logic Low Input Voltage	V_{IL}				0.8	V
PG						
Power Good Threshold		V_{FB} rising (fault)		108		%V_{REF}
		V_{FB} falling (good)		106		
		V_{FB} rising (good)		91		
		V_{FB} falling (fault)		89		
Leakage Current when Pulled High	I_{PG_LKG}	V_{PG} = 5V		5		nA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 18V, typical values are measured at V_{IN} = 12V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PG						
PG Voltage when Pulled Low	V_{PG_LOW}	V_{IN} = 12V, I_{PG} = 2mA			0.3	V
Minimum V_{IN} for Valid Output		V_{PG} < 0.5V at 100μA		1.7	2.1	V
Thermal Shutdown						
Thermal Shutdown	T_{SD}	Temperature rising		175		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			15		℃

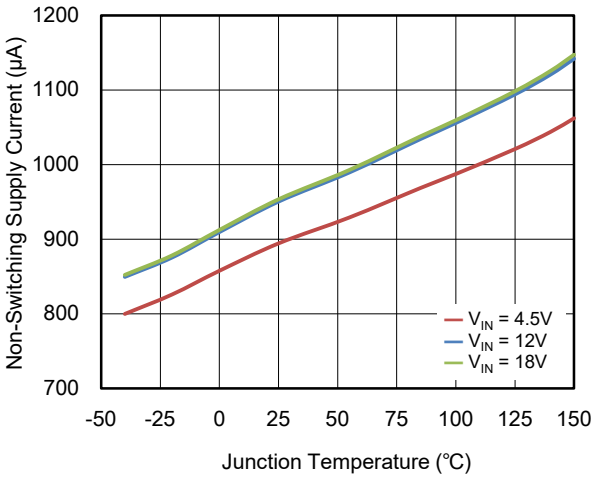
DYNAMIC CHARACTERISTICS

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 18V, typical values are measured at V_{IN} = 12V and T_J = +25℃, unless otherwise noted.)

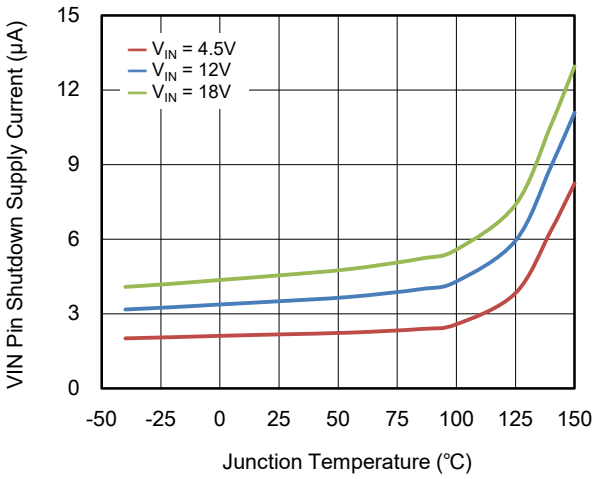
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN						
EN to Start of Switching				158		μs
PG						
Deglitch Time PG Going High				272		Cycles
Deglitch Time PG Going Low				16		Cycles
SW						
Minimum Controllable On-Time	t_{ON_MIN}	Measured at 50% to 50% of VIN, L = 0.68μH, I_{OUT} = 0.1A		94		ns
Minimum Off-Time	t_{OFF_MIN}	$V_{BOOT-SW}$ ≥ 2.6V			0	ns
RT/CLK						
Minimum Switching Frequency (RT Mode)	f_{SW_MIN}	R_{RT} = 260kΩ		200		kHz
Switching Frequency (RT Mode)		R_{RT} = 100kΩ	450	500	550	kHz
Maximum Switching Frequency (RT Mode)	f_{SW_MAX}	R_{RT} = 28.7kΩ		1600		kHz
Switching Frequency Synchronization Range (CLK Mode)	f_{SW_CLK}		200		1600	kHz
RT/CLK Falling Edge to SW Rising Edge Delay (CLK Mode)		Measure at 500kHz with RT resistor in series with RT/CLK		40		ns
Minimum Synchronization Signal Pulse Width (CLK Mode)					35	ns
Hiccup						
Wait Time before Hiccup				512		Cycles
Hiccup Time before Restart				16384		Cycles

TYPICAL PERFORMANCE CHARACTERISTICS

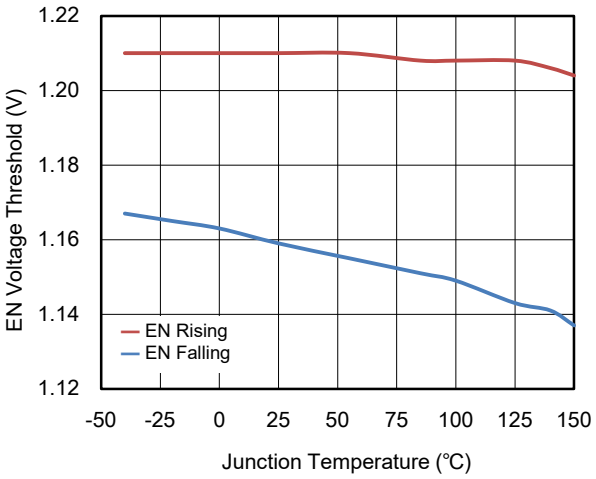
VIN Pin Non-Switching Supply Current vs. Junction Temperature



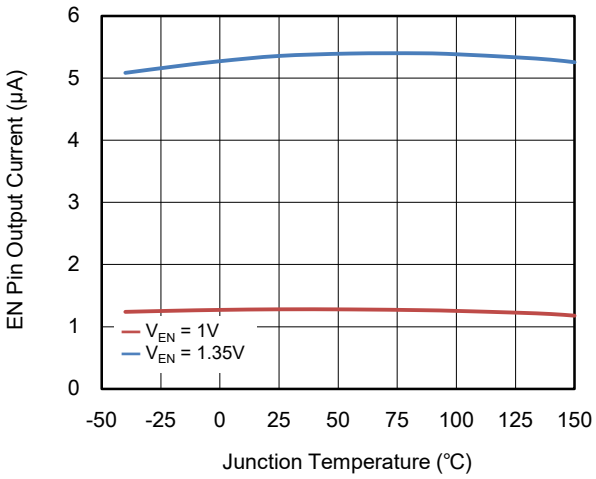
VIN Pin Shutdown Current vs. Junction Temperature



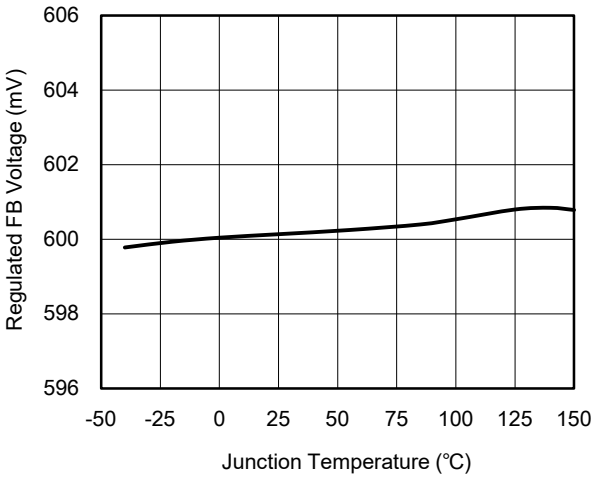
EN Pin Voltage Threshold vs. Junction Temperature



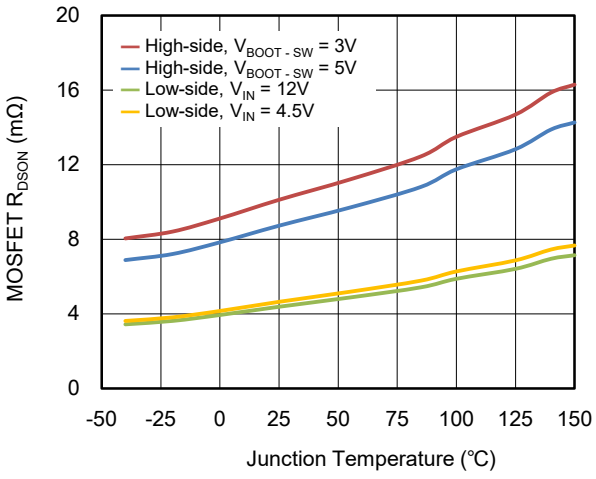
EN Pin Current vs. Junction Temperature



Regulated FB Voltage vs. Junction Temperature

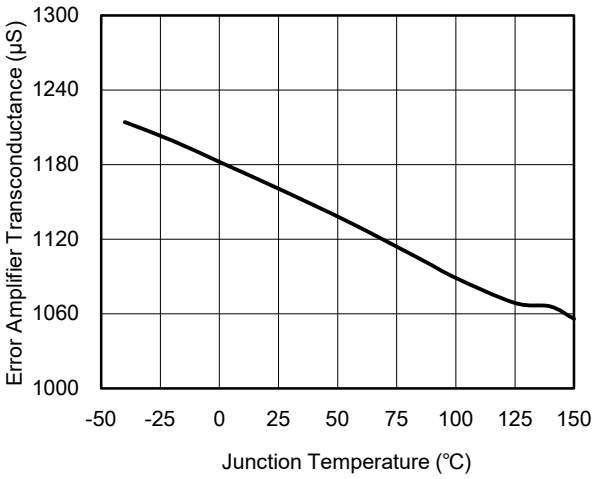


MOSFET R_{DSON} vs. Junction Temperature

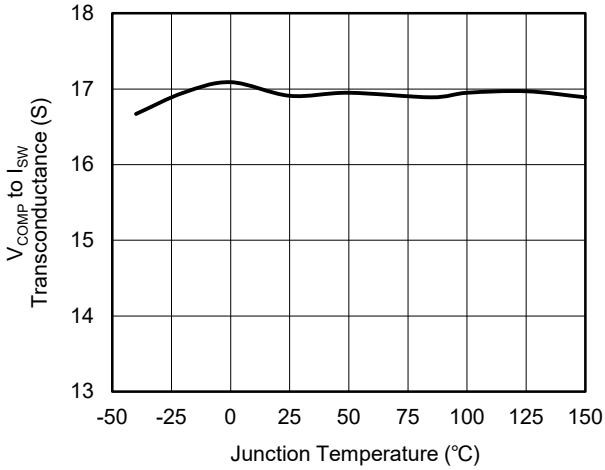


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

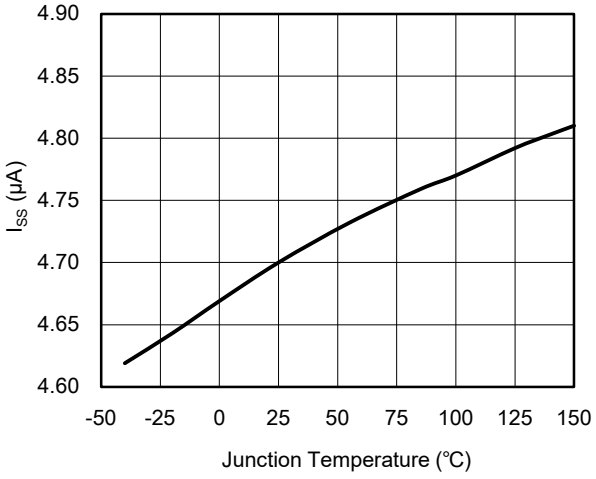
Error Amplifier Transconductance vs. Junction Temperature



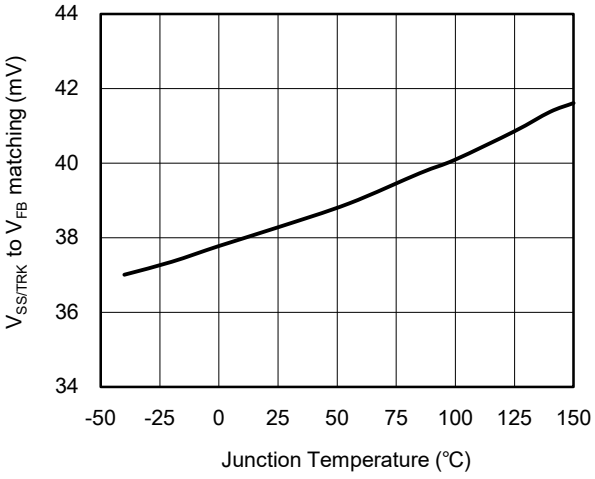
COMP to SW Transconductance vs. Junction Temperature



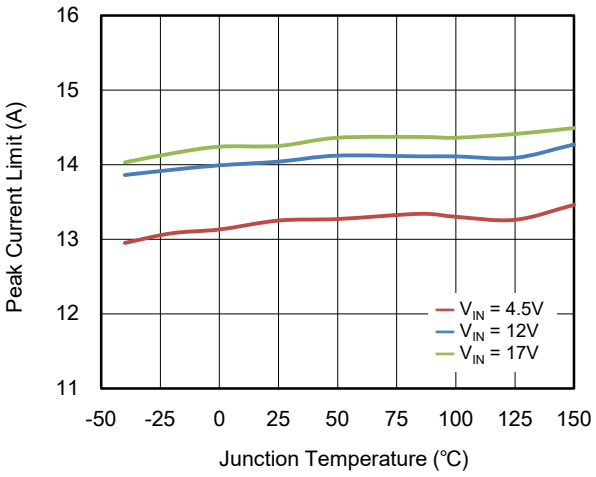
Soft-Start Current vs. Junction Temperature



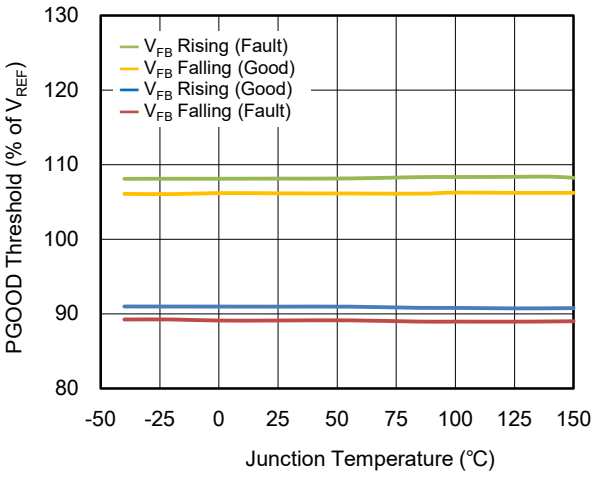
SS/TRK to FB Offset vs. Junction Temperature



High-side Peak Current Limit vs. Junction Temperature

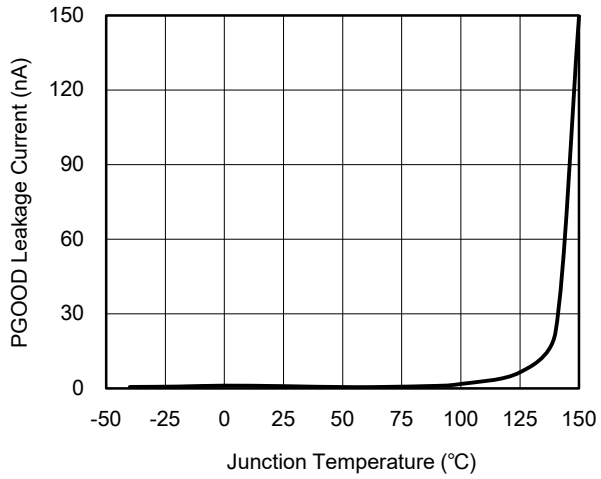


PGOOD Thresholds vs. Junction Temperature

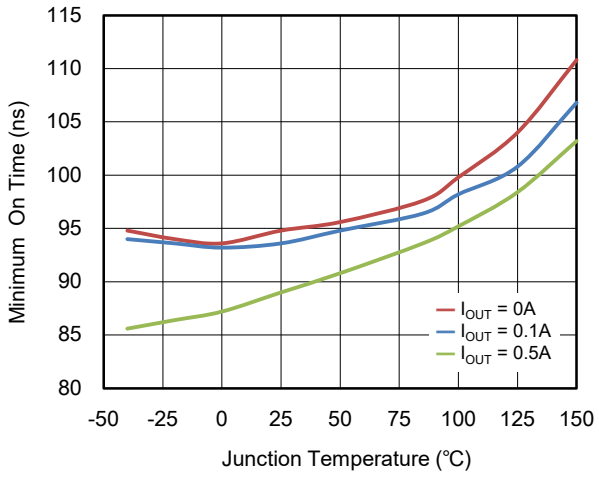


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

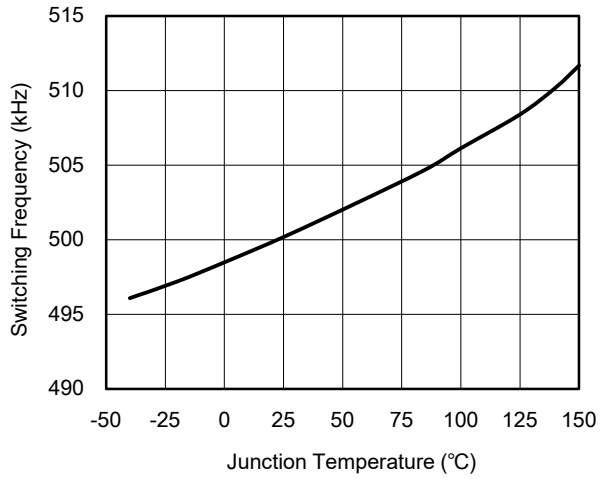
PGOOD Leakage Current vs. Junction Temperature



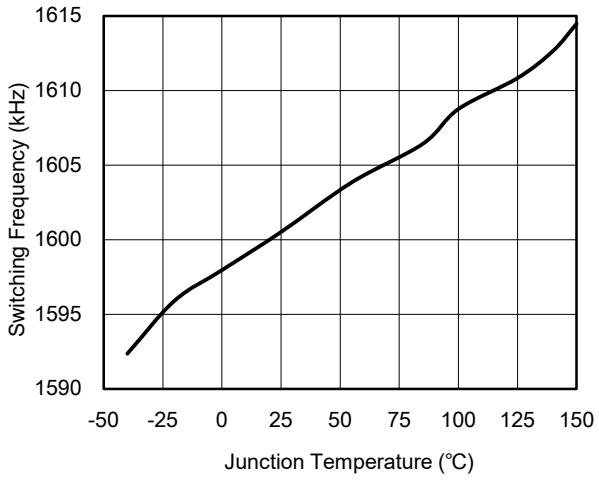
Minimum On-Time vs. Junction Temperature



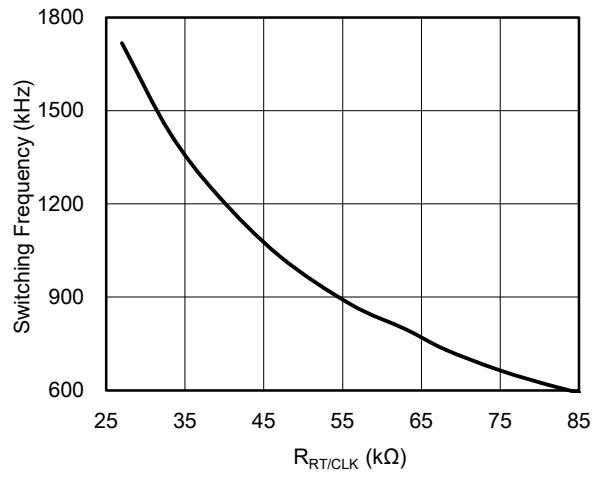
Switching Frequency vs. Junction Temperature (500kHz)



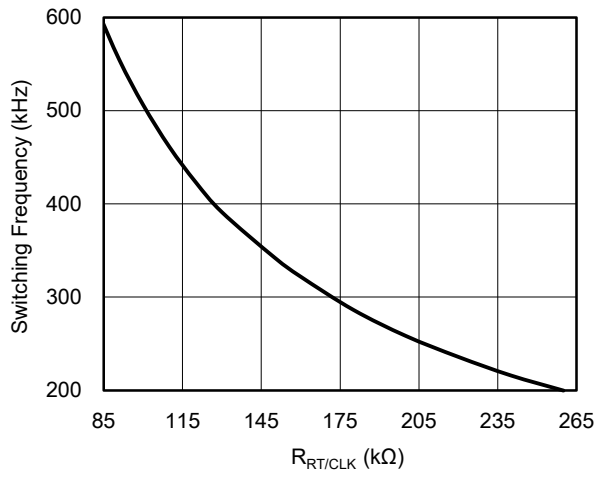
Switching Frequency vs. Junction Temperature (1600kHz)



Switching Frequency vs. RT/CLK Resistor (Low Range)

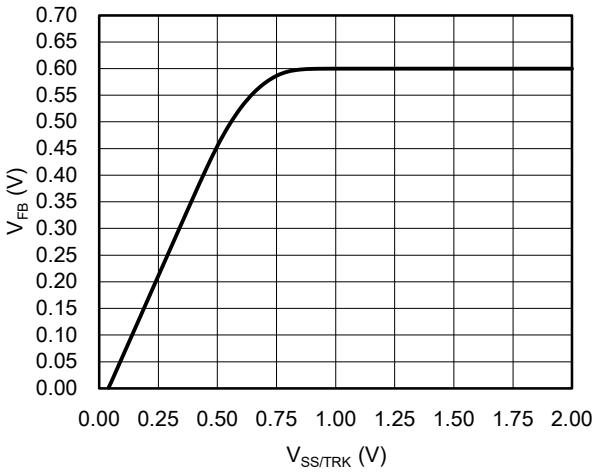


Switching Frequency vs. RT/CLK Resistor (High Range)

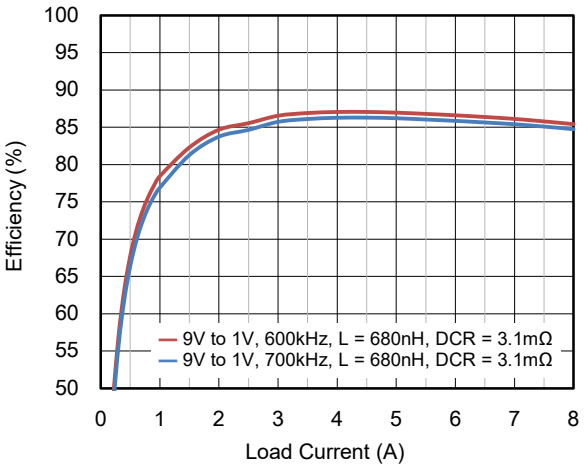


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

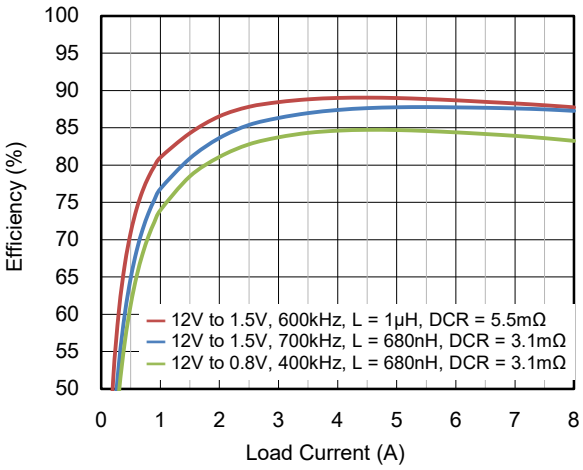
FB Voltage vs. SS/TRK Voltage



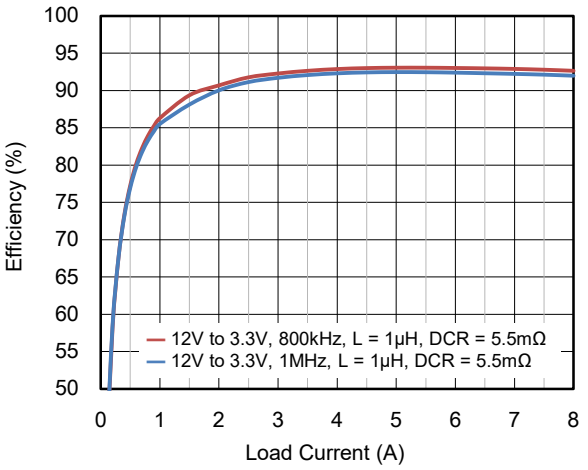
Efficiency for 9V Input to 1V Output



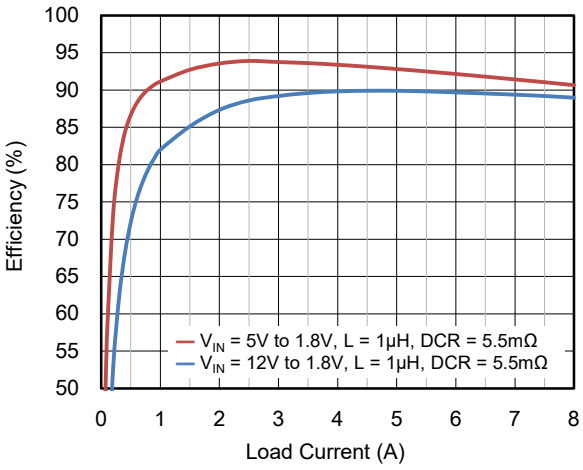
Efficiency for 12V Input to 1.5V and 0.8V Output



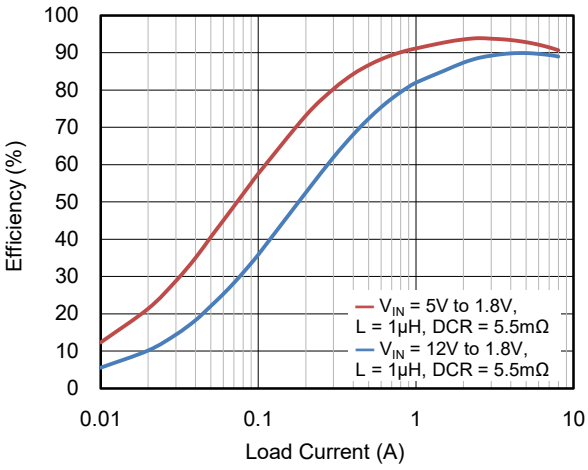
Efficiency for 12V Input to 3.3V Output



Efficiency vs. Load Current



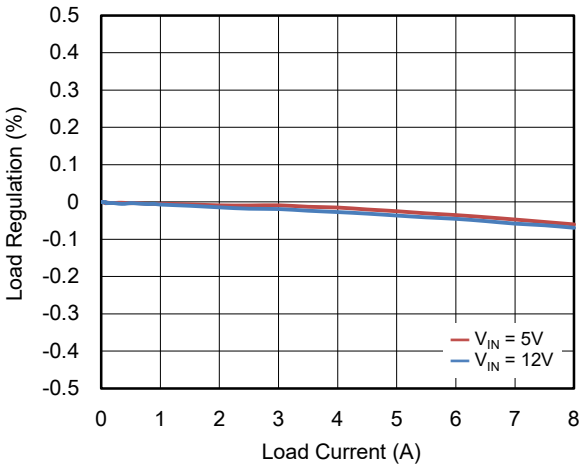
Efficiency vs. Load Current (Log Scale)



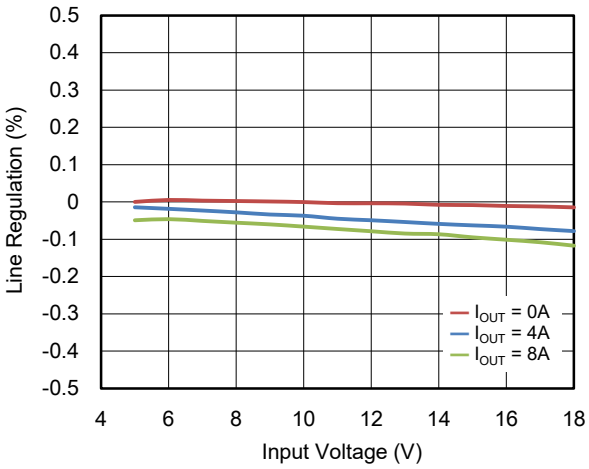
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 700kHz, L = 1μH (DCR = 5.5mΩ), unless otherwise noted.

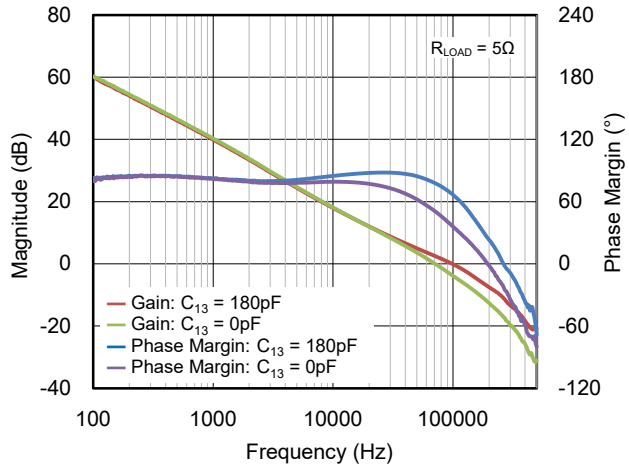
Load Regulation vs. Load Current



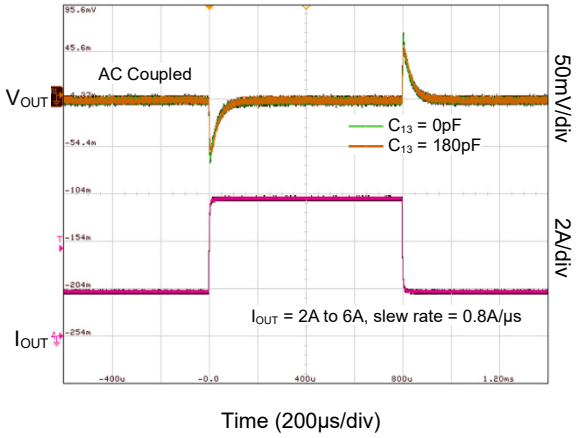
Line Regulation vs. Input Voltage



Loop Response



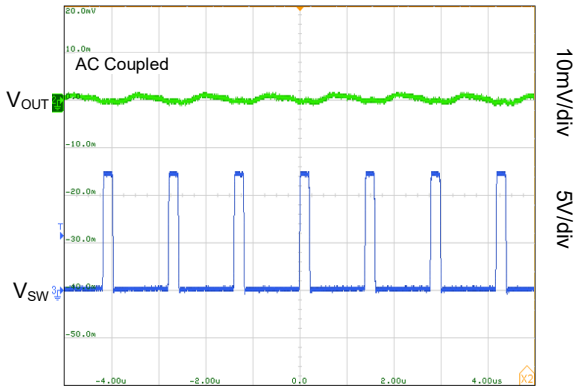
Load Transient Response



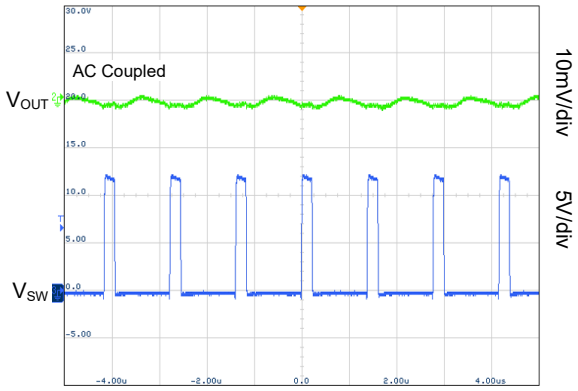
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 700kHz, L = 1μH (DCR = 5.5mΩ), unless otherwise noted.

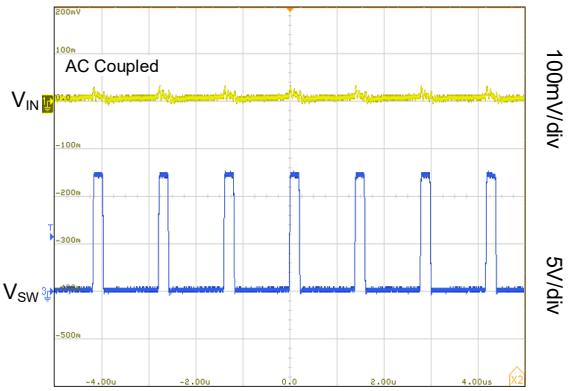
V_{OUT} Ripple 0A



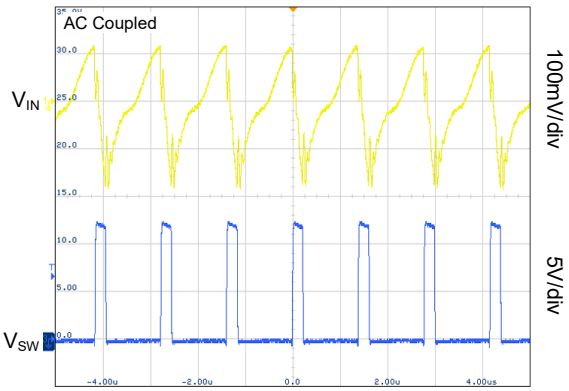
V_{OUT} Ripple 8A



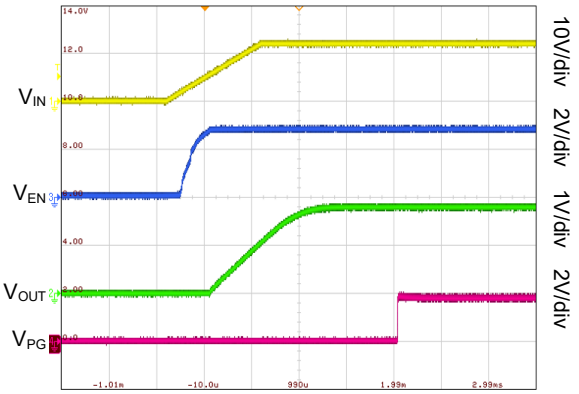
V_{IN} Ripple No Load



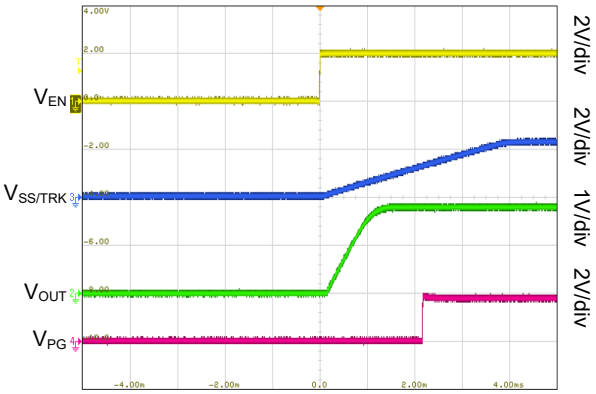
V_{IN} Ripple Full Load



V_{IN} Start-Up



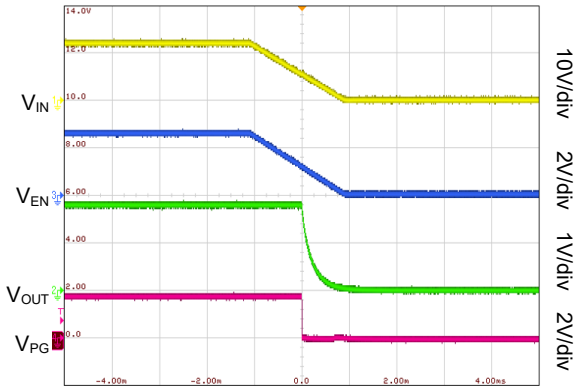
V_{EN} Start-Up



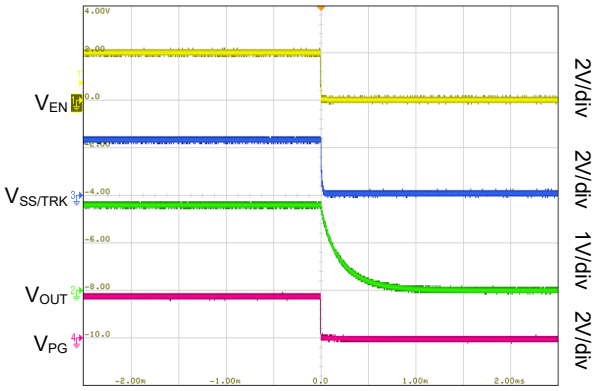
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 700kHz, L = 1μH (DCR = 5.5mΩ), unless otherwise noted.

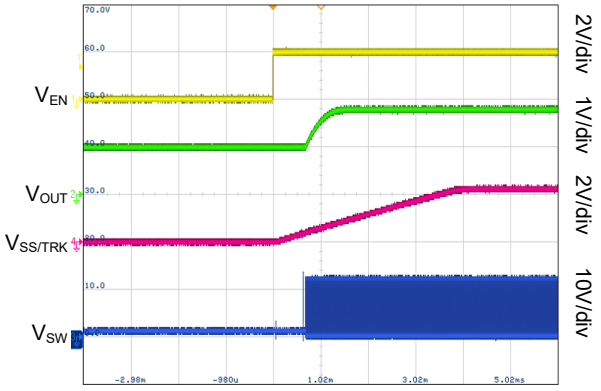
V_{IN} Shutdown



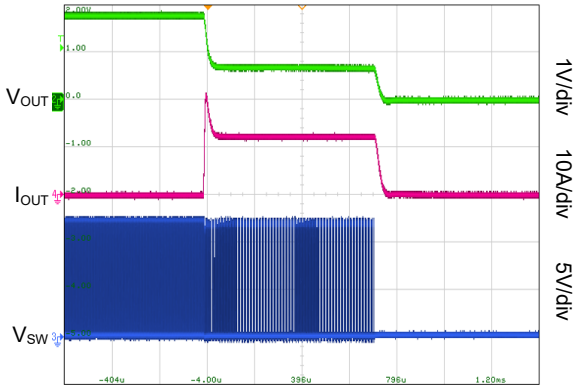
V_{EN} Shutdown



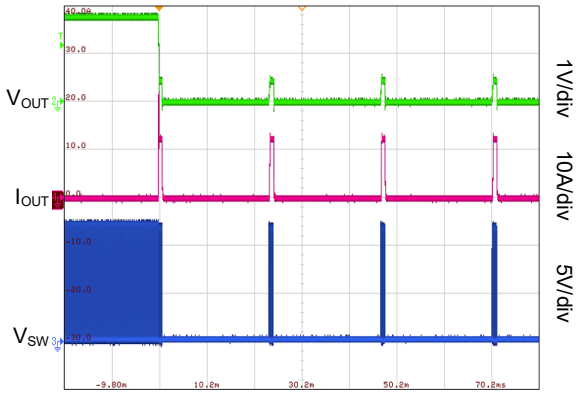
V_{EN} Start-Up with Pre-Bias



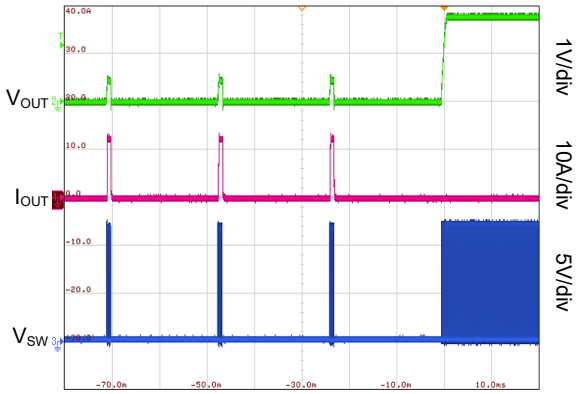
Short-Circuit



Hiccup Entry



Hiccup Recovery



FUNCTIONAL BLOCK DIAGRAM

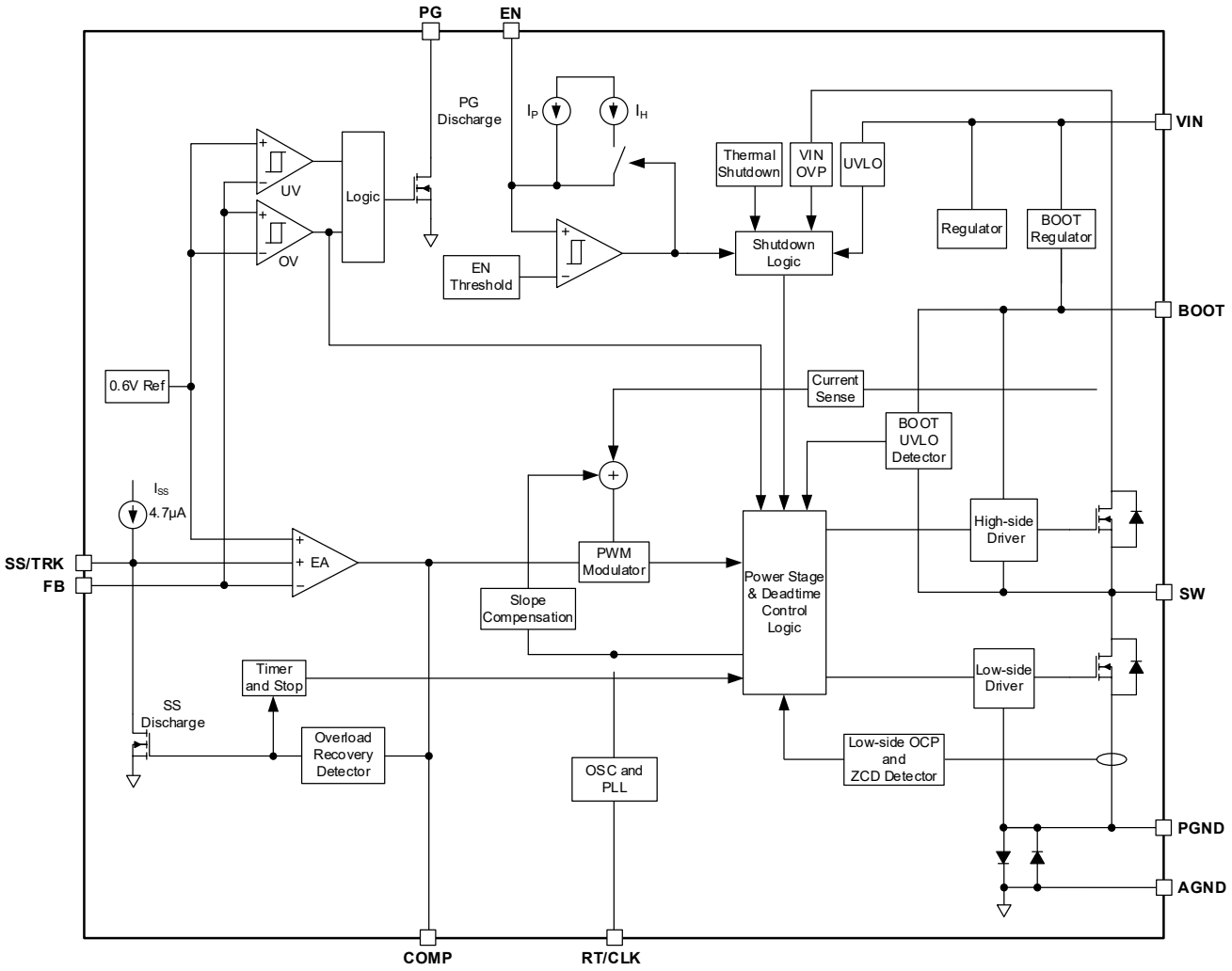


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61184 is a 4.5V to 18V, 8A, synchronous Buck converter with integrated high-side and low-side MOSFETs. The minimum achievable output voltage of this converter is 0.6V, which is equal to the device internal reference voltage (V_{REF}).

As a constant frequency, peak current mode control device, SGM61184 can provide fast transient response with a simple compensation circuit. The wide switching frequency is adjustable from 200kHz to 1600kHz to allow optimizing of the efficiency and size of the converter. For adjusting the internal switching frequency, an external resistor R_{RT} is connected between the RT/CLK pin and GND. The device also accepts an external clock source on this pin to synchronize the oscillator using the internal phase locked loop (PLL).

This device can have a safe and monotonic start-up in output pre-biased conditions. The V_{IN} must exceed the under-voltage lockout threshold (UVLO, 4.05V TYP) for device power-up. The UVLO thresholds can be adjusted (increased) by connecting the EN pin to the tap point of a resistor divider between the VIN pin and GND. The EN internal pull-up current source and the resistor divider determine the UVLO thresholds. When the EN is floated or is pulled high, the device is enabled and the total device current (no switching) is near 950μA. Pulling the EN pin low will shut down the device with 3.5μA (TYP) supply current.

The integrated MOSFETs are optimized for higher efficiency at lower duty cycles. They can efficiently provide up to 8A continuous output current. The integrated bootstrap circuit along with the external boot capacitor provides the bias voltage for the high-side MOSFET driver. The voltage of the bootstrap capacitor that is placed between the BOOT and SW pins is continuously monitored for bootstrap UVLO (BOOT-SW UVLO) detection. If the boot capacitor voltage drops below the bootstrap UVLO, the SW pin will be pulled low to recharge the boot capacitor. 100% duty cycle operation is possible as long as the boot capacitor voltage is higher than the 2.5V (TYP) threshold (preset UVLO level).

The device contains a power good (PG) pin which indicates the status of the output voltage by comparing the FB voltage and the internal reference voltage. PG pin is connected to the drain of internal MOSFET. The PG signal is high when V_{OUT} is between 91% and 106% of its nominal (set) value and goes low if V_{OUT} drops below 89% or rises above 108% of its nominal value.

The SS/TRK (soft-start/tracking) pin can be used to minimize the inrush currents (soft-start function) with a small value capacitor, or for power supply sequencing during power-up with a resistor divider from preceding voltage rail. It is the input pin for the voltage that is followed by the output when the power supply is used in the tracking mode.

The SGM61184 is protected from output over-voltage, over-current and over-heating damage. The output over-voltage transients are effectively minimized by the over-voltage comparator of the power good circuit. When an over-voltage occurs, the high-side switch is forced off and allowed to turn on again if the V_{OUT} drops below 106% of its nominal value.

High-side MOSFET is naturally protected from sourcing over-current by peak current mode control. The low-side MOSFET is also protected bidirectionally against over-current. This feature helps the control of the inductor current to avoid current run away.

If a die temperature is too high ($T_J > T_{SD}$), the device will stop switching and go into shutdown state. It will automatically recover with a soft-start when the junction temperature drops 15℃ (TYP) below the shutdown temperature.

Note that a continued overload condition may cause a cycling thermal shutdown and recovery. It will depend on the temperature and the ventilation conditions of the system.

DETAILED DESCRIPTION (continued)

Power Input Pins

The VIN pin supplies the internal circuits of the device as well as it also provides the supply voltage for the power switches. The V_{IN} operates between 4.5V and 18V, and a voltage divider connected to the EN pin from either VIN pin can be used to adjust the power supply UVLO.

EN Pin and UVLO Programming

The EN pin is used to turn the device on and off. The device starts operation when the EN voltage rises above the enable rising threshold. Pulling the EN voltage below the enable falling threshold stops switching and reduces the device current to the very low quiescent shutdown level. Floating the EN pin will enable the device due to its internal pull-up current source. This current source is used for programming the UVLO threshold. An open-drain or open-collector output connected to the EN pin can be used to control the device. An internal UVLO circuit is implemented on the VIN pin to disable the device and prevent malfunction when the supply voltage is too low. The internal VIN_UVLO hysteresis is 200mV. To program a higher UVLO threshold for the VIN, the EN pin can be configured to one of the configurations shown in Figure 3. Without external components, the internal pull-up current (I_P) sets the EN pin default state to enable. When the device is enabled, the second current source (I_H) is activated. I_P and I_H are used to set the UVLO.

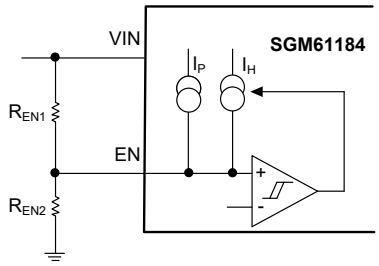


Figure 3. VIN UVLO Setting with a Resistor Divider

The resistor divider can be calculated by Equations 1 and 2 based on the desired UVLO start and stop thresholds.

$$R_{EN1} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_P \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_H} \quad (1)$$

$$R_{EN2} = \frac{R_{EN1} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{EN1} \times (I_P + I_H)} \quad (2)$$

where:

I_H = 4.0μA.

I_P = 1.2μA.

$V_{ENRISING}$ = 1.2V

$V_{ENFALLING}$ = 1.15V.

Soft-Start (SS/TRK)

The lower voltage between the internal VREF and the SS/TRK pins is used as the reference to regulate the output. The soft-start capacitor is connected to the SS/TRK pin and is charged by a 4.7μA internal current source to set the soft-start time (t_{SS}).

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{REF}(\mu A)} \quad (3)$$

where:

V_{REF} = 0.6V.

I_{SS} is the soft-start current source (4.7μA).

Start-Up with Pre-Biased Output

The low-side switch is prohibited from turning on and discharging the output if a pre-biased voltage is sensed on the output before start-up. As long as the SS/TRK pin voltage is below V_{FB}, the low-side switch is not allowed to sink current to have a monotonic start-up with pre-biased output.

Reference Voltage (V_{REF})

A precise 0.6V reference is internally implemented by scaling the output of a temperature-stable band-gap circuit. The reference voltage tolerance over the whole temperature range is ±1.2%. The actual reference voltage for output setting is changed during start-up or tracking.

Output Voltage Setting

The output voltage of the device can be adjusted by resistors R_{FB1} and R_{FB2} which are connected to the FB pin. Use resistors with 1% tolerance or better for good output accuracy. Equation 4 can be used to calculate the R_{FB1} and R_{FB2} (upper and lower resistors) values based on the desired output voltage (V_{OUT}) and V_{REF}.

DETAILED DESCRIPTION (continued)

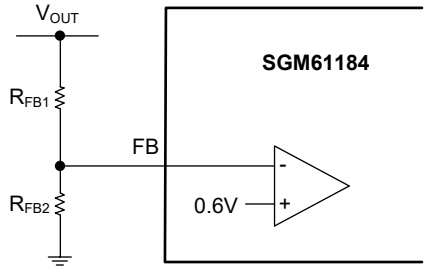


Figure 4. FB Resistor Divider

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \quad (4)$$

where:
V_{REF} = 0.6V.

For example, a 10kΩ resistor can be chosen for R_{FB2} and then R_{FB1} is calculated. Do not choose so large resistors that may cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

The minimal output voltage is determined by the minimum on-time of the high-side switch. The maximal output voltage is constrained by the bootstrap voltage.

Power Good (PG)

The PG is an open-drain output. It is released if there is no fault and the FB pin voltage is in regulation. The PG is pulled low if the FB voltage is lower than 89% or above 108% of the reference voltage. When the device is disabled by EN pin or the voltage of SS/TRK pin is under 1.5V, or if a fault such as UVLO or thermal shutdown occurs, PG is also pulled low.

A 10kΩ to 100kΩ pull-up resistor connected to a voltage rail less than 5.5V is recommended for PG. An option is using the output voltage for PG pull-up. The state of PG is valid only if the V_{IN} > 1.7V. The current sinking capability of PG is limited until V_{IN} exceeds the 4.5V at which the full sinking capacity is available.

Frequency and Synchronization (RT/CLK)

The device can operate in two modes to adjust switching frequency.

In the RT mode, a resistor (R_{RT}) is placed between the RT/CLK and GND pins to set the free running switching frequency of the PLL.

In the CLK mode, an external clock drives the RT/CLK pin and the internal switching clock oscillator is synchronized to CLK by the PLL. The CLK mode overrides the RT mode. The device automatically detects the input clock and switches to the CLK mode.

Constant Frequency PWM

The SGM61184 operates at fixed frequency that can be set by an external resistor or synchronized by external clock.

It is based on peak current control mode architecture. The high-side MOSFET is turned on until the sensing current ramp signal reaches the COMP voltage determined by the EA. If the switch current does not reach the reference value that generates from the COMP voltage at the end of a cycle, the high-side switch remains on for the next cycle until the current meets the reference value.

Continuous Current Mode (CCM)

In most load conditions, the device operates in continuous conduction mode (CCM) (forced PWM). For light loads, the inductor current can be negative when the low-side switch is on. However, if the current reaches the low-side sinking current limit, the low-side switch will be forced off.

It is based on peak current control mode architecture. The high-side MOSFET is turned on until the sensing current ramp signal reaches the COMP voltage determined by the EA. If the switch current does not reach the reference value that generates from the COMP voltage at the end of a cycle, the high-side switch remains on for the next cycle until the current meets the reference value.

Error Amplifier

The output voltage is sensed by a resistor divider through the FB pin and is compared with the internal reference. The error amplifier generates an output current that is proportional to the voltage difference (error), and the transconductance is 1160μA/V. The generated current is then fed into the external compensation network to generate the voltage on the COMP pin, which sets the reference value for the peak current that controls the on-time of the power MOSFET. COMP is pulled down to the ground when the device shuts down.

DETAILED DESCRIPTION (continued)

Slope Compensation

To avoid sub-harmonic oscillations that result in unstable PWM pulses, a small negative-slope compensating ramp is added to the measured switch current before it is used to generate the PWM signal. The slope compensation has no influence on the peak current limit which is maintained over full range of duty cycle.

Input Over-Voltage Protection

The SGM61184 is designed with an input over-voltage protection circuit. During normal operation of the chip, once the input voltage V_{IN} exceeds about 24.2V, the IC stops switching. The high-side and low-side MOSFETs both turn off, and the soft-start capacitor discharges. Until the input voltage V_{IN} is lower than about 23.8V, the OVP state will be released and the device will operate again.

Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. Usually an OVP occurs after removal of an overload condition. When the output voltage is dropped due to a persisting overload, the error amplifier output reaches to its maximum and forces the converter to provide the maximum output current. Upon removal of the overload condition, the regulator output rises quickly because the high inductor current charges the output capacitor rapidly, especially when C_{OUT} is small. The error amplifier will respond and re-adjust itself but not as fast as the output filter and an overshoot occurs.

To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. If the threshold is exceeded, the high-side MOSFET is turned off to stop feeding current to the output, and the low-side MOSFET turns on and rapidly discharges the output voltage. When the FB voltage drops below the OVP threshold, the high-side MOSFET can turn on again in the next cycle.

Over-Current Protection

Both high-side and low-side switches are protected from over-current with cycle-by-cycle current limiting as explained in the next two sections.

High-side Switch Over-Current Protection

Using current mode control, the pulse width (from the beginning of the cycle until high-side switch is turned off) is determined by the compensator output voltage (V_{COMP} at COMP pin) in a cycle-by-cycle basis. In each cycle the high-side switch current is continuously compared with the current set point determined by compensator output (V_{COMP}) and when the high-side current reaches to that reference (peak current), the high-side switch is turned off.

Low-side MOSFET Over-Current Protection

The current of the low-side switch is continuously monitored while it is turned on. Normally, the low-side switch sources current from ground to the load through the inductor. Before the beginning of a new cycle, the low-side current is compared to its current limit which is normally lower than the high-side current limit. Only when the low-side source current drops below its current limit, the high-side MOSFET will be turned on again for the new cycle.

In some operating conditions, the low-side switch sinks current from the load to the ground. If the low-side sinking current exceeds the typical limit of -3.4A, the low-side switch will be immediately turned off and both switches will not be turned on until the end of the cycle.

Thermal shutdown

To protect the device from damage due to overheating, the thermal shutdown feature is implemented to disable the device when the die temperature exceeds +175℃ (TYP). A new power-up sequence is initiated automatically once the temperature falls below +160℃ (15℃ hysteresis, TYP).

Device Functional Modes

Switching Frequency Setting (RT Mode)

Selection of the switching frequency is generally a tradeoff among the solution size, efficiency, and the minimum controllable on-time. The RT resistance can be designed from Equation 5.

$$R_{RT}(k\Omega) = 68775 \times f_{SW}(kHz)^{-1.052} \quad (5)$$

DETAILED DESCRIPTION (continued)

Synchronization (CLK Mode)

The device uses an internal phase locked loop (PLL) to set or synchronize to an external clock signal with the 200kHz to 1600kHz range. Mode change from RT mode to CLK mode is allowed.

For stable synchronization, a square wave clock with 20% to 80% duty cycle must be applied to the RT/CLK pin. The logic low and high levels of the clock must be below 0.8V and above 2.0V respectively. The switching cycle starts with the falling edge of the RT/CLK signal.

If both RT and CLK modes are needed in an application, configuration shown in Figure 5 can be used. The RT mode can be overridden by CLK mode when both R_{RT} and clock are present. Mode switch occurs when the RT/CLK is pulled above 2.0V for the first time. Once CLK mode is selected, the PLL is locked to external CLK and the RT/CLK pin shifts to a high-impedance state. Going back from CLK mode to RT mode is not recommended, because by removing clock, the switching frequency drops to around 100kHz first (waiting for synchronize clock) before recovery to the free running frequency that is set by RT resistor. Figure 6 and Figure 7 show the typical performance for the transition from RT mode to CLK mode then back to RT mode.

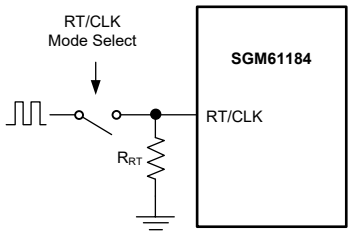


Figure 5. Using RT and CLK Modes Together

Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle)

An integrated bootstrap regulator is used for powering the high-side MOSFET gate driver. A small 0.1μF ceramic capacitor (X5R or X7R grade) with at least 10V rating is required between the BOOT and SW pins to supply the gate driver. It is recharged from VIN source through an internal switch every time the SW goes low. Recharge happens when the BOOT pin voltage is less than VIN and the BOOT-SW voltage is below the required regulation for the high-side gate voltage. The SGM61184 has no minimum off-time. It can operate at 100% duty cycle as long as the BOOT-SW voltage is higher than its UVLO threshold (2.5V, TYP). If the BOOT-SW voltage drops below its UVLO threshold, the high-side switch is turned off and the low-side switch is turned on to recharge the boot capacitor.

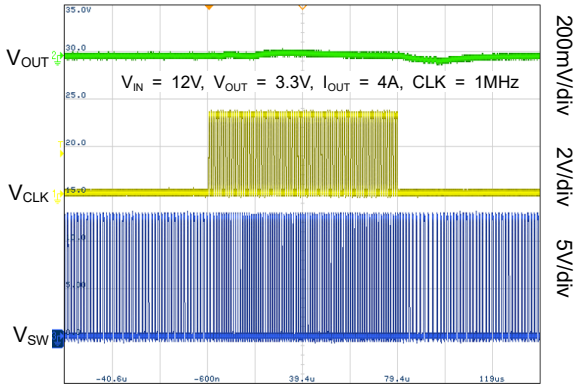


Figure 6. RT to CLK to RT 700kHz

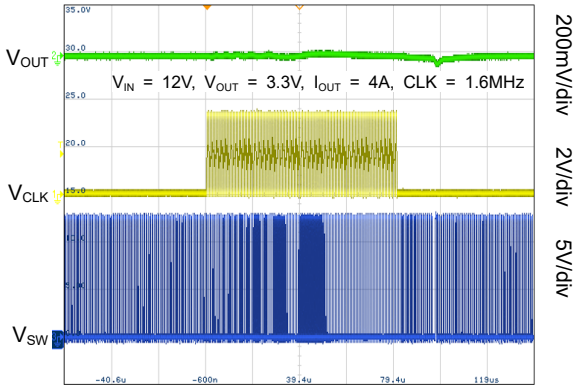


Figure 7. RT to CLK to RT 1200kHz

DETAILED DESCRIPTION (continued)

Start-Up Sequencing (SS/TRK)

The SS/TRK, EN and PG pins allow the implementation of common power supply sequencing methods. A simple sequencing approach is shown in Figure 8 in which the right side of device is powered up after the left one. The PG of the left device is coupled to the EN pin of the right. The right side power supply is enabled after the primary supply reaches regulation.

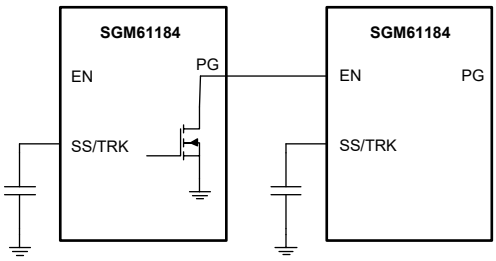


Figure 8. Sequential Start-Up Sequence

Figure 9 shows the ratiometric sequencing of two converters. The SS/TRK and EN inputs of the two devices are tied together. In this configuration, the I_{SS} current sources from the SS/TRK pins are added together and 2 × I_{SS} should be considered to calculate the soft-start capacitor from Equation 3.

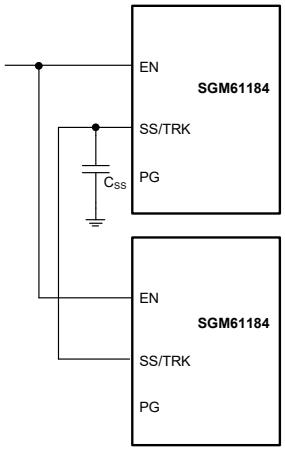


Figure 9. Ratiometric Sequencing of Two Devices

Simultaneous ratiometric sequencing can also be implemented by using a resistor divider as shown in Figure 10 by R_{SS1} and R_{SS2}.

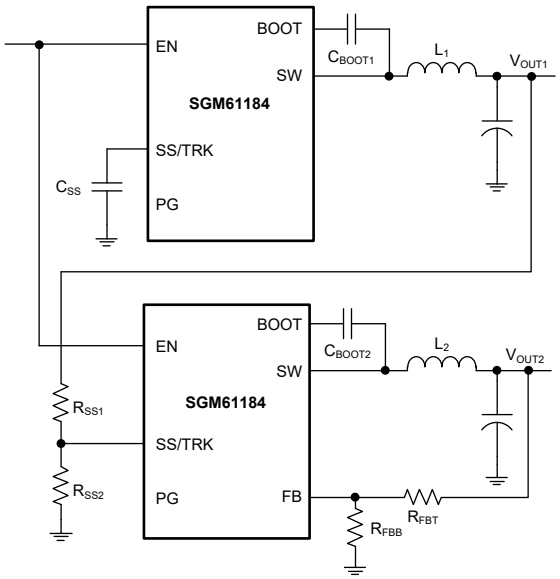


Figure 10. Ratiometric and Simultaneous Start-Up Sequence

In this example, the second power supply output (V_{OUT2}) tracks V_{OUT1} (the output of the first power supply). By proper selection of R_{SS1} and R_{SS2}, V_{OUT2} can ramp up and reach regulation with the same rate, or a little bit faster or slower than V_{OUT1}. Note that V_{OUT2} is tracking V_{OUT1} and reaches regulation first. Equations 7 and 8 can be used to calculate the tracking resistors. ΔV is the desired V_{OUT1} - V_{OUT2} difference when V_{OUT2} reaches regulation. ΔV will be positive when V_{OUT1} change rate is higher than V_{OUT2} start-up rate. It will be negative if V_{OUT2} rate is faster. With simultaneous sequencing, ΔV is zero. To assure the proper device operation, make sure that the selected R_{SS1} is larger than the value given in Equation 9.

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (6)$$

$$R_{SS1} = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSOFFSET}}{I_{SS}} \quad (7)$$

$$R_{SS2} = \frac{V_{REF} \times R_{SS1}}{V_{OUT2} + \Delta V - V_{REF}} \quad (8)$$

$$R_{SS1} > 20000 \times V_{OUT1} \quad (9)$$

The $V_{SSOFFSET}$ is the inherent SS/TRK to FB offset of the device (38mV, TYP) and I_{SS} is the pull-up current source (4.7μA).

APPLICATION INFORMATION

Typical Application

The schematic of a typical application circuit that is used for SGM61184 is given in Figure 11.

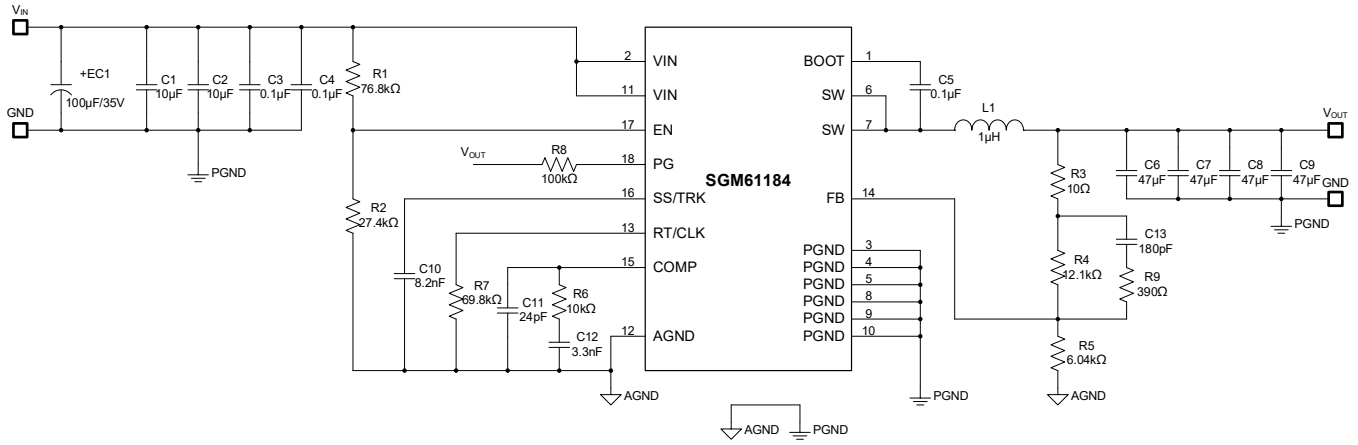


Figure 11. SGM61184 Typical Application Circuit

Design Requirements

In this example, a high frequency regulator with ceramic output capacitors will be designed using SGM61184 and the details will be reviewed. The design requirements are typically determined at the system level. In this example, the known parameters are summarized in Table 1.

Table 1. Design Parameters

Design Parameter	Example Value
Input Voltage Range (V_{IN})	12V nominal, 4.5V to 15V
Output Voltage (V_{OUT})	1.8V
Transient Response	±4%, ±72mV
Output Ripple Voltage	0.5%, 9mV
Output Current Rating (I_{OUT})	8A
Switching Frequency (f_{SW})	700kHz

Operating Frequency

Usually the first parameter to design is the switching frequency (f_{SW}). Higher switching frequencies allow smaller solution size and smaller filter inductors and capacitors, and the bandwidth of the converter can be increased for faster response. It is also easier to filter noises because they also shift to higher frequencies. The drawbacks are increased switching and gate driving losses that result in lower efficiency and tighter thermal limits. Also the duty cycle range and Buck ratio will be limited due to the minimum on-time and/or off-time limits of the converter. In this design, f_{SW} = 700kHz is chosen as a tradeoff. From Equation 10, the nearest standard resistor for this frequency is R_7 = 69.8kΩ.

$$R_7(k\Omega) = 68775 \times f_{SW}(kHz)^{-1.052} \quad (10)$$

Inductor Design

Equation 11 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. During power-up with large output capacitor, over-current, output shorted or load transient conditions, the actual peak current of inductor can be greater than I_{L_PEAK} calculated in Equation 14. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the output capacitor selection. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 ~ 0.4). Choosing a higher K_{IND} value reduces the selected inductance.

$$L_1 = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (11)$$

APPLICATION INFORMATION (continued)

In this example, K_{IND} = 0.3 is chosen and the inductance is calculated to be 0.94μH. The nearest standard value is 1μH. The ripple, RMS and peak inductors current calculations are summarized in Equations 12, 13 and 14 respectively.

$$I_{RIPPLE} = \frac{V_{INMAX} - V_{OUT}}{L_1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (12)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left[\frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times L_1 \times f_{SW}} \right]^2} \quad (13)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (14)$$

For this example, the ripple, RMS, and peak inductor current are calculated as 2.3A, 8.0A and 9.1A respectively.

Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). The minimum output capacitance can be given by Equation 15, which represents that the ΔV_{OUT} (overshoot or undershoot) is approximately equal to the ΔI_{OUT} (load current step) multiplied by the output impedance at crossover frequency. The target crossover frequency is 1/10th of the switching frequency.

$$C_{OUT} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{sw}}{10}} \quad (15)$$

where:

- ΔI_{OUT} is the change in output current.
- f_{SW} is the regulator's switching frequency.
- ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient to a 4A load step is 4%, by inserting ΔV_{OUT} = 72mV and ΔI_{OUT} = 4A, the minimum required capacitance will be 126μF. Generally, the ESR of ceramic capacitors is small enough. The impact of output capacitor ESR on the transient is not taken into account in Equation 15.

Equation 16 can be used for the output ripple criteria and finding the minimum output capacitance needed. In this example, the allowed ripple is 9mV that results in minimum capacitance of 45μF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \quad (16)$$

where:

- $V_{ORIPPLE}$ is the maximum allowable output voltage ripple.
- I_{RIPPLE} is the inductor ripple current.

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 17. Use Equation 17 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement. In this example, the ESR must be less than 4mΩ.

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \quad (17)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 4 × 47μF/6.3V 1206 X5R ceramic capacitor with 3mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 18 calculates the RMS current that the output capacitor must support. In this example, it is 653mA.

$$I_{CORMS} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{\sqrt{12} \times V_{INMAX} \times L_1 \times f_{SW}} \quad (18)$$

APPLICATION INFORMATION (continued)

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61184. At least 4.7μF of effective capacitance (after deratings) is needed on the VIN input. If input power is far away from the device, additional bulk capacitor is recommended in parallel to stabilize input voltage. The RMS current of input capacitor can be calculated from Equation 19 and the maximum I_{CIRMS} occurs at 50% duty cycle. For this example, the maximum input RMS current is 3.9A with the 4.5V minimum input. The ripple current rating of input capacitor should be greater than $I_{CIRMS.}$

$$I_{CIRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{INMIN} - V_{OUT})}{V_{INMIN} \times V_{INMIN}}} \quad (19)$$

In this example, the voltage rating of capacitor should have a safe margin from maximum input voltage. Therefore, select two 10μF, 1206X7R, 25V and two 0.1μF, 0603X7R, 25V capacitors in parallel and put on both sides of the device near both VIN pins to PGND pins. The total input capacitance derates to 7.6μF at the normal input voltage of 12V. They are placed in parallel because the two VIN inputs are tied together to operate from a single supply in this design.

The input voltage ripple can be calculated from Equation 20, the maximum ripple occurs at 50% duty cycle. In this example, the input voltage ripple is 192mV at the 12V normal input.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times D \times (1\text{-}D)}{C_{IN} \times f_{SW}} \quad (20)$$

Soft-Start Capacitor

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. The ramp is needed in many applications due to limited voltage slew rate required by the load or limited available input current to avoid input voltage sag during start-up (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 21 (with I_{SS} = 4.7μA and V_{REF} = 0.6V) can be used to calculate the soft-start capacitor for a required soft-start time (t_{SS}). In this example, the output capacitor value is relatively small (47μF×4) and the soft-start time is not critical because it does not require too much charge for 1.8V output voltage. However, it is better to set a small arbitrary value, like C_{SS} = 8.2nF that results in 1ms start-up time.

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V)} \quad (21)$$

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor with 10V or higher voltage rating must be connected between the BOOT-SW pin. X5R or better dielectric types are recommended.

UVLO Setting

The under-voltage lockout (UVLO) can be programmed from VIN pins by an external voltage divider network. In this design, the turn-on (enable to start switching) occurs when VIN rises above 4.5V. When the regulator is working, it will not stop switching (disabled) until the input falls below 4V. Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 76.8kΩ and R_2 = 27.4kΩ.

Feedback Resistors

A resistor divider created by an upper resistor (R_4) and a lower resistor (R_5) can set the output voltage. Equation 22 calculates the resistors. When R_5 is selected as 6.04kΩ, the nearest 1% resistor for the calculated R_4 value (12.08kΩ) is 12.1kΩ. For higher output accuracy, choose resistors with better tolerance (0.5% or better).

$$R_4 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_5 \quad (22)$$

APPLICATION INFORMATION (continued)

Minimum Output Voltage

There is a minimum output voltage limit for any given input voltage due to the limited minimum switching on-time of the device. Above the 0.6V minimum possible output, the lowest achievable voltage is given by Equation 23.

$$V_{OUTMIN} = t_{ONMIN} \times f_{SWMAX} (V_{INMAX} + I_{OUTMIN} (R_{DSON\_HMIN} - R_{DSON\_LMIN})) - I_{OUTMIN} (R_L + R_{DSON\_HMIN}) \quad (23)$$

where:

• V_{OUTMIN} = Minimum achievable output voltage.
• t_{ONMIN} = Minimum controllable on-time (150ns MAX).
• f_{SWMAX} = Maximum f_{SW} (including tolerance).
• V_{INMAX} = Maximum input voltage.
• I_{OUTMIN} = Minimum load current.
• R_{DSON_HMIN} = Minimum high-side switch R_{DSON} (8.6mΩ to 10mΩ, TYP).
• R_{DSON_LMIN} = Minimum low-side switch R_{DSON} (4.5mΩ to 4.7mΩ, TYP).
• R_L = Output Inductor series resistance.

Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. The recommended calculation method here is quite simple and yields results with high phase margins. In this method, the effects of the slope compensation are ignored. Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

For this design, the target cross frequency $f_C = f_{SW}/10$ = 70kHz. For C_{OUT}, the derated value of 126.8μF and R_{ESR} of 1mΩ are used. Having the crossover frequency, the compensation network (R_6 and C_{12}) can be calculated. R_6 programs the gain of the compensated network at the crossover frequency and can be calculated by Equation 24.

$$R_6 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm_{EA} \times V_{REF} \times gm_{PS}} \quad (24)$$

where:

• gm_{EA} is the gm amplifier gain (1160μA/V).
• gm_{PS} is the power stage gain (17A/V).
• V_{REF} is the reference voltage (0.6V).

C_{12} sets the location of the compensation zero along with R_6. To place this zero on the converter pole, use Equation 25.

$$C_{12} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_6} \quad (25)$$

From Equations 24 and 25, the standard selected values are R_6 = 10kΩ and C_{12} = 3.3nF.

A high frequency pole can also be added by a parallel capacitor if needed. This capacitor is recommended to help filter switching noise that may couple to the COMP voltage signal. Use Equation 26 to calculate the C_{11}. For this design, the closest standard value is 24pF

$$C_{11} = \frac{1}{2\pi \times R_6 \times f_{SW}} \quad (26)$$

The initial compensation based on these calculations is R_6 = 10kΩ, C_{12} = 3.3nF, and C_{11} = 24pF. These values yield a stable design, but it is at a critical point that meets the dynamic response requirements. Type III compensation can be used to improve bandwidth and phase margin. It is used by adding the feed forward capacitor C_{13} in parallel with the upper feedback resistor. The feed forward capacitor generates a not independent zero pole pair. The position of the zero point is calculated by Equation 27.The position of the pole point is calculated by Equation 28. For this design, C_{13} = 180pF and R_9 = 390Ω are selected to obtain a better bandwidth and phase margin. For the typeIII compensation, R_9 is necessary, which can help to adjust the position of zero and pole pairs more flexibly and reduce the switching noise of FB node.

$$f_Z = \frac{1}{2\pi \times (R_4 + R_9) \times C_{13}} \quad (27)$$

$$f_P = \frac{1}{2\pi \times (R_4 \,//\, R_5 + R_9) \times C_{13}} \quad (28)$$

APPLICATION INFORMATION (continued)

Layout Guidelines

- PCB layout is critical for stable and high-performance converter operation.
- Place the nearest input high frequency decoupling capacitor between VIN and AGND pins as close as possible.
- Place a larger input ceramic capacitor close to VIN and GND pins for minimizing the influence of ground bounce.
- Use short and wide trace to connect SW node to the inductor. Minimize the area of switching loop. Otherwise, large voltage spikes on the SW node and poor EMI performance are inevitable.
- Sensitive signals like FB, COMP, EN, RT/CLK traces must be placed away from high dv/dt nodes (such as SW) and not inside any high di/dt loop (like capacitor or switch loops). The ground of these signals should be connected to GND pin and separated with power ground.
- To improve the thermal performance, it is recommended to use 4-layers PCB with large ground planes. Using a group of small thermal vias near the power traces as well as near the input and output capacitors can provide a good heat conduction path from the device to the PCB board.
- Connect VIN, GND pins to large copper areas to increase heat dissipation and long-term reliability. Keep SW area small to avoid emission issue.

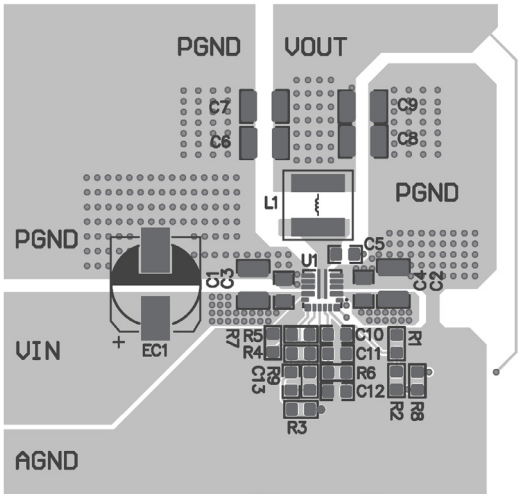


Figure 12. Top Layer

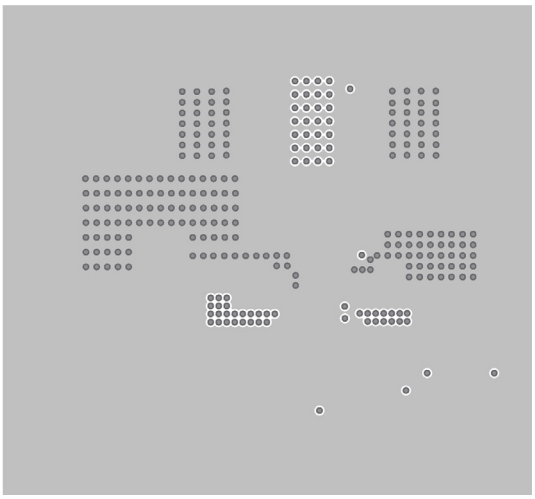


Figure 13. Mid Layer 1

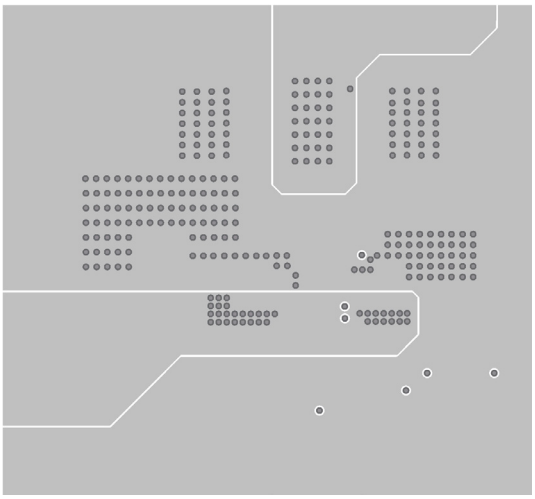


Figure 14. Mid Layer 2

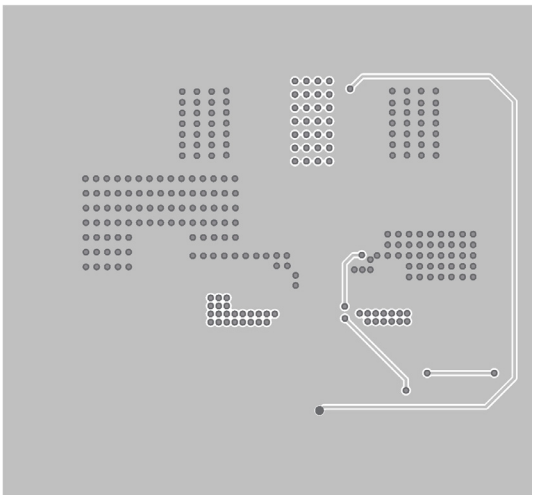


Figure 15. Bottom Layer

REVISION HISTORY

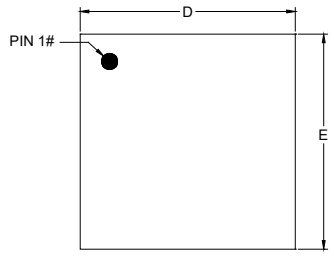
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2024 – REV.A to REV.A.1	Page
Updated the Figure 1 and Figure 2	1, 13
Updated Package Thermal Resistance	2
Added notes for ESD	2
Updated the Input Capacitor Design and Loop Compensation Design sections	22, 23

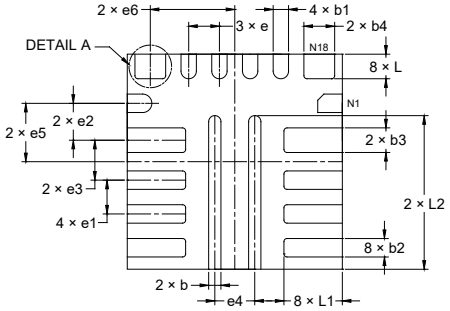
Changes from Original (AUGUST 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

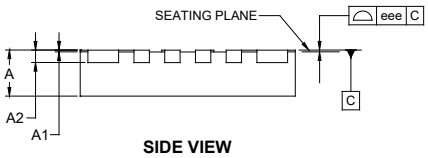
TQFN-3.5×3.5-18AL



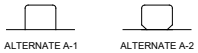
TOP VIEW



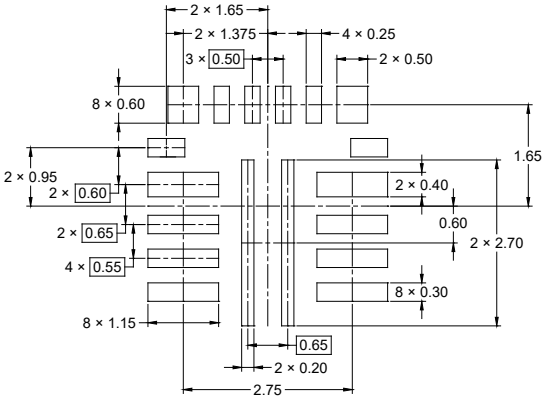
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



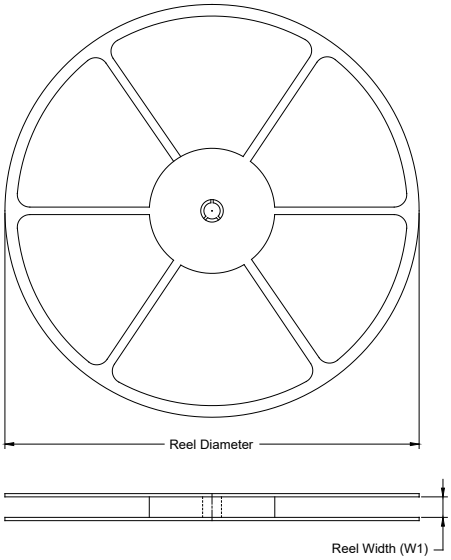
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
b1	0.200	-	0.300
b2	0.250	-	0.350
b3	0.350	-	0.450
b4	0.450	-	0.550
D	3.400	-	3.600
E	3.400	-	3.600
e		0.500 BSC	
e1		0.550 BSC	
e2		0.600 BSC	
e3		0.650 BSC	
e4		0.650 BSC	
e5		0.950 BSC	
e6		1.375 BSC	
L	0.300	-	0.500
L1	0.850	-	1.050
L2	2.400	-	2.600
eee		0.080	

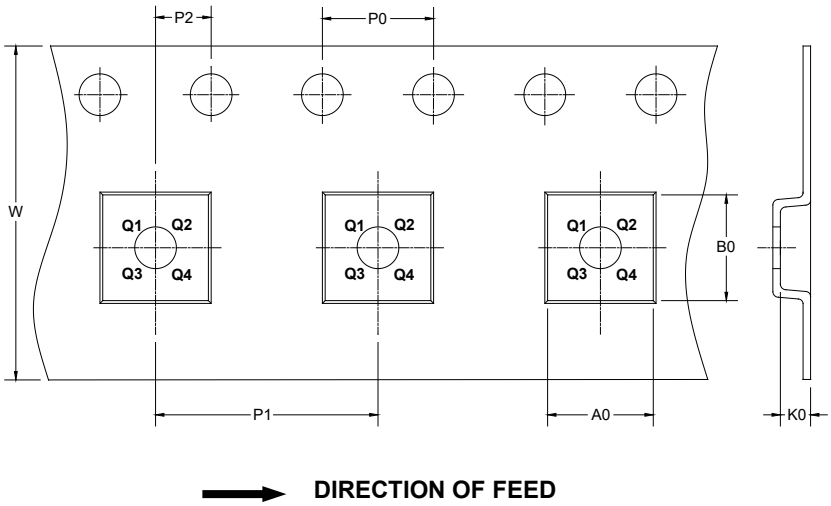
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



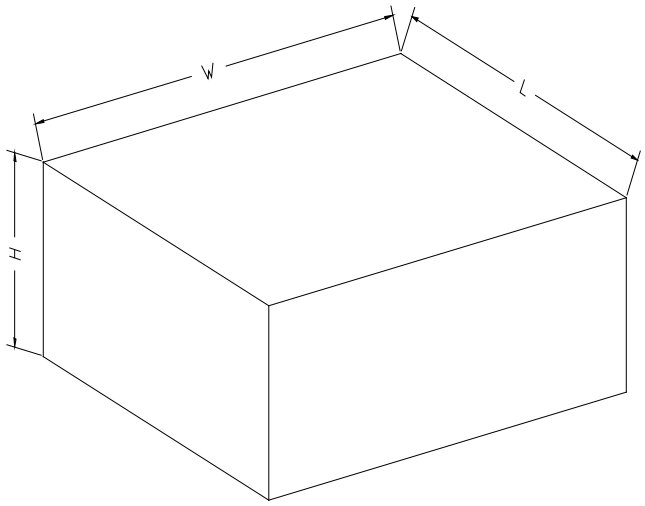
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-18AL	13"	12.4	3.75	3.75	1.05	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002