SGM611A121
I²C Controlled 18V, 12A, High-Efficiency, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM611A121 is a high-efficiency synchronous Buck converter with integrated power MOSFETs and an I²C control interface. It delivers up to 12A of output current and employs an adaptive hysteresis pseudo-constant on-time control (AHP-COT) architecture, which achieves both faster transient response and tighter output voltage regulation compared with conventional control architectures.

In addition to standard mode and fast modes, the I²C interface supports 1Mbit/s fast-mode plus operation. The output voltage can be programmed via the I²C interface, with a reference voltage range of 0.6V to 1.108V and a 4mV adjustment step. Other configurable functions such as voltage slew rate, switching frequency, current-limiting threshold, OCP hiccup/latch-off, OVP auto-recovery/latch-off, auto PSM/PWM and FPWM operating modes can also be set via I²C interface. An integrated 8-bit ADC is implemented to monitor output current and voltage in real time.

The SGM611A121 is available in a Green TQFN-3×4-14L package.

FEATURES

- **2.85V to 18V Operating Input Voltage Range**
- **Adjustable Output Voltage up to 5.5V**
- **12A Continuous Output Current**
- **15A Peak Output Current**
- **1% Internal Reference Voltage Accuracy**
- **I²C-Programmable Internal Reference 0.600V to 1.108V in 4mV Steps**
- **I²C-Programmable Voltage Slew Rate**
- **I²C-Programmable Frequency and Current Limit**
- **I²C-Programmable OCP Hiccup/Latch-Off**
- **I²C-Programmable OVP Auto-Recovery/Latch-Off**
- **I²C-Programmable Auto PSM/PWM and FPWM Modes**
- **Four I²C Addresses Selected by A0 Pin**
- **Adjustable Soft-Start Time**
- **Open-Drain Power Good (PG)**
- **Output/Input Over-Voltage Protection (OVP)**
- **Output Over-Current Protection (OCP)**
- **Integrated ADC for Output Voltage and Output Current Monitoring**
- **Available in a Green TQFN-3×4-14L Package**

APPLICATIONS

Enterprise SSDs
SoC, FPGA and DSP Cores
Networking/Severs
Industry Machines

TYPICAL APPLICATION

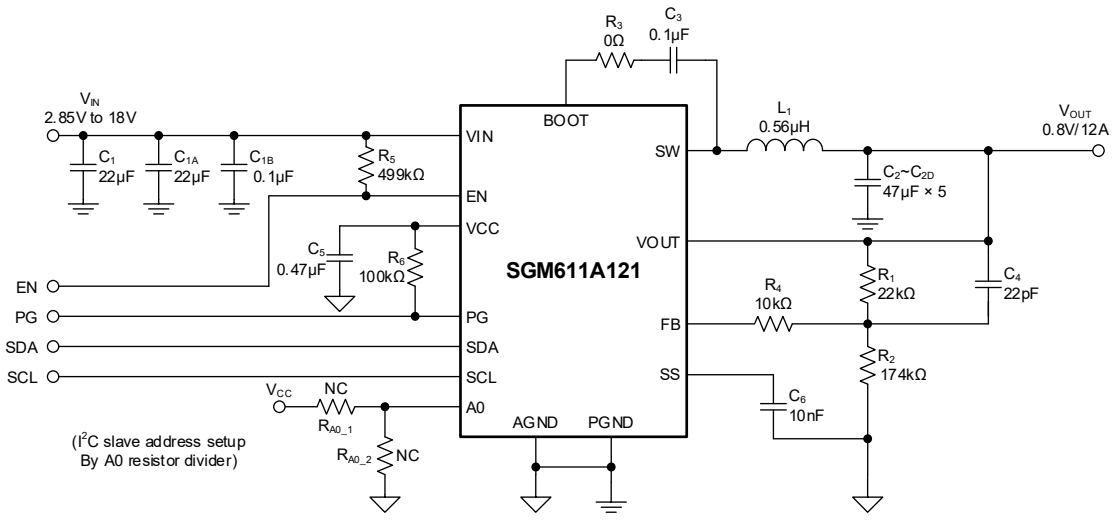


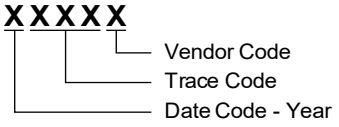
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM611A121	TQFN-3×4-14L	-40℃ to +125℃	SGM611A121XTXM14G/TR	611A121 XTXM14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltage Range
- VIN ..... -0.3V to 19V
- SW ..... -0.3V to V_{IN} + 0.3V
- SW (AC, 10ns Transient) ..... -5V to 25V
- BOOT ..... V_{SW} + 4V
- EN 19V
- VOUT 7V
- All Other Pins ..... -0.3V to 4V

Package Thermal Resistance
- TQFN-3×4-14L, θ_{JA} ..... 53.6℃/W
- TQFN-3×4-14L, θ_{JB} ..... 4.5℃/W
- TQFN-3×4-14L, θ_{JC} ..... 32.1℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 2.85V to 18V
Output Voltage Range, V_{OUT} ..... 0.6V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

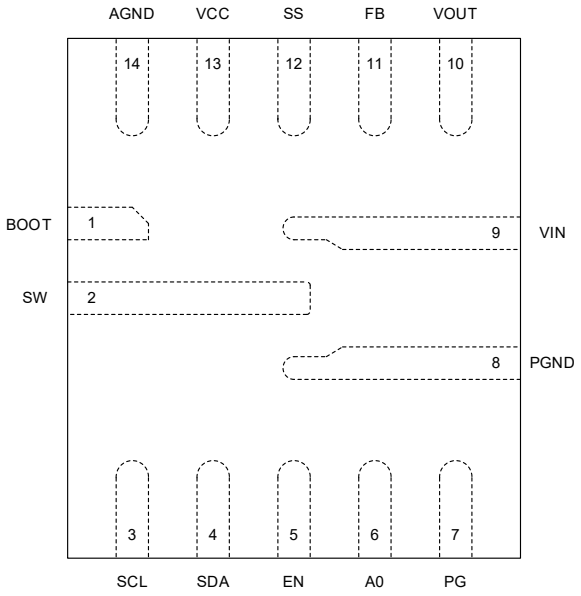
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×4-14L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	BOOT	P	Bootstrap Input to Supply the High-side Gate Driver. A ceramic capacitor (0.1μF) is required between the BOOT and SW pins.
2	SW	P	Switching Node. Connect SW pin to the output inductor.
3	SCL (2)	DI	I²C Clock Signal. Use a pull-up resistor to the logic high rail.
4	SDA (2)	DIO	I²C Data Signal. Use a pull-up resistor to the logic high rail.
5	EN	AI	Enable. Logic high sets the device active. Internally integrated 2MΩ pull-down resistor, can be directly connected to VIN pin. Device is disabled when EN pin is pulled down. Do not leave this pin floating.
6	A0	AI	I²C Address Selection. Four device addresses can be configured via external voltage-divider resistors, with an integrated 2.2MΩ pull-down resistor inside the chip.
7	PG	DO	Power Good Open-Drain Output. If the output voltage is exceed the regulation limit, this pin is pulled low. Leave this pin floating when not in use.
8	PGND	P	Power Ground.
9	VIN	P	Power Input. Place the input capacitors as close as possible to the VIN and PGND pins.
10	VOUT	AI	Output Voltage Sense. It must be connected to output voltage positive terminal nearby the output capacitors.
11	FB	AI	Feedback Input. The output voltage can be programmed by connecting this pin to the midpoint of a resistor divider.
12	SS	AI	Soft-Start Pin. An external capacitor between this pin and AGND pin is used to set the soft-start time.
13	VCC (3)	AO	Internal LDO Output. It needs to be decoupled with a 0.47μF capacitor between this pin and AGND pin.
14	AGND	P	Analog Ground. AGND must be connected to the PGND plane.

NOTES:

1. AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.
2. The SCL/SDA pins do not have a timeout protection mechanism, but they do have a stuck protection mechanism.
3. VCC can only supply pull-up power for the PG signal and is not allowed to power other devices.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Shutdown)	I_{SD}	V_{EN} = 0V, T_J = -40℃ to +100℃		2.3	7.5	μA
		V_{EN} = 0V, T_J = -40℃ to +125℃			18	
Supply Current (Quiescent)	I_Q	No switching, FB = 105% V_{REF}, PSM mode		550	820	μA
High-side Switch On-Resistance	R_{DSON_HS}	$V_{BOOT-SW}$ = 3.3V		12.6		mΩ
Low-side Switch On-Resistance	R_{DSON_LS}	V_{CC} = 3.4V		4.7		mΩ
Switch Leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 12V		0.45		μA
Low-side Valley Current Limit	I_{LIMIT_L}	Adjustable by I²C, T_J = +25℃	11.5	15	19	A
Low-side Negative Current Limit (1)	I_{LIMIT_LN}	In forced PWM mode or OVP state		-6.6		A
Low-side ZCD Threshold	I_{ZCD}			160		mA
Switching Frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 1V	400	500	600	kHz
	f_{SW2}	V_{IN} = 12V, V_{OUT} = 5V	400	500	600	
Minimum Off Time (2)	t_{OFF_MIN}			162		ns
Minimum On Time (2)	t_{ON_MIN}			68		ns
Reference Voltage	V_{REF}	T_J = +25℃		720		mV
		T_J = -40℃ to +125℃	-1		1	%
FB Current	I_{FB}	V_{FB} = 740mV		1	50	nA
A0 Voltage Threshold 1	V_{ADD_1}	Set I²C address 0x61H			0.24	V_{CC}
A0 Voltage Threshold 2	V_{ADD_2}	Set I²C address 0x63H	0.28		0.48	V_{CC}
A0 Voltage Threshold 3	V_{ADD_3}	Set I²C address 0x65H	0.53		0.72	V_{CC}
A0 Voltage Threshold 4	V_{ADD_4}	Set I²C address 0x67H	0.77			V_{CC}
A0 to GND Pull-Down Resistor	R_{A0_PD}			2.2		MΩ
EN Rising Threshold	V_{EN_R}		1.1	1.2	1.3	V
EN Threshold Hysteresis	V_{EN_HYS}			100		mV
EN to GND Pull-Down Resistor	R_{EN}			2		MΩ
VIN Under-Voltage Lockout Threshold Rising	$V_{IN\_UVLO\_R}$		2.55	2.65	2.75	V
VIN Under-Voltage Lockout Threshold Falling	$V_{IN\_UVLO\_F}$		2.4	2.5	2.6	V
Power Good UV Threshold Rising	$V_{PG\_UV\_R}$	Good	86%	90%	94%	V_{REF}
Power Good UV Threshold Falling	$V_{PG\_UV\_F}$	Fault	81%	85%	89%	V_{REF}
Power Good OV Threshold Rising	$V_{PG\_OV\_R}$	Fault	111%	115%	119%	V_{REF}
Power Good OV Threshold Falling	$V_{PG\_OV\_F}$	Good	101%	105%	109%	V_{REF}
Power Good Deglitch Time	t_{PG}	I²C programmable		32		μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
OVP Rising Threshold	V_{OVP_R}	FB voltage rise	121%	125%	129%	V_{REF}
OVP Falling Threshold	V_{OVP_F}	FB voltage fall	106%	110%	114%	V_{REF}
OVP Deglitch	t_{OVP}			5		μs
Output Pin Absolute OV	V_{OVP2}	Output voltage rise	6	6.5	7	V
UVP Threshold	$V_{FB\_UV\_th}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP Deglitch	t_{UVP}			1.7		μs
Soft-Start Current	I_{SS}		4	7.6	11	μA
VCC Voltage	V_{CC}			3.4		V
VCC Load Regulation	V_{CC_REG}	I_{CC} = 20mA			0.5	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL/SDA High-Level Input Voltage	V_{IH}		1.2			V
SCL/SDA Low-Level Input Voltage	V_{IL}				0.4	V
SCL/SDA Hysteresis of Schmitt Trigger Inputs	V_{HYS}			230		mV
SDA Low-Level Output Voltage (Open-Drain) at 3mA Sink Current	V_{OL}				30	mV
SDA Low-Level Output Current	I_{OL}				3	mA
Thermal Shutdown (2)	T_{TSD}	Temperature rise		160		℃
Thermal Hysteresis (2)	T_{TSD_HYS}			20		℃

NOTES:

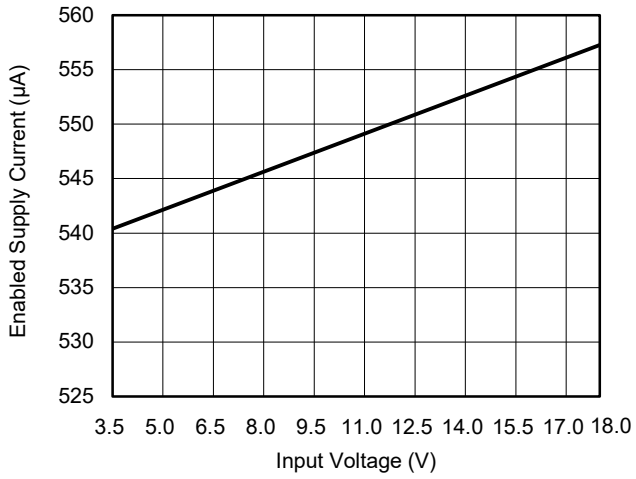
1. The parameter is typically relatively large in characteristic testing.
2. Guaranteed by design and characterization test.

I²C INTERFACE TIMING CHARACTERISTICS

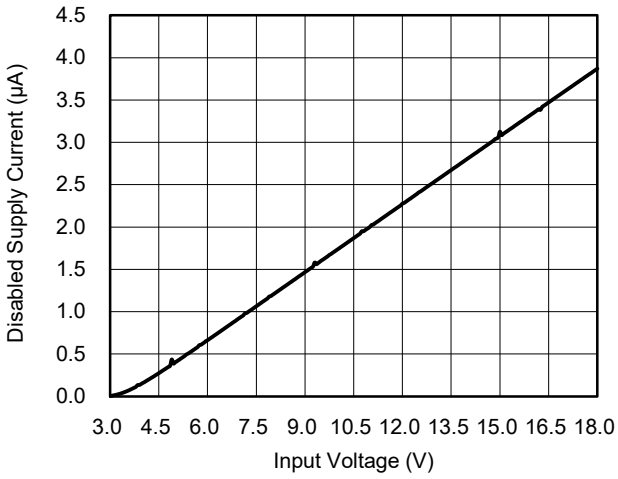
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		100	100	400		1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4		0.6		0.26		μs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		0.5		μs
High Period of SCL Clock	t_{HIGH}	4		0.6		0.26		μs
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4.7		0.6		0.26		μs
Data Setup Time	$t_{SU;DATA}$	250		100		50		ns
Data Hold Time	$t_{HD;DATA}$	0		0		0		μs
Rising Time of SCL Clock	t_{RCL}		1000	20	300		120	ns
Falling Time of SCL Clock	t_{FCL}		300		300		120	ns
Rising Time of SDA Clock	t_{RDA}		1000	20	300		120	ns
Falling Time of SDA Clock	t_{FDA}		300		300		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4		0.6		0.26		μs
Bus Free Time between a STOP and a START Condition	t_{BUF}	4.7		1.3		0.5		μs
Data Valid Time	t_{VD_DAT}		3.45		0.9		0.45	μs
Data Valid Acknowledge Time	t_{VD_ACK}		3.45		0.9		0.45	μs

TYPICAL PERFORMANCE CHARACTERISTICS

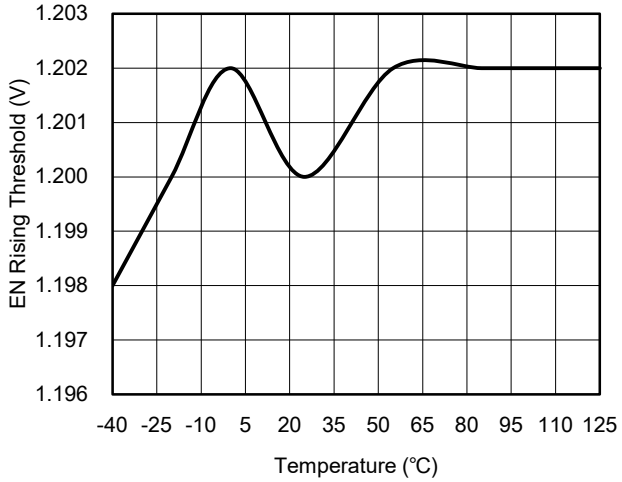
Enabled Supply Current vs. Input Voltage



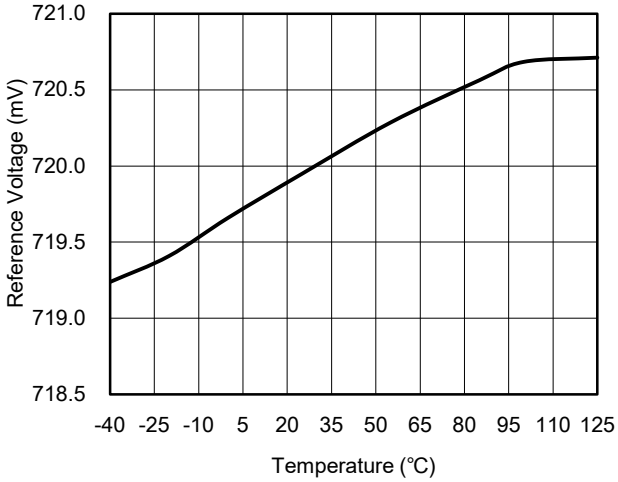
Disabled Supply Current vs. Input Voltage



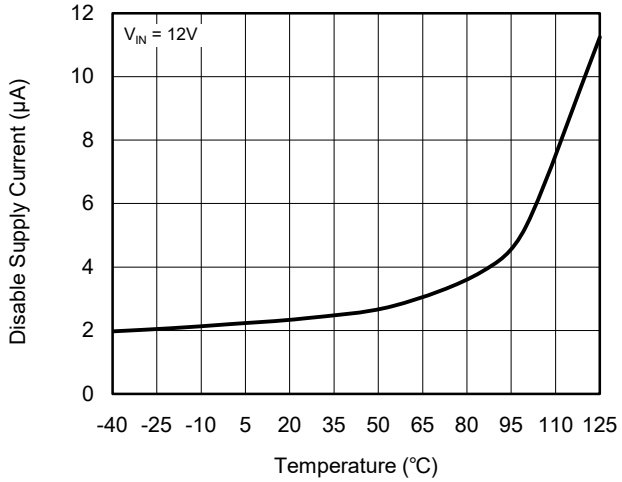
EN Rising Threshold vs. Temperature



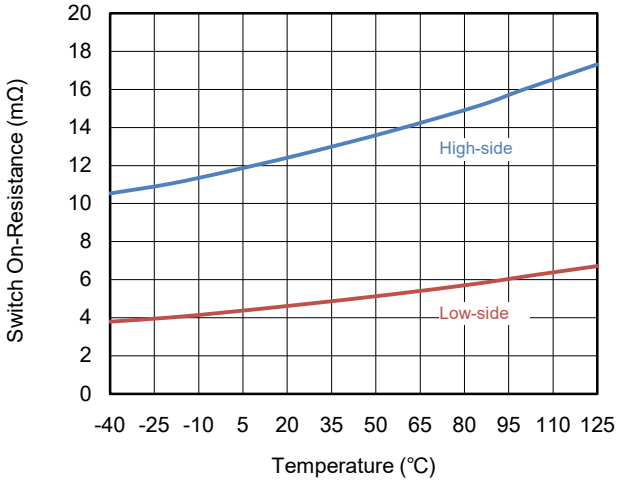
Reference Voltage vs. Temperature



Disable Supply Current vs. Temperature



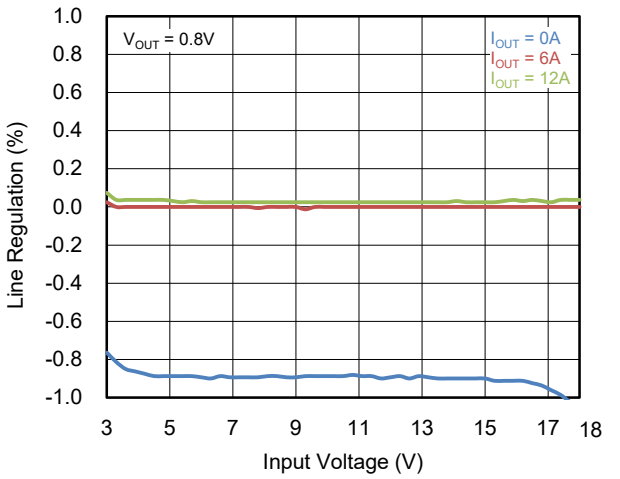
Switch On-Resistance vs. Temperature



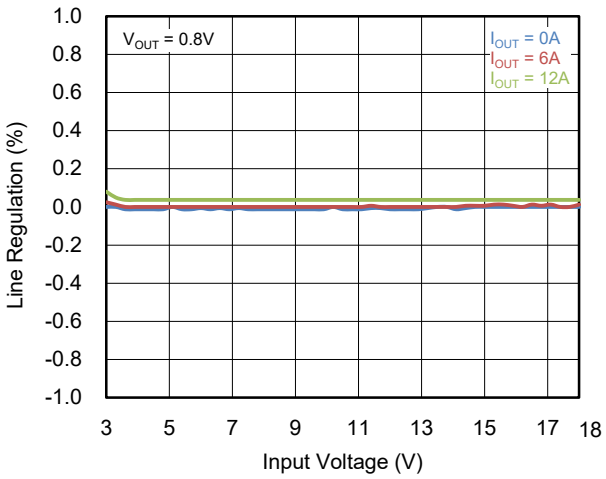
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

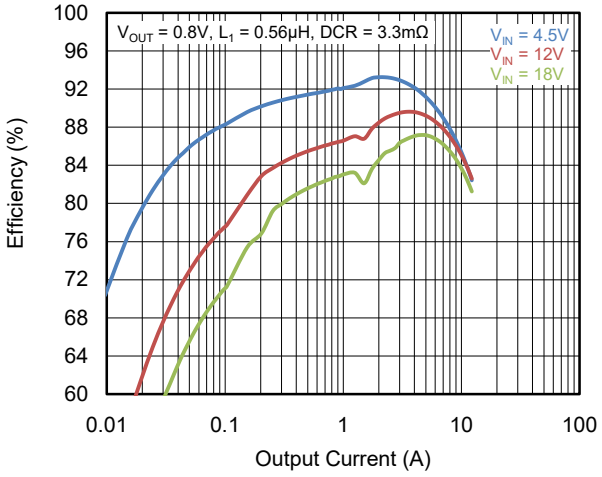
Line Regulation vs. Input Voltage (Auto PSM/PWM Mode)



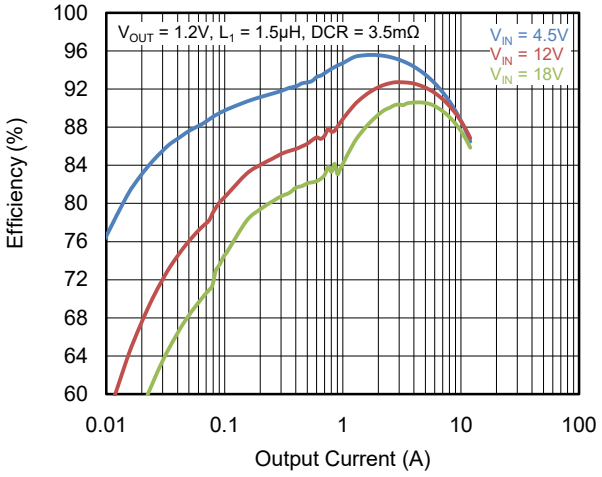
Line Regulation vs. Input Voltage (FPWM)



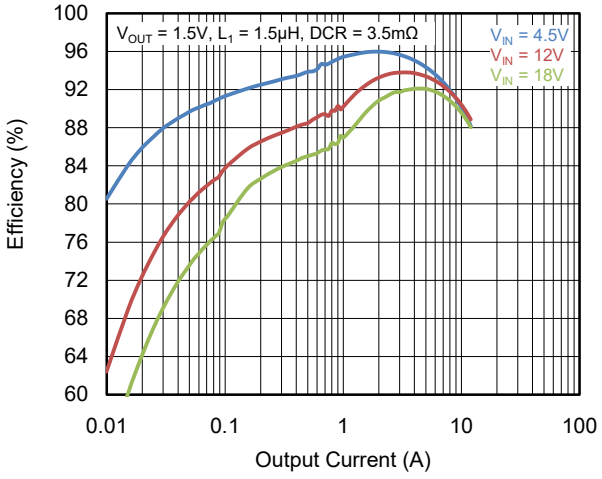
Efficiency vs. Output Current



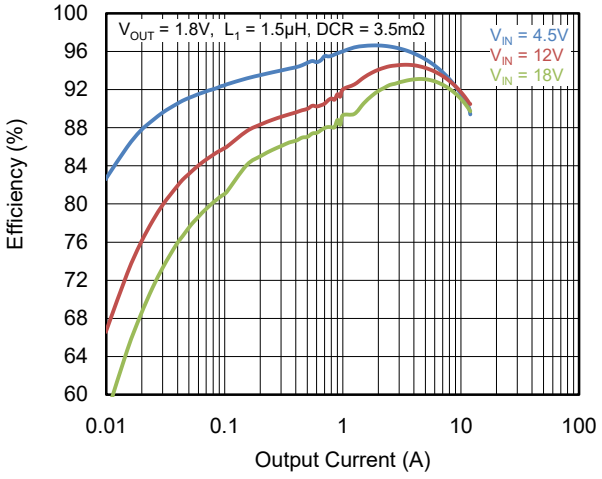
Efficiency vs. Output Current



Efficiency vs. Output Current



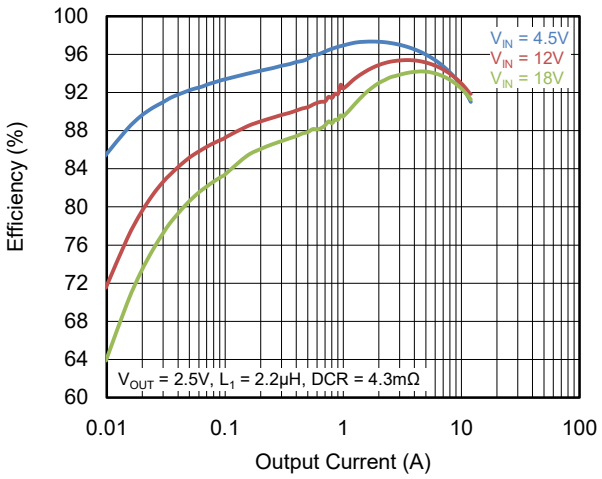
Efficiency vs. Output Current



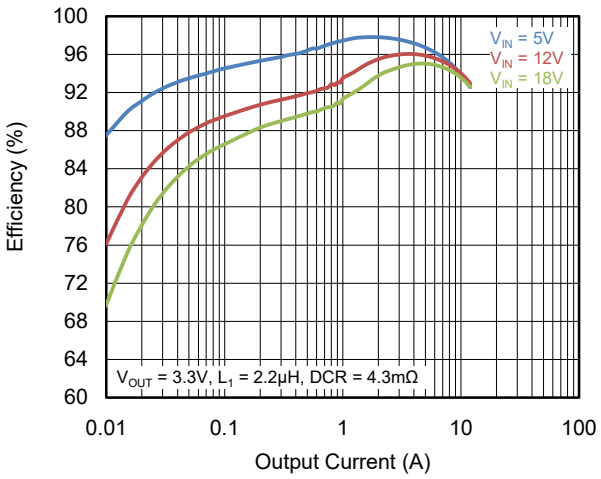
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

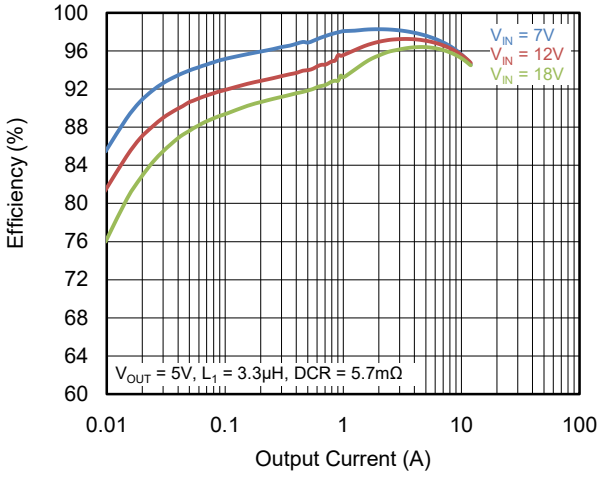
Efficiency vs. Output Current



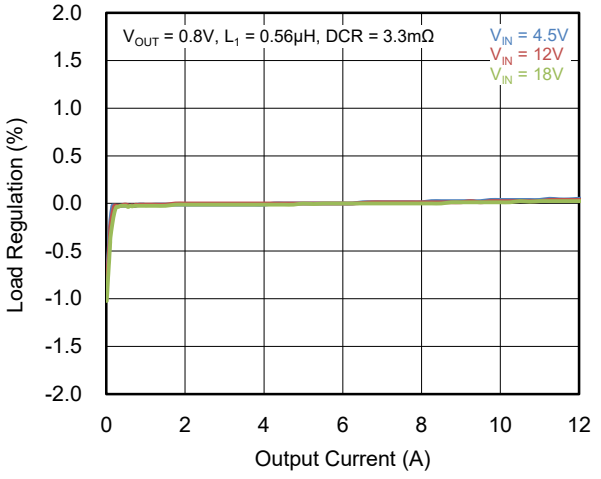
Efficiency vs. Output Current



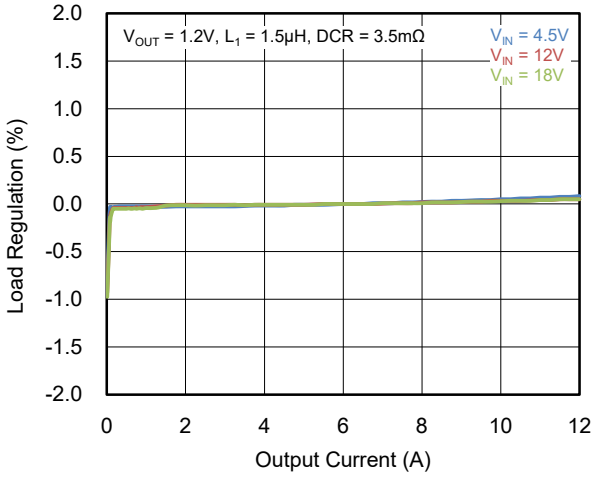
Efficiency vs. Output Current



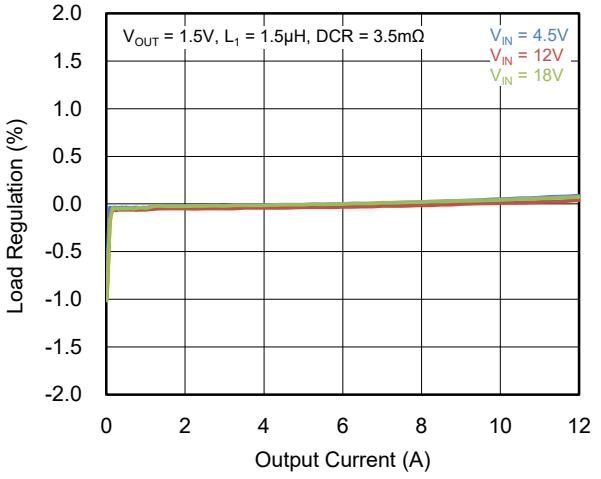
Load Regulation vs. Output Current



Load Regulation vs. Output Current



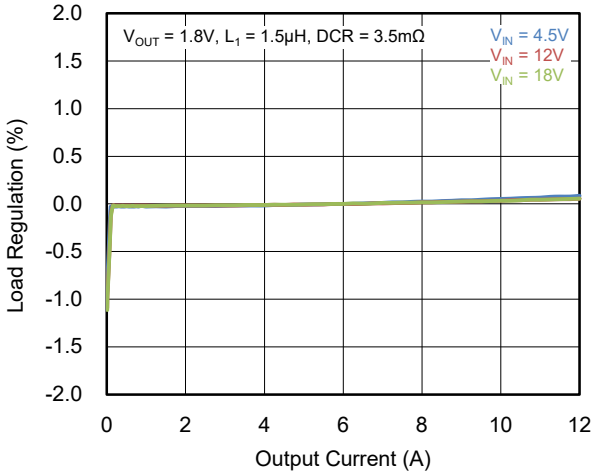
Load Regulation vs. Output Current



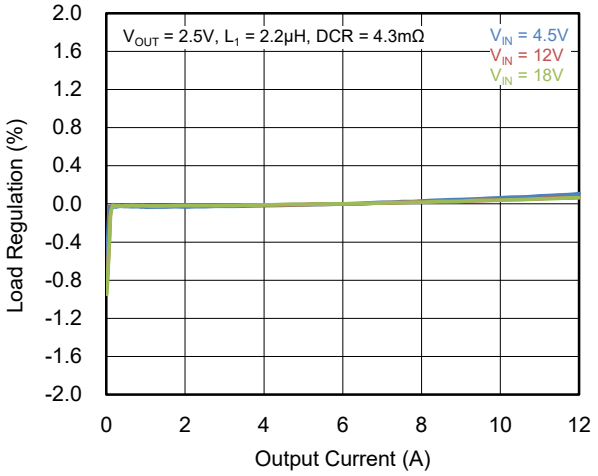
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

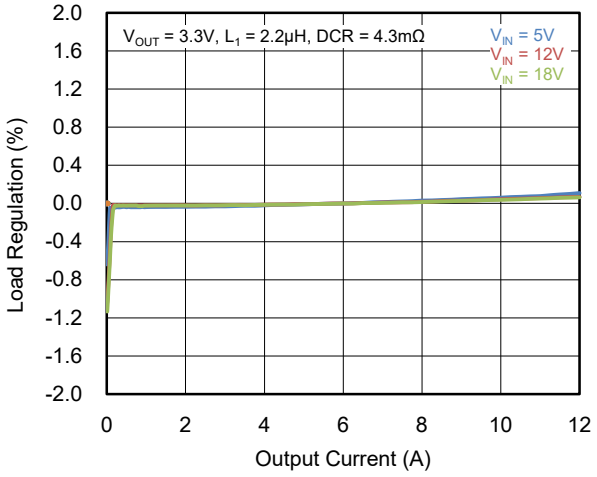
Load Regulation vs. Output Current



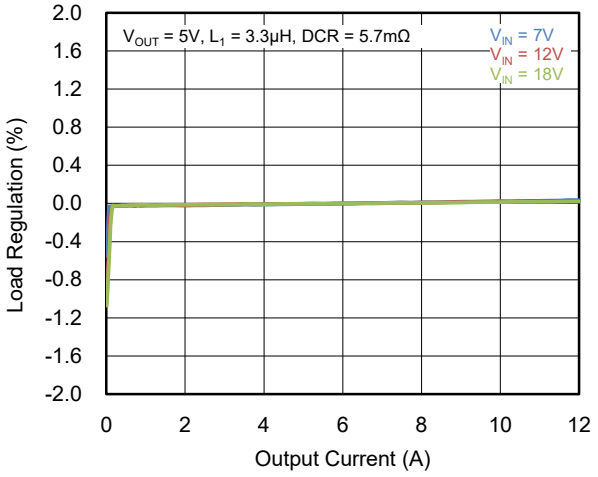
Load Regulation vs. Output Current



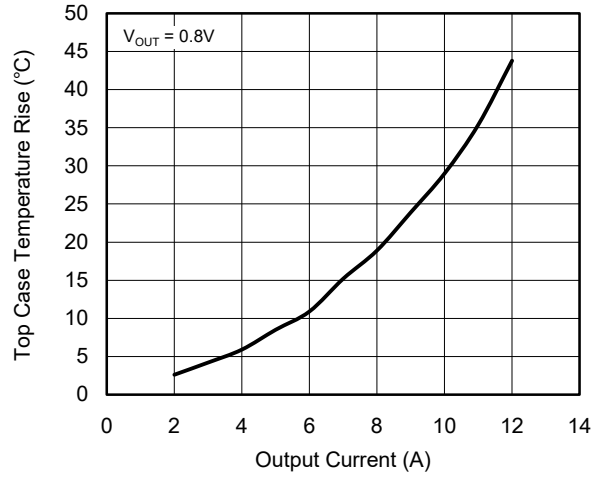
Load Regulation vs. Output Current



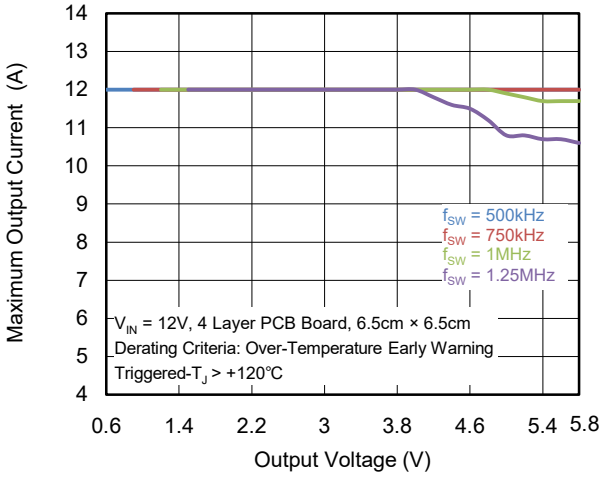
Load Regulation vs. Output Current



Top Case Temperature Rise vs. Output Current



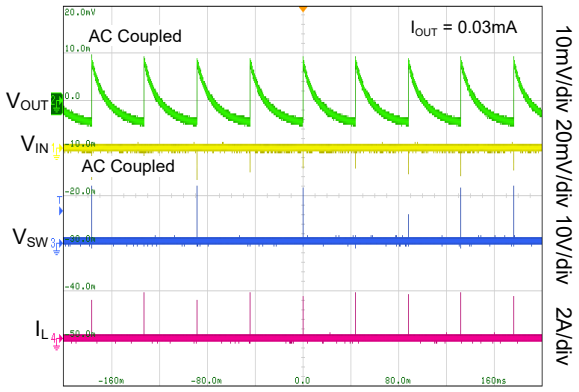
Output Current Derating vs. Frequency and Output Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

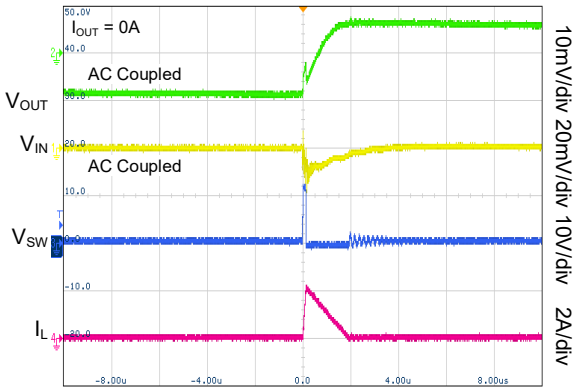
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

Input/Output Ripple



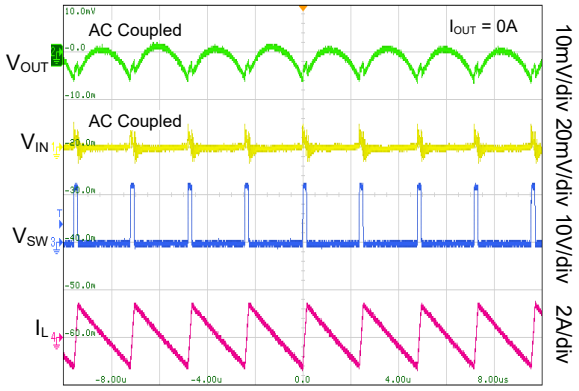
Time (40ms/div)

Input/Output Ripple Zoom In



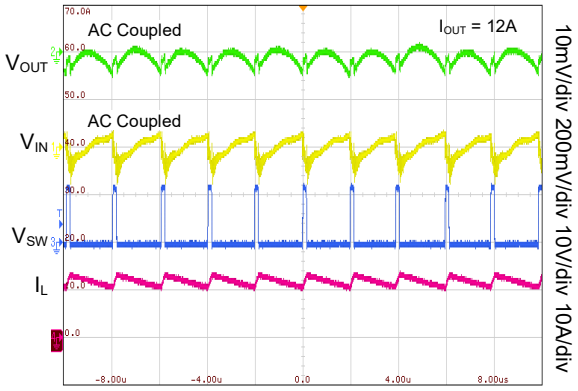
Time (2μs/div)

Input/Output Ripple (FPWM)



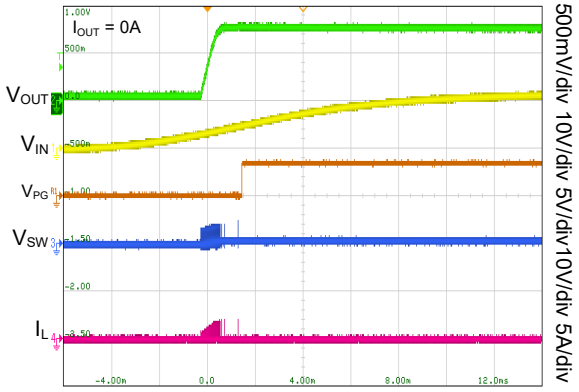
Time (2μs/div)

Input/Output Ripple



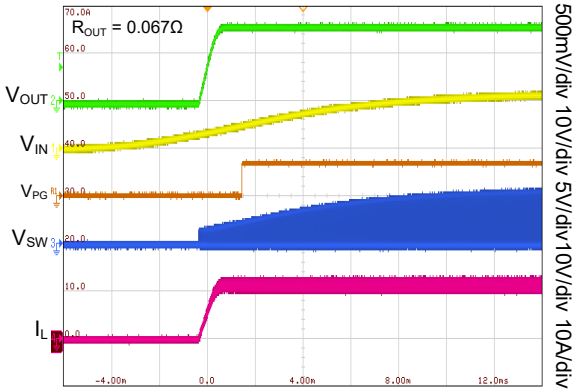
Time (2μs/div)

Startup with Input Voltage Rising



Time (2ms/div)

Startup with Input Voltage Rising

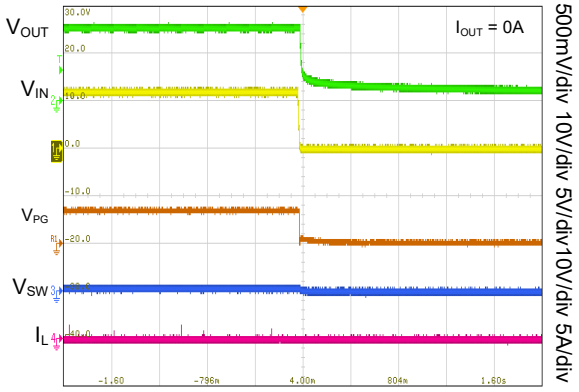


Time (2ms/div)

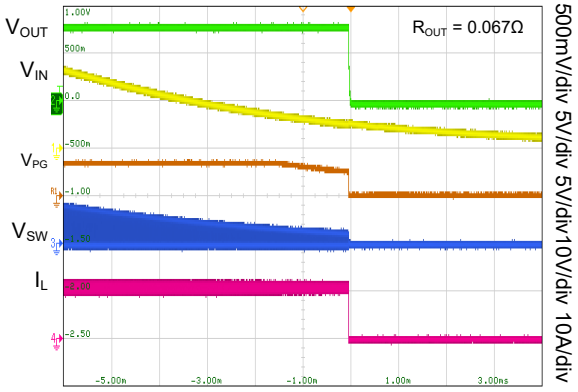
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

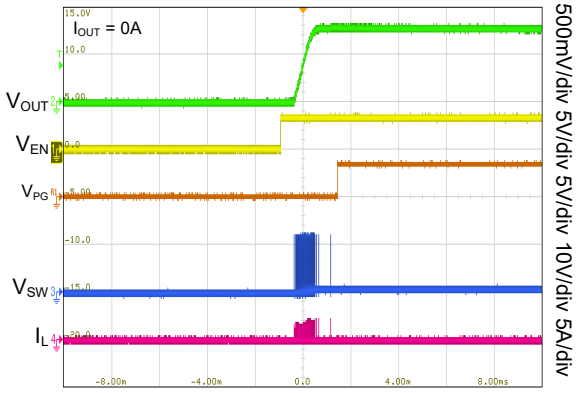
Shutdown with Input Voltage Falling



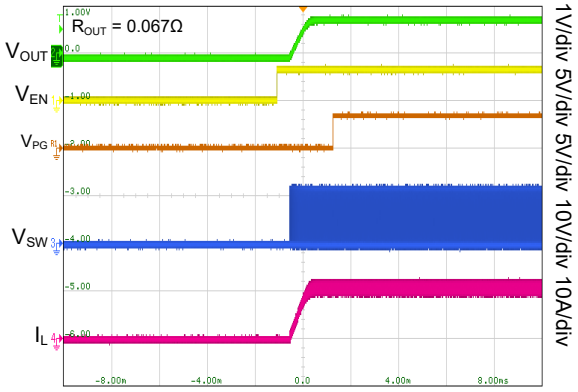
Shutdown with Input Voltage Falling



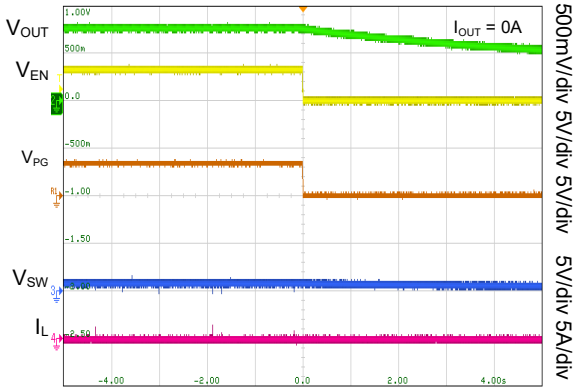
Startup by EN



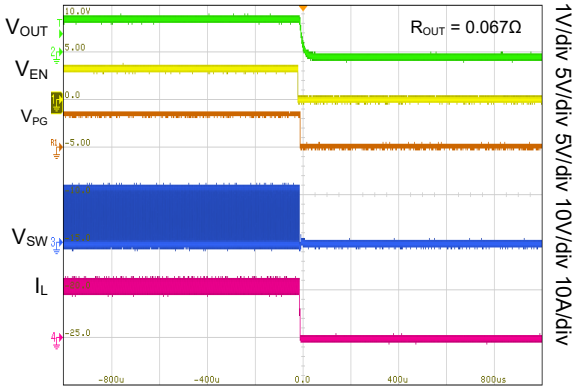
Startup by EN



Shutdown by EN



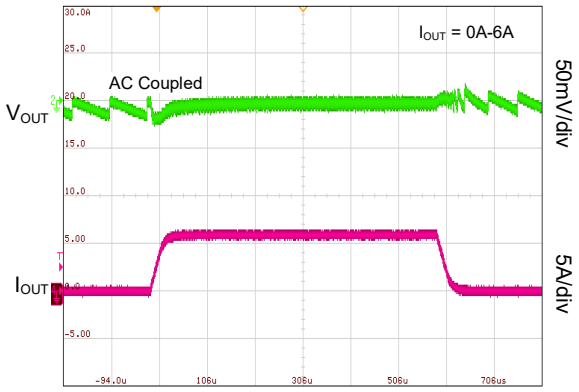
Shutdown by EN



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

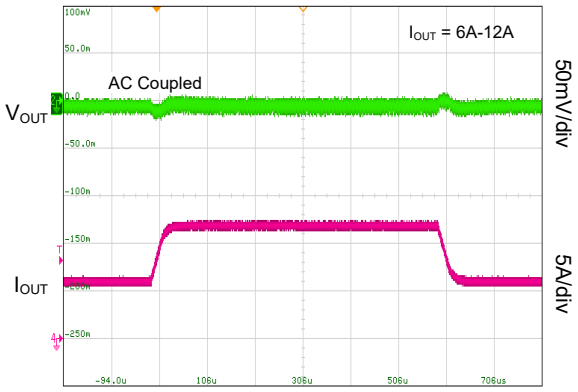
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 0.8V, L_1 = 0.56μH, DCR = 3.3mΩ, f_{SW} = 500kHz, auto PSM/PWM mode, unless otherwise noted.

Load Transient



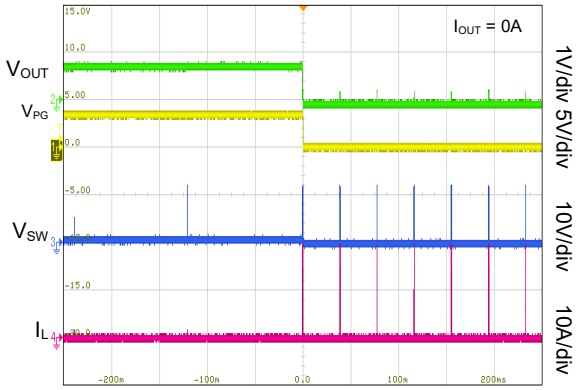
Time (100μs/div)

Load Transient



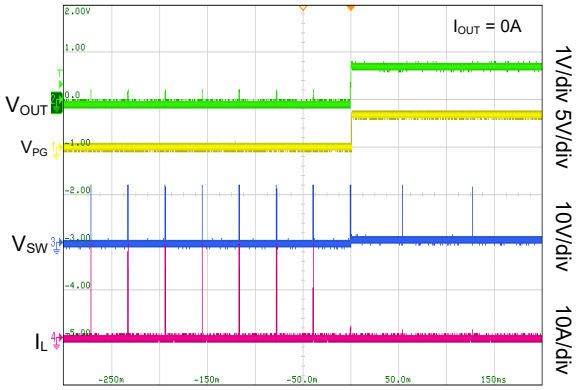
Time (100μs/div)

Short-Circuit Protection Entry



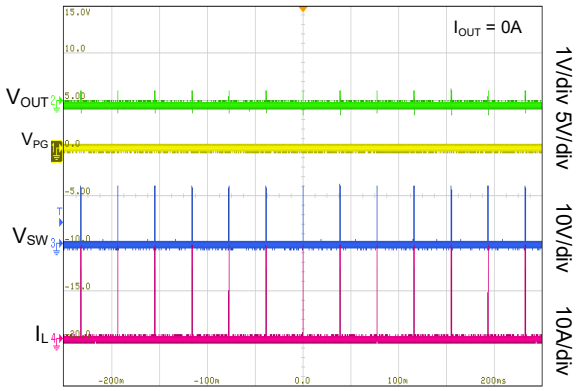
Time (50ms/div)

Short-Circuit Protection Recovery



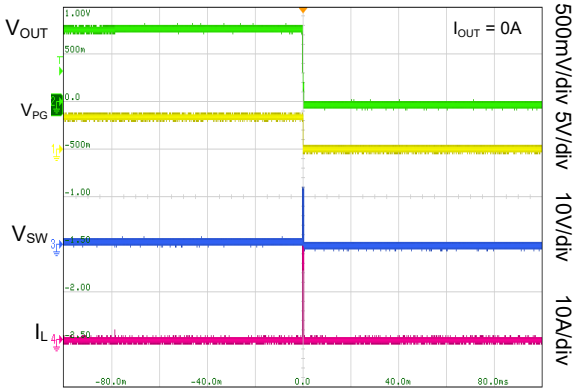
Time (50ms/div)

Short-Circuit Protection Steady State (Short Output to GND)



Time (50ms/div)

Short-Circuit Protection Entry (Latch-Off Mode)



Time (20ms/div)

FUNCTIONAL BLOCK DIAGRAM

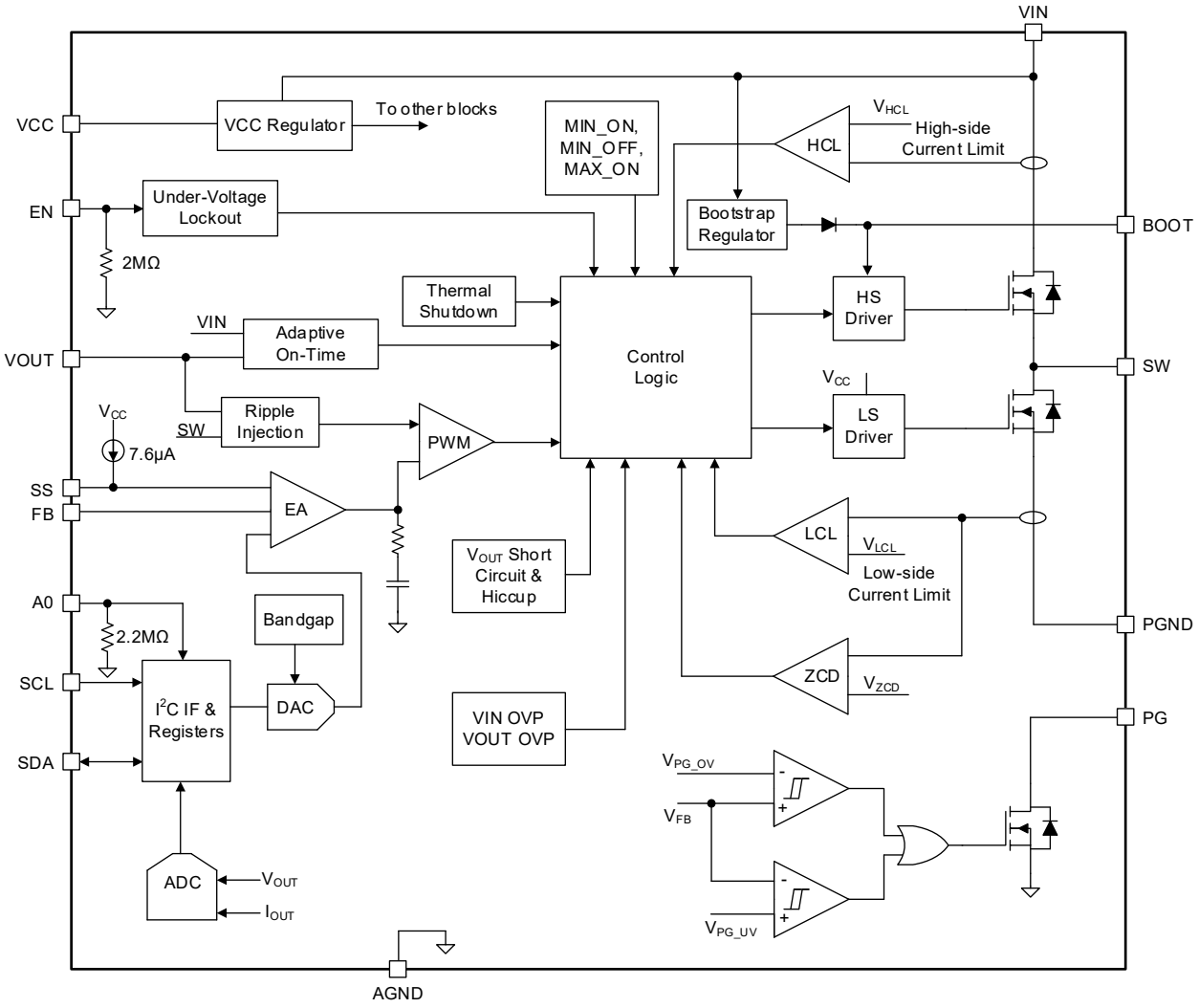


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

SGM611A121 is a high-efficiency synchronous Buck converter with integrated internal power MOSFETs and an I²C control interface. It adopts COT architecture and advanced regulation topology. By default, the device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current decreases, it goes into power saving mode (PSM) to achieve high-efficiency by reducing switching frequency and minimizing quiescent current. The operation mode seamlessly transitions between PWM and PSM to maintain high-efficiency over the entire load range. In PWM mode, the device operates at a typical 500kHz switching frequency.

Under-Voltage Lockout (UVLO)

To prevent malfunction of the device at low input voltages, under-voltage lockout is implemented to shut down the device when input voltage drops below $V_{IN\_UVLO\_F}$. When the input voltage rises above $V_{IN\_UVLO\_R}$, the device will recover to normal operation with a 150mV hysteresis.

Device Enable and Disable (EN)

The EN pin controls device startup and shutdown, including the I²C module. It is enabled by setting the EN pin input to higher than 1.2V. It is disabled when EN pin falls lower than 1.1V. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set target voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off to reduce the device current to 2.3μA. The EN pin features an internal pull-down resistor (typical 2MΩ) to ensure that it remains at the appropriate level. When the I²C interface is active, the start and stop control of the power stage can be achieved by setting the EN bit through I²C.

VCC Regulator

When the EN pin is pulled HIGH, a low-dropout regulator (LDO) powered by the VIN startup to power a portion of the internal circuit. This LDO has a fixed output voltage of 3.4V and accepts an input voltage up to 18V. When the input voltage drops below 3.4V, the output voltage follows the input voltage. A 470nF ceramic capacitor (0603 size) must be placed between the VCC pin and the AGND pin. VCC is intended solely to power the pull-up network for the PG signal and must not be used to supply other circuits.

Soft-Start/Stop and Pre-Bias Startup

An internal soft-start circuit prevents input inrush current and input voltage sags during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.72V, default) upon exiting shutdown or under-voltage lockout (UVLO). The gradual rise of the output voltage limits inrush current while charging the output capacitors, ensuring a smooth output voltage transition. Additionally, soft-start mitigates input voltage drops, which is critical when powering from high-impedance sources such as primary and rechargeable batteries.

The output voltage ramp slope is determined by the external capacitor connected to the SS pin. Reducing the capacitor value shortens the startup time. However, an excessively small value of the capacitor will result in significant overshoot of the output voltage and excessive inrush current during the startup process. If the device enters shutdown (EN pin = LOW or EN bit = 0), UVLO, or thermal shutdown, the SS pin is internally pulled LOW via a resistor. A new soft-start cycle initiates automatically once the device exits these states.

The SGM611A121 supports safe startup into a pre-biased output capacitor upon power-up or enablement. When the device is turning on, a bias on the output may exist due to other sources connected to the load(s) such as multi-rail ICs or simply because of residual charge on the output capacitors. For example, when a device with light load is disabled and quickly re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without pre-biased startup capability, the device cannot start up properly. During the pre-biased startup, switching is inhibited until the internally ramped soft-start reference exceeds the pre-biased voltage. The device then initiates normal operation until the output reaches the regulation target.

By setting the soft-stop control bit to 1 (default is 0), the device can activate the soft-stop function. When this feature is enabled, the output voltage linearly discharges to near 0V in approximately one-fourth of the predefined soft-start duration when the device is disabled by EN pin and EN bit.

DETAILED DESCRIPTION (continued)

Reference Voltage Regulation

Via the I²C interface, the feedback reference voltage can be programmed in the range of 0.600V to 1.108V, with a default value of 0.720V and an adjustable step size of 4mV. The slew rate of the feedback reference voltage can be dynamically programmed via the I²C interface too. Never write to the reference voltage register or the slew rate register while an existing voltage scaling operation is in progress.

Power Good (PG)

The device integrates an independent power good (PG) monitor circuit. The PG pin is forced to a low logic level when the device enters EN shutdown, UVLO, and thermal shutdown states. The PG pin switches to high-impedance state once FB voltage rises up to 90% of the reference voltage, and is pulled low once FB voltage drops below typical 85% of the reference voltage. For over-voltage warning protection, when the FB voltage exceeds 115% of the reference voltage, the PG pin outputs low level. After the FB voltage falls back to 105% of the reference voltage, the PG pin automatically restores to the high-impedance state.

Designed as an open-drain output structure, this pin supports a maximum sinking current rating of 4mA. Table 1 clarifies the state switching rules of the PG pin under all typical operating scenarios. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. If PG function is not used, connect the pin to ground or leave it unconnected, mount an external pull-up resistor to a logic power rail with a maximum voltage limit of 4V.

The response deglitch time for state toggle of this power status pin is configurable through the I²C communication interface, with a factory default deglitch parameter set to 32 μs.

Table 1. PG Output State in Different Conditions

Device Information		PG State	
		High-Z	Low
Output Regulation State	$V_{PG\_OV\_F} \geq V_{FB} \geq V_{PG\_UV\_R}$	√	
	$V_{FB} \leq V_{PG\_UV\_F}$		√
	$V_{FB} \geq V_{PG\_OV\_R}$		√
Shutdown by EN	EN pin = LOW or EN bit = 0		√
Thermal Shutdown	$T_J > T_{TSD}$		√
UVLO	$1V < V_{IN} < V_{IN\_UVLO\_F}$		√
Power Supply Removal	$V_{IN} < 1V$	Uncertain	

Selectable Frequency

The switching frequency of the SGM611A121 is dynamically configurable via the I²C interface. Four preset frequency options are available: 500kHz, 750kHz, 1MHz, and 1.25MHz, selected using configuration bits D[5:4] in register 0x02. At low output voltage settings, it is easy to enter the minimum on-time limit (t_{ON_MIN}) of the high-side MOSFET as the input voltage increases. To ensure stable regulation under these conditions, the maximum allowable switching frequency can be calculated using Equation 1:

$$f_{SW\_MAX} = \frac{1}{t_{ON\_MIN}} \times \frac{V_{OUT}}{V_{IN\_MAX}} \quad (1)$$

where:

f_{SW_MAX} is the maximum switching frequency (MHz) limited by minimum on-time of HS.

t_{ON_MIN} is the minimum on-time (μs) of HS.

V_{IN_MAX} is the maximum input DC voltage.

When the output voltage approaches the input voltage, it is easy to enter the minimum off-time limit (t_{OFF_MIN}) of the high-side MOSFET as the input voltage decreases. This leads to the actual switching frequency not reaching the programmed frequency. The valid range for selecting the switching frequency can be calculated according to the Equation 2:

$$f_{SW\_MAX} = \frac{V_{IN\_MIN} - V_{OUT} - I_{OUT\_MAX} \times \left(R_{DCR} + R_{DSON\_HS}\right)}{t_{OFF\_MIN} \times \left(V_{IN\_MIN} - I_{OUT\_MAX} \times \left(R_{DSON\_HS} - R_{DSON\_LS}\right)\right)} \quad (2)$$

where:

f_{SW_MAX} is maximum switching frequency (MHz) limited by minimum off-time of HS.

V_{IN_MIN} is the minimum input DC voltage.

I_{OUT_MAX} is the maximum output DC current.

R_{DCR} is the DC resistance value (Ω) of the inductor.

R_{DSON_HS} is the high-side MOSFET on-resistance (Ω)

R_{DSON_LS} is the low-side MOSFET on-resistance (Ω)

t_{OFF_MIN} is the minimum off-time (μs) of HS.

When performing the calculations described above, sufficient design margin is strongly recommended. The value of t_{ON_MIN} must be maintained above 100ns, and the value of t_{OFF_MIN} must exceed 270ns.

DETAILED DESCRIPTION (continued)

I²C Slave Address Setting

To accommodate multiple peripherals sharing an I²C bus, the A0 pin acts as a configurable I²C address selection pin. By connecting a resistive voltage divider between the VCC and GND, a stable reference potential can be set. This reference voltage is fed into the A0 pin to flexibly adjust the device I²C address (as shown in Figure 3). The chip will automatically identify and match the corresponding communication address according to the voltage level detected at the A0 pin. This address will be locked immediately after the device completes startup. During I²C bus communication, the host controller sends a 7-bit device address combined with a read/write control bit (the least significant bit, 0 for write operation and 1 for read operation) to form a complete command byte. The voltage division thresholds for A0 and the mapped I²C addresses are listed in Table 2 for design reference.

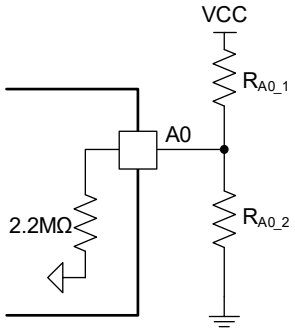


Figure 3. I²C Slave Address Setting

Table 2. I²C Slave Address Set by A0 Resistor Divider

R_{A0_1} (kΩ)	R_{A0_2} (kΩ)	I²C Slave Address	
		Binary	Hex
No connect	No connect	0b1100 001	0x61H
499	300	0b1100 011	0x63H
300	499	0b1100 101	0x65H
100	No connect	0b1100 111	0x67H

Auto Power Saving Mode (PSM)/Pulse Width Modulation (PWM) Mode

As the load current decreases, the inductor current transitions from continuous conduction mode (CCM) to discontinuous conduction mode (DCM). Under COT control, the on-time t_{ON} of the switch in COT mode remains fixed, while the off-time extends correspondingly, causing the switching frequency to decline. When the load current is further reduced, the SGM611A121 series automatically enters the power saving mode. In this mode, the device maintains high-efficiency by lowering the switching frequency and operating at a minimum quiescent current. During PSM operation, the inductor current is discontinuous and the output voltage is marginally lower than the nominal regulated value. The switching frequency drops substantially with decreasing load current under PSM mode.

During medium and heavy loads, the inductor current enters CCM. The device operates in pulse width modulation (PWM) mode with constant on-time control. The nominal switching frequency of the device is determined by the corresponding configuration set via the I²C communication interface.

Forced PWM Mode (FPWM)

Via the I²C communication interface, the device can also be configured to operate in forced pulse width modulation (FPWM) mode by setting the relevant mode control bit to 1. Under light load conditions, the inductor current can enter the negative range when the low-side power switch is turned on. If the current hits the low-side sinking current limit (-6.6A, typical), the low-side switch will be forcibly turned off to protect the circuit. By default, the mode control bit is set to 0.

Switch Current Limits and Short-Circuit Protection (Hiccup)

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the high-side current limit threshold, the HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak.

If 64 consecutive cycles of this current-limiting action occur and V_{FB} falls below $V_{FB\_UV\_th}$, an automatic soft restart (hiccup mode) will be initiated after a typical delay of 40ms. The hiccup cycle repeats until the overload or output short-circuit fault is cleared.

If the device powers on and attempts to start with an output short-circuit condition present, the I²C interface can not be activated until the short-circuit fault is cleared following a normal startup sequence. If REG0x01 D[1] is set to 0 via I²C (default value is 1), the device will enter a latched-off state when hiccup mode is triggered. The device can be released from the latch-off state by reapplying power to V_{IN}, re-enabling the EN pin, or setting the EN bit via the I²C interface.

DETAILED DESCRIPTION (continued)

Output and Input Over-Voltage Protection (V_{OUT} OVP and V_{IN} OVP)

The device integrates an output voltage (V_{OUT}) over-voltage protection circuit to suppress excessive overshoot of the output voltage during steady-state operation. Typically, the output voltage will spike when overload is removed, which immediately triggers the V_{OUT} OVP function. To limit such overshoot amplitudes, the device continuously monitors the feedback voltage at the FB pin and compares it against the internal V_{OUT} OVP threshold. V_{OUT} OVP protection activates when the FB voltage rises above 125% (typical) of the internal reference voltage, at which point the device switches to PWM mode to stabilize output voltage.

During V_{OUT} OVP regulation, the inductor current may enter the negative range, which can cause charging of the input supply capacitor. If the input voltage (V_{IN}) exceeds 18.5V (typical) either during V_{OUT} OVP triggering or the soft-stop process, the device will enter the V_{IN} OVP state, and both the high-side (HS) and low-side (LS) power switches will be disabled simultaneously. Two OVP response modes are configurable via the I² C interface: OVP auto-recovery (default) and OVP latch-off.

In the OVP auto-recovery mode, once the input voltage falls below the V_{IN} OVP release threshold and the output voltage drops to clear the V_{OUT} OVP condition (the FB voltage falls below 110% typical of the reference voltage), the device can automatically resume normal switching operation. If configured for OVP latch-off mode, the device will remain in a latched shutdown state until the fault is cleared and the device is reset. The device can be released from the latch-off state by reapplying power to V_{IN}, re-enabling the EN pin, or setting the EN bit via the I²C interface. During a V_{OUT} OVP event, the device rapidly regulates the output voltage to a safe level, and the low-side sinking current limit remains fully active to provide additional circuit protection.

Output Absolute Over-Voltage Protection (OVP_ABS)

The device can also monitor the output voltage synchronously to determine whether to enter the output absolute over-voltage protection (OVP_ABS) state. If the output voltage exceeds 6.5V, OVP_ABS will be triggered, and the device will enter the FPWM mode to pull down the output voltage simultaneously. During the OVP_ABS state, the V_{IN} OVP function remains enabled. After V_{IN} OVP is triggered, both HS and LS are turned off. Whether the device automatically resumes operation after the input or output voltage falls below the protection threshold is still controlled by the configuration of the I²C register (1 = OVP auto-recovery).

When both the input voltage and EN voltage are higher than their respective rising thresholds, the absolute OVP detection is initiated immediately.

Thermal Protection and Shutdown

Thermal protection is integrated to safeguard the die from overheating damage. If the junction temperature exceeds T_{TSD} threshold, switching operation ceases and the device enters shutdown mode. Automatic recovery with a soft-start is initiated once the junction cools down to 20℃ below the T_{TSD} limit.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM611A121 parameters and get status reports. I²C is well known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM611A121 operates as a slave device that address is selected by A0 pin. It has seven 8-bit registers, numbered from REG00 to REG06. A register read beyond REG06 (0x06) returns 0xFF.

Physical Layer

The standard I²C interface of SGM611A121 supports standard mode, fast mode and fast mode plus communication speeds. The frequency of standard mode is up to 100kbits/s, the fast mode is up to 400kbits/s, and the fast mode plus is up to 1Mbits/s. Bus lines are pulled high by pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 4. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

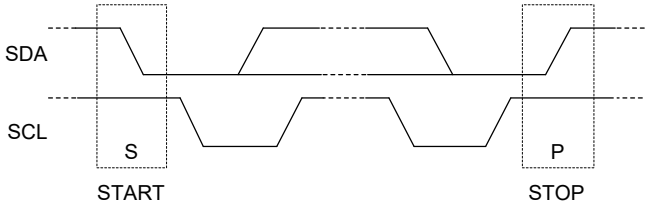


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

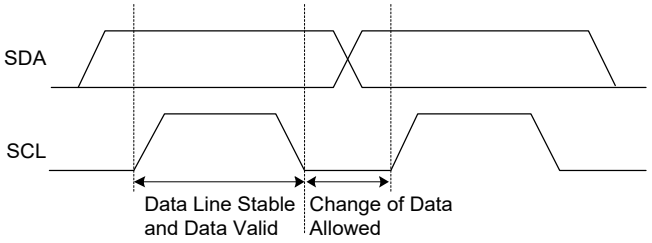


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

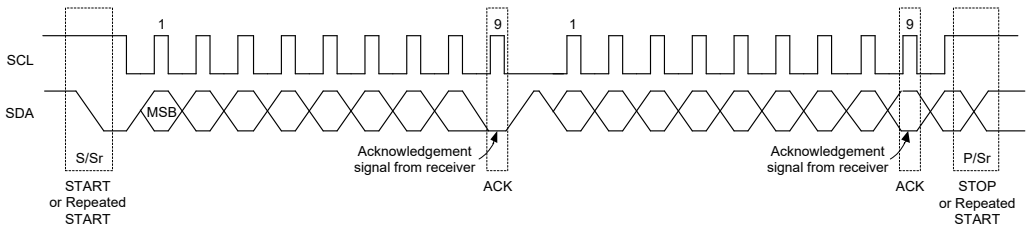


Figure 6. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 9), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

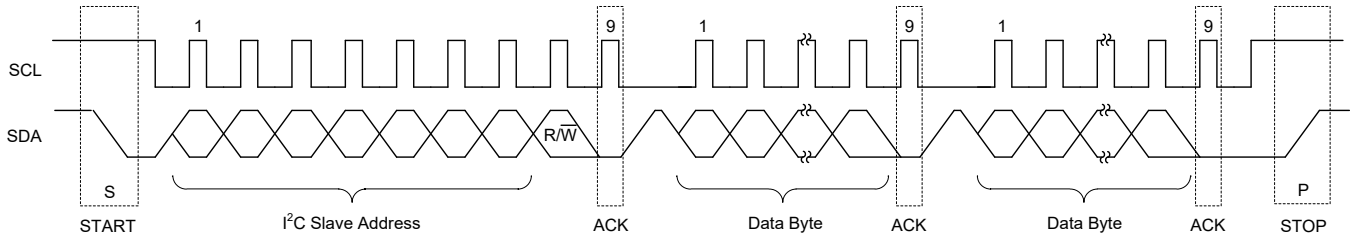


Figure 7. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

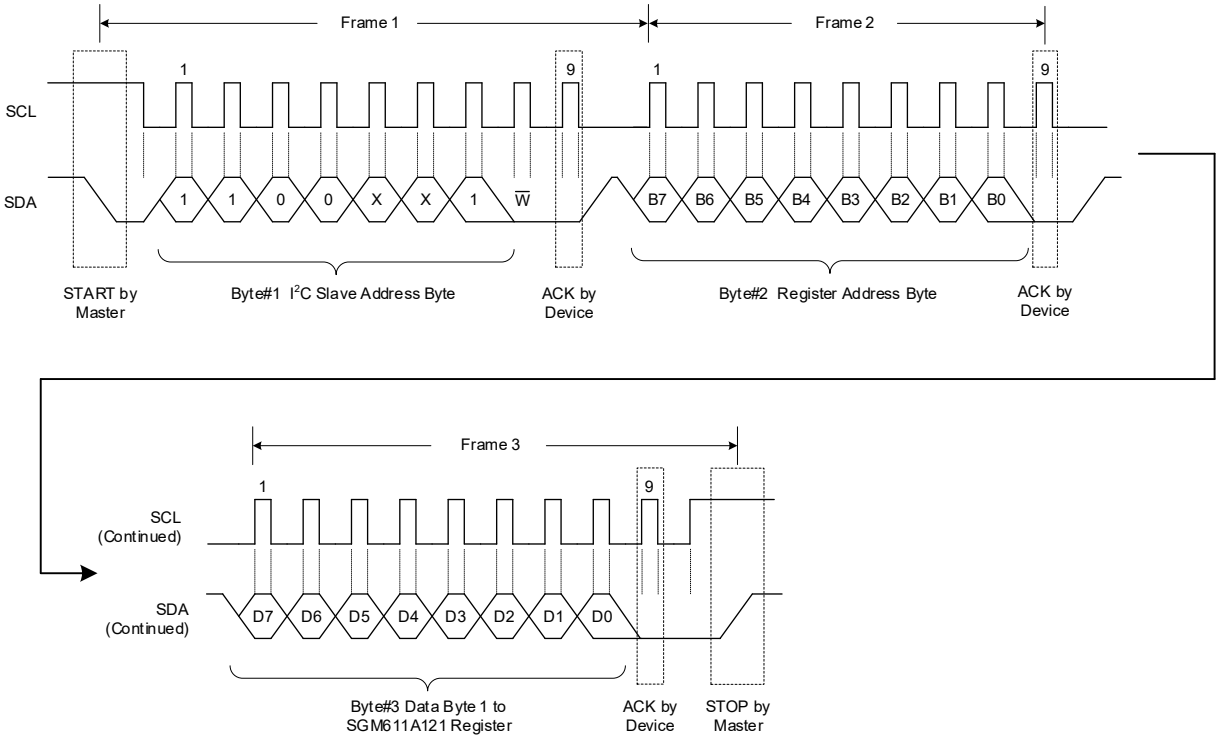


Figure 8. A Single Write Transaction

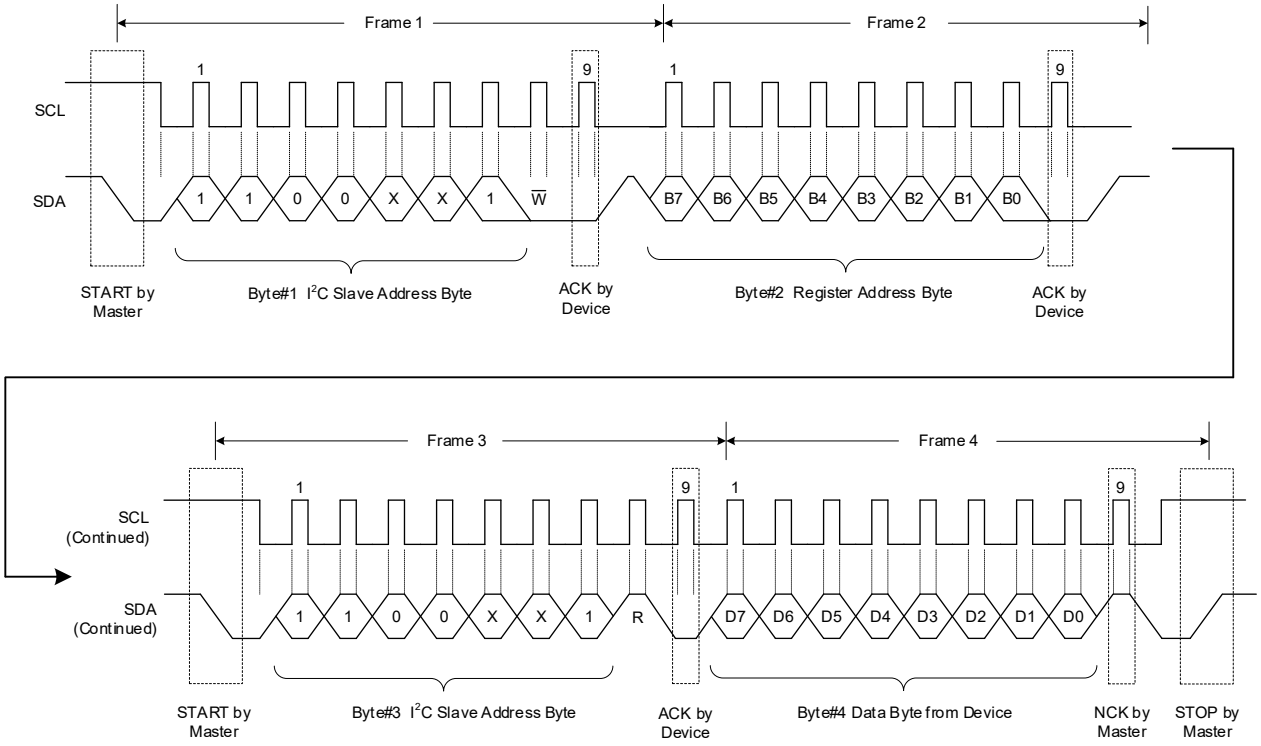


Figure 9. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM611A121 for REG00 through REG06 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers. The multi-write transaction is shown in Figure 10.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition. The multi-read transaction is shown in Figure 11.

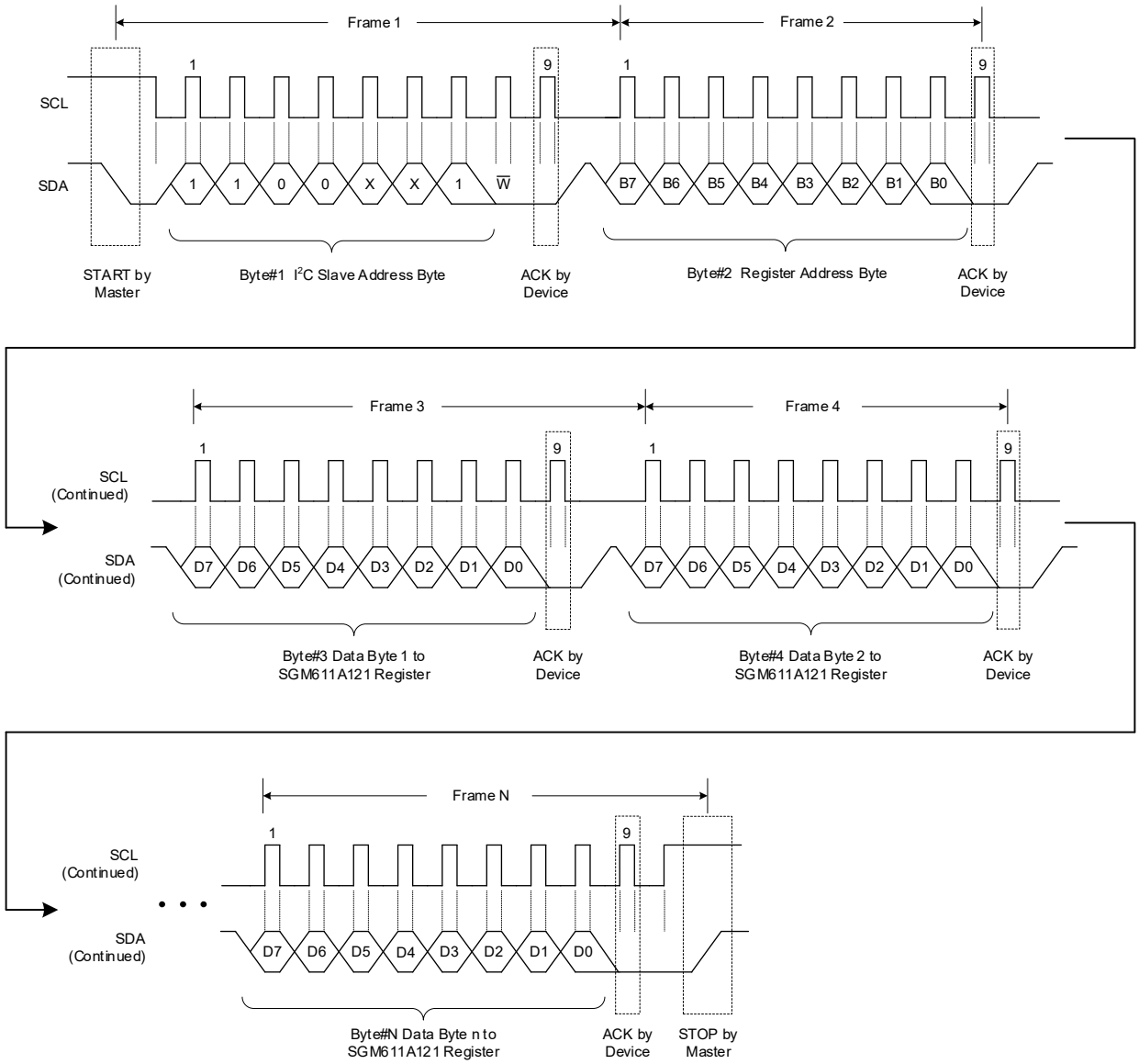


Figure 10. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

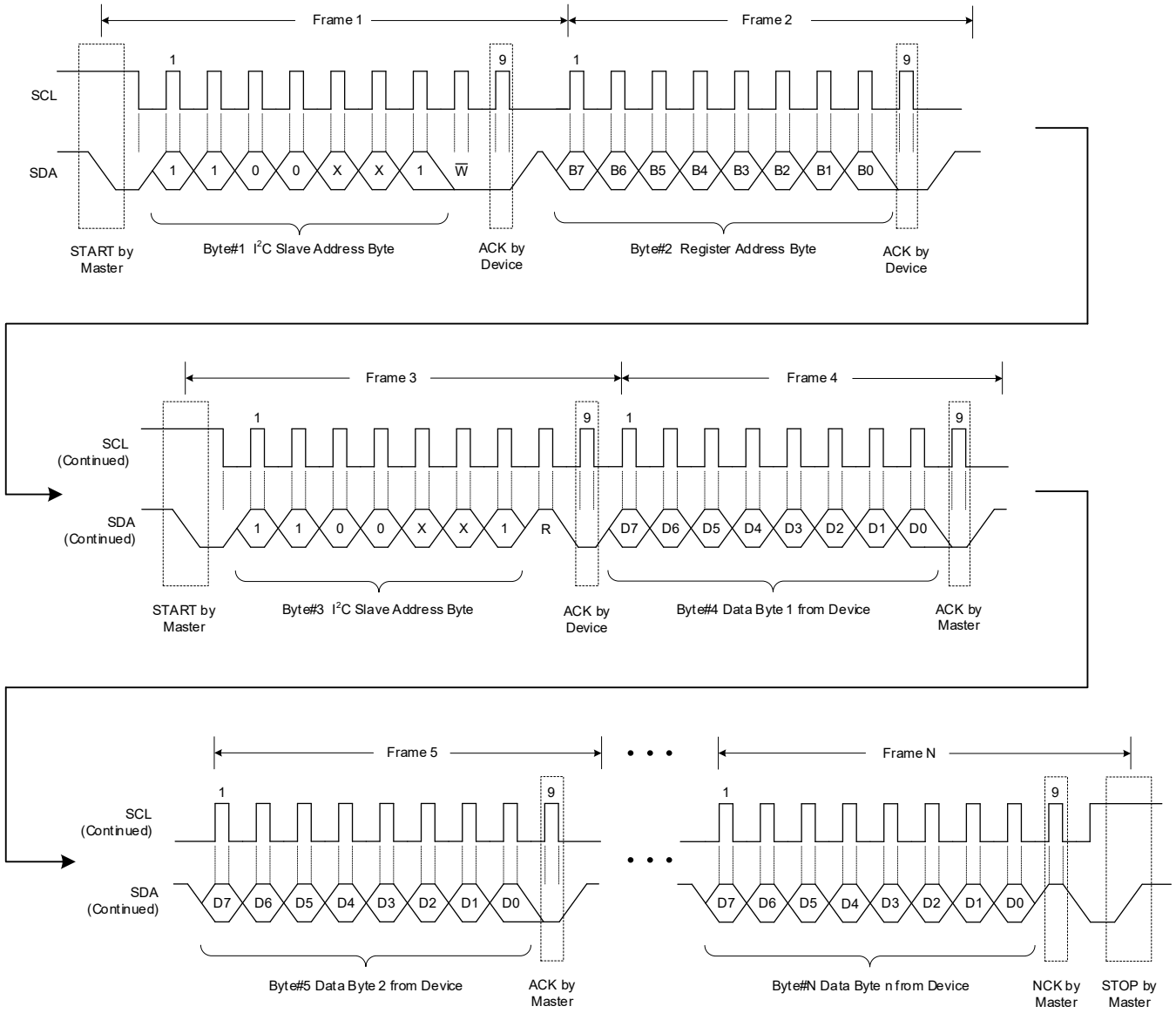


Figure 11. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

I²C Register Address Map

Address	Register Name	Default	TYPE	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	VSEL	0x1E	R/W	Reserved	FB_REF[6:0]						
0x01	SYS_CTRL1	0xA6	R/W	EN	GO_BIT	SR[2:0]			RETRY_OVP_EN	HICCUP_OCP_EN	MODE_FLAG
0x02	SYS_CTRL2	0xC1	R/W	PG_DEG_TIME[1:0]		FREQ[1:0]		SOFT_STOP_EN	VALLY_CURRENT[2:0]		
0x03	Output Current	0x00	R	IOUT[7:0]							
0x04	Output Voltage	0x00	R	VOUT[7:0]							
0x05	ID1	0x7X	R	VENDOR_ID[3:0]				DIE_ID[3:0]			
0x06	STATUS	0xF0	R	Reserved				OC_STAT	OTEW_STAT	OT_STAT	PG_STAT

REG0x00: VSEL Register [Reset = 0x1E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6:0]	FB_REF[6:0]	001 1110	R/W	Feedback Reference Voltage Setting Bits 0000000 = 0.6V 0000001 = 0.604V 0000010 = 0.608V …… 0011110 = 0.72V (default) …… 1111101 = 1.1V 1111110 = 1.104V 1111111 = 1.108V

REGISTER MAPS (continued)

REG0x01: SYS_CTRL1 Register [Reset = 0xA6]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	EN	1	R/W	Enable Command (I²C circuit is shutdown when EN pin is low. This function is only valid when EN pin is high.) 0 = Disable 1 = Enable (default)
D[6]	GO_BIT	0	R/W	I²C Writing Authority Bit of the Feedback Reference Voltage scaling examples: 1. Set the GO_BIT to 1 to initiate voltage scaling. 2. Write to REG0x00 to configure the target feedback reference voltage. 3. The GO_BIT is automatically cleared to 0 upon completion of voltage scaling. The user can read back this bit to verify if voltage adjustment is in progress. 4. To perform a second voltage scaling, set the GO_BIT to 1 again. 5. Rewrite REG0x00 to update the new feedback reference voltage. Do not perform reference voltage scaling again during the reference voltage scaling process.
D[5:3]	SR[2:0]	100	R/W	Voltage Slew Rate Selection 000 = 40mV/μs 001 = 30mV/μs 010 = 20mV/μs 011 = 10mV/μs 100 = 5mV/μs (default) 101 = 2.5mV/μs 110 = 1.25mV/μs 111 = 0.625mV/μs Do not change the voltage slew rate during voltage scaling.
D[2]	RETRY_OVP_EN	1	R/W	OVP Mode Selection 0 = Latch-off (once output OVP and V_{IN} OVP are both triggered) 1 = Auto-recovery (default)
D[1]	HICCUP_OCP_EN	1	R/W	Over-Current Protection Mode Selection 0 = Latch-off 1 = Hiccup (default)
D[0]	MODE_FLAG	0	R/W	Mode Selection 0 = Auto PSM/PWM mode (default) 1 = FPWM mode

REGISTER MAPS (continued)

REG0x02: SYS_CTRL2 Register [Reset = 0xC1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PG_DEG_TIME[1:0]	11	R/W	PG Pin Deglitch Time 00 = 1.6μs 01 = 9μs 10 = 15μs 11 = 32μs (default)
D[5:4]	FREQ[1:0]	00	R/W	Switching Frequency Set Bits 00 = 500kHz (default) 01 = 750kHz 10 = 1MHz 11 = 1.25MHz
D[3]	SOFT_STOP_EN	0	R/W	Soft-Stop after I²C Shutdown Command 0 = Disable (default) 1 = Enable
D[2:0]	VALLY_CURRENT[2:0]	001	R/W	Valley Current Limit 000 = 17A 001 = 15A (default) 010 = 13A 011 = 10.5A 100 = 9A 101 = 7.5A 110 = 6.5A 111 = 5.5A

REG0x03: Output Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IOUT[7:0]	00000000	R	Output Current Monitor Bits 00000000 = 0A (default) 00000001 = 0.05A 00000010 = 0.1A …… 01111000 = 6A 01111001 = 6.05A 01111010 = 6.1A …… 11111101 = 12.65A 11111110 = 12.7A 11111111 = 12.75A

REG0x04: Output Voltage Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	VOUT[7:0]	00000000	R	Output Voltage Monitor Bits Refer to Table 3

REGISTER MAPS (continued)

Table 3. Output Voltage Chart

D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)
0000 0000	0.500	0010 1011	1.367	0101 0110	2.235	1000 0001	3.102	1010 1100	3.969	1101 0111	4.837
0000 0001	0.520	0010 1100	1.387	0101 0111	2.255	1000 0010	3.122	1010 1101	3.989	1101 1000	4.857
0000 0010	0.540	0010 1101	1.408	0101 1000	2.275	1000 0011	3.142	1010 1110	4.010	1101 1001	4.877
0000 0011	0.561	0010 1110	1.428	0101 1001	2.295	1000 0100	3.162	1010 1111	4.030	1101 1010	4.897
0000 0100	0.581	0010 1111	1.448	0101 1010	2.315	1000 0101	3.183	1011 0000	4.050	1101 1011	4.917
0000 0101	0.601	0011 0000	1.468	0101 1011	2.335	1000 0110	3.203	1011 0001	4.070	1101 1100	4.937
0000 0110	0.621	0011 0001	1.488	0101 1100	2.356	1000 0111	3.223	1011 0010	4.090	1101 1101	4.958
0000 0111	0.641	0011 0010	1.509	0101 1101	2.376	1000 1000	3.243	1011 0011	4.110	1101 1110	4.978
0000 1000	0.661	0011 0011	1.529	0101 1110	2.396	1000 1001	3.263	1011 0100	4.131	1101 1111	4.998
0000 1001	0.682	0011 0100	1.549	0101 1111	2.416	1000 1010	3.283	1011 0101	4.151	1110 0000	5.018
0000 1010	0.702	0011 0101	1.569	0110 0000	2.436	1000 1011	3.304	1011 0110	4.171	1110 0001	5.038
0000 1011	0.722	0011 0110	1.589	0110 0001	2.456	1000 1100	3.324	1011 0111	4.191	1110 0010	5.058
0000 1100	0.742	0011 0111	1.609	0110 0010	2.477	1000 1101	3.344	1011 1000	4.211	1110 0011	5.079
0000 1101	0.762	0011 1000	1.630	0110 0011	2.497	1000 1110	3.364	1011 1001	4.231	1110 0100	5.099
0000 1110	0.782	0011 1001	1.650	0110 0100	2.517	1000 1111	3.384	1011 1010	4.252	1110 0101	5.119
0000 1111	0.803	0011 1010	1.670	0110 0101	2.537	1001 0000	3.404	1011 1011	4.272	1110 0110	5.139
0001 0000	0.823	0011 1011	1.690	0110 0110	2.557	1001 0001	3.425	1011 1100	4.292	1110 0111	5.159
0001 0001	0.843	0011 1100	1.710	0110 0111	2.578	1001 0010	3.445	1011 1101	4.312	1110 1000	5.179
0001 0010	0.863	0011 1101	1.730	0110 1000	2.598	1001 0011	3.465	1011 1110	4.332	1110 1001	5.200
0001 0011	0.883	0011 1110	1.751	0110 1001	2.618	1001 0100	3.485	1011 1111	4.352	1110 1010	5.220
0001 0100	0.903	0011 1111	1.771	0110 1010	2.638	1001 0101	3.505	1100 0000	4.373	1110 1011	5.240
0001 0101	0.924	0100 0000	1.791	0110 1011	2.658	1001 0110	3.526	1100 0001	4.393	1110 1100	5.260
0001 0110	0.944	0100 0001	1.811	0110 1100	2.678	1001 0111	3.546	1100 0010	4.413	1110 1101	5.280
0001 0111	0.964	0100 0010	1.831	0110 1101	2.699	1001 1000	3.566	1100 0011	4.433	1110 1110	5.300
0001 1000	0.984	0100 0011	1.851	0110 1110	2.719	1001 1001	3.586	1100 0100	4.453	1110 1111	5.321
0001 1001	1.004	0100 0100	1.872	0110 1111	2.739	1001 1010	3.606	1100 0101	4.473	1111 0000	5.341
0001 1010	1.024	0100 0101	1.892	0111 0000	2.759	1001 1011	3.626	1100 0110	4.494	1111 0001	5.361
0001 1011	1.045	0100 0110	1.912	0111 0001	2.779	1001 1100	3.647	1100 0111	4.514	1111 0010	5.381
0001 1100	1.065	0100 0111	1.932	0111 0010	2.799	1001 1101	3.667	1100 1000	4.534	1111 0011	5.401
0001 1101	1.085	0100 1000	1.952	0111 0011	2.820	1001 1110	3.687	1100 1001	4.554	1111 0100	5.421
0001 1110	1.105	0100 1001	1.972	0111 0100	2.840	1001 1111	3.707	1100 1010	4.574	1111 0101	5.442
0001 1111	1.125	0100 1010	1.993	0111 0101	2.860	1010 0000	3.727	1100 1011	4.595	1111 0110	5.462
0010 0000	1.145	0100 1011	2.013	0111 0110	2.880	1010 0001	3.747	1100 1100	4.615	1111 0111	5.482
0010 0001	1.166	0100 1100	2.033	0111 0111	2.900	1010 0010	3.768	1100 1101	4.635	1111 1000	5.502
0010 0010	1.186	0100 1101	2.053	0111 1000	2.920	1010 0011	3.788	1100 1110	4.655	1111 1001	5.522
0010 0011	1.206	0100 1110	2.073	0111 1001	2.941	1010 0100	3.808	1100 1111	4.675	1111 1010	5.543
0010 0100	1.226	0100 1111	2.093	0111 1010	2.961	1010 0101	3.828	1101 0000	4.695	1111 1011	5.563
0010 0101	1.246	0101 0000	2.114	0111 1011	2.981	1010 0110	3.848	1101 0001	4.716	1111 1100	5.583
0010 0110	1.266	0101 0001	2.134	0111 1100	3.001	1010 0111	3.868	1101 0010	4.736	1111 1101	5.603
0010 0111	1.287	0101 0010	2.154	0111 1101	3.021	1010 1000	3.889	1101 0011	4.756	1111 1110	5.623
0010 1000	1.307	0101 0011	2.174	0111 1110	3.041	1010 1001	3.909	1101 0100	4.776	1111 1111	5.643
0010 1001	1.327	0101 0100	2.194	0111 1111	3.062	1010 1010	3.929	1101 0101	4.796		
0010 1010	1.347	0101 0101	2.214	1000 0000	3.082	1010 1011	3.949	1101 0110	4.816		

REGISTER MAPS (continued)

REG0x05: ID1 Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	VENDOR_ID[3:0]	0111	R	Set to 0111 internally
D[3:0]	DIE_ID[3:0]	1111	R	IC revision.

REG0x06: STATUS Register [Reset = 0xF0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	1111	R	Reserved
D[3]	OC_STAT	0	R	Output Over-Current Indication 0 = Normal (default) 1 = OC fault
D[2]	OTEW_STAT	0	R	Over-Temperature Early Warning 0 = Normal (default) 1 = T_J > +120℃
D[1]	OT_STAT	0	R	Over-Temperature Indication 0 = Normal (default) 1 = Thermal shutdown fault
D[0]	PG_STAT	0	R	Output Power Good Indication 0 = Out of normal range (default) 1 = 95% < V_{OUT} < 115%

APPLICATION INFORMATION

In this section, power supply design with the SGM611A121 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

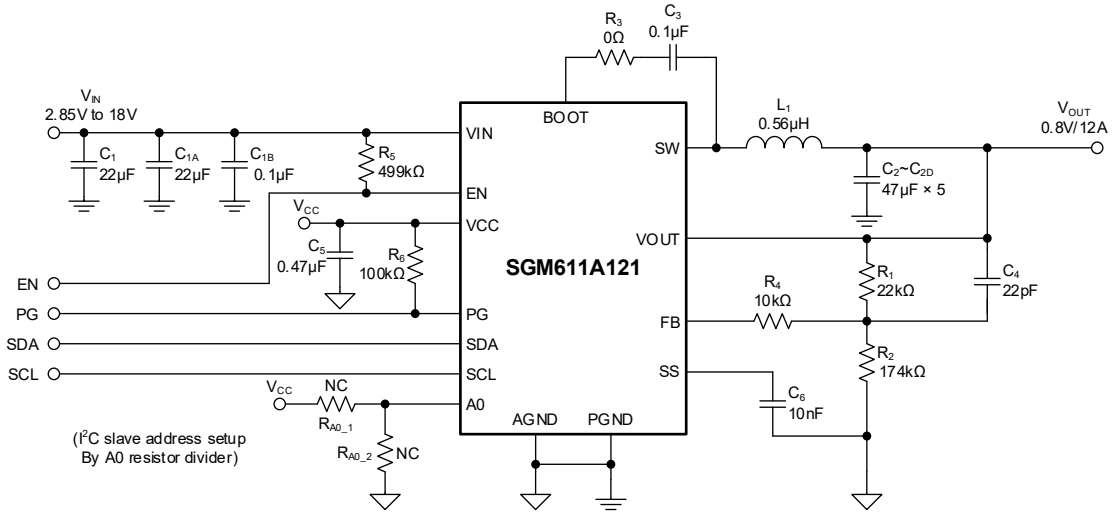


Figure 12. 0.8V Output Voltage Application of SGM611A121

Design Requirements

Table 4 summarizes the requirements for this example as shown in Figure 12. The selected components are given in Table 5.

Table 4. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.85V to 18V
Output Voltage	0.8V
Maximum Output Current	12A
Switching Frequency	500kHz

Table 5. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1, C_{1A}	Ceramic Capacitor, 22μF, 25V, X7S, Size1206, P/N:GRM31CC71E226ME15	muRata
C_{1B}, C_3	Ceramic Capacitor, 0.1μF, 25V, X7R, Size 0603	muRata
C_2~C_{2D}	Ceramic Capacitor, 47μF, 6.3V, X5R, Size 0603, P/N:GRM188R60J476ME15	muRata
C_4	Ceramic Capacitor, 22pF, 50V, C0G, Size 0603	Standard
C_5	Ceramic Capacitor, 0.47μF, 16V, X7R, Size 0603	Standard
C_6	Ceramic Capacitor, 10nF, 25V, X7R, Size 0603	Standard
L_1	0.56μH, Power Inductor, DCR_{MAX} = 3.3mΩ, $I_{SAT(30\%)}$ = 25A, $I_{RMS\ (40℃)}$ = 24A, P/N:WCX0634CR56MT	Sunlord
R_1	22kΩ, Chip Resistor,1/16W, 1%, Size 0603	Standard
R_2	174kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	0Ω, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_4	10kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_5	499kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_6	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Input Capacitor Selection (C_{IN})

Use ceramic capacitors (X5R, X7R, or equivalent types) for decoupling between the VIN and PGND pins. These capacitors must be positioned as close to the IC as physically possible. For typical applications circuits, it is recommended to use two 22μF ceramic capacitors. Designs with long input traces or fast transient load requirements may require extra bulk capacitance, such as 100μF electrolytic or tantalum capacitors. For high-frequency noise suppression, 0.1μF capacitors must be placed directly adjacent to critical VIN and PGND pins on the same PCB layer as the IC. The voltage rating of the capacitors must exceed the maximum input voltage. The total ripple current rating of the input capacitors must exceed the maximum RMS capacitor current calculated from the regulator's operating conditions, including duty cycle and load current, which can be calculated by Equation 3. Increasing the capacitance value helps lower input voltage ripple and enhance overall system stability. Ceramic capacitance decreases under DC bias conditions. For example, a 22μF capacitor may degrade to approximately 6.9μF at 12V input voltage. The input ripple voltage depends on the input capacitance, switching frequency, and duty cycle. Worst-case ripple appears near 50% duty cycle. It can be calculated by Equation 4.

APPLICATION INFORMATION (continued)

$$I_{C\_RMS} = I_{OUT\_MAX} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \quad (3)$$

where:

I_{C_RMS} is the maximum RMS current of capacitor.

I_{OUT_MAX} is the maximum output DC current.

V_{IN_MIN} is the minimum input voltage.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times f_{SW}} \quad (4)$$

where:

ΔV_{IN} is the input ripple voltage peak-to-peak.

I_{OUT_MAX} is the maximum output DC current.

C_{IN} is the effective input capacitance value (μF).

f_{SW} is switching frequency (MHz).

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that raises the converter conduction losses. Conversely, a larger inductance leads to slower transient response and a bigger physical footprint. The inductor saturation current I_{SAT} shall be higher than I_{L_MAX}, with adequate margin maintained. In general, the saturation current above high-side current limit is sufficient. Typically, the peak-to-peak inductor current is designed to be 20% to 40% of the maximum output current. Equation 5 and Equation 6 can be used to select the appropriate inductance value based on ΔI_L. Care shall be taken to prevent triggering of the negative current limit protection under no-load operating conditions.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

Output Capacitor Selection (C_{OUT})

The architecture of the SGM611A121 supports the use of small-form-factor ceramic output capacitors with low equivalent series resistance (ESR). These capacitors are recommended to achieve low output voltage ripple. Generally, ceramic capacitors feature a capacitance tolerance of -20% to +20% relative to the nominal value. To maintain low impedance at high frequencies and minimize capacitance variation across temperature, it is recommended to use X5R or X7R dielectric materials. DC bias voltage can lead to a considerable reduction in ceramic capacitance, with the degree of degradation dependent on capacitor specifications including package size, voltage rating, and temperature characteristics. If the switching frequency is significantly reduced due to the reduction of the input voltage, increasing the output capacitance is recommended to ensure robust system stability.

Steady-state output ripple voltage depends on inductor current ripple and capacitor impedance. The minimum required capacitance is given by Equation 7:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

where:

ΔV_{OUT} is the output ripple voltage (peak-to-peak).

L is the inductance value (μH).

f_{SW} is switching frequency (MHz).

R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

C_{OUT} is the output capacitance value (μF).

Soft-Start Capacitor Selection (C_{SS})

The ramp rate of soft-start output voltage can be adjusted by selecting an external SS capacitor, which is charged by the internal 7.6μA (typical) constant current source. The relationship between soft-start time and capacitance is presented in Equation 8 below:

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{7.6\mu A} \quad (8)$$

where:

C_{SS} is the capacitance value (nF) required at the SS pin.

t_{SS} is the desired soft-start ramp time (ms).

V_{REF} is the internal reference voltage.

Output Voltage Adjustment

Equation 9 can be used to select the feedback resistors (R_1 and R_2) shown in Figure 12, in order to set the target output voltage (V_{OUT}):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (9)$$

APPLICATION INFORMATION (continued)

To prevent excessive noise sensitivity at the FB pin, the resistance of R_2 is recommended to be no more than 200kΩ. A smaller R_2 value (e.g., 10kΩ) delivers stronger noise immunity, but also increases power dissipation in the voltage divider network.

The internal reference voltage V_{REF} is configurable via I^2C, with a default value of 0.72V. Extreme caution must be exercised to ensure the output voltage does not exceed the absolute OVP protection threshold.

The procedure to adjust V_{REF} through I^2C is as follows:

1. Set GO_BIT (REG0x01 D[6]) to 1.

2. Write REG0x00 D[6:0] to configure the target reference voltage.

Upon the configuration is completed, GO_BIT resets to 0 automatically. To perform another adjustment, step 1 must be repeated. Do not initiate a new reference voltage scaling operation while the current scaling process is ongoing.

Bootstrap Capacitor

To sustain stable switching behavior, a 100nF ceramic capacitor should be placed across the BOOT-SW pins, with preference given to components exhibiting minimal DC voltage dependence.

Controlled MOSFET turn-on and transient spike suppression can be achieved by placing a current-limiting resistor in the bootstrap path. Although this scheme dampens switching-edge overshoot, it introduces appreciable efficiency degradation due to elevated conduction losses. Prototype layouts are recommended to include a default 0 Ω short path for the bootstrap circuit to enable subsequent impedance tuning, in the event that PCB parasitics cause switching spikes to exceed device ratings.

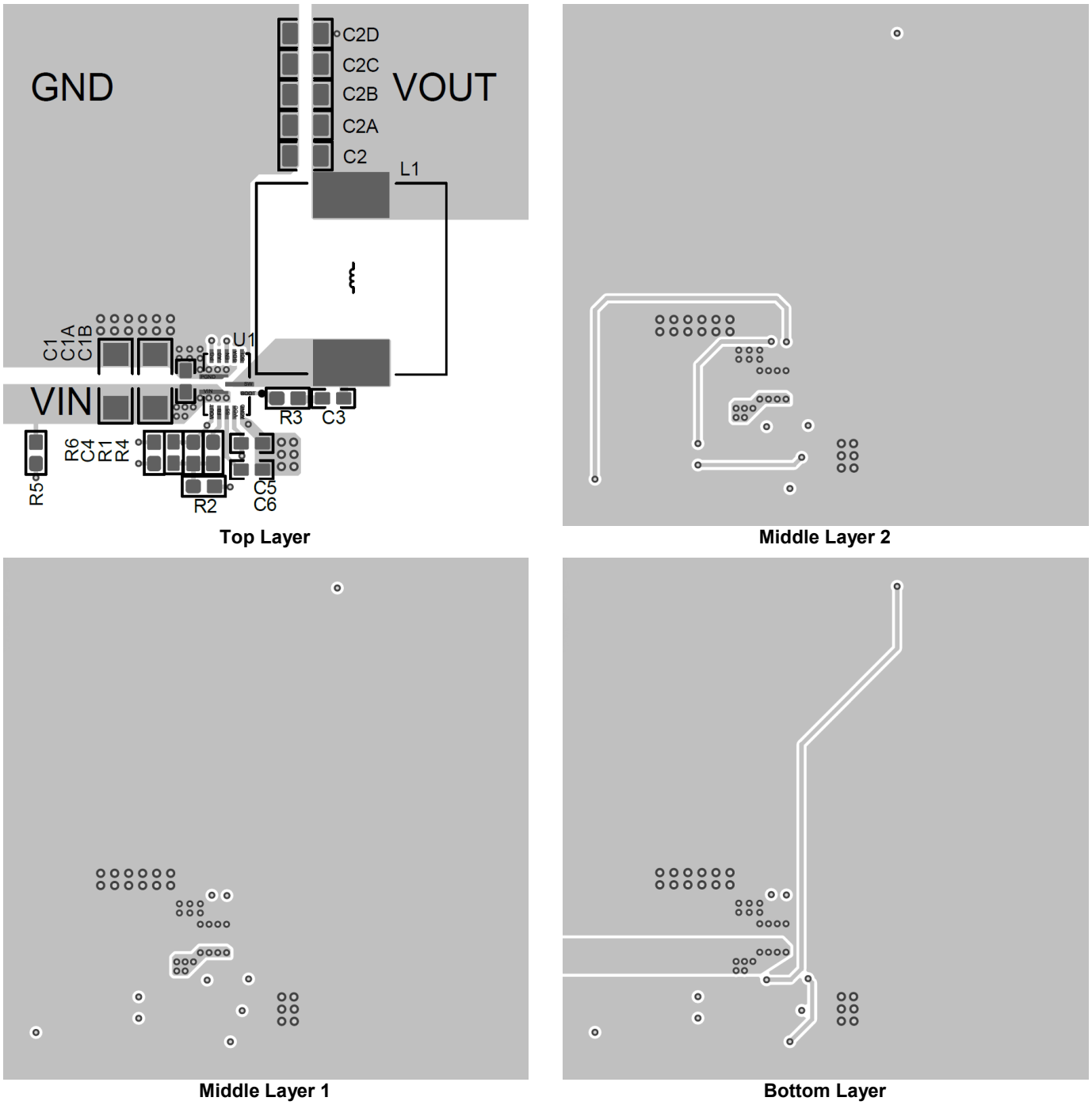
Layout Guidelines

A critical element of a high frequency switching power supply is the PCB layout. A well-optimized layout enhances overall performance of the system, whereas a suboptimal layout can lead to stability degradation and elevated EMI issues. The following guidelines are provided for designing a robust PCB layout with the SGM611A121.

- Use short, wide traces for power path routing to minimize trace parasitic resistance and inductance.
- For improved thermal performance, the VIN and PGND nets should be implemented across in at least two PCB layers.
- To achieve optimal power integrity, place the 100nF low ESR decoupling capacitor as close as possible to the VIN-PGND pins, with other input capacitors positioned nearby as well. It is not recommended to place the remaining input capacitors on a different PCB layer. If this arrangement is unavoidable, use a sufficient number of vias close to the capacitors to lower the impedance between the capacitors and the IC.
- Place the inductor as close as practical to SW (pin 2) to shorten the SW node trace length and thereby improve EMI performance.
- Connect the ground returns of the input and output capacitors close to the PGND pin at a single common point to avoid ground potential shift and minimize the high-frequency current loop area.
- Route VOUT pin and FB pin connections away from the high-frequency and noisy conductors such as power traces and SW node to prevent magnetic and electric noise coupling.
- Place the output voltage divider network close to the FB pin on the same layer as the IC.
- Use as many vias as possible near the PGND pin to connect the PGND copper planes of all layers directly beneath the device, improving noise immunity and thermal dissipation.
- The AGND pin must connect to the PGND net only through a small number of tightly grouped vias, which should be placed close to the AGND pin.
- Place the BOOT-SW capacitor as close as possible to the BOOT (pin 1) and SW (pin 2); the same placement rule applies to components around the VCC/SS pins and AGND pins.
- The lower feedback resistor of the FB divider and the A0 resistor must be connected to the AGND island.

Refer to Figure 13 for a recommended PCB layout.

APPLICATION INFORMATION (continued)



Top Layer

Middle Layer 2

Middle Layer 1

Bottom Layer

Figure 13. PCB Layout

APPLICATION INFORMATION (continued)

Application Schematics for Other Output Voltage Options

All circuits are based on a 0.72V default reference voltage.

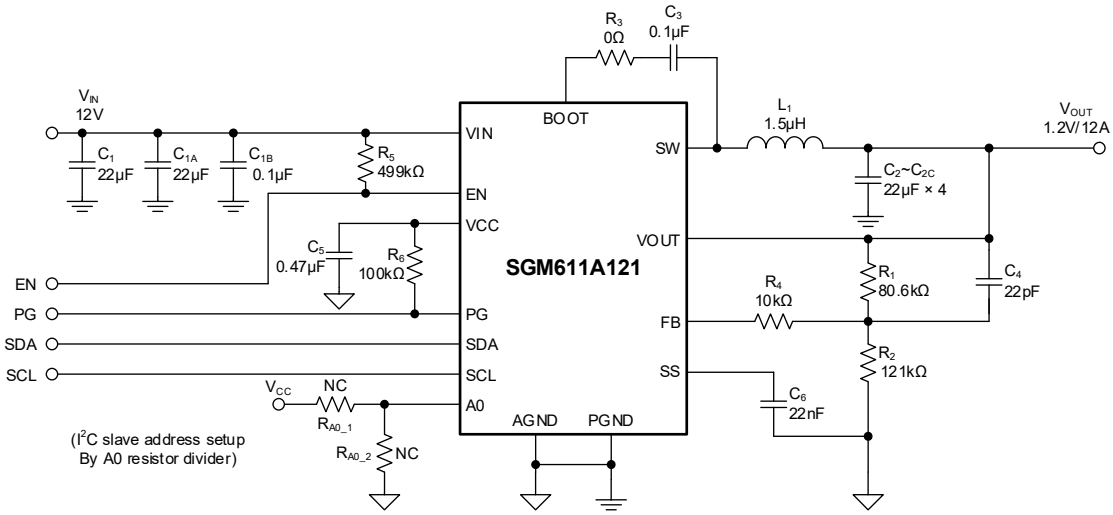


Figure 14. 1.2V Output Voltage Application

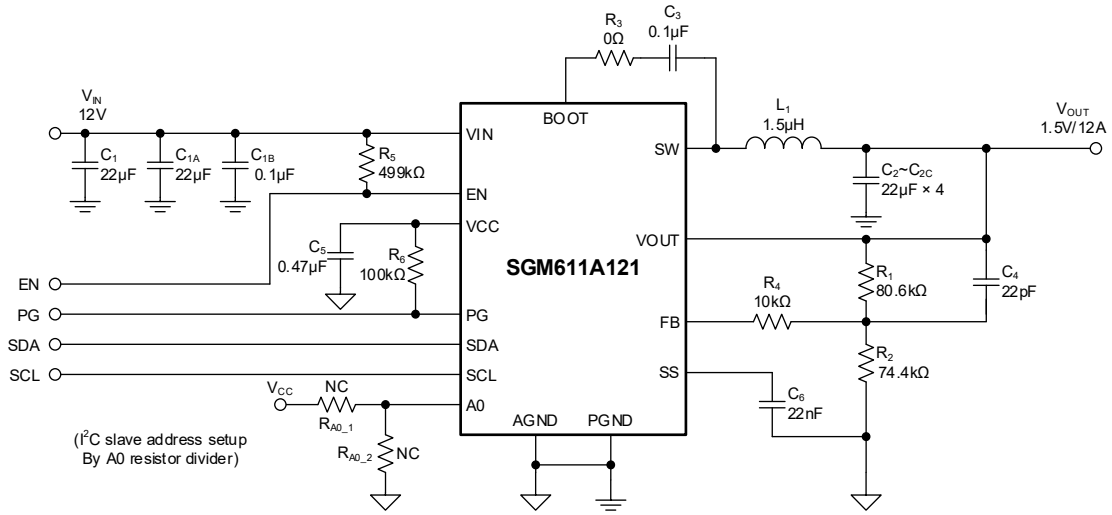


Figure 15. 1.5V Output Voltage Application

APPLICATION INFORMATION (continued)

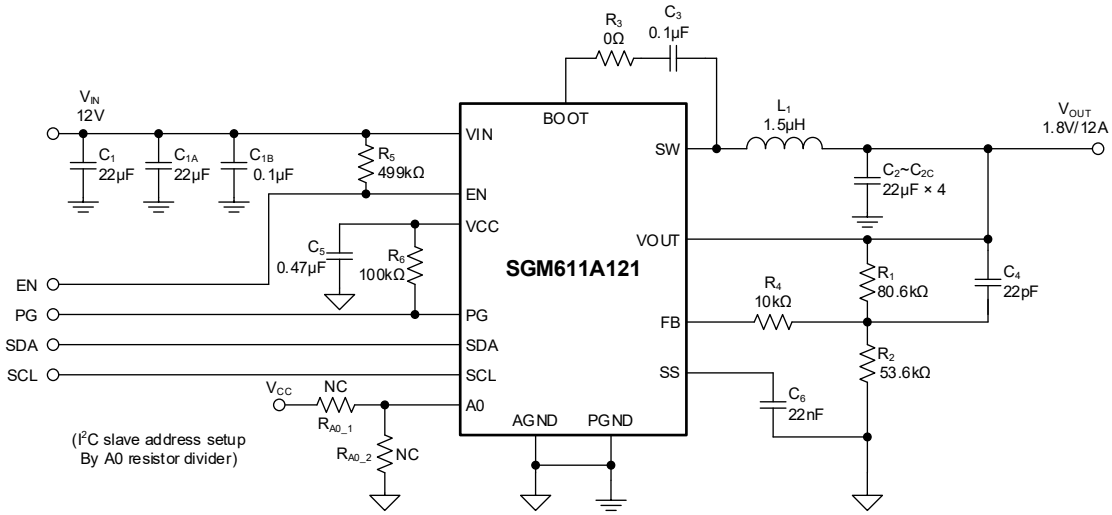


Figure 16. 1.8V Output Voltage Application

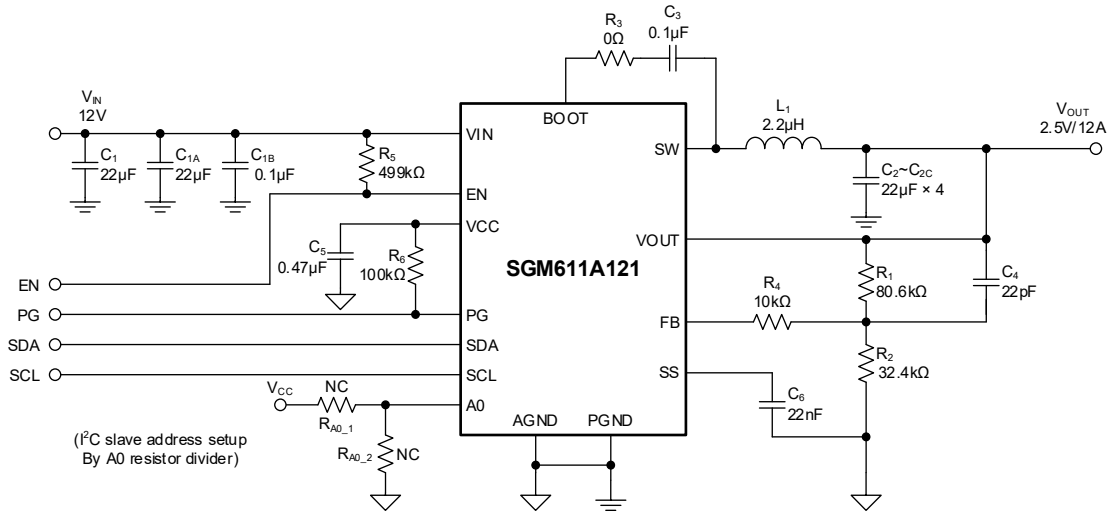


Figure 17. 2.5V Output Voltage Application

APPLICATION INFORMATION (continued)

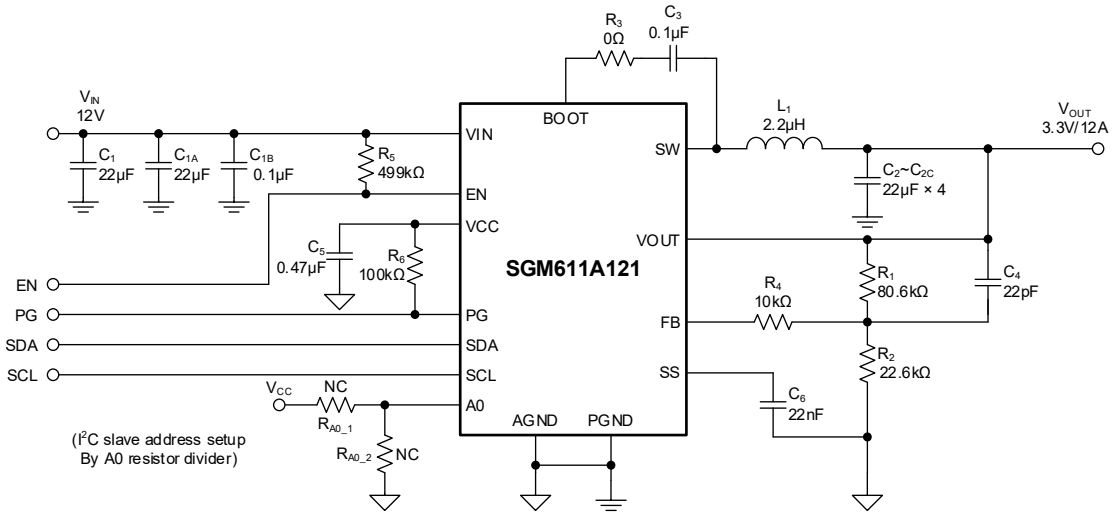


Figure 18. 3.3V Output Voltage Application

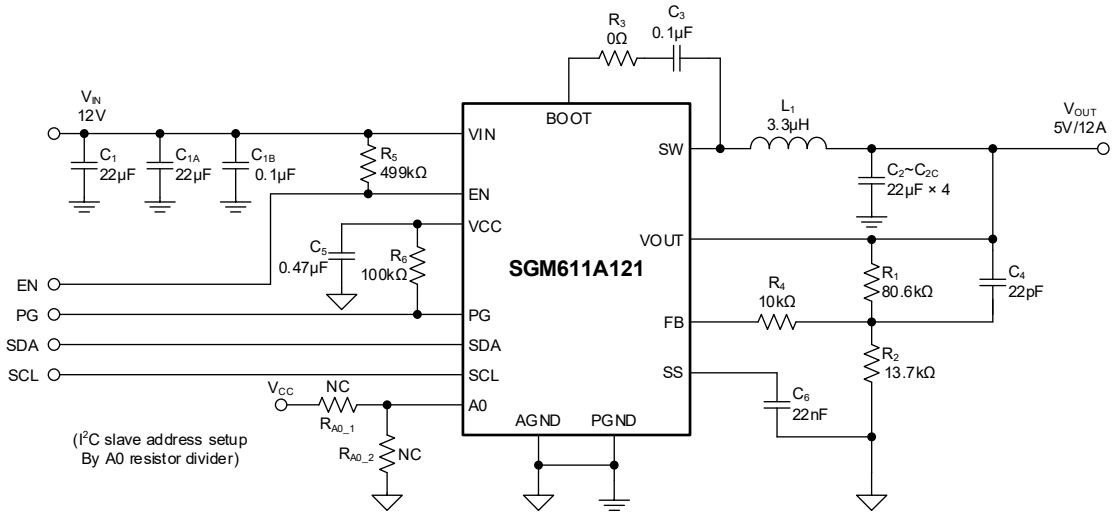


Figure 19. 5V Output Voltage Application

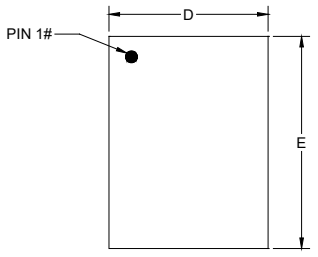
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

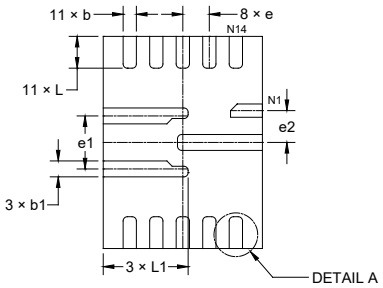
Changes from Original to REV.A (JULY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

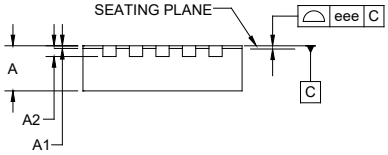
TQFN-3×4-14L



TOP VIEW

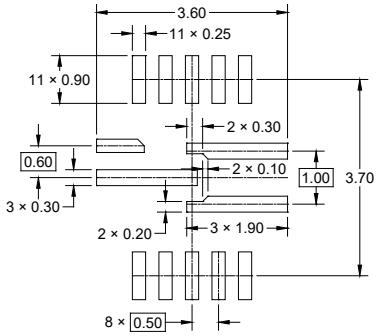


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



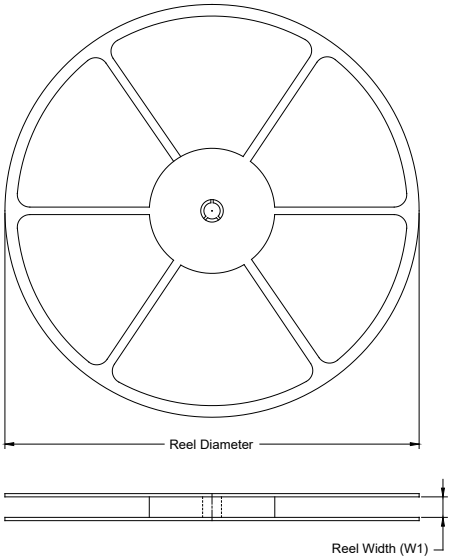
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
b1	0.250	-	0.350
D	2.900	-	3.100
E	3.900	-	4.100
e		0.500 BSC	
e1		1.000 BSC	
e2		0.600 BSC	
L	0.500	-	0.700
L1	1.500	-	1.700
eee		0.080	

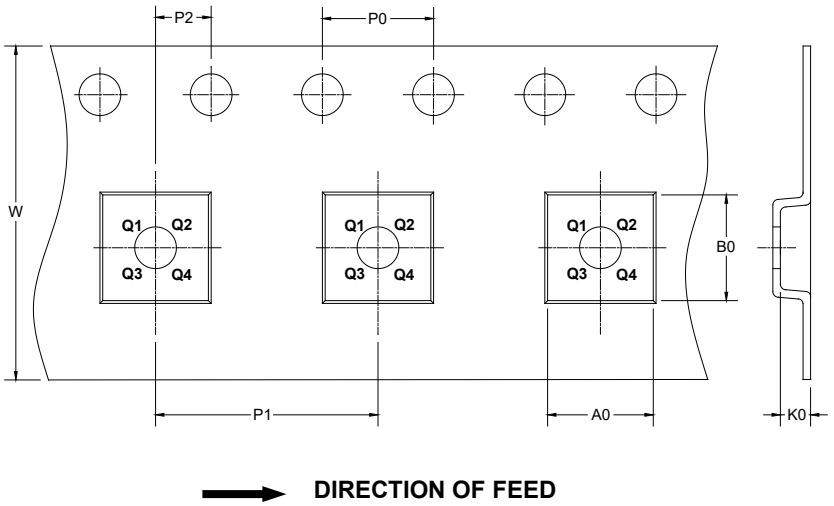
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



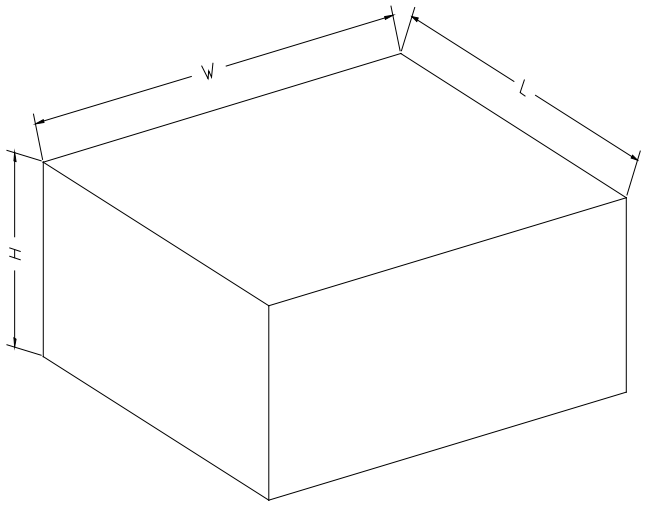
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-14L	13"	12.4	3.40	4.40	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002