SGM42322
20V, 2.5A Three-Phase Integrated FET Motor Driver

GENERAL DESCRIPTION

The SGM42322 is a triple half-bridge driver, which is designed to drive three-phase brushless DC motors.

The device has multiple protection functions, including under-voltage lockout (UVLO), over-current protection (OCP) at fixed level and thermal shutdown (TSD). The nFAULT pin is used to indicate the fault problems.

The SGM42322 is available in a Green TQFN-2×2.5-16L package.

TYPICAL APPLICATION

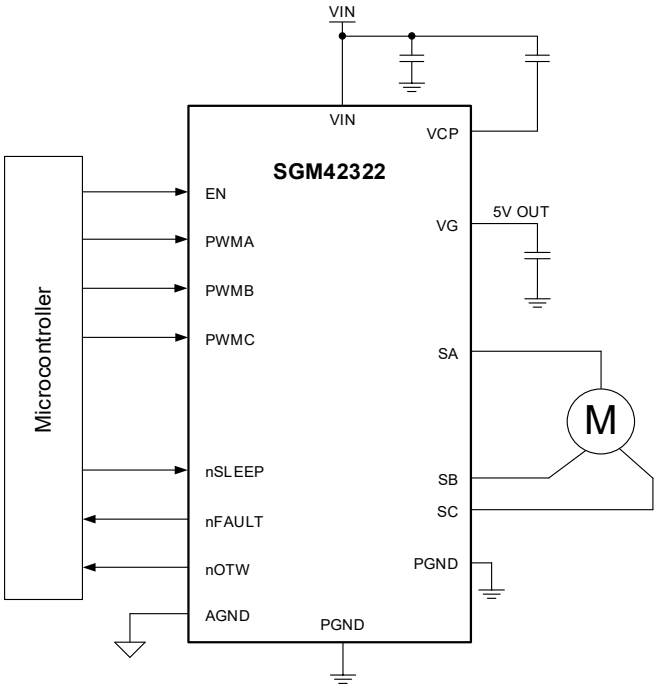


Figure 1. Typical Application Circuit

FEATURES

- **Operating Supply Voltage: 3V to 20V**
- **High Output Current Capability**
  - **2.5A Continuous Current, 5A Peak Current**
- **MOSFET On-Resistance:**
  - **115mΩ (HS + LS) at +25℃ (TYP)**
- **PWM Logic Inputs**
- **Built-in LDO Regulator: 5V, 30mA**
- **Sleep-Mode with Typical 30μA Quiescent Current (LDO Operating)**
- **Internal Charge Pump Supports 100% PWM Duty Cycle Driving**
- **Automatic Synchronous Rectification**
- **Integrated Protection Features**
  - **Under-Voltage Lockout (UVLO)**
  - **Thermal Shutdown (TSD)**
  - **Over-Current Protection (OCP) at Fixed Level**
  - **Open-Drain Fault Reporting (TSD, OCP) Output**
- **Available in a Green TQFN-2×2.5-16L Package**

APPLICATIONS

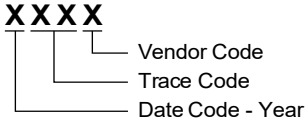
Three-Phase BLDC Motor Drivers

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42322	TQFN-2×2.5-16L	-40℃ to +125℃	SGM42322XTXH16G/TR	29H XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Operating Supply Voltage 22V
Power Supply VM Ramp Rate ..... < 2V/μs
SA, SB, SC Voltage ..... -0.3V to V_{IN} + 0.3V
VCP Voltage ..... V_{IN} – 0.3V to V_{IN} + 5V
Voltage at All Other Pins ..... -0.3V to 5V
Package Thermal Resistance
TQFN-2×2.5-16L, θ_{JA} ..... 59.7℃/W
TQFN-2×2.5-16L, θ_{JB} ..... 5℃/W
TQFN-2×2.5-16L, θ_{JC} ..... 38.8℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Supply Voltage ..... 3V to 20V
PWMx Input frequency ..... < 200kHz
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

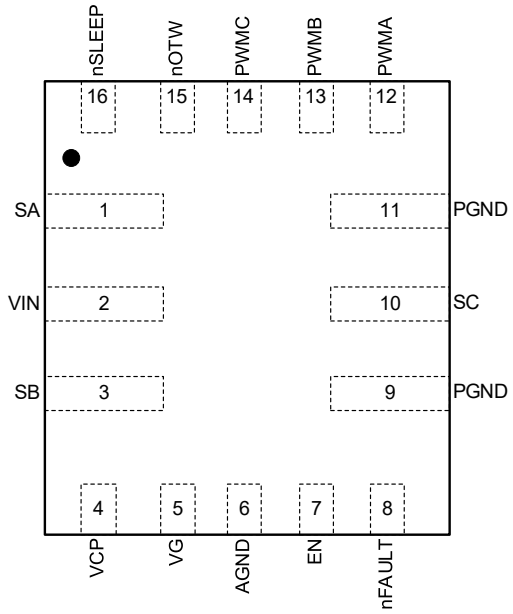
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2×2.5-16L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SA	O	Phase A Output.
2	VIN	P	Input Power.
3	SB	O	Phase B Output.
4	VCP	P	Charge Pump Output. Connect a 1μF, 16V, X7R ceramic capacitor to VIN.
5	VG	P	Low-side Gate Drive Bypass. Connect a 4.7μF, 10V, X7R ceramic capacitor to ground.
6	AGND	G	Analog Ground.
7	EN	I	Enable Input for Power Stage. Logic high for enable all the three phases.
8	nFAULT	O	Fault Indication. Open-drain output type, logic low when in fault condition.
9, 11	PGND	G	Power Ground. Recommended to be connected directly to GND.
10	SC	O	Phase C Output.
12	PWMA	I	Phase A PWM Input.
13	PWMB	I	Phase B PWM Input.
14	PWMC	I	Phase C PWM Input.
15	nOTW	O	Over-Temperature Warning. Open-drain output type, logic low when in OTW condition.
16	nSLEEP	I	Sleep Mode Input. Logic low for sleep mode. Logic high for normal operation. Internal pull down.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

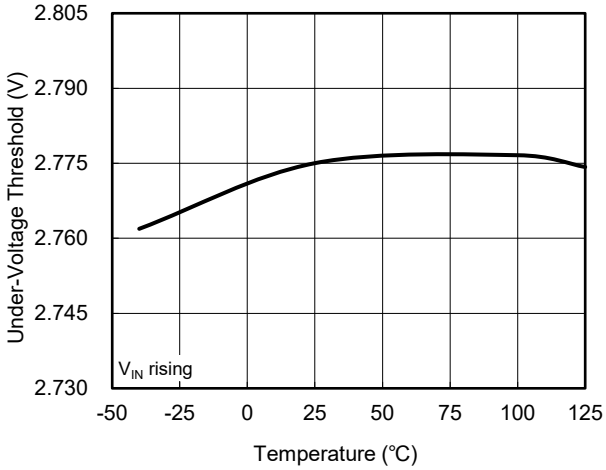
(T_J = +25℃, V_{IN} = 10V, PGND = GND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Input Supply Voltage	V_{IN}		3		20	V
Quiescent Current	I_Q	nSLEEP = high, EN = low		1	2	mA
	I_{nSLEEP}	nSLEEP = low		30	60	μA
Control Logic						
Input Low Threshold	V_{IL}				0.4	V
Input High Threshold	V_{IH}		1.5			V
Logic Input Current	I_{INH}	V_{IN} = 5V	-20		20	μA
	I_{INL}	V_{IN} = 0V	-20		20	μA
Power-Up Delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		0.8		ms
Internal Pull-Down Resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT Pull-Down R_{ON}	R_{ON_nFAULT}			5		Ω
VG Regulator						
VG Pin Voltage	V_G	I_{OUT} = 0mA to 30mA	4.5	4.95	5.28	V
Protection Circuits						
UVLO Threshold	V_{UVLO}	V_{IN} rising	2.62	2.8	2.95	V
UVLO Hysteresis	ΔV_{UVLO}			220		mV
OCP Threshold	I_{OCP}		5	6.5	8	A
OCP Deglitch Time	t_{OCD}			2.5		μs
Thermal Shutdown Threshold	T_{SD}	T_J rising		160		℃
Thermal Shutdown Hysteresis	T_{HYS}			25		℃
Thermal Warning Threshold				145		℃
Thermal Warning Hysteresis				25		℃
Output						
LS FET On-Resistance	R_{DSON_LS}	I_{OUT} = 1A		55		mΩ
HS FET On-Resistance	R_{DSON_HS}	I_{OUT} = 1A		60		
Output Rise Time	t_R	R_{LOAD} = 50Ω		25		ns
Output Fall Time	t_F	R_{LOAD} = 50Ω		25		ns
Dead Time	t_D	R_{LOAD} = 50Ω		30		ns
PWMx to Sx Delay Time Rising	t_{DLY_R}			120		ns
PWMx to Sx Delay Time Falling	t_{DLY_F}			140		ns
Charge Pump						
Charge Pump Output Voltage	V_{CP}			V_{IN} + 4.5		V

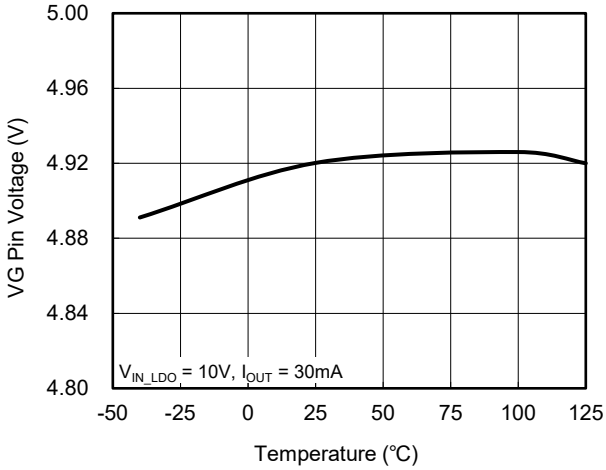
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUT} = 1A, unless otherwise noted.

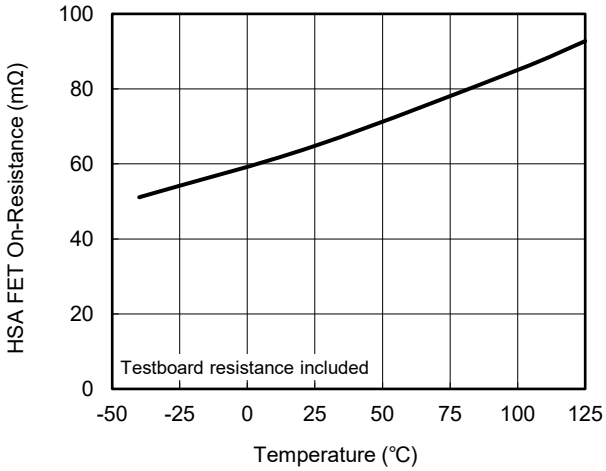
Under-Voltage Threshold vs. Temperature



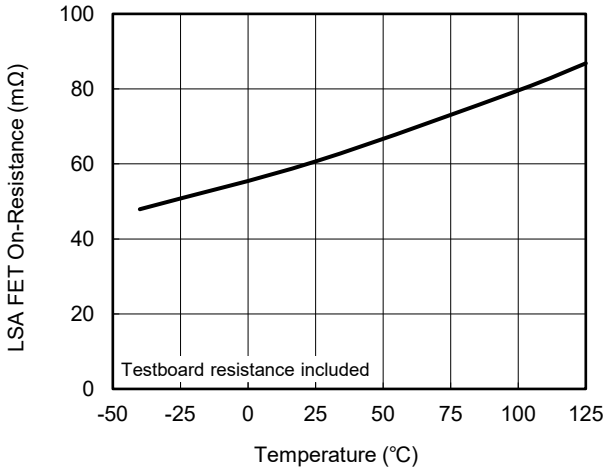
VG Pin Voltage vs. Temperature



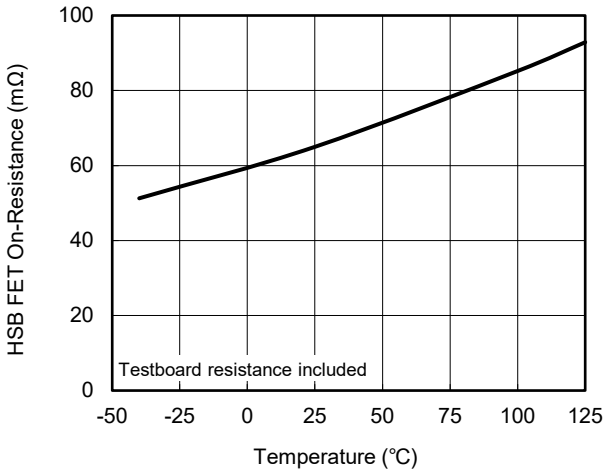
HSA FET On-Resistance vs. Temperature



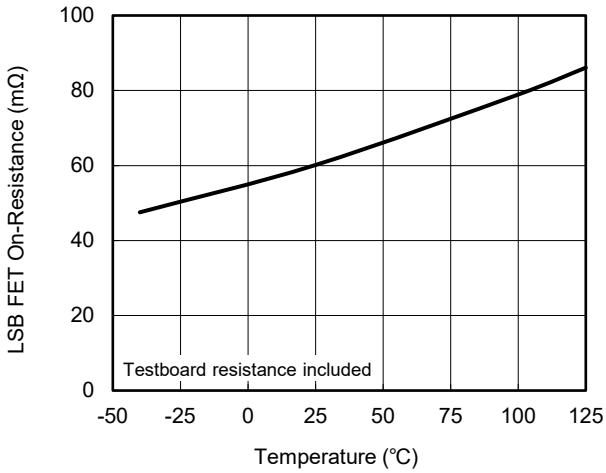
LSA FET On-Resistance vs. Temperature



HSB FET On-Resistance vs. Temperature



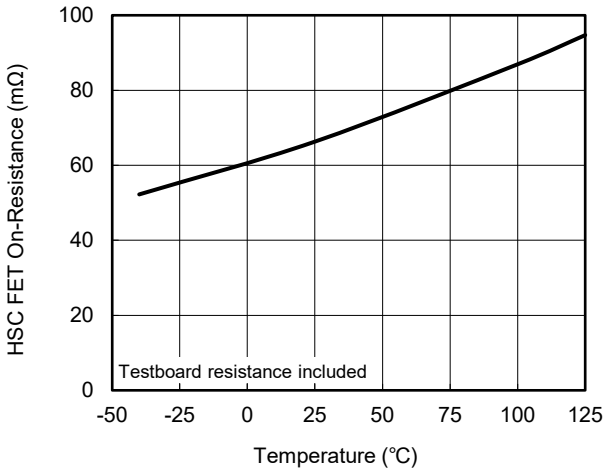
LSB FET On-Resistance vs. Temperature



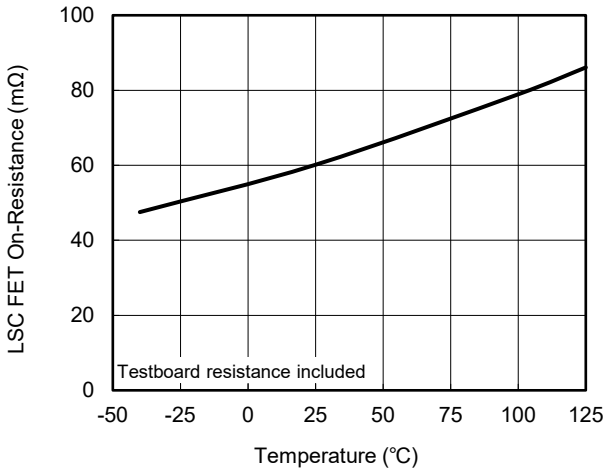
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

I_{OUT} = 1A, unless otherwise noted.

HSC FET On-Resistance vs. Temperature

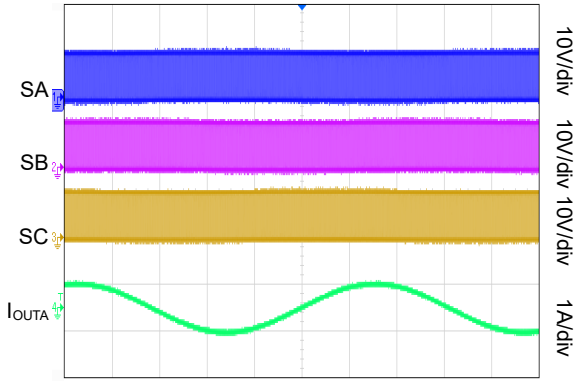


LSC FET On-Resistance vs. Temperature

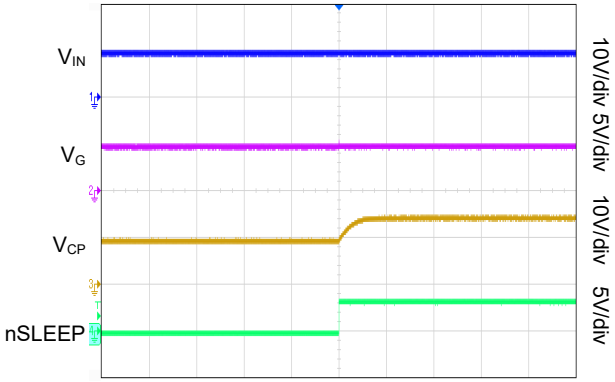


T_A = +25℃, V_{IN} = 10V, output with resistive-inductive load (3Ω + 1mH per phase, star connection), unless otherwise noted.

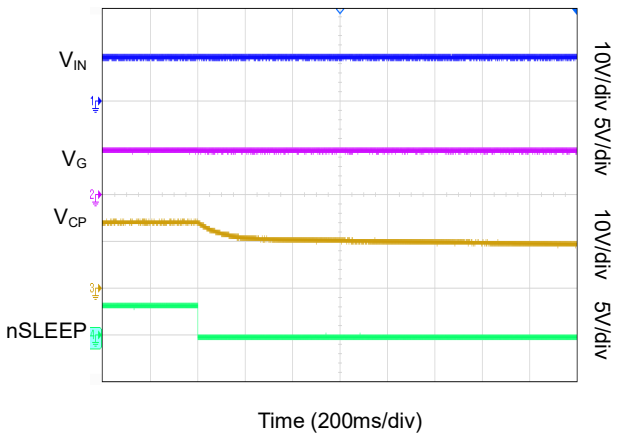
Steady State



nSLEEP Start-Up



nSLEEP Shutdown



FUNCTIONAL BLOCK DIAGRAM

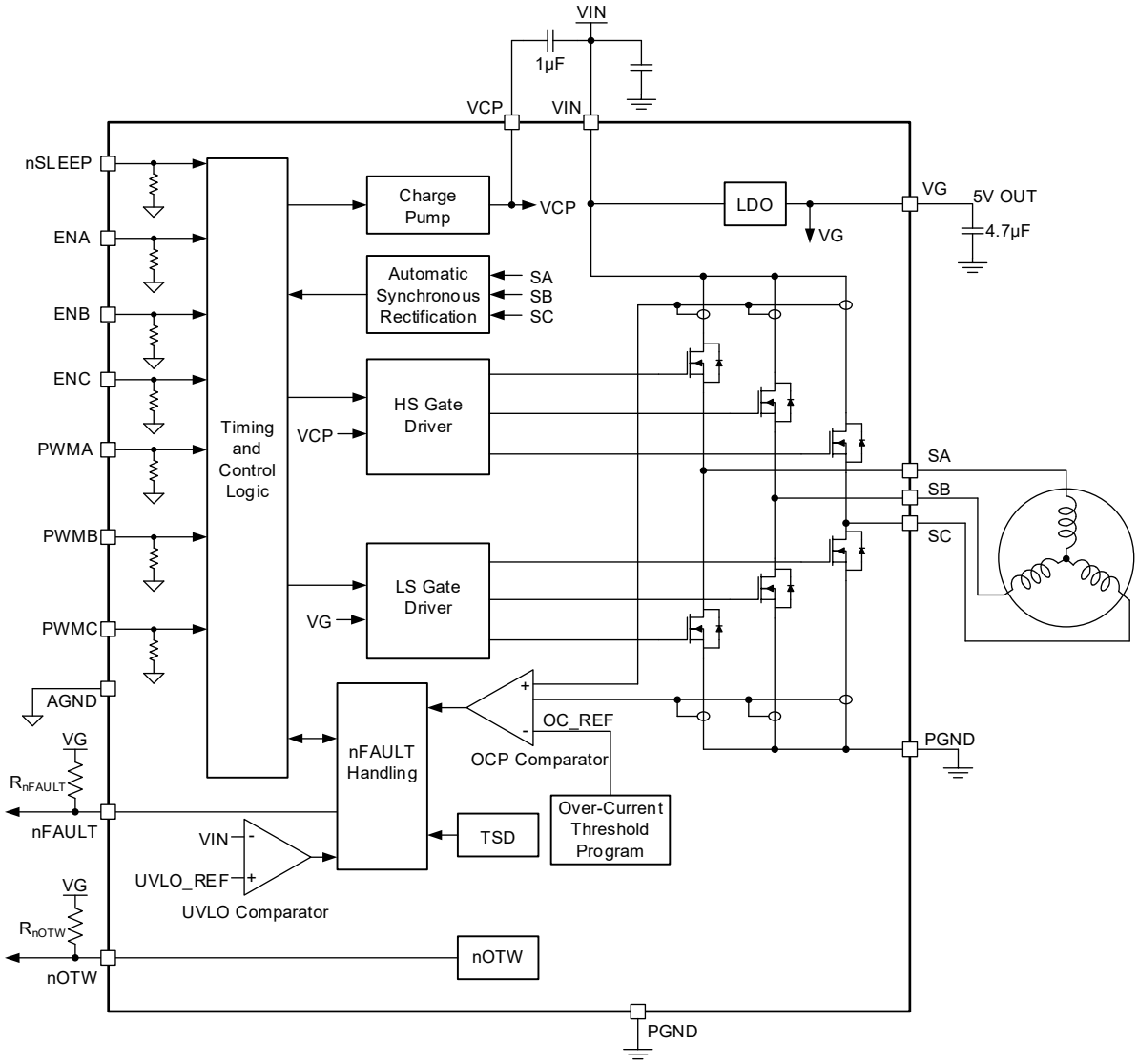


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM42322 is an integrated 115mΩ (combination of HS and LS FETs on-resistance) driver for three-phase BLDC motor drive applications. The device reduces system component counts, cost and complexity by integrating three half-bridge FETs, and protection circuits.

Input Logic

Please refer to input control logic in Table 1.

Table 1. When nSLEEP = High (1)

EN	PWMx	Sx
H	H	VIN
H	L	GND
L	X	Hi-Z

NOTE:

1. when nSLEEP = low , no matter EN Pin or PWMx Pin is high or low , the output is shut down and kept in Hi-Z status.

nSLEEP Operation

This active-low input is used to minimize power consumption when the device is not in use. Sleep mode disables most of the internal circuitry, including the output FETs and charge pump. Logic high allows normal operation. If the charge pump output capacitor is fully discharged, the device must take about 0.8ms to respond to the inputs. The nSLEEP input is pull-down internally.

The device does not have special power up sequence requirement, however, SGMICRO still recommends pulling up nSLEEP signal before sending PWM signal to output.

Automatic Synchronous Rectification

The SGM42322 has automatic synchronous rectification feature (active demagnetization) which reduces power losses in device by reducing body-diode conduction losses. If both half-bridge power FETs are turned off, then the automatic synchronous rectification applies, the inductor current decays through FETs instead of the body-diodes.

The device includes a HS output comparator and a LS output comparator for each half-bridge channel, which detect the respective body-diodes' current flow. The HS output comparator compares the half-bridge output voltage with respect to V_{IN}. The LS output comparator compares the half-bridge output voltage with respect to PGND. When both HS FET and LS FET of a channel are turned off, upon the flow of the recirculation current: if the LS body-diode conducts, the half-bridge output voltage is driven below PGND, and the LS output comparator trips, then the LS FET will be on until the recirculation current reduces to zero. Similarly, if the HS body-diode conducts, the half-bridge output voltage is driven above V_{IN}, and the HS output comparator trips, then the HS FET is turned on until the current flowing through it reduces to zero.

nFAULT Output

The nFAULT is an open-drain output that needs to be pulled up externally. The nFAULT will be pulled low in OC (over-current) or TSD (thermal shutdown) condition.

UVLO Protection

At any time, the V_{IN} power supply falls below the V_{UVLO} threshold (V_{IN} falling threshold), all of the integrated FETs, driver charge pump and digital logic controller are disabled and the internal logic is reset. The device will resume normal operation when power supply goes higher than V_{UVLO} threshold.

Thermal Shutdown (TSD)

All bridges and drivers are shutdown if a junction over-temperature occurs in the device and the nFAULT will be pulled low. Once the temperature goes back to the safe level, the device resumes its operation.

Over-Current Protection

A MOSFET over-current event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCD} deglitch time, all the three half-bridges will be disabled (shutdown), and the nFAULT pin will be driven low. Output is disabled and needs to reset for normal operation.

An over-current may occur due to a short between a switching node and ground or to the VIN supply line, or to the other node of the bridge (a winding short). Figure 3 shows a simplified diagram of the OCP circuit for one output.

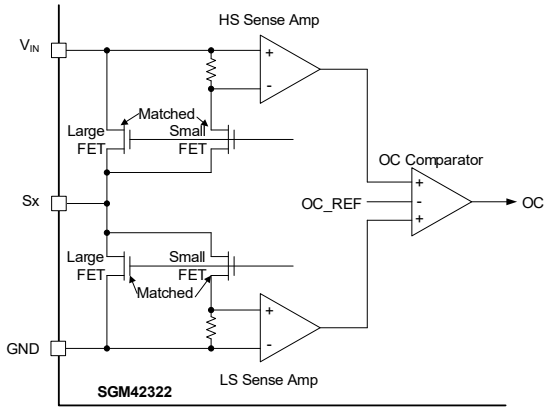


Figure 3. OCP Circuit

DETAILED DESCRIPTION (continued)

5V LDO Output

A 5V LDO regulator is provided to internal low-side gate drive and external circuitry, whose output capability is 30mA. A bypass capacitor of 4.7μF to 10μF is required from VG to ground. The VG regulator remains operational in sleep mode.

Charge Pump

The charge pump is used to generate a gate supply which is greater than V_{IN} to turn on the high-side FETs. A 1μF (10V or higher) ceramic capacitor is required between VIN and VCP pins.

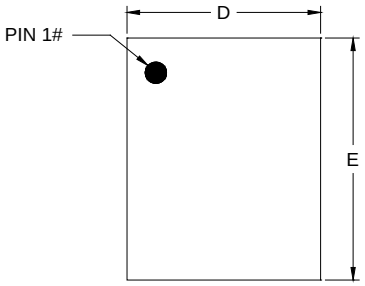
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

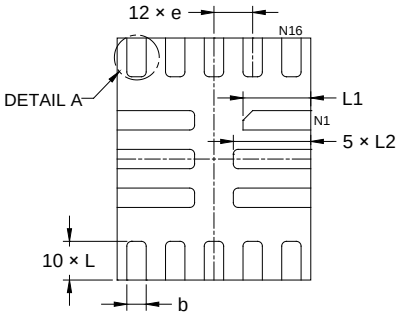
Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

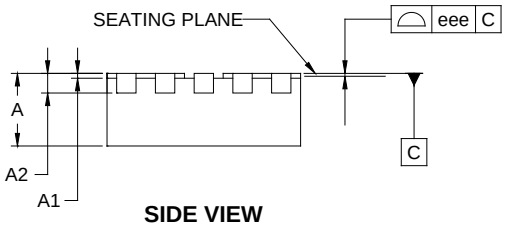
TQFN-2×2.5-16L



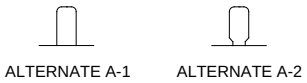
TOP VIEW



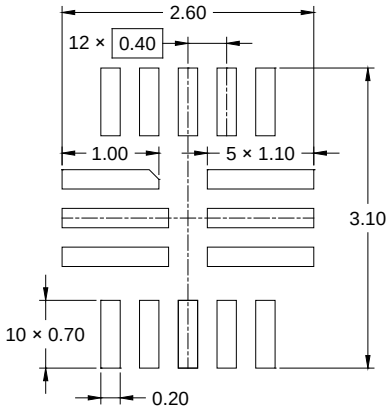
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



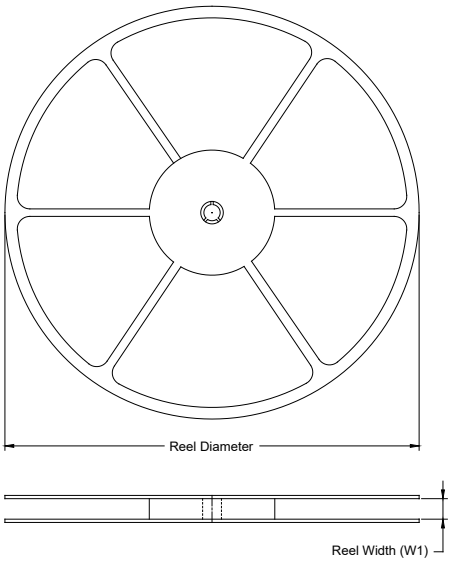
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
D	1.900	-	2.100
E	2.400	-	2.600
e	0.400 BSC		
L	0.300	-	0.500
L1	0.600	-	0.800
L2	0.700	-	0.900
eee	0.080		

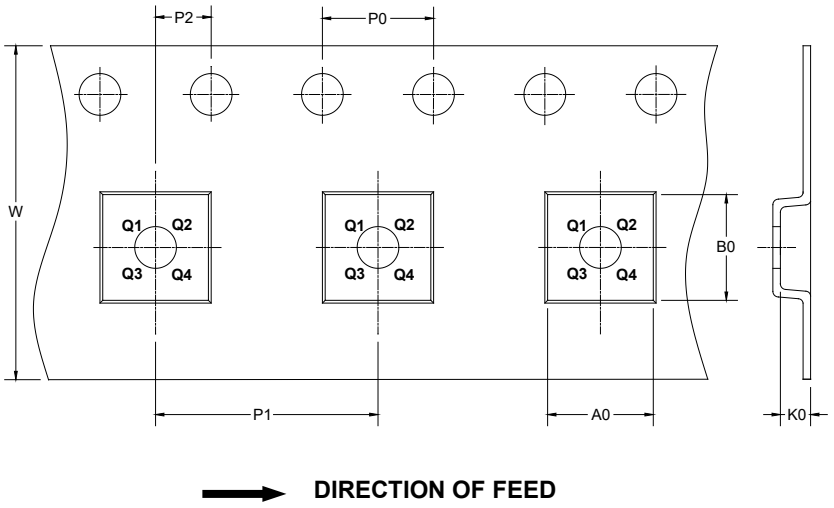
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



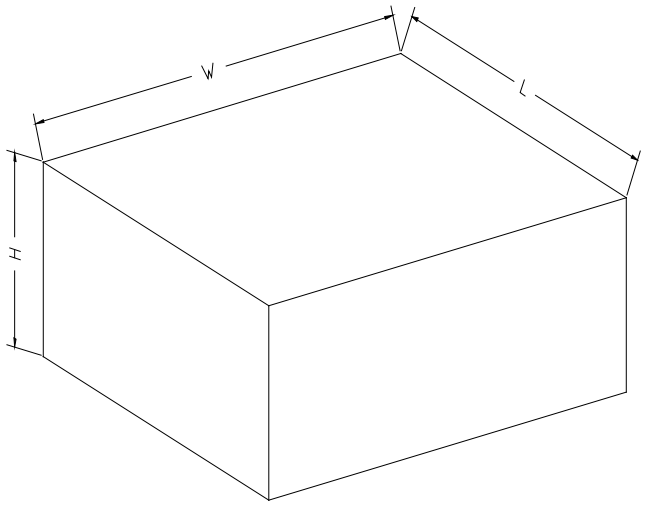
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2.5-16L	7"	9.5	2.20	2.70	1.00	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002