# SGM6026
# 3A, 2.3MHz, I²C Programmable Synchronous Buck Converter

## GENERAL DESCRIPTION

The SGM6026 is a synchronous Buck converter with integrated I²C interface to adjust the output voltage, where the I²C interface can operate up to 3.4MHz. The SGM6026 is capable to operate from 2.5V to 5.5V input voltage range, which is suitable for Li-Ion battery.

The SGM6026 is a high power density device capable of delivering 3A continuous load current while achieving over 80% efficiency across the entire load range down to 10mA. The device switches at 2.3MHz that allows the use of small external components.

The SGM6026 implements pulse frequency modulation (PFM) at light load conditions to improve the efficiency. The device can be configured in FPWM mode for applications where a fixed frequency is required for the entire operating load range. The device consumes only 35μA (TYP) quiescent at PFM mode while maintaining excellent transient response during large load steps. At heavy load, the device automatically adjusts the switching frequency to the fixed 2.3MHz. The device consumes 1μA (TYP) current in shutdown mode to further reduce the power consumption.

The SGM6026 is available in a Green WLCSP-1.2×2-15B package.

## FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **I²C Programmable Output Voltage:**
  **0.6V to 1.39375V in 6.25mV Steps (Default: 1.15625V)**
- **3A Continuous Output Current Capability**
- **35μA (TYP) Quiescent Current in PFM Mode**
- **2.3MHz Fixed Frequency Operation**
- **Excellent Load Transient**
- **I²C Programmable Output Voltage Transition Slew Rate**
- **I²C Compatible Interface up to 3.4Mbps**
- **PFM Mode for High Efficiency in Light Load**
- **Input Under-Voltage Lockout (UVLO)**
- **Thermal Shutdown and Overload Protection**
- **Available in a Green WLCSP-1.2×2-15B Package**

## APPLICATIONS

Core Supply for DSP, ASICs, CPUs, and FPGAs
DDR Memory Power Supplies
SSD
Camera and Optical Modules
Smart Phones

## TYPICAL APPLICATION

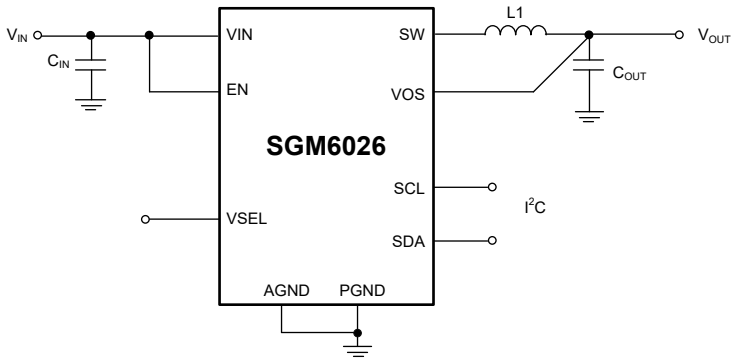


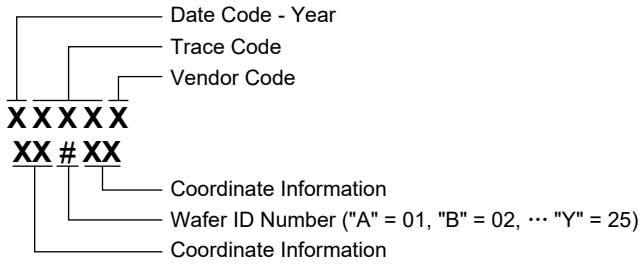

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM6026 | WLCSP-1.2×2-15B | -40℃ to +85℃ | SGM6026YG/TR | 6026<br>XXXXX<br>XX#XX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

SW, VIN Voltages
IC Not Switching ..... -0.3V to 7.0V
IC Switching..... -0.3V to 6.5V
EN Voltage..... -0.3V to MIN(7V, $V_{IN}$ + 0.3V)
All Other Pins Voltages
IC Not Switching ..... -0.3V to MIN(7V, $V_{IN}$ + 0.3V)
VOUT Voltage..... -0.3V to 6.5V
Maximum Slew Rate of $V_{IN}$ > 6.5V, PWM Switching.....
..... 100V/ms
Package Thermal Resistance
WLCSP-1.2×2-15B, $\theta_{JA}$..... 63.8℃/W
WLCSP-1.2×2-15B, $\theta_{JB}$..... 18.8℃/W
WLCSP-1.2×2-15B, $\theta_{JC}$ ..... 27.0℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Input Voltage Range .....2.5V to 5.5V
Output Current Range .....0A to 3A
Operating Ambient Temperature Range.....-40℃ to +85℃
Operating Junction Temperature Range.....-40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

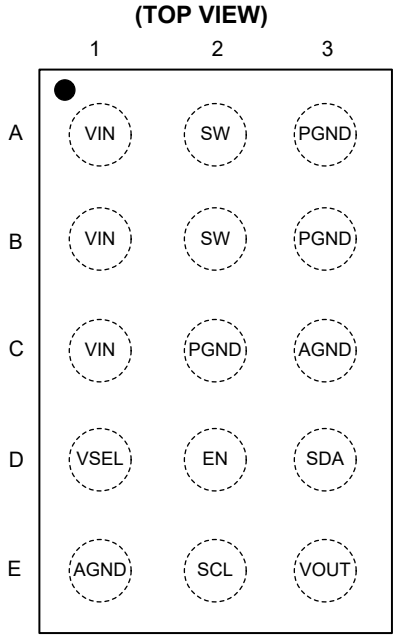
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION




**WLCSP-1.2×2-15B**

## PIN DESCRIPTION

| PIN | NAME | DESCRIPTION |
|---|---|---|
| A1, B1, C1 | VIN | Input Power Supply Pin. Connect the CIN capacitor to this pin. |
| A2, B2 | SW | Switching Node. Connect to the inductor. |
| A3, B3, C2 | PGND | Power Ground. Source connection of the internal N-channel low-side MOSFET. $C_{IN}$ and $C_{OUT}$ should be returned with a minimal trace length to these pins. |
| C3, E1 | AGND | Analog Ground. |
| D1 | VSEL | Voltage Selection Pin. When pulled low, VSEL0 register sets the output voltage. When pulled high, VSEL1 register sets the output voltage. Polarity of pin selects forced PWM or auto PFM/PWM mode of operation, which is in conjunction with the MODE bits in the CONTROL register (**REG0x02**). VSEL0 = Auto PFM, and VSEL1 = FPWM. An internal pull-down resistor (250kΩ) is put on this pin and is only activated with logic low. |
| D2 | EN | Enable Pin. The device is in shutdown mode when this pin is pulled low with an internal pull-down resistor (250kΩ). Register content is saved when this pin is low. |
| D3 | SDA | $I^2C$ Bus Serial Data. |
| E2 | SCL | $I^2C$ Bus Serial Clock. |
| E3 | VOUT | VOUT Sense Pin. Connect to $C_{OUT}$. |

# ELECTRICAL CHARACTERISTICS

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 3.6V. All typical values are measured at $T_J$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V and EN = HIGH, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Quiescent Current | $I_Q$ | $I_{LOAD}$ = 0 | | 35 | | μA |
| | | $I_{LOAD}$ = 0, MODE bit = 1 (forced PWM) | | 15 | | mA |
| H/W Shutdown Supply Current | $I_{SD}$ | $T_J$ = -40℃ to +85℃, EN = GND | | 0.2 | 3 | μA |
| S/W Shutdown Supply Current | | $T_J$ = -40℃ to +85℃, EN = $V_{IN}$, BUCK_ENx = 0, 2.5V ≤ $V_{IN}$ ≤ 5.5V | | 5 | 12 | μA |
| Under-Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ rising | | 2.3 | 2.45 | V |
| Under-Voltage Lockout Hysteresis | | | | 160 | | mV |
| **EN, VSEL, SDA, SCL** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V | 0.9 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V | | | 0.4 | V |
| Input Bias Current | $I_{IN}$ | Input tied to GND or VIN | | 0.01 | 1 | μA |
| **$V_{OUT}$ Regulation** | | | | | | |
| VOUT DC Accuracy | $V_{REG}$ | $T_J$ = -40℃ to +85℃, $V_{OUT}$ from minimum to maximum, auto PFM/PWM | -2.5 | | 2.5 | % |
| Load Regulation | | $I_{OUT(DC)}$ = 1A to 3A | | 0.1 | | %/A |
| Line Regulation | | 2.5V ≤ $V_{IN}$ ≤ 5.5V, $I_{OUT(DC)}$ = 1.5A | | 0.05 | | %/A |
| Transient Response | $V_{TRSP}$ | $I_{LOAD}$ = 0.01A to 1.5A, $t_R$ = $t_F$ = 1μs, $V_{OUT}$ = 1.15625V | | +19/ -63 | | mV |
| **Power Switch/Protection** | | | | | | |
| PMOS Peak Current Limit | $I_{LIM_PEAK}$ | | 3.3 | 4.75 | 6.6 | A |
| Thermal Shutdown | $T_{SD}$ | | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 20 | | ℃ |
| Input OVP Shutdown | $V_{SDWN}$ | Rising threshold | | 6.04 | | V |
| | | Falling threshold | 5.5 | 5.76 | | |
| **Frequency Control** | | | | | | |
| Oscillator Frequency | $f_{SW}$ | | 1.95 | 2.3 | 2.65 | MHz |
| **DAC** | | | | | | |
| Resolution | | | | 7 | | Bits |
| Differential Nonlinearity (1) | | | | | 0.5 | LSB |
| **Soft-Start** | | | | | | |
| Regulator Enable to Regulated $V_{OUT}$ | $t_{SS}$ | $R_{LOAD}$ > 5Ω, $V_{OUT}$ = 1.15625V, from EN rising edge to 95% $V_{OUT}$ | | 190 | | μs |

NOTE:

1. Monotonicity guaranteed by design.

## I²C TIMING SPECIFICATIONS

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 3.6V. All typical values are measured at $T_J$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V and EN = HIGH, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | Standard mode | | | 100 | kHz |
| | | Fast mode | | | 400 | |
| | | Fast mode plus | | | 1000 | |
| | | High-speed mode, $C_B$ ≤ 100pF | | | 3400 | |
| | | High-speed mode, $C_B$ ≤ 400pF | | | 1700 | |
| Bus-Free Time between Stop and Start Conditions | $t_{BUF}$ | Standard mode | | 4.7 | | μs |
| | | Fast mode | | 1.3 | | |
| | | Fast mode plus | | 0.5 | | |
| Start or Repeated Start Hold Time | $t_{HD_STA}$ | Standard mode | | 4 | | ns |
| | | Fast mode | | 600 | | |
| | | Fast mode plus | | 260 | | |
| | | High-speed mode | | 160 | | |
| SCL Low Period | $t_{LOW}$ | Standard mode | | 4.7 | | μs |
| | | Fast mode | | 1.3 | | |
| | | Fast mode plus | | 0.5 | | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 160 | | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 320 | | |
| SCL High Period | $t_{HIGH}$ | Standard mode | | 4 | | ns |
| | | Fast mode | | 600 | | |
| | | Fast mode plus | | 260 | | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 60 | | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 120 | | |
| Repeated Start Setup Time | $t_{SU_STA}$ | Standard mode | | 4.7 | | ns |
| | | Fast mode | | 600 | | |
| | | Fast mode plus | | 260 | | |
| | | High-speed mode | | 160 | | |
| Data Setup Time | $t_{SU_DAT}$ | Standard mode | | 250 | | ns |
| | | Fast mode | | 100 | | |
| | | Fast mode plus | | 50 | | |
| | | High-speed mode | | 10 | | |
| Data Hold Time | $t_{HD_DAT}$ | Standard mode | 0 | | 3.45 | ns |
| | | Fast mode | 0 | | 900 | |
| | | Fast mode plus | 0 | | 450 | |
| | | High-speed mode, $C_B$ ≤ 100pF | 0 | | 70 | |
| | | High-speed mode, $C_B$ ≤ 400pF | 0 | | 150 | |
| SCL Rise Time | $t_{RCL}$ | Standard mode | | | 1500 | ns |
| | | Fast mode | | | 1000 | |
| | | Fast mode plus | | | 500 | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 10 | | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 20 | | |

## I²C TIMING SPECIFICATIONS (continued)

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 3.6V. All typical values are measured at $T_J$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V and EN = HIGH, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL Fall Time | $t_{FCL}$ | Standard mode | | | 800 | ns |
| | | Fast mode | | | 600 | |
| | | Fast mode plus | | | 400 | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 10 | 40 | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 20 | 80 | |
| Rise Time of SCL after a Repeated Start Condition and after ACK Bit | $t_{RCL1}$ | High-speed mode, $C_B$ ≤ 100pF | | 10 | 80 | ns |
| | | High-speed mode, $C_B$ ≤ 400pF | | 20 | 160 | |
| SDA Rise Time | $t_{RDA}$ | Standard mode | | | 800 | ns |
| | | Fast mode | | | 600 | |
| | | Fast mode plus | | | 400 | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 10 | 80 | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 20 | 160 | |
| SDA Fall Time | $t_{FDA}$ | Standard mode | | | 800 | ns |
| | | Fast mode | | | 600 | |
| | | Fast mode plus | | | 400 | |
| | | High-speed mode, $C_B$ ≤ 100pF | | 10 | 80 | |
| | | High-speed mode, $C_B$ ≤ 400pF | | 20 | 160 | |
| Stop Condition Setup Time | $t_{SU_STO}$ | Standard mode | | 4 | | ns |
| | | Fast mode | | 600 | | |
| | | Fast mode plus | | 120 | | |
| | | High-speed mode | | 160 | | |
| Capacitive Load for SDA and SCL | $C_B$ | | | | 400 | pF |

**Table 1. Recommended External Components for 3.0A (MAX) Load Current**

| COMPONENT | DESCRIPTION | VENDOR | PARAMETER | TYP | UNITS |
|---|---|---|---|---|---|
| $L_1$ | 330nH, 2016 Case Size | See Table 2 | | | |
| $L_1$ Alternative (1) | 470nH 2016 Case Size | | | | |
| $C_{OUT1}$, $C_{OUT2}$ | 47μF, 6.3V, X5R, 0603 | GRM188R60J476ME15 (Murata) | C | 47 | μF |
| $C_{OUT1}$, $C_{OUT2}$ Alternative (1) | 22μF, 10V, X5R, 0603 | GRM188R61A226ME15D (Murata) | C | 22 | |
| $C_{IN}$ | 1 Piece; 4.7μF, 10V, X5R, 0603 | GRM188R61A475KE15D (Murata) | C | 4.7 | |
| $C_{BY}$ (1) | 1 Piece; 100nF, 6.3V, X5R, 0201 | GRM033R60J104KE19D (Murata) | C | 100 | nF |

NOTE 1. If the reference design is not followed, $L_1$ alternative and $C_{OUT1}$, $C_{OUT2}$ alternative can be applied. It is recommended to use an optional capacitor $C_{BY}$ to reduce any high frequency component on VIN bus.

**Table 2. Recommended Inductors**

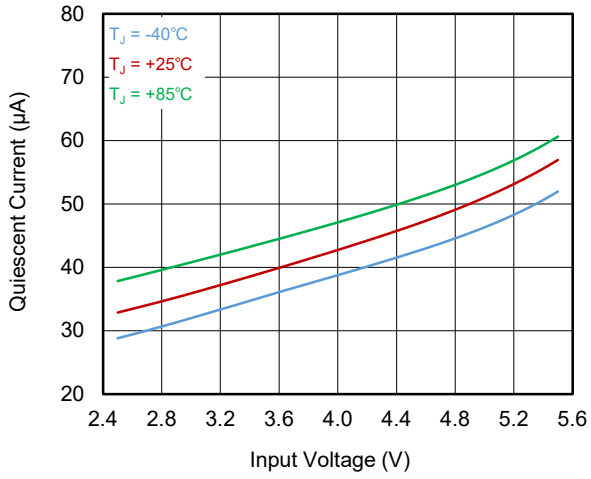
| MANUFACTURER | PART # | L (nH) | DCR (mΩ, TYP) | $I_{SAT}$ (1) | L | W | H |
|---|---|---|---|---|---|---|---|
| Murata | DFE201612E-R33M | 330 | 21 | 6.3 | 2.0 | 1.6 | 1.2 |
| Murata | DFE201612E-R47M | 470 | 26 | 5.5 | 2.0 | 1.6 | 1.2 |
| Wurth Elektronik | 74479276147 | 470 | 26 | 6.3 | 2.0 | 1.6 | 1.0 |
| Cyntek | HMLQ20161B-R47MDR | 470 | 20 | 5.8 | 2.0 | 1.6 | 1.2 |

NOTE 1. $I_{SAT}$: the DC current reduces the inductance by 30%.

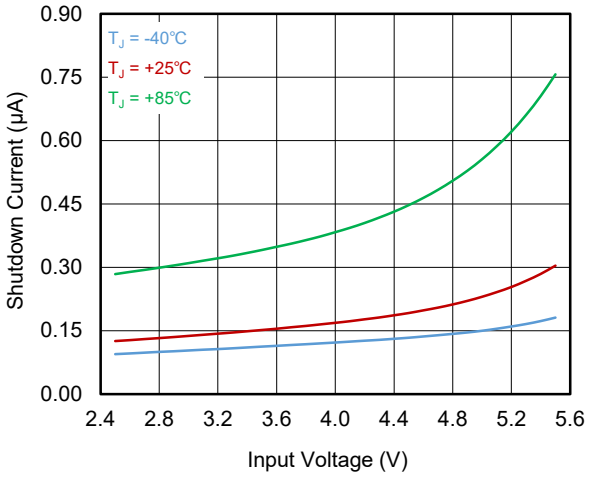
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V, $V_{SEL}$ = EN = $V_{IN}$, unless otherwise noted.

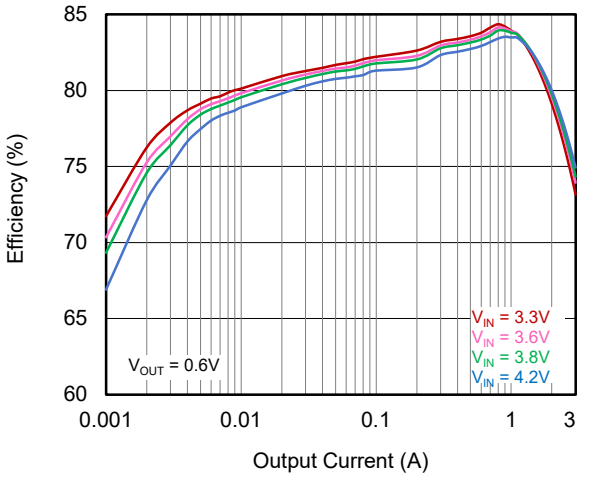
Quiescent Current vs. Input Voltage



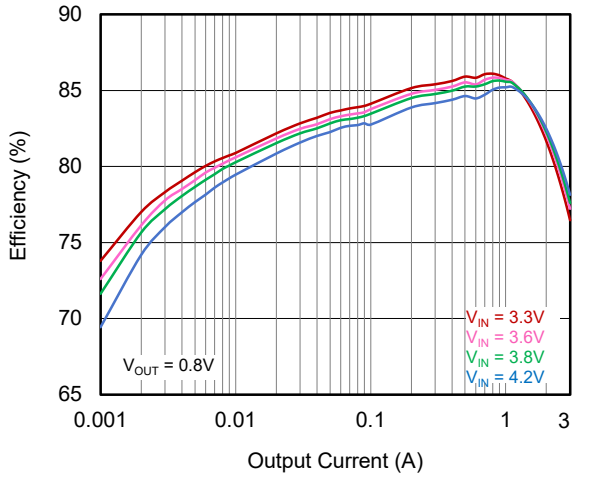

Shutdown Current vs. Input Voltage



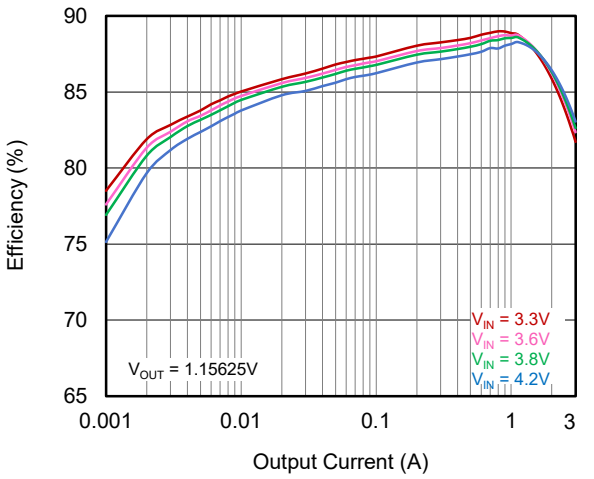

Efficiency vs. Output Current



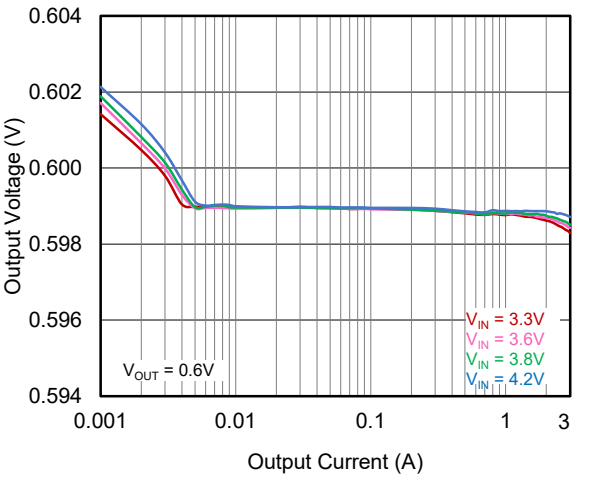

Efficiency vs. Output Current




Efficiency vs. Output Current



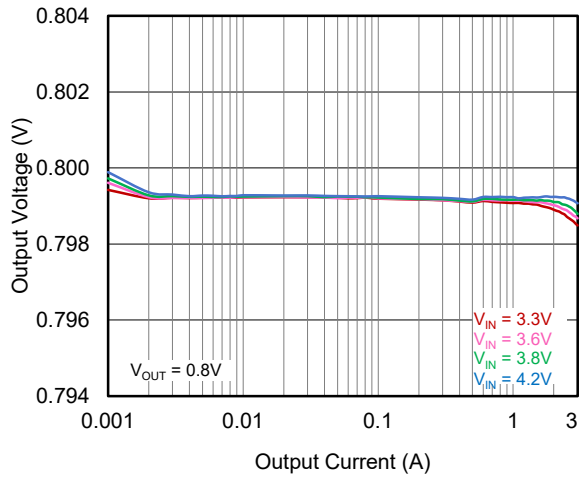

Output Voltage vs. Output Current



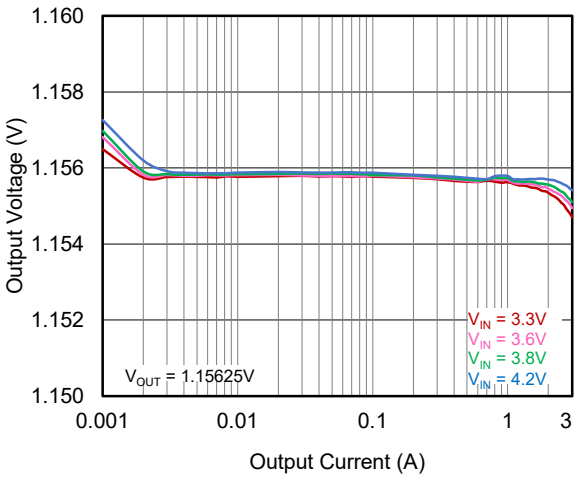
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V, $V_{SEL}$ = EN = $V_{IN}$, unless otherwise noted.

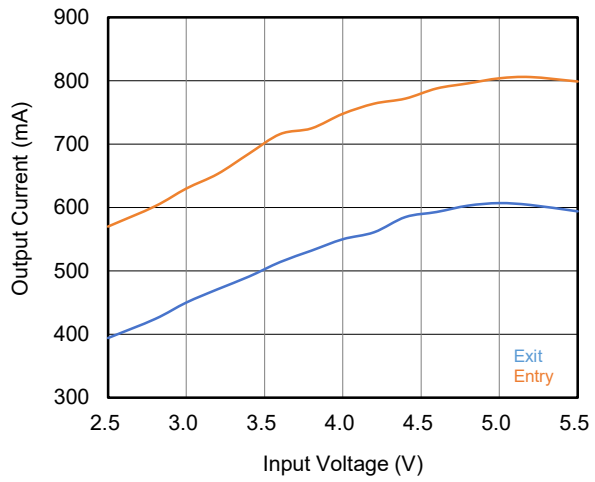
Output Voltage vs. Output Current



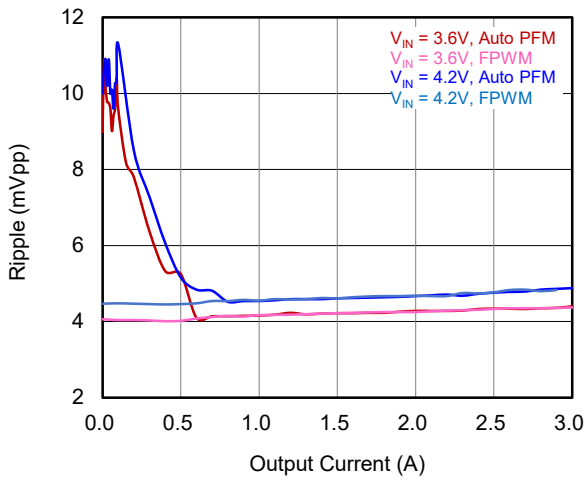

Output Voltage vs. Output Current



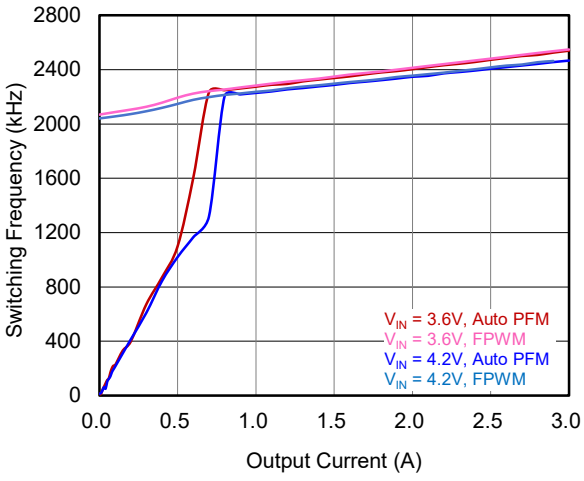

PWM Entry/Exit Level vs. Input Voltage



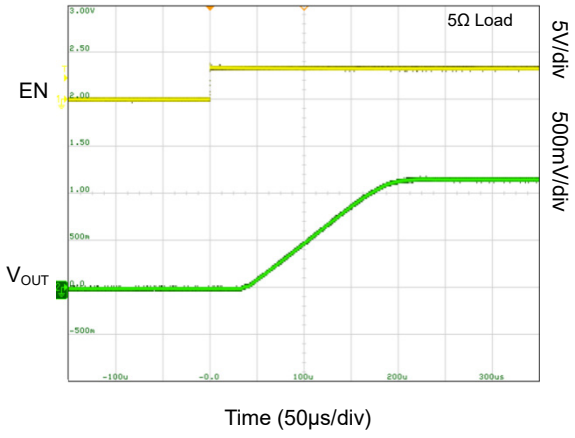

Ripple vs. Output Current




Switching Frequency vs. Output Current



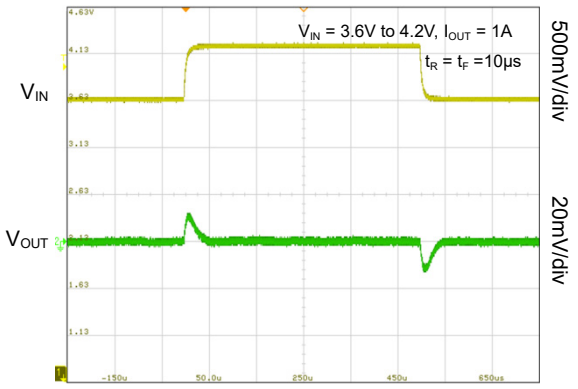

Start-up



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

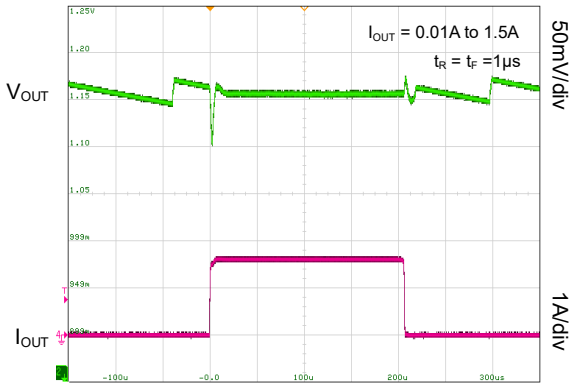
$T_A$ = +25℃, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.15625V, $V_{SEL}$ = EN = $V_{IN}$, unless otherwise noted.

Line Transient



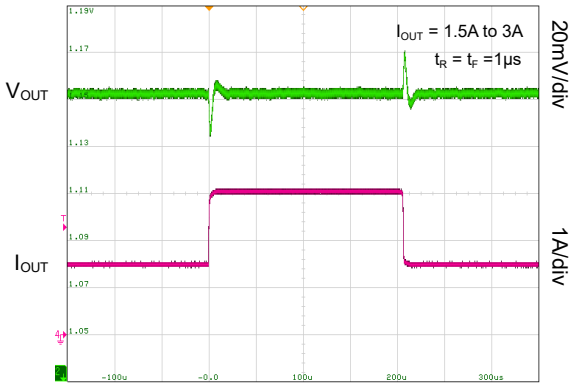

Time (100μs/div)

Load Transient




Time (50μs/div)

Load Transient




Time (50μs/div)

# DETAILED DESCRIPTION

## Operation Description

The SGM6026 is a synchronous Buck converter with an input voltage range of 2.5V to 5.5V. The device can deliver output current up to 3A with above 80% efficiency. The nominal frequency of SGM6026 when operate at PWM mode is 2.3MHz. Benefiting from this, the value of external inductor can be reduced to 330nH or 470nH with output capacitor reduced to 44μF. At light load, the device enters PFM to obtain high efficiency.

The SGM6026 supports $I^2C$ communication with transfer rate up to 3.4Mbps. The $I^2C$ interface allows:

• Real-time adjusts the output voltage with a step of 6.25mV.
• Change modes between FPWM and auto PFM.
• Adjust voltage transition speed.
• Enable and disable the device.

## Control Scheme

The SGM6026 adopts the constant on-time (COT) architecture to provide superior load transient performance. The device maintains a constant switching frequency over a wide operation range. Using the advanced control architecture, the SGM6026 supports low-ESR ceramic output capacitor and offers the excellent load and line regulation performance.

At light load, the device automatically operates in single-pulse PFM to provide excellent light load efficiency. The control scheme offers smooth transition between PFM and PWM modes.

The PFM can be disabled by configuring the MODE bits in the CONTROL register along with the VSEL pin state. Refer to the CONTROL register (**REG0x02**) for more details.

## Enable and Soft-Start

When the EN is low, the power FETs and the internal control circuits are off, and the device consumes very low current. Under this state, the $I^2C$ interface still works if the input voltage is above the UVLO and the device registers maintain the content. At power-on reset (POR), all the registers are reset.

The device offers an output discharge through internally connecting a load from VOUT to GND. The function can be activated through enabling the OUTPUT_DISCHARGE bit high (CONTROL register, bit 8) and pulling the EN pin or BUCK_ENx bit low.

When both EN and BUCK_ENx bit is high, the device is enabled and starts soft-start. During soft-start, the internal reference ramps slowly to achieve soft output ramp. The soft-start mechanism effectively reduces the inrush current drawn from the input source, as well as providing a controlled output voltage rising ramp. For pre-biased output voltage start-up, the device starts up from the pre-biased voltage to the programmed output voltage.

If the output capacitance is large, the device could fail to start. The maximum value of output capacitor during soft-start with a constant-current load is approximately:

$$C_{OUT_MAX} \approx \left(I_{PEAK} - I_{LOAD}\right) \times \frac{320\mu F}{V_{OUT}} \quad (1)$$

where $C_{OUT_MAX}$ is in μF and $I_{LOAD}$ is the constant current load during soft-start in A.

If the device is reaches the over-current limit for 16 consecutive switching cycles, the device shuts down and would attempt to restart after 1.7ms delay. This behavior prevents the device from over-heating during soft-start with heavy load.

Beside hardware EN enable control, the device also offers software enable/disable control. When the EN pin is high, the BUCK_ENx bits are available to control the device. Both BUCK_EN0 and BUCK_EN1 bits are initiated high after POR. If VESL is low, BUCK_EN0 bit can enable/disable the device regardless of the state of BUCK_EN1. If VSEL is high, BUCK_EN1 bit can control the device regardless of the state of BUCK_EN0.

**Table 3. Hardware and Software Enable**

| PINS | | BITS | | OUTPUT | MODE |
|---|---|---|---|---|---|
| EN | VSEL | BUCK_EN0 | BUCK_EN1 | | |
| 0 | X | X | X | Off | Shutdown |
| 1 | 0 | 0 | X | Off | Shutdown |
| 1 | 0 | 1 | X | On | Auto PFM |
| 1 | 1 | X | 0 | Off | Shutdown |
| 1 | 1 | X | 1 | On | FPWM |

# DETAILED DESCRIPTION (continued)

## VSEL Pin and I²C Programming Output Voltage

The output voltage is programmed by the NSELx control bits in VSELx register which is given as:

$$V_{OUT} = 0.6V + NSELx \times 6.25mV \quad (2)$$

For example, if NSEL = 1100100 (100 decimal), then $V_{OUT}$ = 0.6mV + 0.625mV = 1.225V.

The state of VSEL pin decides which VSELx register takes control of the output voltage. Setting VSEL low selects VSEL0 and setting VSEL high corresponds to VSEL1. Both VSEL0 and VSEL1 are reset at POR.

## Output Ramp Speed Control

When the output is adjusted to a higher voltage, the device offers eight level of output ramp speed through the SLEW bits in the CONTROL register.

**Table 4. Output Ramp Speed**

| SLEW BIN (bit [6:4]) | RAMP SPEED |
|---|---|
| 000 | 64.00mV/μs |
| 001 | 32.00mV/μs |
| 010 | 16.00mV/μs |
| 011 | 8.00mV/μs |
| 100 | 4.00mV/μs |
| 101 | 2.00mV/μs |
| 110 | 1.00mV/μs |
| 111 | 0.50mV/μs |

For transition to a lower voltage, the device automatically enters FPWM mode.

## Under-Voltage Lockout (UVLO)

The SGM6026 offers input under-voltage lockout to prevent false triggering with unstable input source. The device's UVLO rising voltage is 2.3V (TYP) and falling threshold is 2.14V (TYP). The device stops operation as soon as the input voltage drops below the falling threshold.

## Input Over-Voltage Protection (OVP)

The SGM6026 offers input over-voltage protection to protect the device from damage. The device stops switching when $V_{IN}$ exceeds $V_{SDWN}$ (6.04V, TYP). An internal filter is incorporated to prevent false triggering due to noise.

## Switch Current Limiting

The device implements over-current protection when the load exceeds the maximum allowed current to prevent excessive current drawn from battery type inputs. During an output short scenario or a saturated inductor, the inductor current will reach the current limit threshold. When current limit threshold is reached, the device turns off the high-side switch to terminate the inductor current from further increase, and the low-side switch turns on to ramp down the inductor current to the low-side switch current limit.

If the high-side or low-side switch current limit is triggered during a switching cycle, the counter is incremented by one. When the counter reaches 16, the switching is terminated immediately. The device would re-attempt to soft-start after 1.7ms delay.

## Thermal Shutdown

Under heavy load or high ambient temperature, the device junction temperature rises continuously. As the junction temperature exceeds above the $T_{SD}$ (+150℃, TYP), the device stops switching and enters thermal shutdown. The device has a 20℃ (TYP) thermal shutdown hysteresis to allow the device to resume operation automatically with an internal soft-start.

## MONITOR Register (REG0x05)

The MONITOR register indicates the regulation state of the device. After power-up, the register is 1000 0001.

## I²C Serial Interface

Standard I²C interface is used to program SGM6026 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM6026 operates as a slave device that address is 60.

The interface of SGM6026 supports four communication modes defined in the I²C specification: standard mode (100kbps), fast mode (400kbps), fast mode plus mode (1Mbps) and high-speed mode (3.4Mbps). The data transfer protocols for the standard, fast and fast plus modes are the same, while the protocol for high-speed is different.

# DETAILED DESCRIPTION (continued)

## I²C Data Communication for Standard, Fast and Fast Plus Modes

### START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

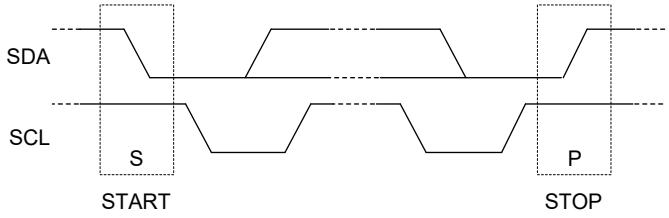



**Figure 2. I²C Bus in START and STOP Conditions**

### Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 3.

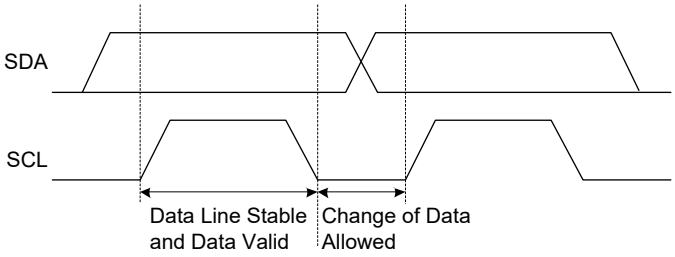



**Figure 3. I²C Bus Bit Transfer**

### Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 4 shows the byte transfer process with I²C interface.

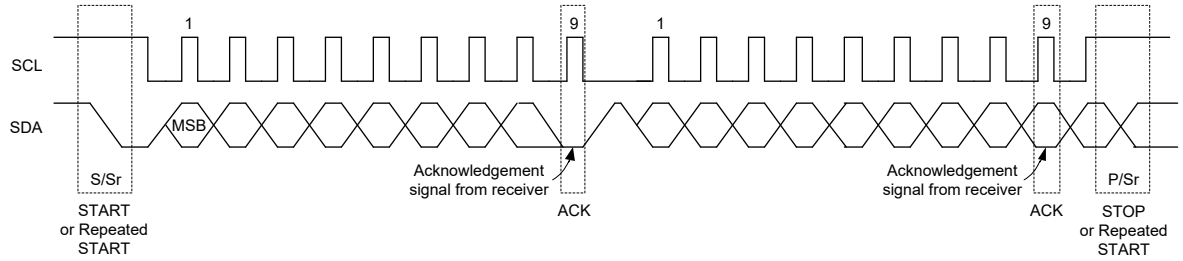



**Figure 4. Byte Transfer Process**

### Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

## DETAILED DESCRIPTION (continued)

### Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 5.

**WRITE:** If the master wants to write in the register, the third byte can be written directly as shown in Figure 6 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

**READ:** If the master wants to read a single register (Figure 7), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

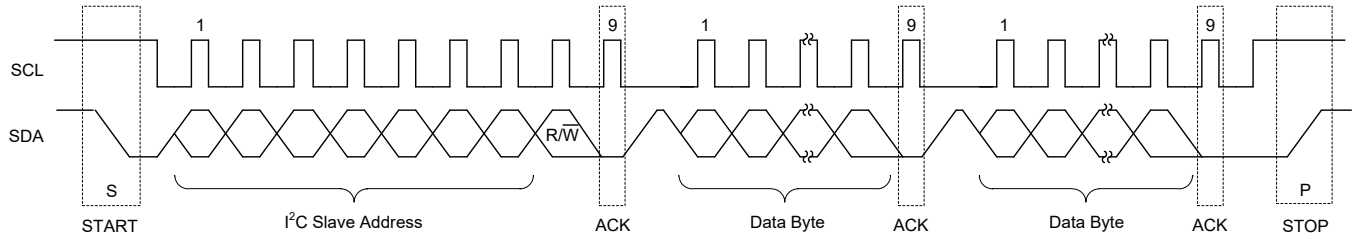



**Figure 5. Data Transfer Transaction in Standard, Fast and Fast Plus Modes**

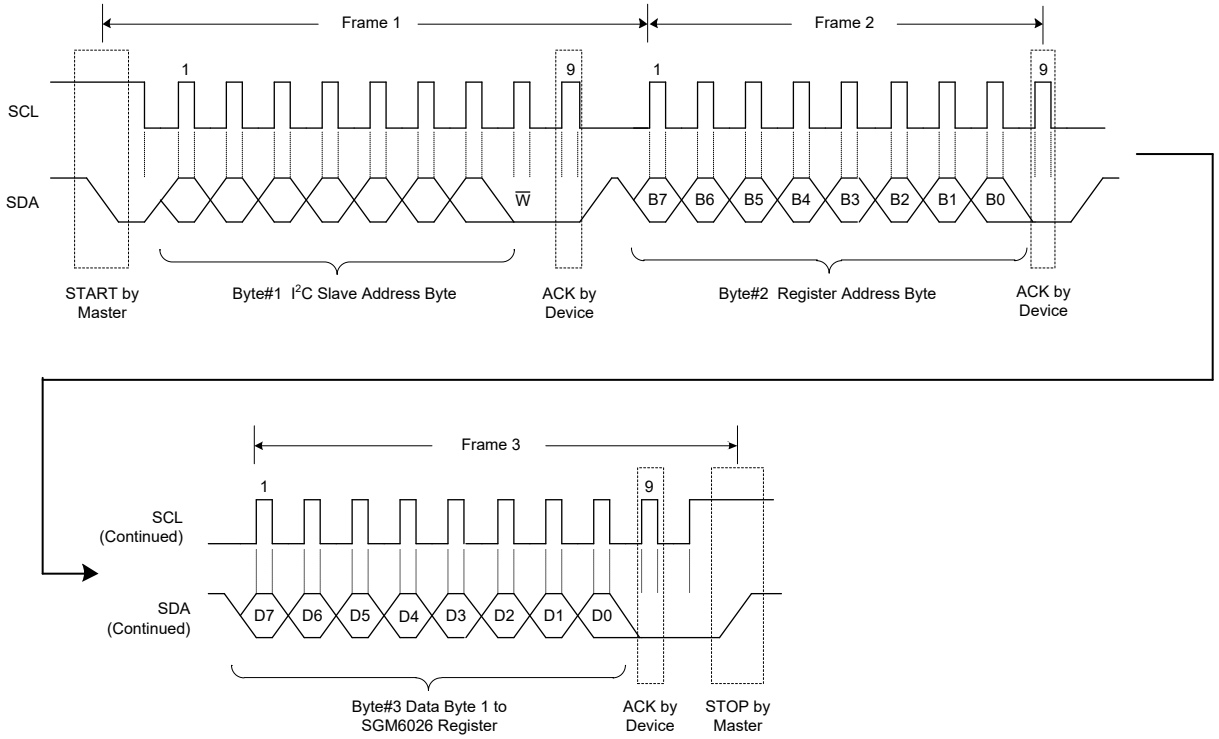



**Figure 6. A Single Write Transaction in Standard, Fast and Fast Plus Modes**

## DETAILED DESCRIPTION (continued)

### High-Speed (HS) Mode

The protocol for high-speed mode is different from standard, fast and fast plus modes. The high-speed mode is entered after the master sends the HS master code 0000 1XXX after a start condition. The HS master code is sent at standard, fast or fast plus mode with rate less than 1Mbps. The slave device is not allowed to acknowledge the HS master code, while they need to recognize and shift the interface to HS mode. Then, the master sends a repeated start condition. After that, the transaction in HS mode begins where the protocol is the same as standard, fast and fast plus mode except that the transmission rate is increased to 3.4Mbps. The master sends a stop condition to stop the HS mode. Instead, repeated start condition is necessary to maintain transmission in HS mode.

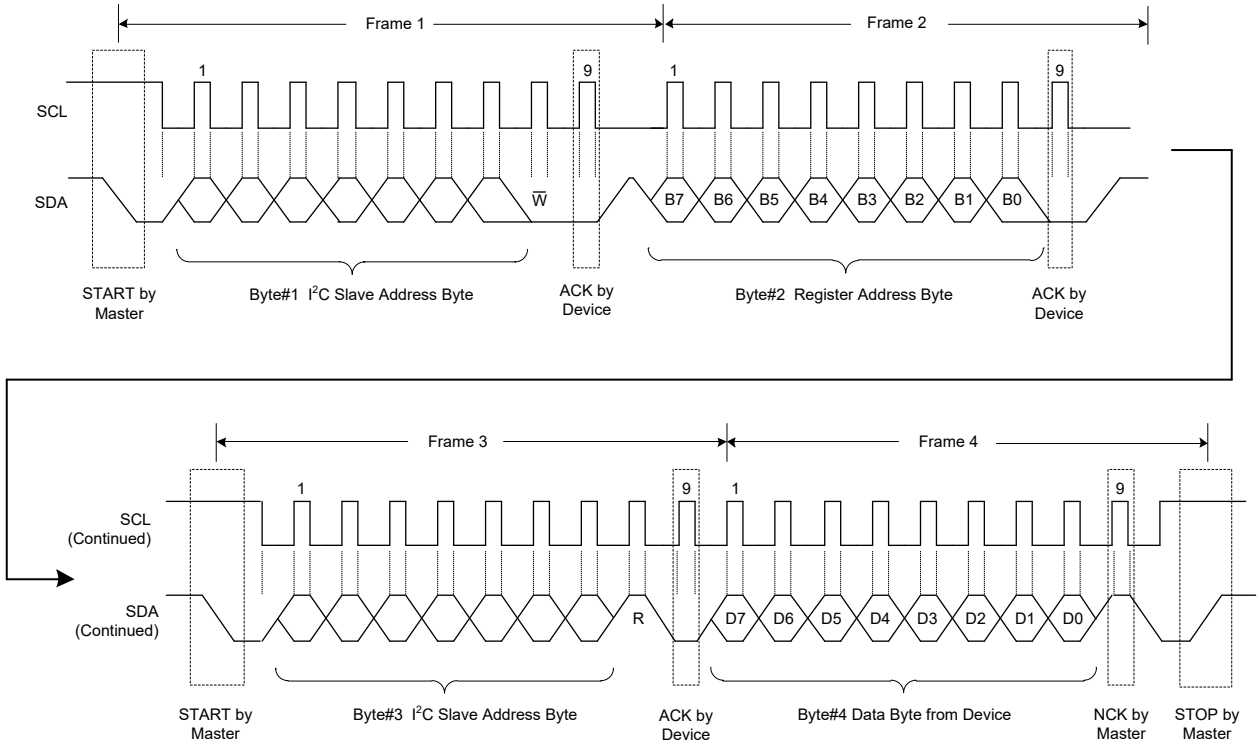



**Figure 7. A Single Read Transaction in Standard, Fast and Fast Plus Modes**

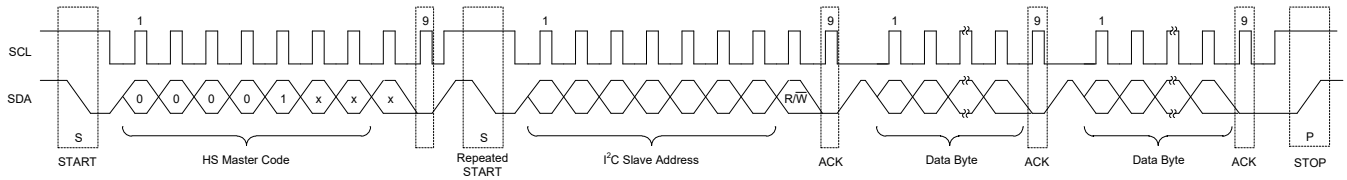



**Figure 8. Data Transfer Transaction in HS Mode**

# REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

## I²C Slave Address of SGM6026: 0xXX

| ADDRESS | REGISTER NAME | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | VSEL0 | BUCK_EN0 | NSEL0[6:0] | | | | | | |
| 0x01 | VSEL1 | BUCK_EN1 | NSEL1[6:0] | | | | | | |
| 0x02 | CONTROL | OUTPUT_ DISCHARGE | SLEW[6:4] | | | Reserved | RESET | MODE[1:0] | |
| 0x03 | ID1 | VENDOR[7:5] | | | Reserved | DIE_ID[3:0] | | | |
| 0x04 | ID2 | Reserved | | | | DIE_REV[3:0] | | | |
| 0x05 | MONITOR | PGOOD | UVLO | OVP | POS | NEG | RESET-STAT | OT | BUCK_STATUS |

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit.

W/C: Writing a ‘0’ clears the bit. Writing a ‘1’ has no effect.

# REGISTER MAPS (continued)

## REG0x00: VSEL0 Register [Reset = 0XD9]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | BUCK_EN0 | 1 | R/W | Software Buck Enable.<br>When EN pin is low, the regulator is off.<br>When EN pin is high, BUCK_EN bit takes precedent. |
| D[6:0] | NSEL0[6:0] | 101 1001 | R/W | Set $V_{OUT}$ value from 0.6V to 1.39375V (Default: 1.15625V). |

## REG0x01: VSEL1 Register [Reset = 0xD9]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | BUCK_EN1 | 1 | R/W | Software Buck Enable.<br>When EN pin is low, the regulator is off.<br>When EN pin is high, BUCK_EN bit takes precedent. |
| D[6:0] | NSEL1[6:0] | 101 1001 | R/W | Set $V_{OUT}$ value from 0.6V to 1.39375V (Default: 1.15625V). |

## REG0x02: CONTROL Register [Reset = 0x82]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | OUTPUT_ DISCHARGE | 0 | R/W | 0 = When disabled, $V_{OUT}$ is not discharged.<br>1 = When disabled, $V_{OUT}$ discharges through an internal pull-down. |
| D[6:4] | SLEW[6:4] | 111 | R/W | Set the slew rate for positive voltage transitions. |
| D[3] | Reserved | 0 | R/W | Always reads back 0. |
| D[2] | RESET | 0 | R/W | 1 = Reset all registers to default values.<br>Always reads back 0. |
| D[1:0] | MODE | 10 | R/W | In combination with the VSEL pin, these two bits set the operation of the Buck to be either in Auto PFM/PWM mode during light load or forced PWM mode.<br>Mode of Operation<br>VSEL Pin Binary Operation<br>Low X0 Auto PFM/PWM<br>Low X1 Forced PWM<br>High 0X Auto PFM/PWM<br>High 1X Forced PWM |

## REG0x03: ID1 Register [Reset = 0x81]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:5] | VENDOR[7:5] | 100 | R | Signifies On Semiconductor as the IC vendor. |
| D[4] | Reserved | 0 | R | Always reads back 0. |
| D[3:0] | DIE_ID[3:0] | 0001 | R | Die ID. |

## REG0x04: ID2 Register [Reset = 0x08]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Always reads back 0000. |
| D[3:0] | DIE_REV[3:0] | 1000 | R | Die Revision. |

## REGISTER MAPS (continued)

### REG0x05: MONITOR Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | PGOOD | 0 | R | 1 = Buck is enabled and soft-start is completed. |
| D[6] | UVLO | 0 | R | 1 = $V_{IN}$ is less than the UVLO threshold. |
| D[5] | OVP | 0 | R | 1 = $V_{IN}$ is greater than the OVP threshold. |
| D[4] | POS | 0 | R | 1 = A positive voltage transition is in progress and the output voltage has not yet reached its new set point. |
| D[3] | NEG | 0 | R | 1 = A negative voltage transition is in progress and the output voltage has not yet reached its new set point. |
| D[2] | RESET_STAT | 0 | R | 1 = A register reset was performed. This bit is cleared after REG0x05 is read. |
| D[1] | OT | 0 | R | 1 = Thermal shutdown is active. |
| D[0] | BUCK_STATUS | 0 | R | 0 = Buck disabled (default)<br>1 = Buck enabled |

# APPLICATION INFORMATION

Figure 9 below shows a typical schematic for a 1.15625V output application with a wide input voltage range.

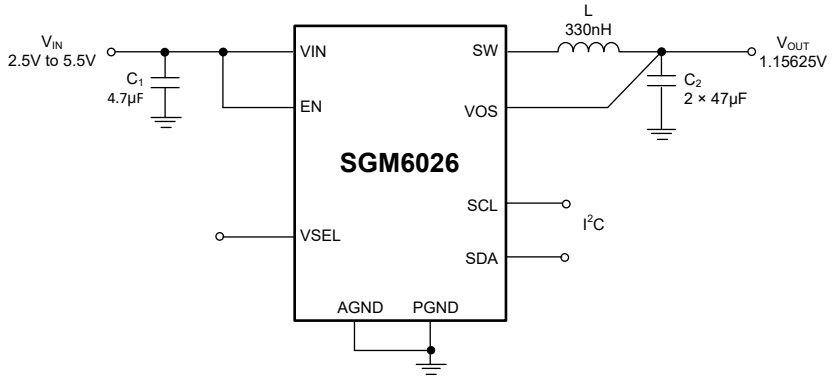



**Figure 9. Typical Application Circuit**

Table 5 below shows the operation conditions of this design example.

**Table 5. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage | 2.5V to 5.5V |
| Output Voltage | 1.15625V |
| Maximum Output Current | 3A |

### Inductor Selection

The inductance of the output filter (L) determines the peak-to-peak ripple current and indirectly affects the converter efficiency and output voltage ripple. It also determines the current at which the PWM to PFM transition occurs (CCM to DCM). The ripple current ($\Delta I_L$) can be estimated from Equation 3. It shows that $\Delta I_L$ decreases with larger inductance values and increases at higher voltage levels ($V_{IN}$ or $V_{OUT}$).

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

In steady state, the maximum inductor current can be calculated from Equation 4.

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2} \quad (4)$$

Where, f is switching frequency, L is inductance value, $\Delta I_L$ is the inductor peak-to-peak ripple current and $I_{L_MAX}$ is the peak inductor current. The maximum current should never reach the inductor saturation level. This situation can happen after a large load step. A common conservative option is to choose an inductor with a saturation current equal to or higher than the high-side switch current limit.

### Input Capacitor

A low ESR ceramic capacitor must be connected close to the VIN and GND pins to provide the pulsating input current of the converter and minimize switching noise and ringing. A 4.7μF ceramic capacitor is satisfied for most applications, however, if a high impedance source such as a coin cell-battery is used, larger input capacitance ($C_{IN}$ ≥ 10μF) is preferred to prevent voltage drops during start-up or load steps. There is no high limit for the input capacitance, however, note that the higher leakage current of a large input capacitor will increase the total quiescent current of the power supply. In addition, a 100nF bypass capacitor ($C_{BY}$) is recommended in parallel with the input capacitor to reduce high frequency noise on the bus.

### Output Capacitor

The architecture of SGM6026 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR) to achieve low output voltage ripple. X5R or X7R dielectrics are recommended. For SGM6026, 2 × 22μF or 2 × 47μF for $C_{OUT}$ are suitable for operation.

## APPLICATION INFORMATION (continued)

**Layout Guidelines**

$C_1$ is the input capacitor and $C_2$ is the input bypass capacitor (0.1μF, optional). $C_3$ and $C_4$ are the output capacitors. $L_1$ is the inductor.

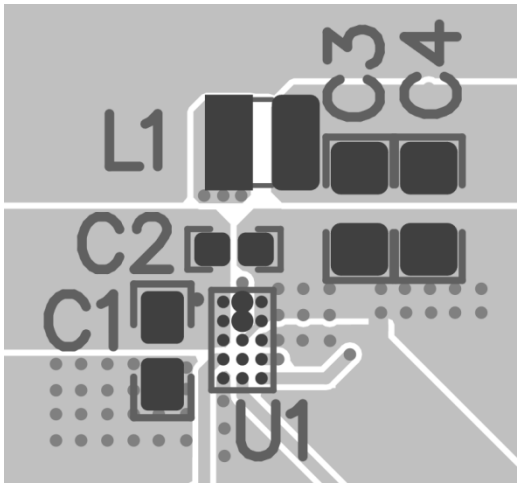



**Figure 10. PCB Layout Example**

## REVISION HISTORY

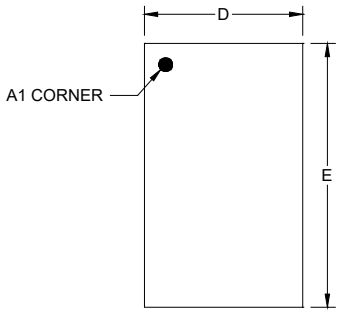
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| NOVEMBER 2026 – REV.A to REV.A.1 | Page |
|---|---|
| Added MIN and MAX values of PMOS Peak Current Limit in ELECTRICAL CHARACTERISTICS section | 4 |
| Updated Table 1, Table 2 and TYPICAL PERFORMANCE CHARACTERISTICS | 6, 7, 8 |

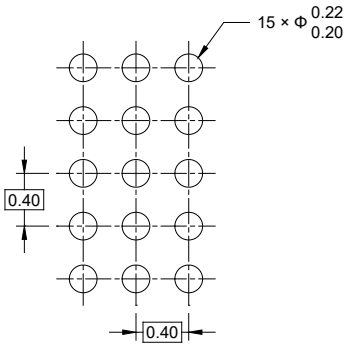
| Changes from Original (DECEMBER 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

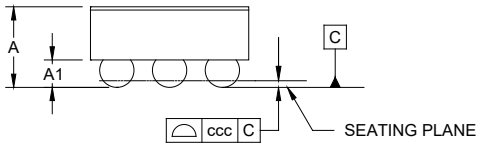
## WLCSP-1.2×2-15B



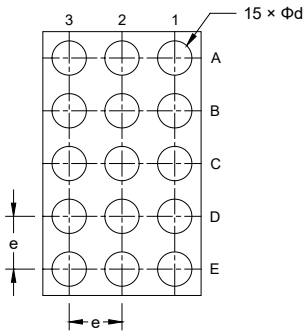

TOP VIEW




**RECOMMENDED LAND PATTERN** (Unit: mm)




SIDE VIEW



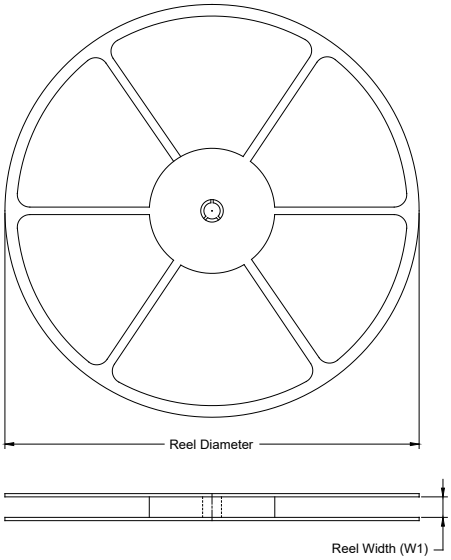

BOTTOM VIEW

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 0.661 |
| A1 | 0.188 | - | 0.228 |
| D | 1.172 | - | 1.232 |
| E | 1.972 | - | 2.032 |
| d | 0.230 | - | 0.290 |
| e | 0.400 BSC | | |
| ccc | 0.050 | | |

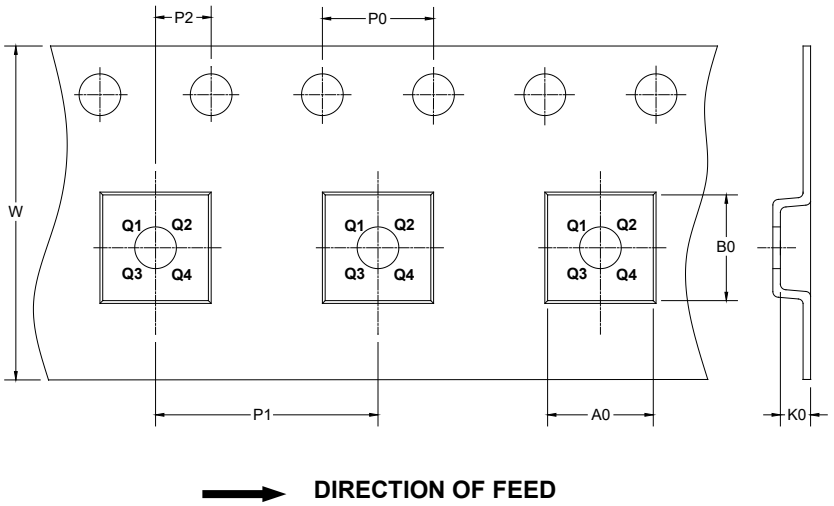
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



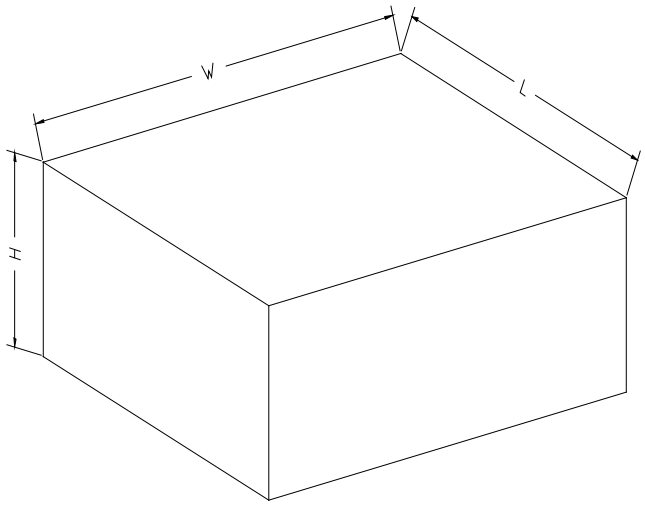

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-1.2×2-15B | 7" | 8.6 | 1.32 | 2.15 | 0.77 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002