SGM4522Q
Automotive, Bidirectional 8:1, 5V, 1-Channel Multiplexer with Injection Current Control

GENERAL DESCRIPTION

The SGM4522Q is a single 8-channel CMOS analog multiplexer with injection current control. The device has three control inputs that can be used as selecting one of the 8 channels (Sx) to connect to the common terminal (Dx). The multiplexer supports bidirectional signal transmission in the voltage range from GND to V_{DD}.

All logic inputs of the SGM4522Q are allowed to be equal to the power supply voltage and compatible with TTL and CMOS logic thresholds standards during normal operation of the power supply. Besides, all control inputs are also designed with fail-safe function. It allows the voltage of all control pins within the maximum absolute withstand voltage range to exceed the V_{DD} without damaging the device.

The injection current control function of the SGM4522Q allows signals on disabled signal channels to exceed the V_{DD} without affecting the enabled signal channel. In addition, all pins of the SGM4522Q except GND are not designed with internal diodes path to the V_{DD} pin, so as not to damage the components connected to the power pin and avoid injecting reverse current into the power supply.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM4522Q is available in Green TSSOP-16 and TQFN-2.5×3.5-16AL packages. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **V_{DD} Operation Range: 1.62V to 5.5V**
- **Injection Current Control**
- **Back-Powering Protection**
  No ESD Diodes between All Ports and V_{DD}
- **Bidirectional Signal Path**
- **Rail-to-Rail Operation**
- **Control Pin Fail-Safe Function**
- **Break-Before-Make Switching**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and TQFN-2.5×3.5-16AL Packages**

APPLICATIONS

Automotive System
Battery Management Systems (BMS)
Signal Multiplexing and Demultiplexing
Diagnostics and Monitoring in Automotive
ADC and DAC System

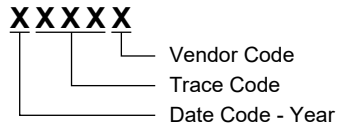
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM4522Q	TSSOP-16	-40℃ to +125℃	SGM4522QTS16G/TR	0DNTS16 XXXXX	Tape and Reel, 4000
	TQFN-2.5×3.5-16AL	-40℃ to +125℃	SGM4522QTVF16G/TR	0NGTVF XXXXX YYYYYY	Tape and Reel, 8000

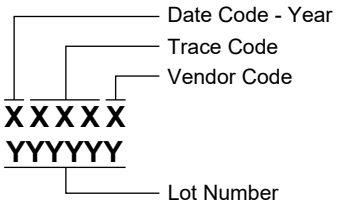
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

TSSOP-16



TQFN-2.5×3.5-16AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.5V to 6V
Logic Control Input Pin Voltage ($\overline{EN}$, A0, A1, A2), V_{SEL} or V_{EN} ..... -0.5V to 6V
Source or Drain Voltage, V_S or V_D ..... -0.5V to (V_{DD} + 0.5V)
Continuous Current through Switch (Sx, D Pins), I_S or $I_{D(CONT)}$
-40℃ to +125℃ ..... -50mA to 50mA
Continuous Current through GND, I_{GND} .... -100mA to 100mA
Package Thermal Resistance
TSSOP-16, θ_{JA} ..... 130.8℃/W
TSSOP-16, θ_{JB} ..... 88.2℃/W
TSSOP-16, θ_{JC} ..... 53.6℃/W
TQFN-2.5×3.5-16AL, θ_{JA} ..... 63.8℃/W
TQFN-2.5×3.5-16AL, θ_{JB} ..... 25.4℃/W
TQFN-2.5×3.5-16AL, $\theta_{JC(TOP)}$ ..... 51.3℃/W
TQFN-2.5×3.5-16AL, $\theta_{JC(BOT)}$ ..... 7.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD} ..... 1.62V to 5.5V
Signal Path Input/Output Voltage, V_S or V_D ..... 0V to V_{DD}
Logic Control Input Pin Voltage ($\overline{EN}$, A0, A1, A2), V_{SEL} or V_{EN} ..... 0V to 5.5V
Continuous Current through Switch (Sx, D Pins), I_S or $I_{D(CONT)}$
-40℃ to +125℃ ..... -50mA to 50mA
Current per Input into Source or Drain Pins when Signal Voltage Exceeds Recommended Operating Voltage, I_{OK} ..... -50mA to 50mA
Injected Current into Single Off Switch Input, I_{INJ} ..... -50mA to 50mA
Total Injected Current into All Off Switch Inputs Combined, I_{INJ_ALL} ..... -100mA to 100mA
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

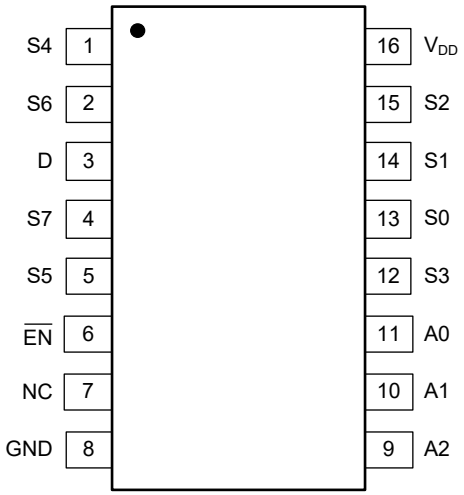
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

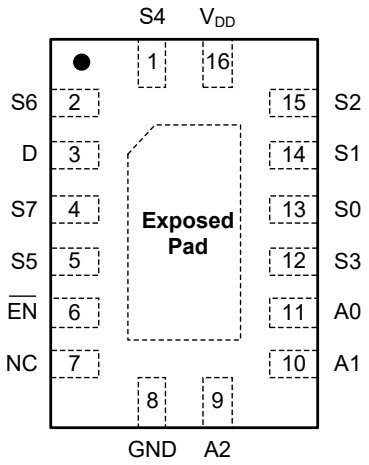
PIN CONFIGURATIONS

SGM4522Q (TOP VIEW)



TSSOP-16

SGM4522Q (TOP VIEW)



TQFN-2.5×3.5-16AL

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-16	TQFN-2.5×3.5-16AL		
1	1	S4	Source Pin 4. Signal input or output path.
2	2	S6	Source Pin 6. Signal input or output path.
3	3	D	Drain Pin (Common Terminal). Signal input or output path.
4	4	S7	Source Pin 7. Signal input or output path.
5	5	S5	Source Pin 5. Signal input or output path.
6	6	$\overline{EN}$	Enable Control Input Pin (Active Low). When $\overline{EN}$ is set to high, common terminal is disconnected to any other signal ports.
7	7	NC	No Connection.
8	8	GND	Ground Pin.
9	9	A2	Digital Address A2 Pin.
10	10	A1	Digital Address A1 Pin.
11	11	A0	Digital Address A0 Pin.
12	12	S3	Source Pin 3. Signal input or output path.
13	13	S0	Source Pin 0. Signal input or output path.
14	14	S1	Source Pin 1. Signal input or output path.
15	15	S2	Source Pin 2. Signal input or output path.
16	16	V_{DD}	Power Supply Pin. It is recommended to connect a 0.1μF to 10μF capacitor between V_{DD} and GND to get good power supply decoupling.
—	Exposed Pad	Exposed Pad	Exposed Pad. It can be connected to GND or be left floating.

FUNCTIONAL BLOCK DIAGRAM

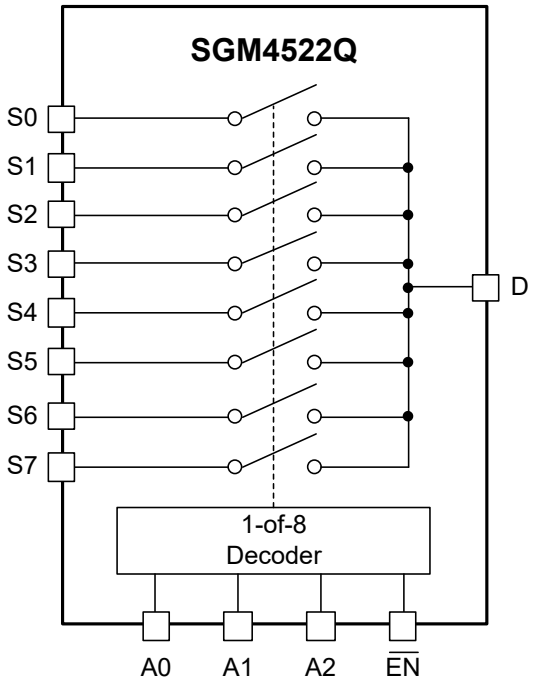


Figure 1. Block Diagram

FUNCTION TABLE

$\overline{EN}$	SELECT INPUTS			SELECTED SIGNAL PATH CONNECTED TO DRAIN (D) PIN
	A2	A1	A0	
0	0	0	0	S0
0	0	0	1	S1
0	0	1	0	S2
0	0	1	1	S3
0	1	0	0	S4
0	1	0	1	S5
0	1	1	0	S6
0	1	1	1	S7
1	***X***	***X***	***X***	All Channels are OFF

NOTE: ***X*** = Don't care.

ELECTRICAL CHARACTERISTICS

(At specified V_{DD} ±10%, typical values measured at nominal V_{DD}, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
On-Resistance	R_{ON}	V_S = 0V to V_{DD}, I_{SD} = 0.5mA, Test Circuit 1	V_{DD} = 1.8V	+25℃		950	1600	Ω
				Full			1800	
			V_{DD} = 2.5V	+25℃		260	385	
				Full			420	
			V_{DD} = 3.3V	+25℃		150	210	
				Full			240	
			V_{DD} = 5V	+25℃		93	120	
				Full			150	
On-Resistance Matching between Inputs	ΔR_{ON}	V_S = 0V to V_{DD}, I_{SD} = 0.5mA, Test Circuit 1	V_{DD} = 1.8V	+25℃		11	90	Ω
				Full			95	
			V_{DD} = 2.5V	+25℃		2.5	18	
				Full			20	
			V_{DD} = 3.3V	+25℃		1.2	8.5	
				Full			10	
			V_{DD} = 5V	+25℃		1	6	
				Full			7	
On-Resistance Flatness	R_{FLAT}	V_S = 0V to V_{DD}, I_{SD} = 0.5mA, Test Circuit 1	V_{DD} = 1.8V	+25℃		825	1400	Ω
				Full			1500	
			V_{DD} = 2.5V	25℃		175	270	
				Full			310	
			V_{DD} = 3.3V	+25℃		83	125	
				Full			130	
			V_{DD} = 5V	+25℃		40	60	
				Full			70	
Channel On Leakage Current	$I_{D(ON)}$ $I_{S(ON)}$	Switch On V_D = V_S = 0.8 × V_{DD} or V_D = V_S = 0.2 × V_{DD}, Test Circuit 2	V_{DD} = 1.8V	Full		±10	±800	nA
			V_{DD} = 2.5V	Full		±10	±800	
			V_{DD} = 3.3V	Full		±10	±800	
			V_{DD} = 5V	Full		±10	±800	
Source Off Leakage Current	$I_{S(OFF)}$	Switch Off V_D = 0.8 × V_{DD}/ 0.2 × V_{DD}, V_S = 0.2 × V_{DD}/ 0.8 × V_{DD}, Test Circuit 3	V_{DD} = 1.8V	Full		±10	±800	nA
			V_{DD} = 2.5V	Full		±10	±800	
			V_{DD} = 3.3V	Full		±10	±800	
			V_{DD} = 5V	Full		±10	±800	
Drain Off Leakage Current (Common Drain Pin)	$I_{D(OFF)}$	Switch Off V_D = 0.8 × V_{DD}/ 0.2 × V_{DD}, V_S = 0.2 × V_{DD}/ 0.8 × V_{DD}, Test Circuit 3	V_{DD} = 1.8V	Full		±10	±800	nA
			V_{DD} = 2.5V	Full		±10	±800	
			V_{DD} = 3.3V	Full		±10	±800	
			V_{DD} = 5V	Full		±10	±800	
V_{DD} Supply Current	I_{DDH}	Logic Inputs = V_{DD}	V_{DD} = 1.8V	Full		0.01	1	μA
			V_{DD} = 2.5V	Full		0.01	1	
			V_{DD} = 3.3V	Full		0.01	1	
			V_{DD} = 5V	Full		0.01	1	
V_{DD} Supply Current	I_{DDL}	Logic Inputs = 0V	V_{DD} = 1.8V	Full		0.2	1	μA
			V_{DD} = 2.5V	Full		0.3	1	
			V_{DD} = 3.3V	Full		0.4	1	
			V_{DD} = 5V	Full		0.6	1	

ELECTRICAL CHARACTERISTICS (continued)

(At specified V_{DD} ±10%, typical values measured at nominal V_{DD}, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX (1)	UNITS
Source Off Capacitance	C_{SOFF}	V_S = V_{DD} / 2, f = 1MHz	V_{DD} = 1.8V	Full		10	15	pF
			V_{DD} = 2.5V	Full		10	15	
			V_{DD} = 3.3V	Full		9.5	15	
			V_{DD} = 5V	Full		9	15	
Drain Off Capacitance	C_{DOFF}	V_S = V_{DD} / 2, f = 1MHz	V_{DD} = 1.8V	Full		15	20	pF
			V_{DD} = 2.5V	Full		15	20	
			V_{DD} = 3.3V	Full		14.5	20	
			V_{DD} = 5V	Full		14	20	
On Capacitance	C_{ON}	V_S = V_{DD} / 2, f = 1MHz	V_{DD} = 1.8V	Full		27.5	35	pF
			V_{DD} = 2.5V	Full		27.5	35	
			V_{DD} = 3.3V	Full		27	35	
			V_{DD} = 5V	Full		26	35	

NOTE:

1. Specified by design and characterization, not production tested.

LOGIC AND DYNAMIC CHARACTERISTICS

(At specified V_{DD} ±10%, typical values measured at nominal V_{DD}, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Logic Inputs ($\overline{EN}$, A0, A1, A2)								
Input Logic High	V_{IH}	V_{DD} = 1.8V		Full	1.0		5.5	V
		V_{DD} = 2.5V		Full	1.1		5.5	
		V_{DD} = 3.3V		Full	1.15		5.5	
		V_{DD} = 5V		Full	1.25		5.5	
Input Logic Low	V_{IL}	V_{DD} = 1.8V		Full	0		0.55	V
		V_{DD} = 2.5V		Full	0		0.65	
		V_{DD} = 3.3V		Full	0		0.8	
		V_{DD} = 5V		Full	0		0.9	
Logic High Input Leakage Current	I_{IH}	V_{LOGIC} = 1.8V or V_{DD}		Full		0.01	1	μA
Logic Low Input Leakage Current	I_{IL_AI}	V_{LOGIC} = 0V, V_{DD} = 1.8V to 5V		Full	-1	-0.01		μA
	I_{IL_EN}	V_{LOGIC} = 0V	V_{DD} = 1.8V	Full	-1	-0.2		
			V_{DD} = 2.5V	Full	-1	-0.3		
			V_{DD} = 3.3V	Full	-1	-0.4		
			V_{DD} = 5V	Full	-1	-0.6		
Logic Input Capacitance	C_{IN}	V_{LOGIC} = 0V, 1.8V or V_{DD}, f = 1MHz		Full		6.5	10	pF
Dynamic Characteristics								
Charge Injection	Q_{INJ}	V_S = V_{DD} / 2, R_S = 0Ω, C_L = 100pF, Test Circuit 4	V_{DD} = 1.8V	+25℃		-2		pC
			V_{DD} = 2.5V	+25℃		-6		
			V_{DD} = 3.3V	+25℃		-10		
			V_{DD} = 5V	+25℃		-18		
Off-Isolation	O_{ISO}	V_{BIAS} = V_{DD} / 2, V_S = 200mVpp, R_L = 50Ω, C_L = 12pF, f = 100kHz, Test Circuit 5	V_{DD} = 1.8V	+25℃		-100		dB
			V_{DD} = 2.5V	+25℃		-100		
			V_{DD} = 3.3V	+25℃		-100		
			V_{DD} = 5V	+25℃		-100		
		V_{BIAS} = V_{DD} / 2, V_S = 200mVpp, R_L = 50Ω, C_L = 12pF, f = 1MHz, Test Circuit 5	V_{DD} = 1.8V	+25℃		-80		dB
			V_{DD} = 2.5V	+25℃		-80		
			V_{DD} = 3.3V	+25℃		-80		
			V_{DD} = 5V	+25℃		-80		
Channel-to-Channel Crosstalk	X_{TALK}	V_{BIAS} = V_{DD} / 2, V_S = 200mVpp, R_L = 50Ω, C_L = 12pF, f = 100kHz, Test Circuit 6	V_{DD} = 1.8V	+25℃		-95		dB
			V_{DD} = 2.5V	+25℃		-95		
			V_{DD} = 3.3V	+25℃		-95		
			V_{DD} = 5V	+25℃		-95		
		V_{BIAS} = V_{DD} / 2, V_S = 200mVpp, R_L = 50Ω, C_L = 12pF, f = 1MHz, Test Circuit 6	V_{DD} = 1.8V	+25℃		-75		dB
			V_{DD} = 2.5V	+25℃		-75		
			V_{DD} = 3.3V	+25℃		-75		
			V_{DD} = 5V	+25℃		-75		
-3dB Bandwidth	BW	V_{BIAS} = V_{DD} / 2, V_S = 200mVpp, R_L = 50Ω, C_L = 12pF, Test Circuit 7	V_{DD} = 1.8V	+25℃		215		MHz
			V_{DD} = 2.5V	+25℃		200		
			V_{DD} = 3.3V	+25℃		190		
			V_{DD} = 5V	+25℃		190		

TIMING CHARACTERISTICS

(At specified V_{DD} ±10%, typical values measured at nominal V_{DD}, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Switching Characteristics								
Propagation Delay Time	t_{PD}	C_L = 50pF, Sx to D, D to Sx	V_{DD} = 1.8V	Full		25	35	ns
			V_{DD} = 2.5V	Full		13.5	25	
			V_{DD} = 3.3V	Full		9.5	20	
			V_{DD} = 5V	Full		6.5	17	
		C_L = 15pF, V_{DD} = 5V		Full		3.5	12	
Transition-Time between Inputs	t_{TRANS} (2)	R_L = 10kΩ, C_L = 50pF, Ax to D, Ax to Sx, Test Circuit 8	V_{DD} = 1.8V	Full		140	175	ns
			V_{DD} = 2.5V	Full		70	100	
			V_{DD} = 3.3V	Full		48	75	
			V_{DD} = 5V	Full		35	60	
		R_L = 10kΩ, C_L = 15pF, V_{DD} = 5V, Test Circuit 8		Full		32	55	
Turn-On Time from Enable	t_{ON_EN} (3)	R_L = 10kΩ, C_L = 50pF, $\overline{EN}$ to D, $\overline{EN}$ to Sx, Test Circuit 9	V_{DD} = 1.8V	Full		62	75	ns
			V_{DD} = 2.5V	Full		35	50	
			V_{DD} = 3.3V	Full		25	42	
			V_{DD} = 5V	Full		20	35	
		R_L = 10kΩ, C_L = 15pF, V_{DD} = 5V, Test Circuit 9		Full		20	48	
Turn-Off Time from Enable	t_{OFF_EN} (4)	R_L = 10kΩ, C_L = 50pF, $\overline{EN}$ to D, $\overline{EN}$ to Sx, Test Circuit 9	V_{DD} = 1.8V	Full		110	135	ns
			V_{DD} = 2.5V	Full		60	100	
			V_{DD} = 3.3V	Full		35	70	
			V_{DD} = 5V	Full		20	45	
		R_L = 10kΩ, C_L = 15pF, V_{DD} = 5V, Test Circuit 9		Full		15	40	
Break-Before-Make Delay Time	t_D	R_L = 10kΩ, C_L = 15pF, Sx to D, D to Sx, Test Circuit 10	V_{DD} = 1.8V	Full	2	48		ns
			V_{DD} = 2.5V	Full	0.5	19		
			V_{DD} = 3.3V	Full	0.5	14		
			V_{DD} = 5V	Full	0.5	10		

NOTES:

1. Specified by design and characterization, not production tested.
2. If the input logic signal's high level amplitude is V_{IH}(MIN) and low level amplitude is V_{IL}(MAX), the t_{TRANS} will be 1.5μs.
3. If the input logic signal's high level amplitude is V_{IH}(MIN) and low level amplitude is V_{IL}(MAX), the t_{ON_EN} will be 1.5μs.
4. If the input logic signal's high level amplitude is V_{IH}(MIN) and low level amplitude is V_{IL}(MAX), the t_{OFF_EN} will be 0.5μs.

INJECTION CURRENT COUPLING

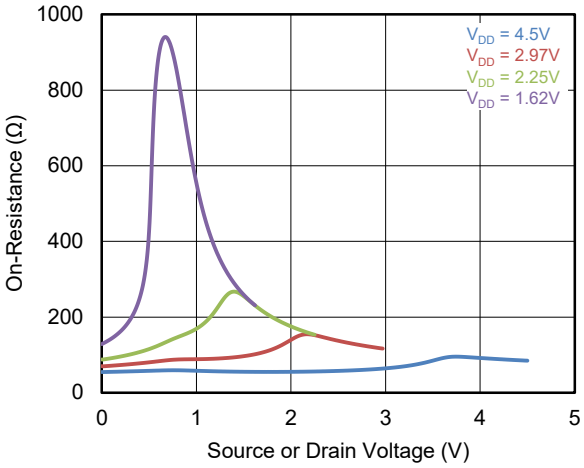
(At specified V_{DD} ±10%, typical values measured at nominal V_{DD} and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Injection Current Coupling, Test Circuit 11								
Maximum Shift of Output Voltage of Enabled Analog Input	ΔV_{OUT}	R_S ≤ 3.9kΩ, I_{INJ} ≤ 1mA	V_{DD} = 1.8V	Full		0.01	1	mV
			V_{DD} = 5V	Full		0.01	0.5	
		R_S ≤ 3.9kΩ, I_{INJ} ≤ 10mA	V_{DD} = 1.8V	Full		0.01	1	
			V_{DD} = 5V	Full		0.01	0.5	
		R_S ≤ 20kΩ, I_{INJ} ≤ 1mA	V_{DD} = 1.8V	Full		0.01	1	
			V_{DD} = 5V	Full		0.01	0.5	
		R_S ≤ 20kΩ, I_{INJ} ≤ 10mA	V_{DD} = 1.8V	Full		0.01	1	
			V_{DD} = 5V	Full		0.01	0.5	

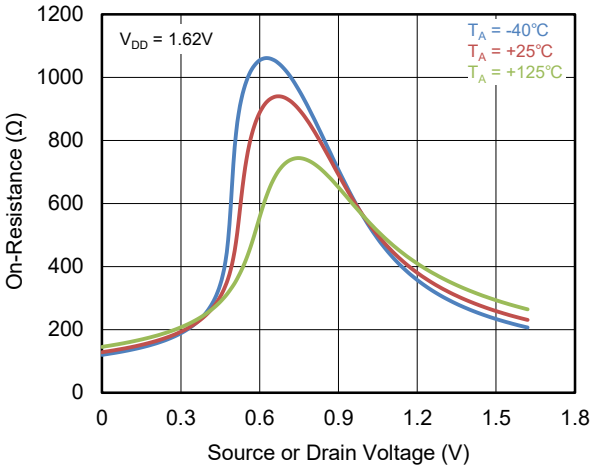
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

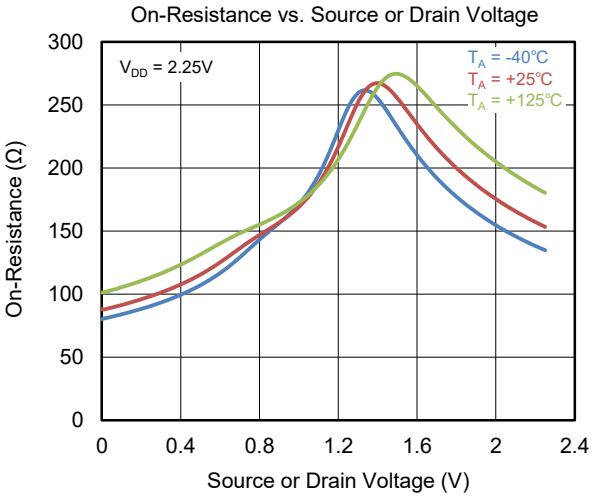
On-Resistance vs. Source or Drain Voltage



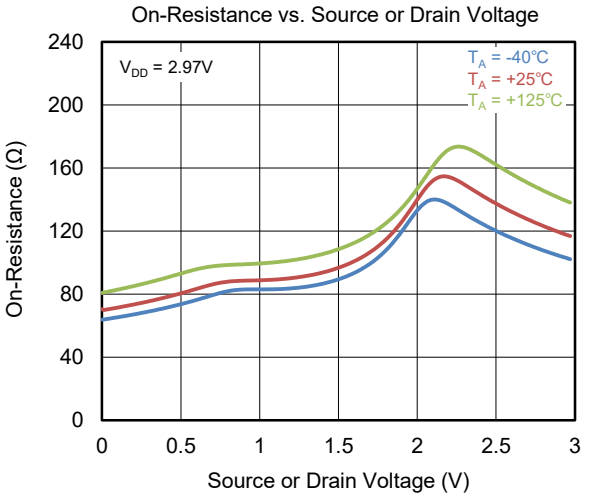
On-Resistance vs. Source or Drain Voltage



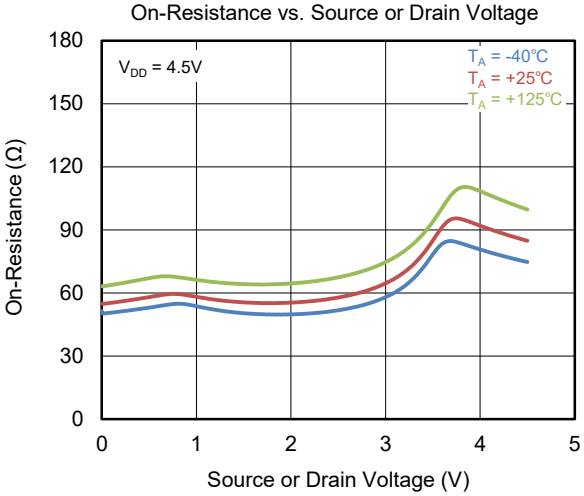
On-Resistance vs. Source or Drain Voltage



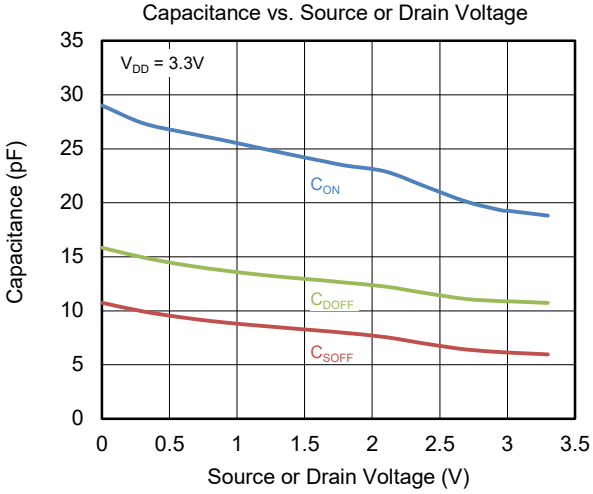
On-Resistance vs. Source or Drain Voltage



On-Resistance vs. Source or Drain Voltage



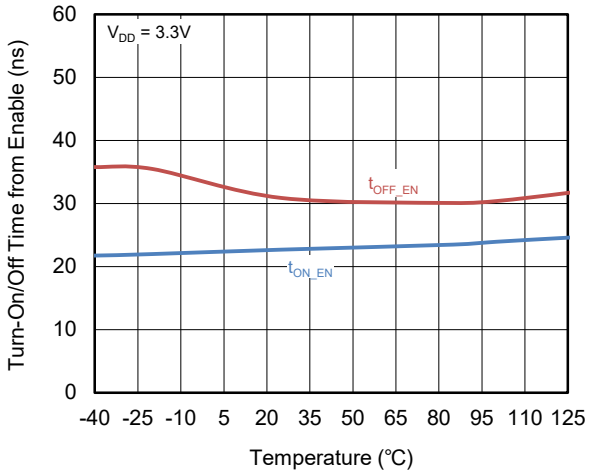
Capacitance vs. Source or Drain Voltage



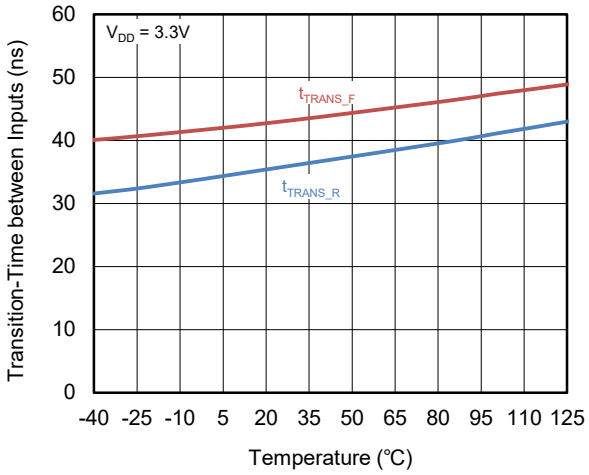
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

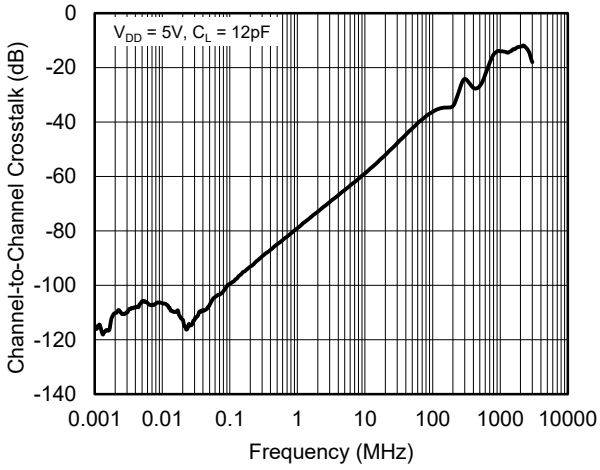
Turn-On/Off Time from Enable vs. Temperature



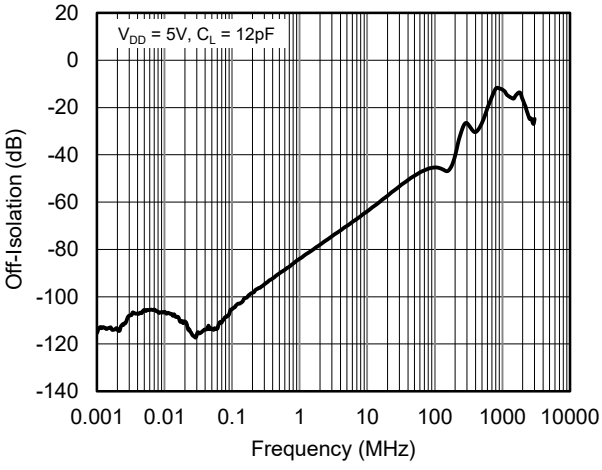
Transition-Time between Inputs vs. Temperature



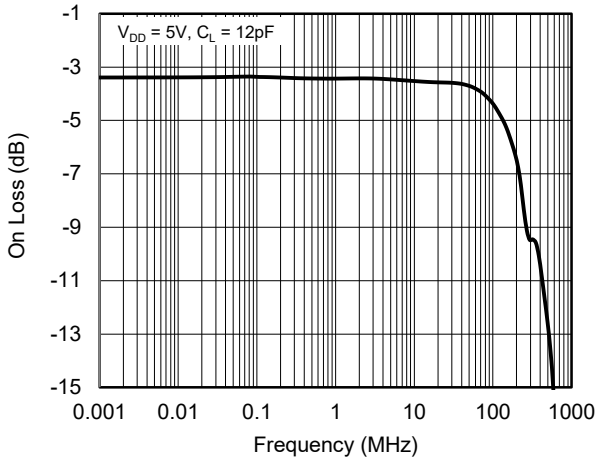
Channel-to-Channel Crosstalk vs. Frequency



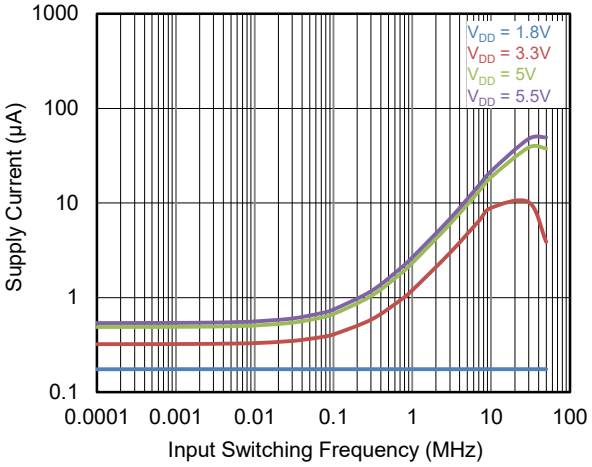
Off-Isolation vs. Frequency



On Loss vs. Frequency

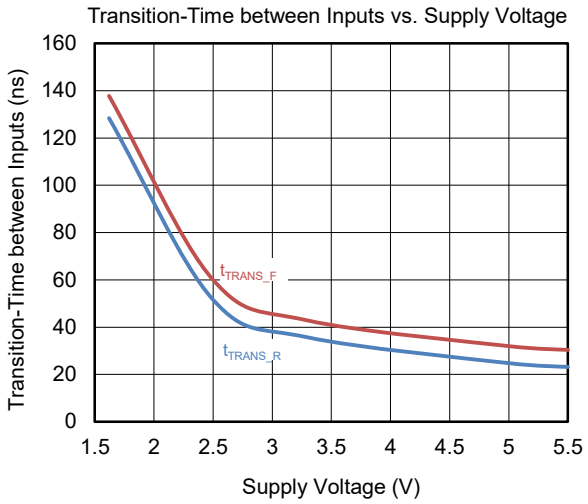


Supply Current vs. Input Switching Frequency

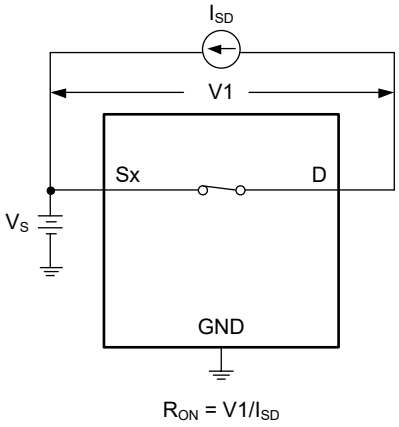


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

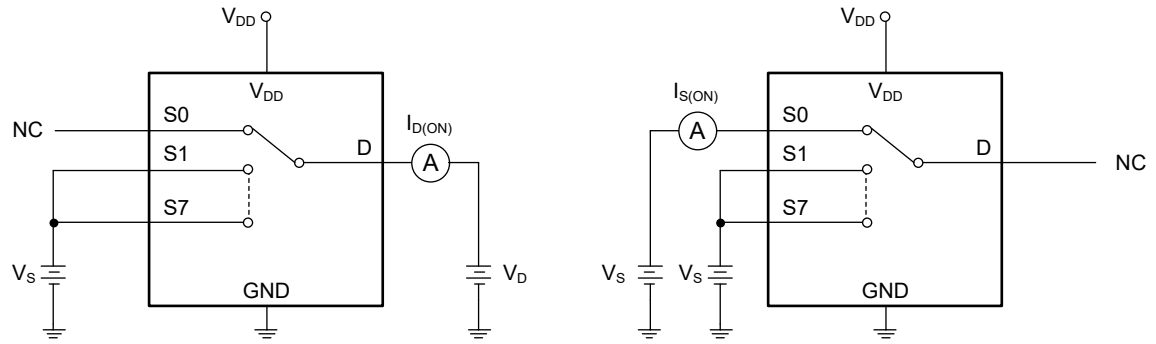
T_A = +25℃, unless otherwise noted.



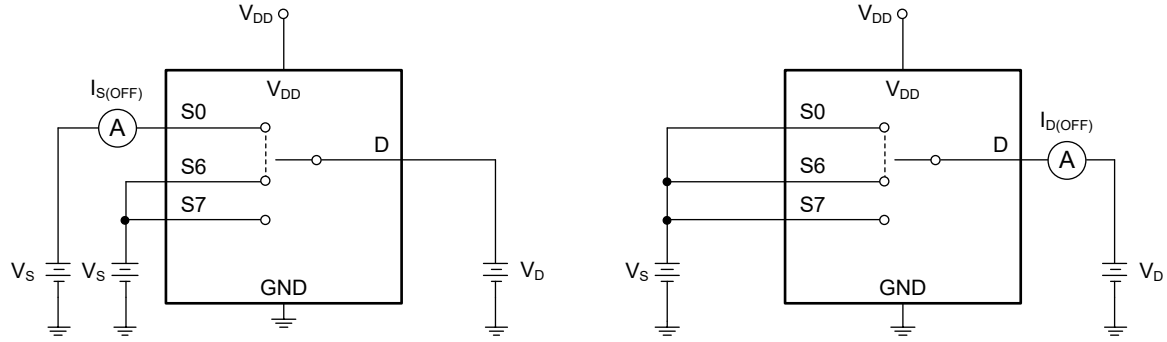
TEST CIRCUITS



Test Circuit 1. On-Resistance

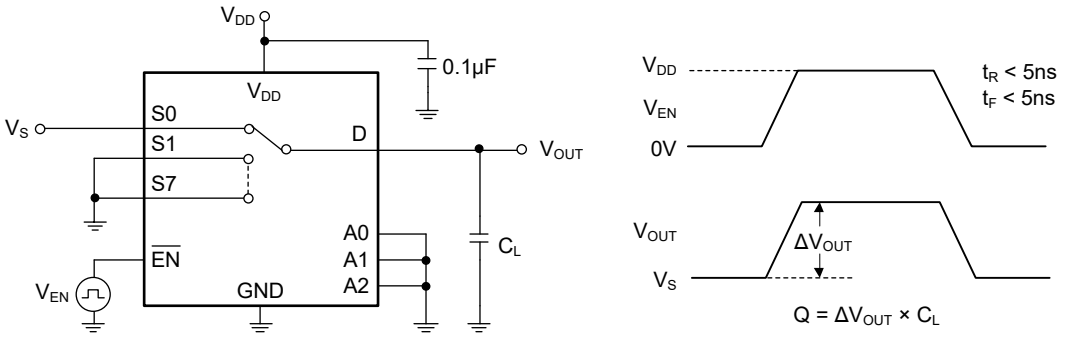


Test Circuit 2. On Leakage

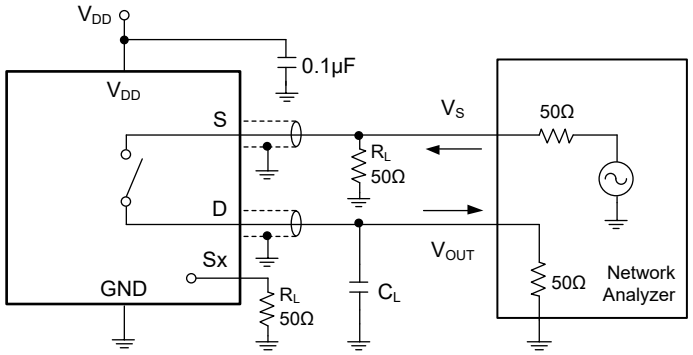


Test Circuit 3. Off Leakage

TEST CIRCUITS (continued)

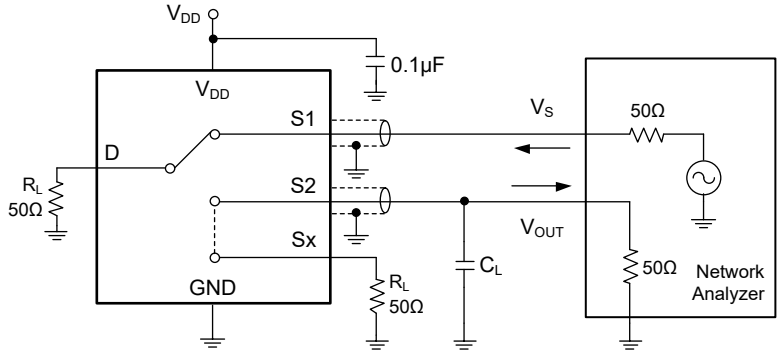


Test Circuit 4. Charge Injection (Q)



Off-Isolation = $20\log(V_{OUT}/V_S)$

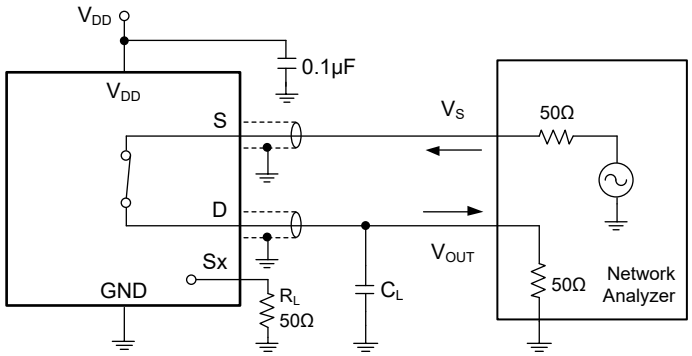
Test Circuit 5. Off-Isolation



Channel-to-Channel Crosstalk = $20\log(V_{OUT}/V_S)$

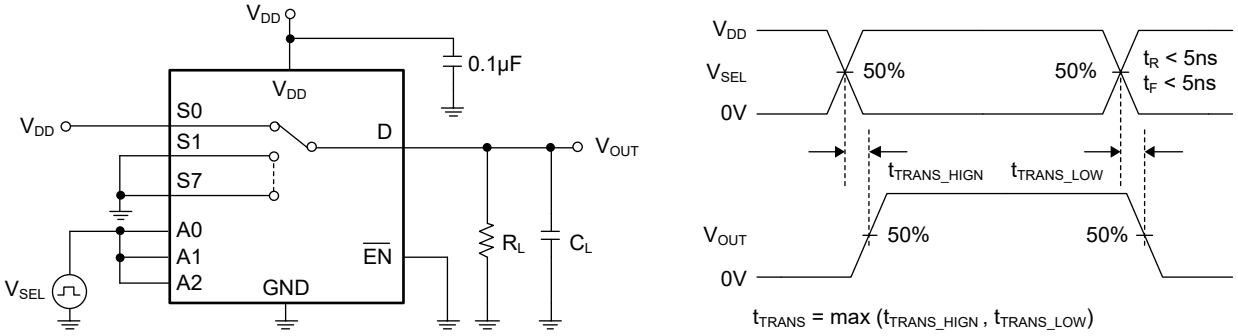
Test Circuit 6. Channel-to-Channel Crosstalk

TEST CIRCUITS (continued)



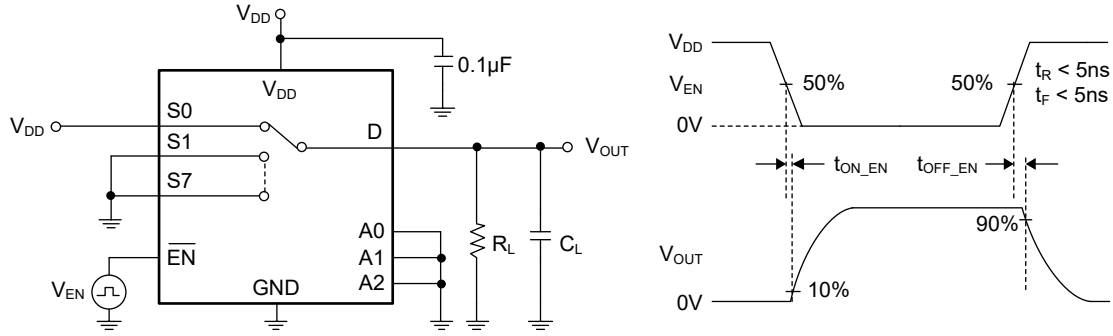
On Loss = $20\log(V_{OUT}/V_S)$

Test Circuit 7. On Loss



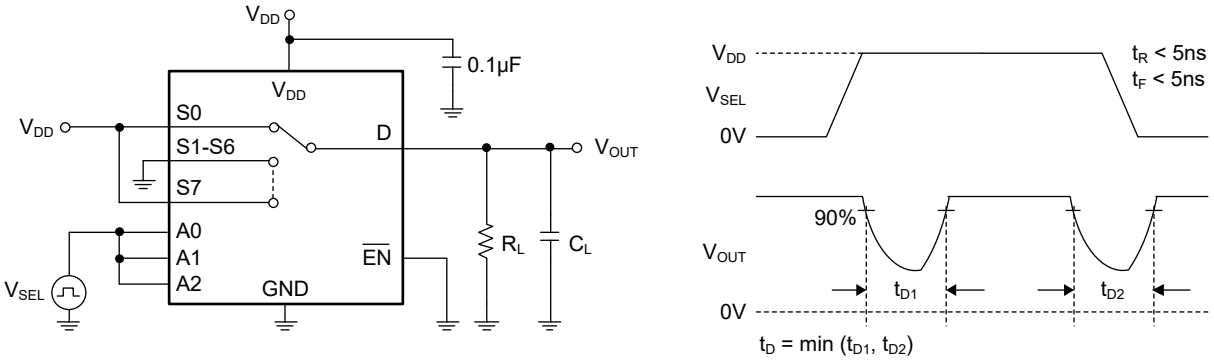
$t_{TRANS} = \max(t_{TRANS\_HIGN}, t_{TRANS\_LOW})$

Test Circuit 8. Transition Time (t_{TRANS})

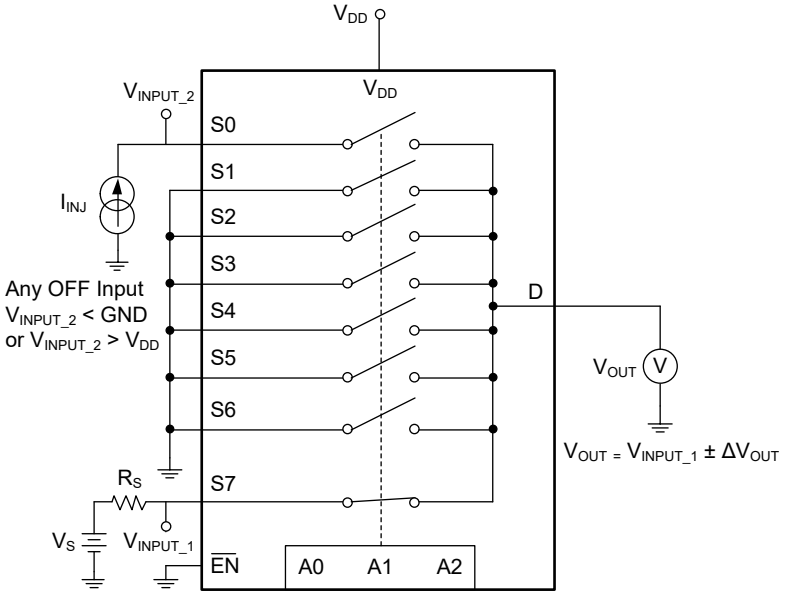


Test Circuit 9. Switching Times (t_{ON}, t_{OFF})

TEST CIRCUITS (continued)



Test Circuit 10. Break-Before-Make Delay Time (t_D)



Test Circuit 11. Injection Current

APPLICATION INFORMATION

The SGM4522Q is a single 8-channel CMOS analog multiplexer and all signal paths support rail-to-rail operation. All control input pins are also designed with fail-safe function and operate up to 5.5V withstand voltage regardless of the supply voltage. This function can prevent reverse current injection to V_{DD} pin from control pins even though the voltage of control pins already exceeds the V_{DD} pin. All signal ports of the SGM4522Q have injection current control circuit between signal inputs and V_{DD} or GND. It can prevent the signal path from back feeding, and also prevent GND pin from back leaking to signal inputs when the voltage of signal inputs is below the GND pin.

Based on the above special features, the SGM4522Q can be used to simplify circuit design and decrease overall system cost in automotive applications.

Logic Control

The logic control input pins include $\overline{EN}$, A0, A1, and A2. The logic input thresholds of the SGM4522Q are related to the power supply. The thresholds will increase as the power supply voltage increases. This feature allows the logic control inputs of the SGM4522Q to be connected to processors with lower logic I/O rails and no additional level shifters are required.

Fail-Safe Function

All control input pins ($\overline{EN}$, A0, A1 and A2) of the SGM4522Q are designed with fail-safe function and operate up to 5.5V withstand voltage regardless of the supply voltage. This special design eliminates the need for strict timing control for the SGM4522Q between the V_{DD} pin and control input pins. All control pins are allowed to be powered on earlier than the power supply and without damage. The fail-safe function reduces the complexity of system circuit design. For instance, when V_{DD} = 0V, the fail-safe function allows the control pins of the SGM4522Q to be connected to 5.5V. In this case, the switch is disabled because there is no power supply. Another application, when V_{DD} = 1.8V, the switch is enabled. The feature allows the control pins to be connected to interface with a logic level of another device up to 5.5V and without the need for additional level shifter.

Enable Control

The SGM4522Q has an enable control pin ($\overline{EN}$). When the $\overline{EN}$ pin is driven to high and power supply is normal, all the signal paths are disabled and the drain pin is open to any source pins. On the contrary, when the $\overline{EN}$ pin is driven to low, one of the signal paths is closed according to the logic of address pins (A0, A1 and A2).

Injection Current Control

Injection current is defined as the current flowing into the input pin when the input voltage is higher than power supply (V_{DD} + ΔV) or lower than ground (V_{SS}). Typical CMOS switches are designed with ESD diodes between the input pin and the V_{DD}/GND pin. These diodes will form a leakage path when the input voltage exceeds the power supply or below ground. This leakage may affect the reliability of the power system. Different applications determine that the injection current can come from different sources.

The current injected by switches or transient events is easy to occur in harsh environments of automotive systems or factory automation.

When the input signals are from various sensors or current sources, the injection current can also affect other self-contained systems.

Injected Current Impact to Typical CMOS Switches

The unexpected injected current may affect the common terminal voltage in application. Typical CMOS switches adopt a parallel structure of NMOS and PMOS and have designed with ESD diodes at the input as shown in Figure 2. These ESD diodes have the function of clamping input voltage. When current is injected into a disabled signal path and the forward diode voltage of the ESD diode (V_F) is higher than the PMOS threshold voltage (V_T), the PMOS in the circuit will be turned ON from OFF and form a leakage path between source and drain on disabled signal path. This situation causes the drain voltage to be changed by the source voltage in disabled signal path and it is not expected in applications. The simplified architecture of typical CMOS switch and the associated injected current path are shown in Figure 2.

APPLICATION INFORMATION (continued)

For typical CMOS switch structures, the injected current path is difficult to eliminate. In applications, the impact of injected current can be reduced by adding additional diodes with low forward voltage or resistors network externally at input pin. All signal terminals are not allowed to exceed the voltage of the ESD diode (V_T) higher than V_{DD}.

R_{ON} Changes Caused by Current Injection

On-resistance (R_{ON}) of typical CMOS switches is affected by the power supply voltage for enabled switch paths. Assuming the source pin voltage in disabled signal path is higher than the supply voltage by a forward diode voltage (V_F). This will cause an error (ΔV) at the drain pin. Figure 3 shows the injected current impact on R_{ON}. For example, when S2 is selected for conduction to D, there is an injection current at the disabled S1 pin and the voltage of S1 pin increases above V_{DD} to the ESD protection diode is forward biased, the V_{DD} voltage will be changed. Changes in supply voltage cause changes in on-resistance (R_{ON}) between S2 and D, thereby causing a ΔV error at the D pin. This unexpected error in the output can cause some trouble related to false trigger events, incorrect signal acquisition or abnormal signal detection, thus potentially compromising the accuracy and reliability of the system.

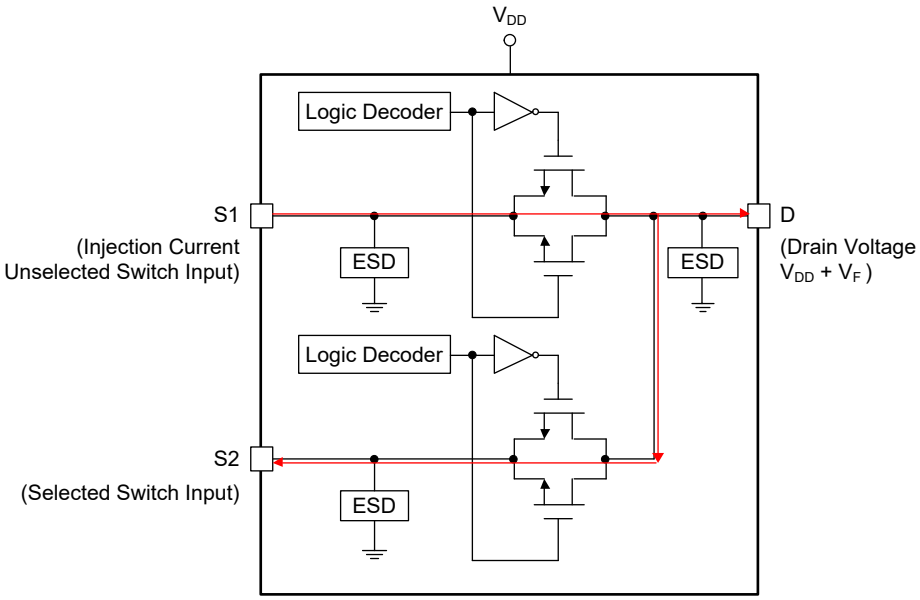


Figure 2. Typical CMOS Switch and Associated Injected Current Path

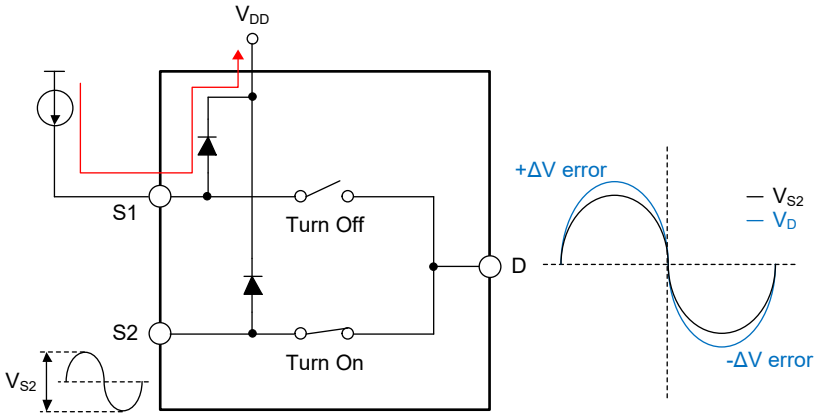


Figure 3. Injected Current Impact on R_{ON}

APPLICATION INFORMATION (continued)

To simplify circuit design and avoid adding additional protection in the system, the SGM4522Q is designed with an internal injection current control function. It allows signals on disabled signal channels to exceed the power supply voltage without affecting the enabled signal channel and typical CMOS switches do not have this feature. There is no need to add additional diodes and resistor networks to keep the input signals within the supply voltage in applications. In addition, there is no internal diode path from all pins except GND to the V_{DD} pin. This design eliminates the risk of damaging components connected to the supply pin or reverse current injection to the power supply. Figure 4 shows a design block diagram of injection current control circuit of the SGM4522Q.

Each source or drain pin (Sx, D) of the SGM4522Q has completely independent injection current control circuit. It includes a control circuit and a FET, which is enabled and shunts unexpected current from the inputs to GND once over-voltage or current injection at the inputs occurs. The prerequisite for enabling this current control circuit is that the input terminal (Sx, D) is disabled by the control pins and the injected current causes the voltage at the pin to be higher than V_{DD} or less than GND. Figure 5 shows injected current at input pin when over-voltage or current injection at the inputs occurs.

Each injection current circuit can handle a maximum rated current of 50mA and the SGM4522Q can accept a maximum injection current of 100mA at any time. Assuming multiple source terminals are injected at the same time, the SGM4522Q can only accept a total current of 100mA. If the current injected exceeds 100mA, the SGM4522Q is at risk of damage. So a series current limiting resistor may be required and must be sized appropriately based on the system application. Figure 6 shows an application circuit of using a series current limiting resistors when over-voltage event occurs.

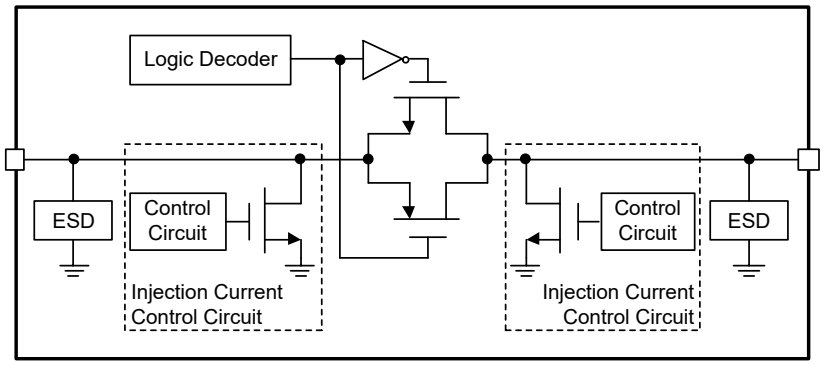


Figure 4. Design Block Diagram of Injection Current Control

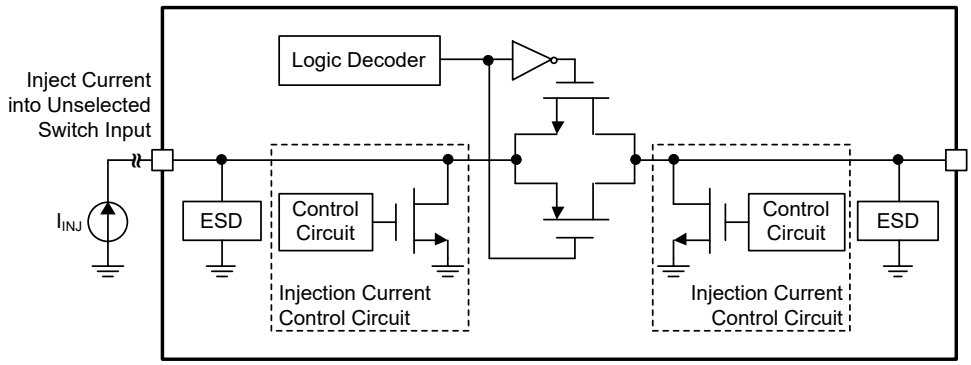


Figure 5. Injected Current at Input Pin

APPLICATION INFORMATION (continued)

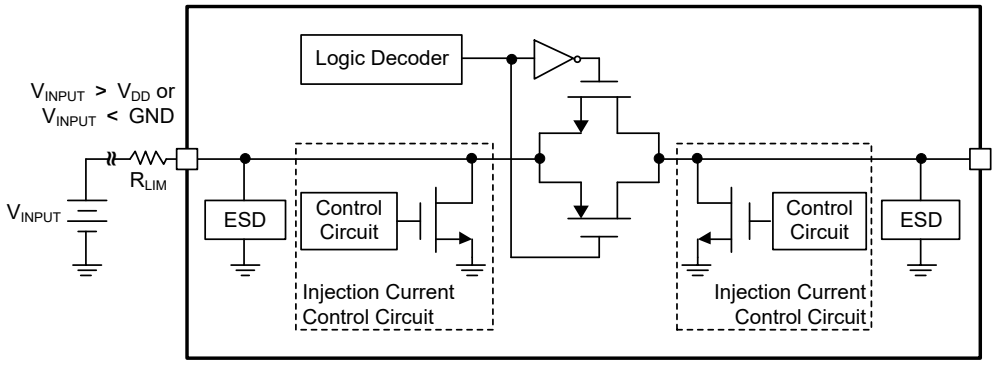


Figure 6. Over-Voltage Event with Series Resistor

Once the voltage at the source or drain pins exceeds V_{DD} or falls below GND, the FET is enabled for any disabled signal path and shunts unexpected current from the inputs to GND. In this scene, a series of resistors is required to limit the total current injected into the input to within 100mA. An example is as follow:

SGM4522Q is Powered and the Input Signal is Higher than V_{DD} (V_{DD} = 5V, V_{INPUT} = 5.5V)

For the typical CMOS switch with an internal ESD diode, when the input signal exceeds the V_{DD} pin, the internal ESD diode will be forward biased and the current injected into the power supply from the input. In this case, if the inputs have no additional protective devices, the power supply system may be at risk of damage. Even though the use of limiting resistors can reduce the risk to a certain extent, this risk cannot be completely eliminated due to the architecture of the typical CMOS switch. When the input voltage is too high and exceeds V_{DD}, the application circuit still requires a series of limiting resistors, because the injected current control circuit of the SGM4522Q can only handle injection current less than 100mA. The current path of the SGM4522Q is from inputs to GND and does not have the same problems as the current injected into the power rail.

In addition, the injection current control circuit of the SGM4522Q can work well in both unselected and selected paths. It should be noted when the injection current occurs in the selected path, the injection current will also flow through the source to drain path not just flow into ground.

Power Supply and Decoupling

Power supply range of the V_{DD} pin is from 1.62V to 5.5V. Besides, the V_{DD} pin is not allowed to exceed the maximum absolute withstand voltage because over-voltage will cause damage to the SGM4522Q.

In general, the V_{DD} pin should be installed with a 0.1μF to 10μF ceramic capacitor to prevent power disturbance from other power supply components and the bypass capacitor should be placed as close as possible to the V_{DD} pin for the best power supply decoupling. Multiple capacitors with different capacitance values can also be placed to reject noise of different frequencies in applications with high requirements for noise. One end of this decoupling capacitor should be directly connected to the GND pin of the SGM4522Q as short as possible in PCB layout design.

REVISION HISTORY

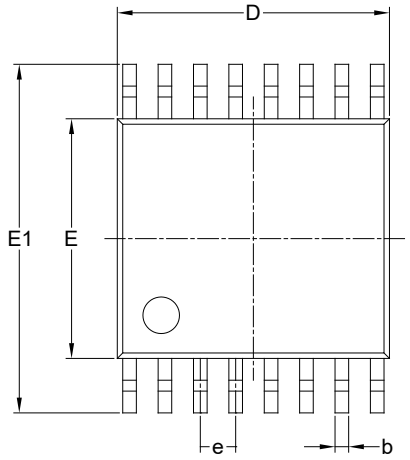
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

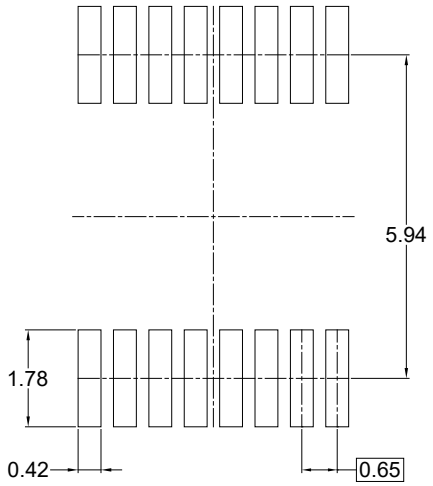
OCTOBER 2025 – REV.A to REV.A.1	Page
Updated Absolute Maximum Ratings section	3
Updated Electrical Characteristics section	6
Updated Test Circuits section	15

Changes from Original (JULY 2024) to REV.A	Page
Changed from product preview to production data	All

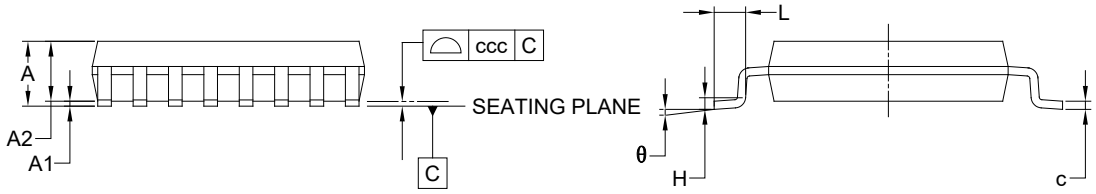
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

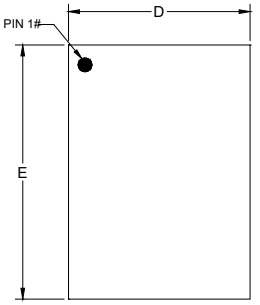


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

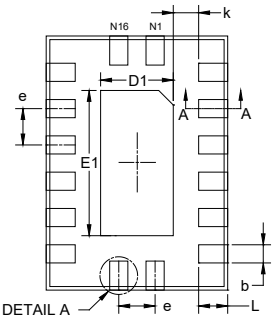
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

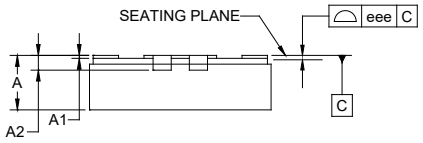
TQFN-2.5×3.5-16AL



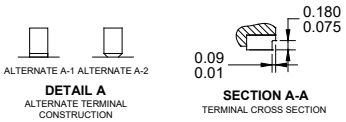
TOP VIEW

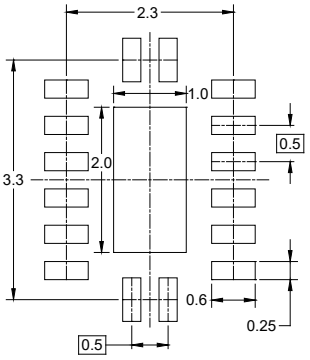


BOTTOM VIEW



SIDE VIEW





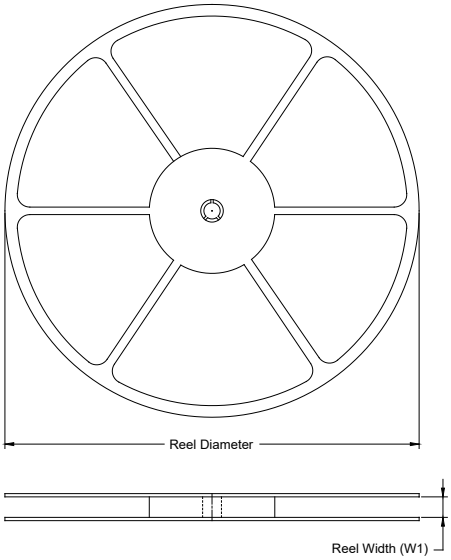
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	2.400	-	2.600
D1	0.900	-	1.100
E	3.400	-	3.600
E1	1.900	-	2.100
e	0.500 BSC		
k	0.350 REF		
L	0.300	-	0.500
eee	0.080		

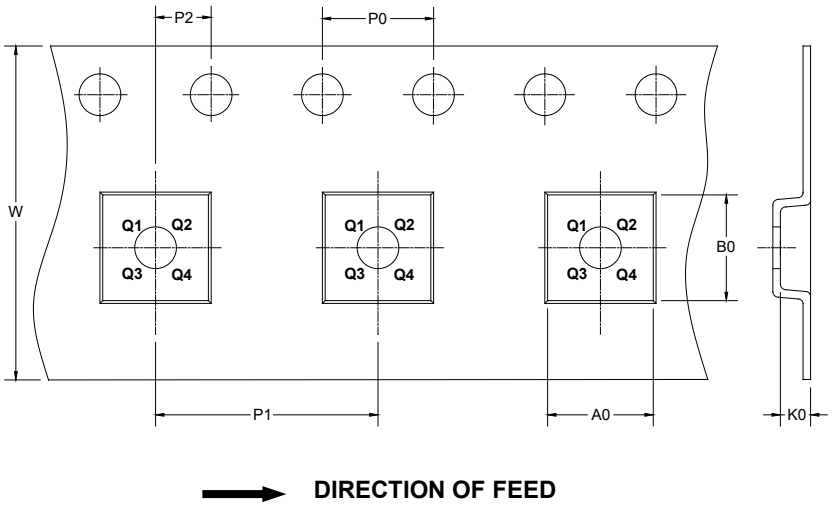
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



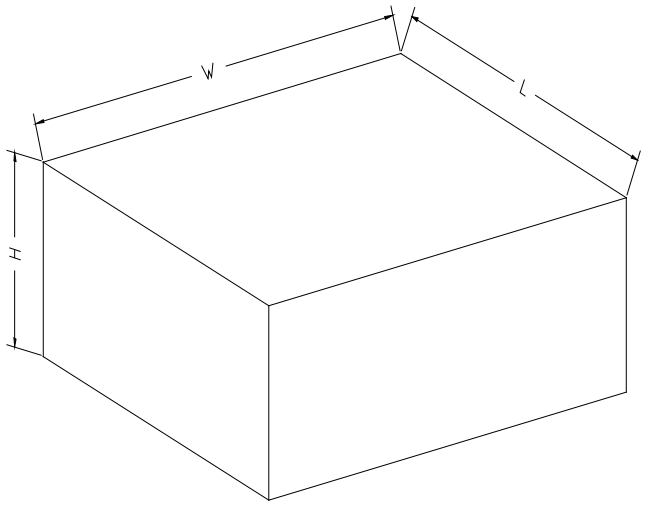
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-2.5×3.5-16AL	13"	12.4	2.80	3.80	1.13	4.0	4.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002