SGM2092
500mA, Fast Transient Response, Low Voltage, Low Noise and Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2092 is a CMOS, fast transient response, low voltage and low dropout voltage linear regulator. It is capable of supplying 500mA output current with typical dropout voltage of only 35mV. The output voltage range is from 0.6V to 5.0V.

Other features include logic-controlled shutdown mode, current limit and thermal shutdown protection. The SGM2092 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2092 is suitable for applications which need low noise and fast transient response power supply, such as power supply of camera module in smart phone, etc.

The SGM2092 is available in a Green WLCSP-1.2×0.8-6B package. It operates over an operating temperature range of -40℃ to +125℃.

FEATURES

- **Operating Input Voltage Range: 1.5V to 5.5V**
- **Enable Pin Accept Voltages Higher than the Supply Voltage and up to 5.5V**
- **Adjustable Output from 0.6V to 5.0V**
- **500mA Output Current**
- **Output Voltage Accuracy: ±1% at +25℃**
- **Quiescent Current: 85μA (TYP)**
- **Low Dropout Voltage: 35mV (TYP) at 500mA, $V_{OUT(NOM)}$ = 5.0V**
- **Low Noise: 15μV_{RMS} (TYP)**
- **Current Limit and Thermal Protection**
- **Excellent Load and Line Transient Responses**
- **UVLO with Hysteresis**
- **With Output Automatic Discharge**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green WLCSP-1.2×0.8-6B Package**

APPLICATIONS

Portable Equipment
Industrial and Medical Equipment

TYPICAL APPLICATION CIRCUIT

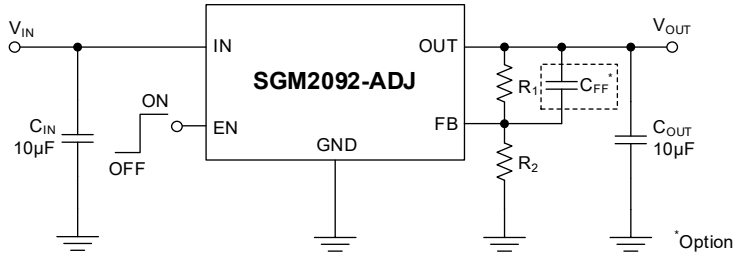


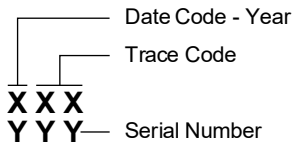
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2092-ADJ	WLCSP-1.2×0.8-6B	-40℃ to +125℃	SGM2092-ADJXG/TR	XXX 1O0	Tape and Reel, 10000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN to GND ..... -0.3V to 6V
OUT, FB to GND ..... -0.3V to (V_{IN} + 0.3V)
EN to GND ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.2×0.8-6B, θ_{JA} ..... 150.9℃/W
WLCSP-1.2×0.8-6B, θ_{JB} ..... 50.9℃/W
WLCSP-1.2×0.8-6B, θ_{JC} ..... 57.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±8000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 1.5V to 5.5V
Enable Input Voltage Range ..... 0V to 5.5V
Input Effective Capacitance, C_{IN} ..... 2μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 2μF to 220μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

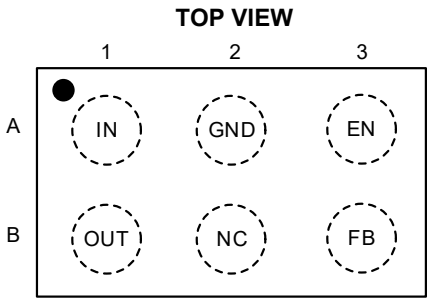
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



WLCSP-1.2×0.8-6B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	IN	Input Supply Voltage Pin. It is recommended to use a 4.7μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
A2	GND	Ground.
A3	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
B1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 2μF to 220μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
B2	NC	No Connection.
B3	FB	Feedback Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.

FUNCTIONAL BLOCK DIAGRAM

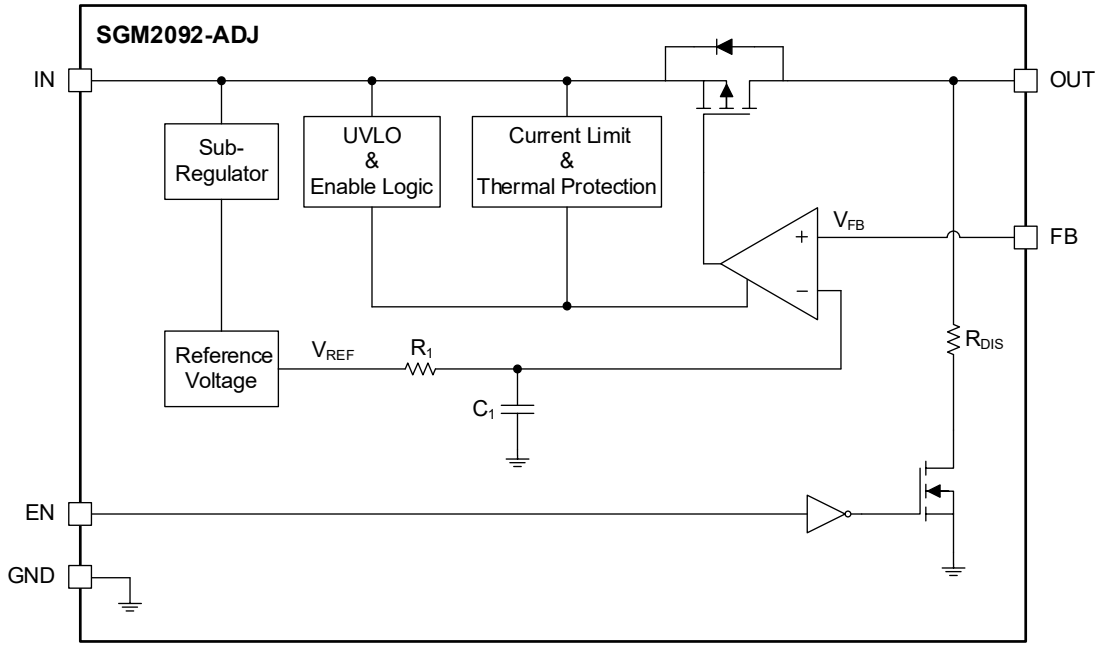


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

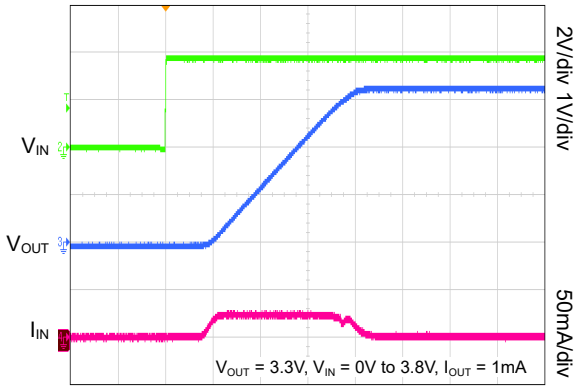
(V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 1.5V (whichever is greater), C_{IN} = 10μF, C_{OUT} = 10μF, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{IN}			1.5		5.5	V
Output Voltage Range	V_{OUT}			0.6		5.0	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V, I_{OUT} = 10mA	T_J = +25℃	-1		+1	%
			T_J = -40℃ to +125℃	-1.5		+1.5	
Reference Voltage	V_{FB}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V, I_{OUT} = 10mA	T_J = +25℃	0.594	0.6	0.606	V
			T_J = -40℃ to +125℃	0.591	0.6	0.609	
FB Pin Input Current	I_{FB}	V_{FB} = 0.7V			1	100	nA
Under-Voltage Lockout	V_{UVLO}	V_{IN} rising			1.3	1.5	V
		V_{IN} falling		1.2	1.28		
Line Regulation	ΔV_{OUT_LNR}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V, I_{OUT} = 0.1mA			1.3	8	mV
Load Regulation	ΔV_{OUT_LDR}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2V (whichever is greater), I_{OUT} = 0.1mA to 500mA			1.2	12	mV
Dropout Voltage	V_{DROP}	I_{OUT} = 500mA, when V_{OUT} falls to 95% × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 5.0V			35	80	mV
Output Current Limit	I_{LIMIT}	V_{IN} = V_{OUT} + 1.6V, V_{OUT} = 90% × $V_{OUT(NOM)}$		0.55	1.1		A
Output Short-Circuit Current	I_{SHORT}	V_{IN} = $V_{OUT(NOM)}$ + 2V, V_{OUT} = 0V			300		mA
Quiescent Current	I_Q	I_{OUT} = 0mA			85	350	μA
Ground Pin Current	I_{GND}	I_{OUT} = 500mA			620		μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V			0.25	2.5	μA
Enable Threshold Voltage	V_{IH}	EN input voltage high		1.0		5.5	V
	V_{IL}	EN input voltage low		0		0.4	
Enable Input Current	I_{EN}	V_{EN} = 0V, V_{IN} = 5.5V			5	500	nA
		V_{EN} = 5.5V, V_{IN} = 5.5V			5	1000	nA
Output Discharge Resistance	R_{DIS}	V_{EN} = 0V, V_{IN} = 5.5V			95		Ω
Start-Up Time	t_{STR}	From assertion of V_{EN} to V_{OUT} = 90% × $V_{OUT(NOM)}$			2		ms
Power Supply Rejection Ratio	PSRR	V_{OUT} = 0.6V, V_{IN} = 1.5V, Ripple 0.2V_{P-P}, I_{OUT} = 50mA, C_{OUT} = 2.2μF	f = 1kHz		50		dB
			f = 100kHz		37		
			f = 1MHz		32		
		V_{OUT} = 3.3V, V_{IN} = 3.8V, Ripple 0.2V_{P-P}, I_{OUT} = 50mA, C_{OUT} = 2.2μF	f = 1kHz		61		
			f = 100kHz		41		
			f = 1MHz		36		
Output Voltage Noise	e_n	V_{OUT} = 0.6V, V_{IN} = 1.5V, C_{OUT} = 2.2μF, f = 10Hz to 100kHz	I_{OUT} = 1mA		21		μV_{RMS}
			I_{OUT} = 500mA		15		
		V_{OUT} = 3.3V, V_{IN} = 3.8V, C_{OUT} = 2.2μF, f = 10Hz to 100kHz	I_{OUT} = 1mA		55		
			I_{OUT} = 500mA		52		
Thermal Shutdown Temperature	T_{SHDN}	T_J rising			160		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}	Hysteresis			15		℃

TYPICAL PERFORMANCE CHARACTERISTICS

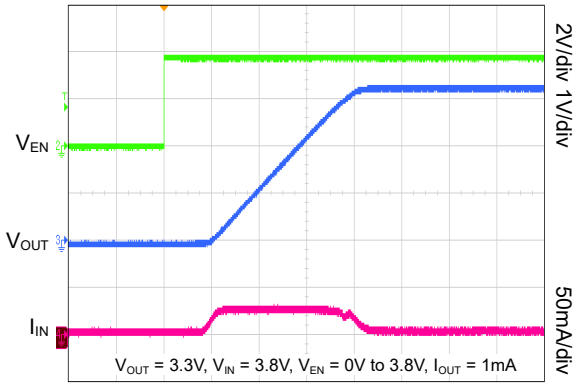
T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 1.5V (whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

V_{IN} Power-On Time



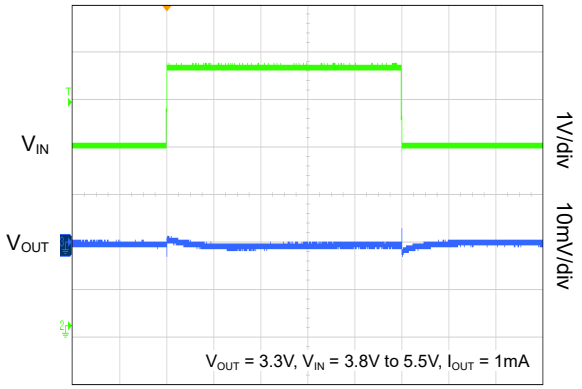
Time (500μs/div)

Enable Turn-On Response



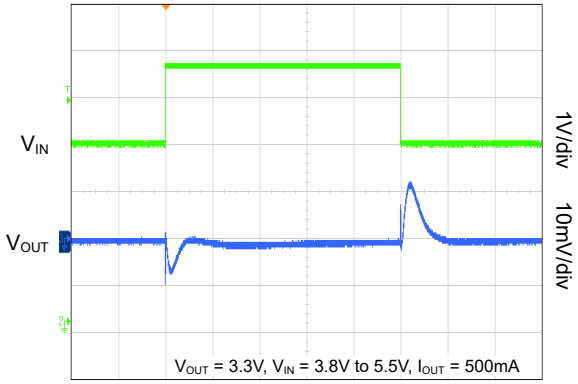
Time (500μs/div)

Line Transient Response



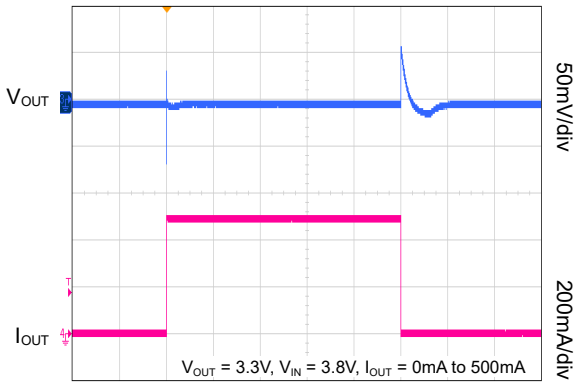
Time (10ms/div)

Line Transient Response



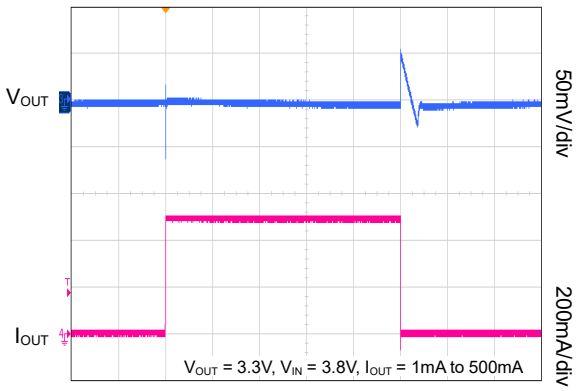
Time (100ms/div)

Load Transient Response



Time (100ms/div)

Load Transient Response

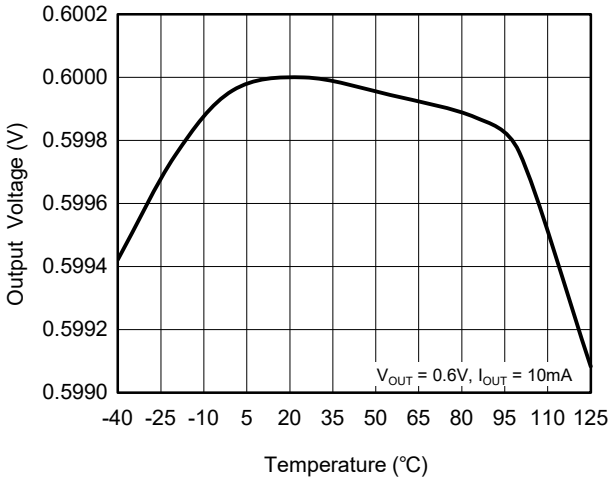


Time (2ms/div)

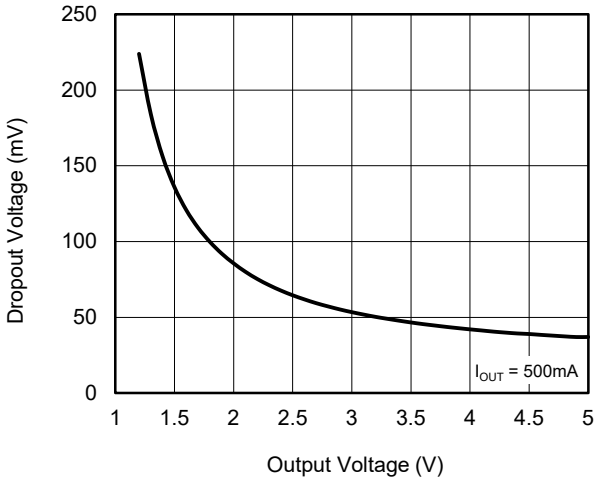
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 1.5V (whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

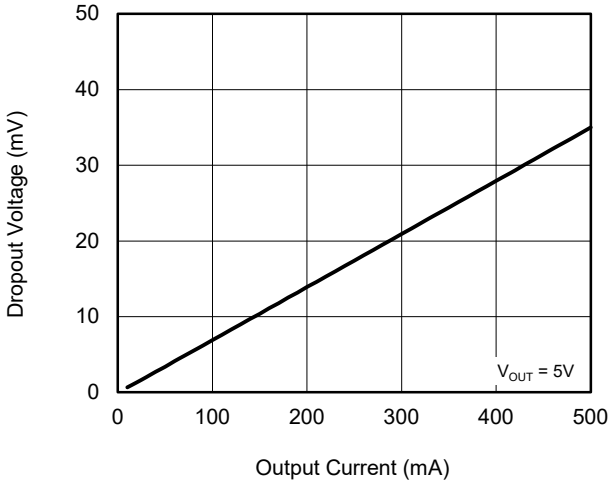
Output Voltage vs. Temperature



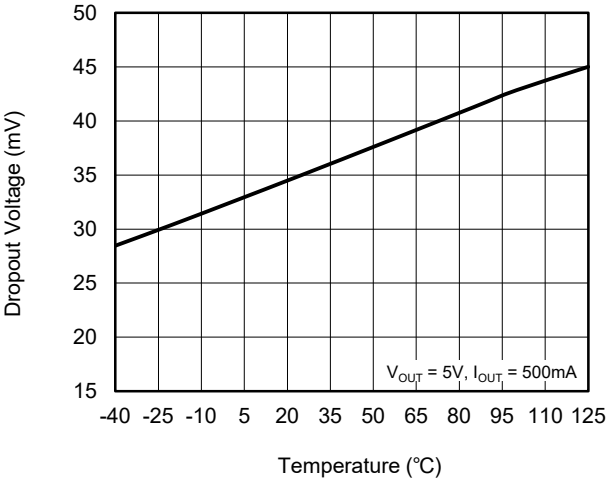
Dropout Voltage vs. Output Voltage



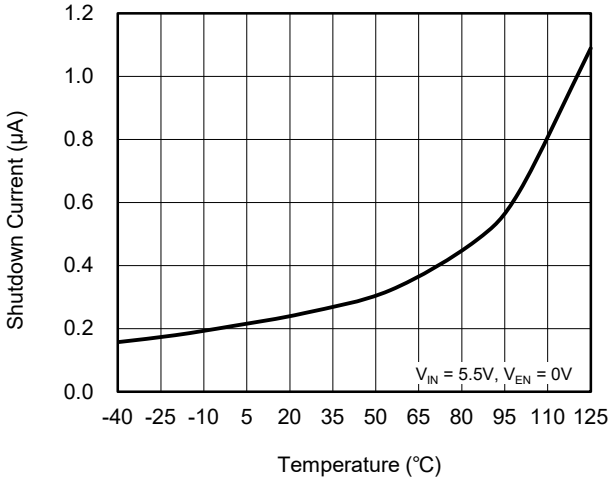
Dropout Voltage vs. Output Current



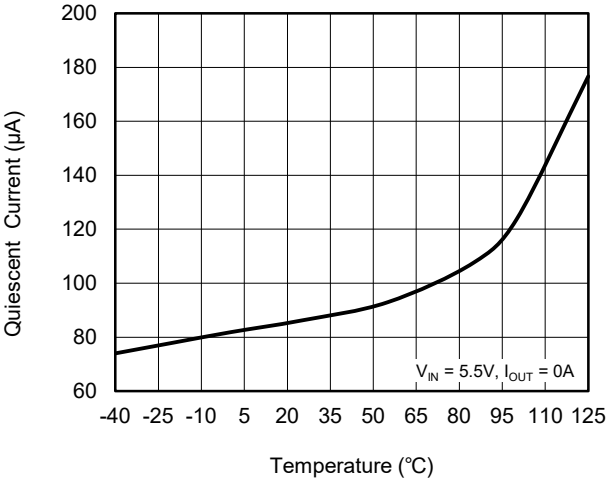
Dropout Voltage vs. Temperature



Shutdown Current vs. Temperature



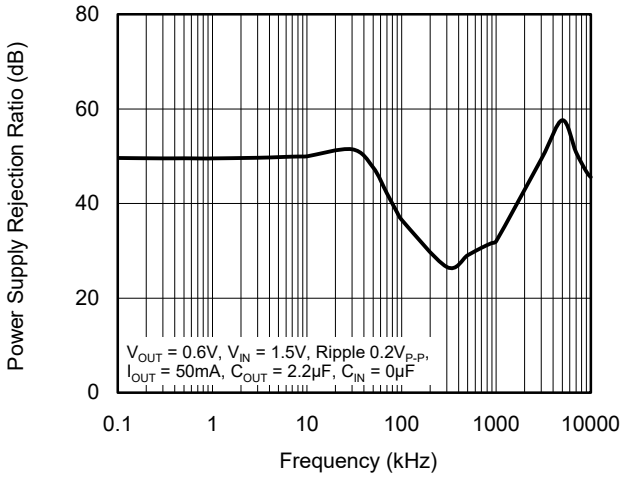
Quiescent Current vs. Temperature



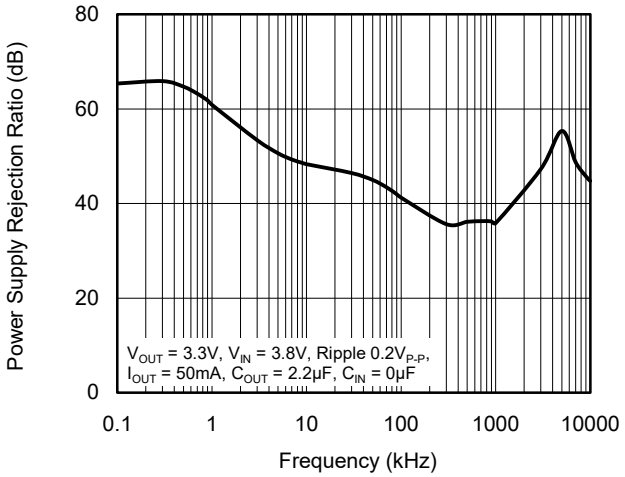
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 1.5V (whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

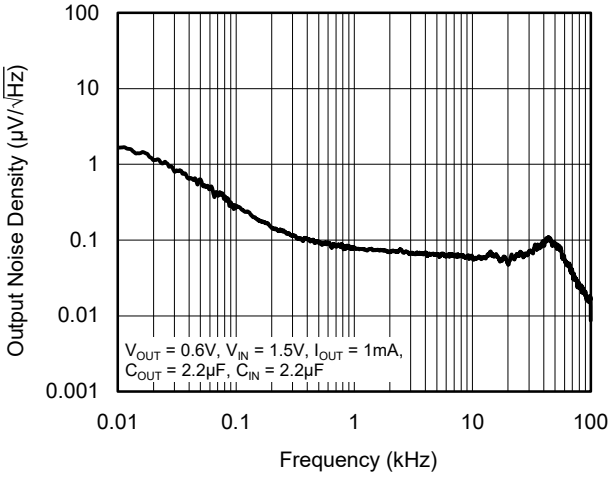
Power Supply Rejection Ratio vs. Frequency



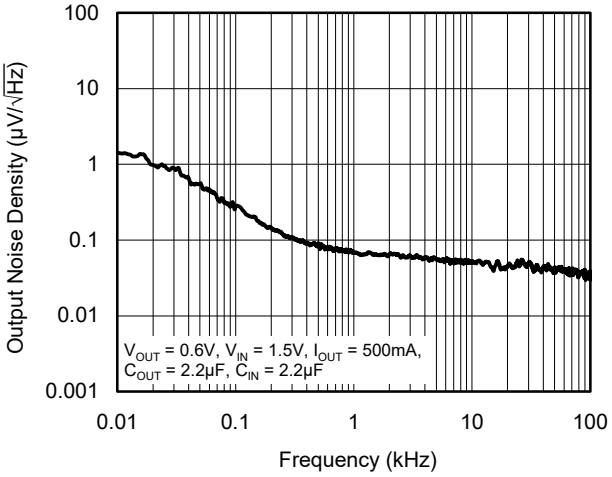
Power Supply Rejection Ratio vs. Frequency



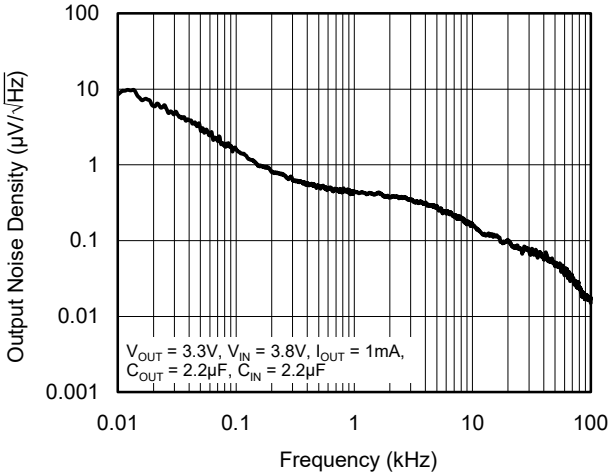
Output Noise Density vs. Frequency



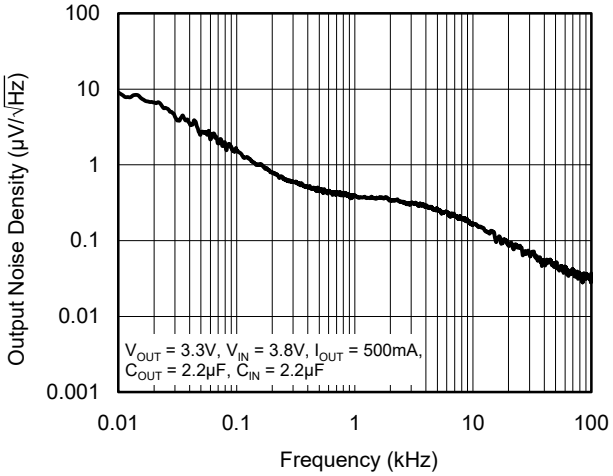
Output Noise Density vs. Frequency



Output Noise Density vs. Frequency



Output Noise Density vs. Frequency



APPLICATION INFORMATION

The SGM2092 is a low noise and low dropout LDO and provides 500mA output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2092 useful in a variety of applications. The SGM2092 provides protection functions for output overload, output short-circuit condition and overheating.

The SGM2092 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 0.25μA (TYP).

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 4.7μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

One or more output capacitors are required to maintain the stability of the LDO, and the output capacitors should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R and X5R ceramic capacitors as output capacitors. Ceramic capacitors have low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitors is affected by temperature, DC bias and package size.

For example, Figure 3 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10μF±10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

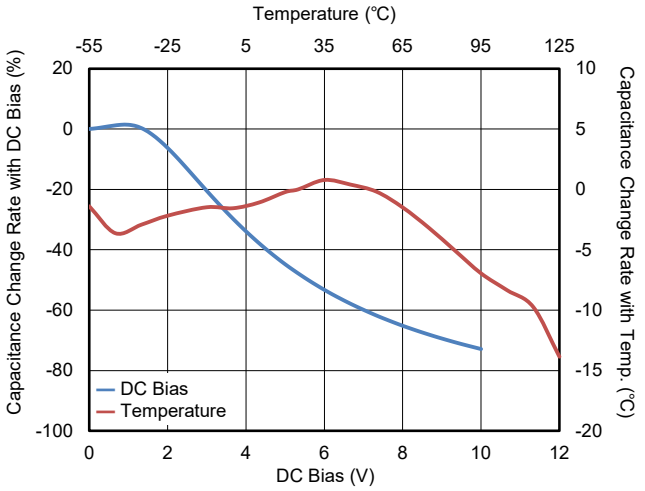


Figure 3. Capacitance vs. DC Bias and Temperature Characteristics

The SGM2092 requires a minimum effective capacitance of 4.7μF for C_{OUT} to ensure stability. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Adjustable Regulator

The output voltage of the SGM2092-ADJ can be adjusted from 0.6V to 5.0V. The FB pin will be connected to two external resistors as shown in Figure 4. The output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

V_{OUT} is output voltage and V_{FB} is the internal voltage reference, V_{FB} = 0.6V.

One parallel capacitor (C_{FF}) with R_1 can be used to improve the PSRR, increase the transient response and reduce the output noise. The resistance range of R_2 is recommended to be between 5kΩ and 130kΩ.

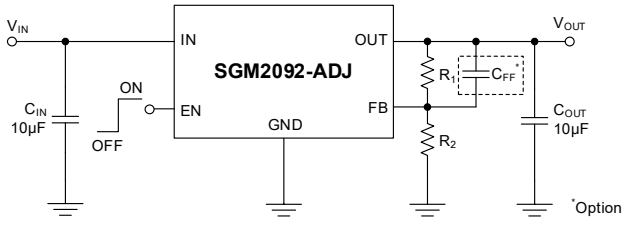


Figure 4. Adjustable Output Voltage Application

APPLICATION INFORMATION (continued)

Enable Operation

The SGM2092 uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.4V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 95Ω (TYP) resistor.

When the EN pin voltage is higher than 1.0V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the IN pin and attempts to disable the output of the device if any of these rails collapses. The local input capacitance prevents severe brownouts in most applications.

Output Current Limit Protection

When overload events happen, the output current is internally limited to 1.1A (TYP). When the OUT pin is shorted to ground, the output current is internally limited to 300mA (TYP).

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2092 will be in shutdown state and it will remain in this state until the die temperature decreases to +145℃.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2092 can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2092 is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (2)$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN pin and OUT pin separately.

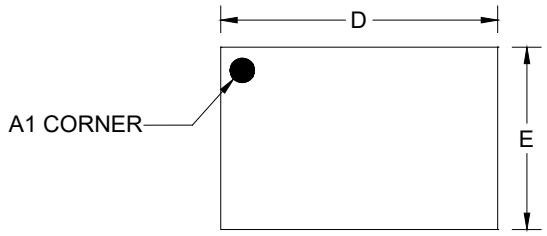
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

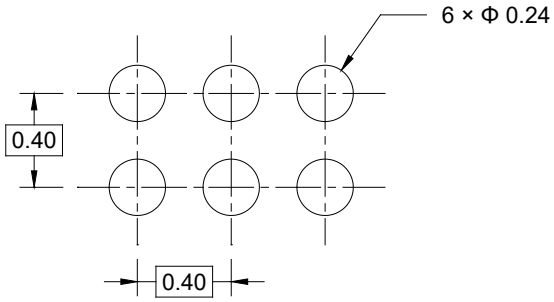
Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

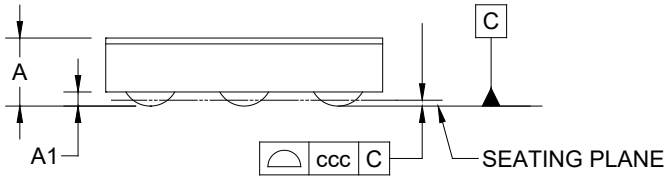
WLCSP-1.2×0.8-6B



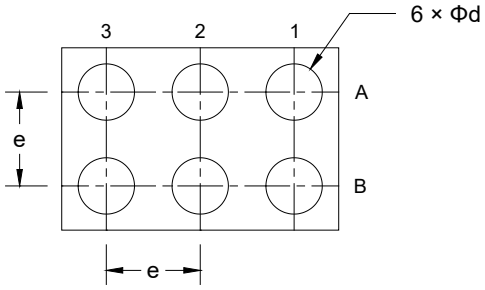
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



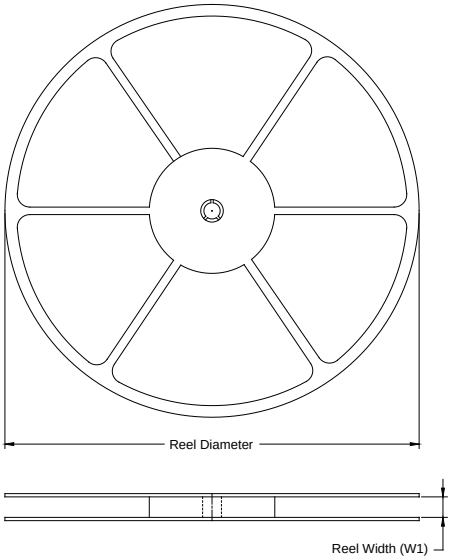
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.318
A1	0.050	-	0.070
D	1.150	-	1.210
E	0.747	-	0.807
d	0.210	-	0.270
e	0.400 BSC		
ccc	0.050		

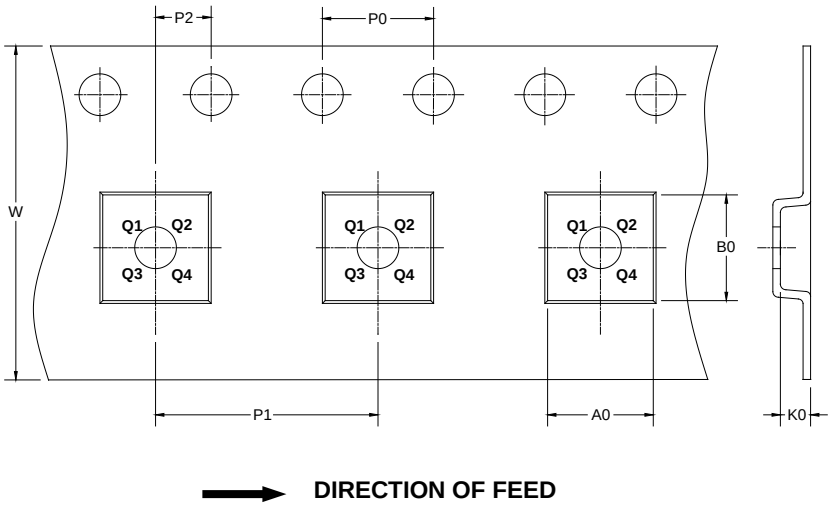
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



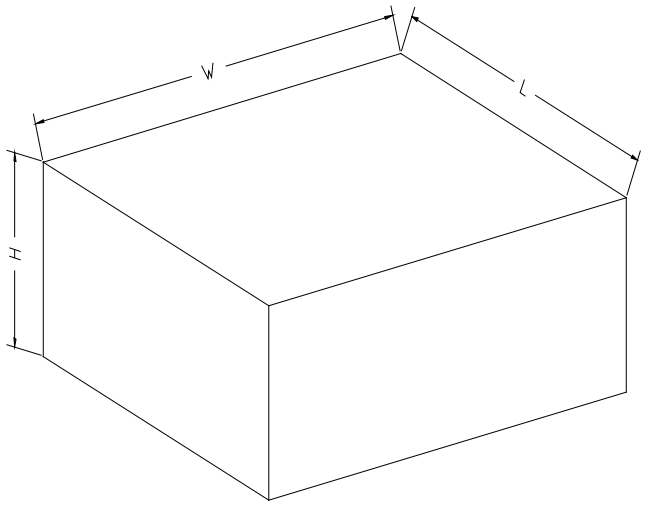
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.2×0.8-6B	7"	9.5	0.87	1.30	0.38	4.0	2.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002