TD25C320/TD25C160/TD25C080
32-Kbit, 16-Kbit and 8-Kbit SPI Serial EEPROM

GENERAL DESCRIPTION

The TD25C320/160/080 is a serial EEPROM device accessed through the SPI bus. The device is designed to operate in a supply voltage range of 1.7V to 5.5V, with a maximum of 20MHz transfer rate. The operating temperature range is from -40℃ to +105℃.

The serial EEPROM memory is organized as 128/64/32 pages of 32 bytes each, totaling 4096/2048/1024 × 8 bits. The device offers an additional 32-byte Identification Page for users to store sensitive application parameters. This page can be permanently locked in Read-only mode after the application data is written into the Identification Page. The device also offers a separate memory block containing a factory programmed 128-bit Unique ID. This block is in Read-only mode and can be accessed by sending a specific Read command.

The TD25C320/160/080 is available in Green SOIC-8, TSSOP-8 and UTDFN-2×3-8AL packages.

FEATURES

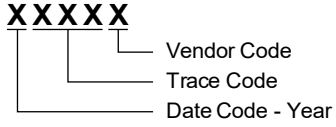
- **Serial Peripheral Interface (SPI) Compatible**
  - **SPI Modes 0 (0, 0) and 3 (1, 1) Supported**
- **Supply Voltage Range: 1.7V to 5.5V**
- **High Speed Clock: 20MHz**
- **Byte and Page (up to 32 Bytes) Write Mode**
- **Self-timed Write Cycle (3ms MAX)**
- **Block Write Protection**
  - **Quarter, Half or Whole Memory Array**
- **Additional 32-byte Write Lockable Page and 128-bit Unique ID**
- **High Reliability**
  - **Endurance: 1,000,000 Write Cycles at T_A = +25℃**
  - **Data Retention: 100 Years at T_A = +25℃**
  - **ESD Protection (HBM): ±4000V**
- **Operating Temperature Range: -40℃ to +105℃**
- **RoHS Compliant and Halogen Free**
- **Available in Green SOIC-8, TSSOP-8 and UTDFN-2×3-8AL Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TD25C080	SOIC-8	-40℃ to +105℃	TD25C080GS8G/TR	TD 25C080GS8 XXXXX	Tape and Reel, 4000
	TSSOP-8	-40℃ to +105℃	TD25C080GTS8G/TR	TD 34DGTS8 XXXXX	Tape and Reel, 5000
	UTDFN-2×3-8AL	-40℃ to +105℃	TD25C080GUJN8G/TR	34JJN8 XXXXX	Tape and Reel, 3000
TD25C160	SOIC-8	-40℃ to +105℃	TD25C160GS8G/TR	TD 25C160GS8 XXXXX	Tape and Reel, 4000
	TSSOP-8	-40℃ to +105℃	TD25C160GTS8G/TR	TD 34EGTS8 XXXXX	Tape and Reel, 5000
	UTDFN-2×3-8AL	-40℃ to +105℃	TD25C160GUJN8G/TR	34KJN8 XXXXX	Tape and Reel, 3000
TD25C320	SOIC-8	-40℃ to +105℃	TD25C320GS8G/TR	TD 25C320GS8 XXXXX	Tape and Reel, 4000
	TSSOP-8	-40℃ to +105℃	TD25C320GTS8G/TR	TD 34FGTS8 XXXXX	Tape and Reel, 5000
	UTDFN-2×3-8AL	-40℃ to +105℃	TD25C320GUJN8G/TR	34LJN8 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... -0.5V to 6V
Output Voltage ..... -0.5V to (V_{CC} + 0.5V)
Input Voltage ..... -0.5V to 6V
DC Output Current 5mA
Ambient Temperature with Power Applied ... -55℃ to +130℃
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +105℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

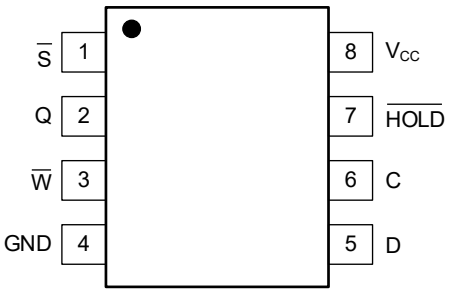
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

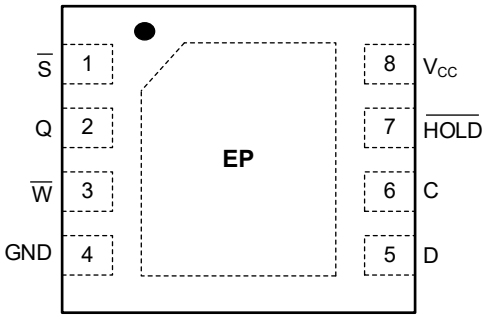
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8/TSSOP-8

(TOP VIEW)



UTDFN-2×3-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	$\overline{S}$	I	Chip Select. When this input is driven high, the device becomes deselected, and the Q pin assumes a high-impedance state. The device remains in Standby mode as long as no internal Write cycle is active. Driving Chip Select ($\overline{S}$) low selects the device and activates it. After power-up, a Chip Select ($\overline{S}$) falling edge is required before any instruction.
2	Q	O	Serial Data Output. This output is employed for serial data transmission out of the device. The falling edge of Serial Clock (C) shifts serial data out.
3	$\overline{W}$	I	Write Protect. This input pin locks the write-protected memory region size. During all Write instructions this pin must be driven high or low and kept stable.
4	GND	G	Ground. The ground reference for the device power supply (V_{CC}). GND should be connected to the system ground.
5	D	I	Serial Data Input. This input transfers serial data into the device. It accepts instructions, addresses, and write data. The rising edge of Serial Clock (C) latches input values.
6	C	I	Serial Clock. The serial interface timing is referenced by this input. The rising edge of Serial Clock (C) captures instructions, addresses, and data from Serial Data Input (D), while the falling edge transitions Serial Data Output (Q).
7	$\overline{HOLD}$	I	Hold. This input suspends all serial communication with the device without releasing the chip select. When the device enters Hold mode, the Serial Data Output (Q) is set to a high-impedance state. The logic states of Serial Data Input (D) and Serial Clock (C) pins are Don't Care. The Hold condition can only be triggered when the device is selected (Chip Select ($\overline{S}$) = Low).
8	V_{CC}	P	Device Power Supply. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may lead spurious results and should not be attempted.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Operating conditions: T_A = -40℃ to +105℃, V_{CC} = 1.7V to 5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Voltage	V_{CC}		1.7	5.5	V
Supply Current (Read)	I_{CC1}	V_{CC} = 1.7V at 5MHz, Q = open		1	mA
		V_{CC} = 2.5V at 10MHz, Q = open		5	
		V_{CC} = 5.5V at 20MHz, Q = open		10	
Supply Current (Write)	I_{CC2}	During t_{WC}, $\overline{S}$ = V_{CC}, V_{CC} = 1.7V		1	mA
		During t_{WC}, $\overline{S}$ = V_{CC}, V_{CC} = 5.5V		2	
Standby Current	I_{SB}	$\overline{S}$ = V_{CC}, V_{CC} = 1.7V		1	μA
		$\overline{S}$ = V_{CC}, V_{CC} = 5.5V		3	
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND		1	μA
Output Leakage Current	I_{LO}	$\overline{S}$ = V_{CC}, V_{OUT} = V_{CC} or GND		1	μA
Input Low Voltage	V_{IL}	1.7V ≤ V_{CC} < 2.5V	-0.45	0.25 × V_{CC}	V
		2.5V ≤ V_{CC} < 5.5V	-0.45	0.3 × V_{CC}	
Input High Voltage	V_{IH}	1.7V ≤ V_{CC} < 2.5V	0.75 × V_{CC}	V_{CC} + 1	V
		2.5V ≤ V_{CC} < 5.5V	0.7 × V_{CC}	V_{CC} + 1	
Output Low Voltage	V_{OL}	V_{CC} = 1.7V, I_{OL} = 0.15mA		0.2	V
		V_{CC} = 2.5V, I_{OL} = 1.5mA or V_{CC} = 5V, I_{OL} = 2mA		0.4	
Output High Voltage	V_{OH}	V_{CC} = 1.7V, I_{OH} = -0.1mA	V_{CC} - 0.2		V
		V_{CC} = 2.5V, I_{OH} = -0.4mA or V_{CC} = 5V, I_{OH} = -2mA	V_{CC} - 0.8		

ELECTRICAL CHARACTERISTICS (continued)

AC Characteristics

(Operating range: T_A = -40℃ to +105℃, V_{CC} = 1.7V to 5.5V, C_L = 50pF. Measurement conditions: input rise and fall time ≤ 50ns; input pulse voltages: 0.2 × V_{CC} to 0.8 × V_{CC}; input and output timing reference voltages: 0.3 × V_{CC} to 0.7 × V_{CC}, unless otherwise noted.)

PARAMETER	SYMBOL	V_{CC} = 1.7V to 5.5V		V_{CC} = 2.5V to 5.5V		V_{CC} = 4.5V to 5.5V		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Frequency	f_{SCL}		5		10		20	MHz
Clock High Time	t_{WH}	80		40		20		ns
Clock Low Time	t_{WL}	80		40		20		ns
Input Rise Time	t_{RI} (1)		80		40		15	ns
Input Fall Time	t_{FI} (1)		80		40		15	ns
$\overline{S}$ High Time	t_{CS}	60		40		25		ns
$\overline{S}$ Active Setup Time	t_{CSLS}	60		30		20		ns
$\overline{S}$ Active Hold Time	t_{CSLH}	60		30		20		ns
$\overline{S}$ Not Active Setup Time	t_{CSHS}	60		30		20		ns
$\overline{S}$ Not Active Hold Time	t_{CSHH}	60		30		20		ns
Data in Setup Time	t_{SU}	20		10		5		ns
Data in Hold Time	t_{HD}	20		10		5		ns
Clock Low to Output Valid	t_V		80		40		20	ns
Output Hold Time	t_{HO}	0		0		0		ns
Output Disable Time	t_{DIS}		100		50		25	ns
Output Rise Time	t_{RO} (1)		80		40		15	ns
Output Fall Time	t_{FO} (1)		80		40		15	ns
$\overline{HOLD}$ Setup Time	t_{SUHD}	20		10		5		ns
$\overline{HOLD}$ Hold Time	t_{HDHD}	20		10		5		ns
$\overline{HOLD}$ to Output Low - Z	t_{LZ}	0	100	0	50	0	25	ns
$\overline{HOLD}$ to Output High - Z	t_{HZ}		100		50		25	ns
Write Cycle Time	t_{WR}		3		3		3	ms

NOTE: 1. This parameter is ensured by characterization only.

Pin Capacitance

(Operating range for pin capacitance: T_A = +25°C, f_C = 5MHz, V_{CC} = 1.7V to 5.5V.)

PARAMETER (1)	SYMBOL	CONDITIONS	MAX	UNITS
Output Capacitance (Q)	C_{OUT}	V_{OUT} = 0V	8	pF
Input Capacitance (D)	C_{IN}	V_{IN} = 0V	8	pF
Input Capacitance (Other Pins)			6	

NOTE: 1. These parameters are ensured by characterization only.

Reliability Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	UNITS
Write Cycle Endurance	N_W	T_A = +25℃, Page mode	1×10^6	cycle
		T_A = +105℃, Page mode	1×10^5	cycle
Data Retention	D_R	T_A = +25℃	100	year

TIMING REQUIREMENTS

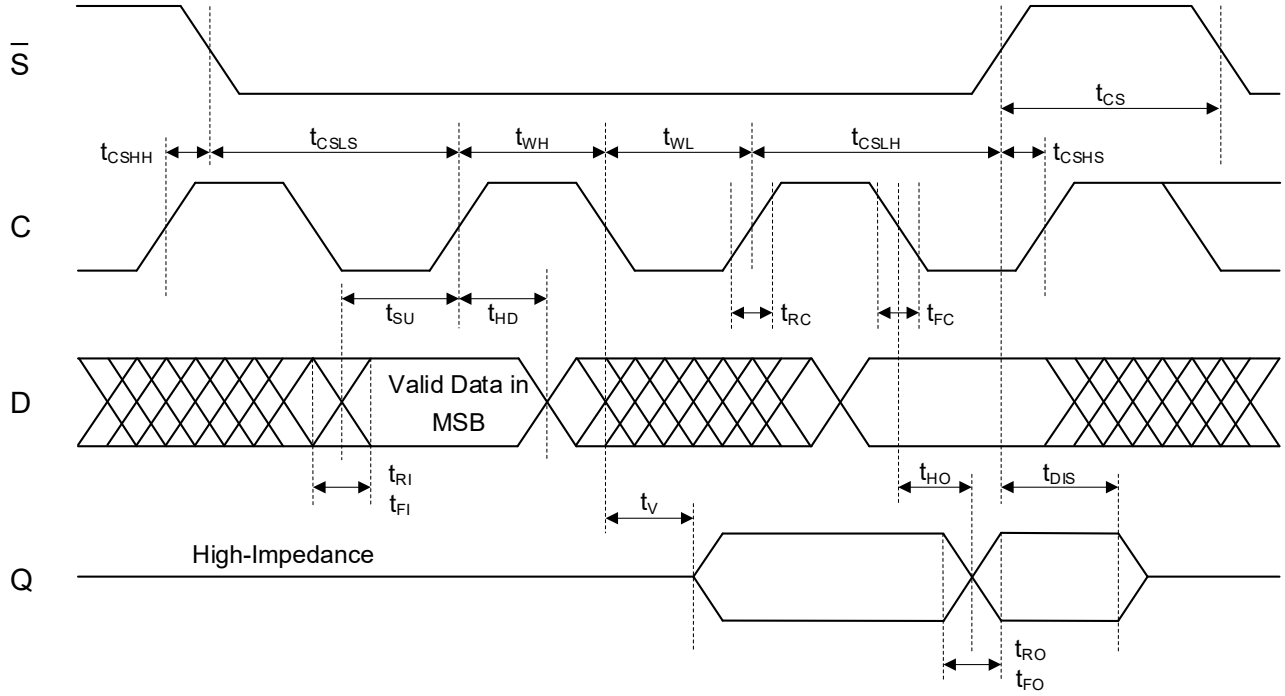


Figure 1. Serial Input/Output Timing

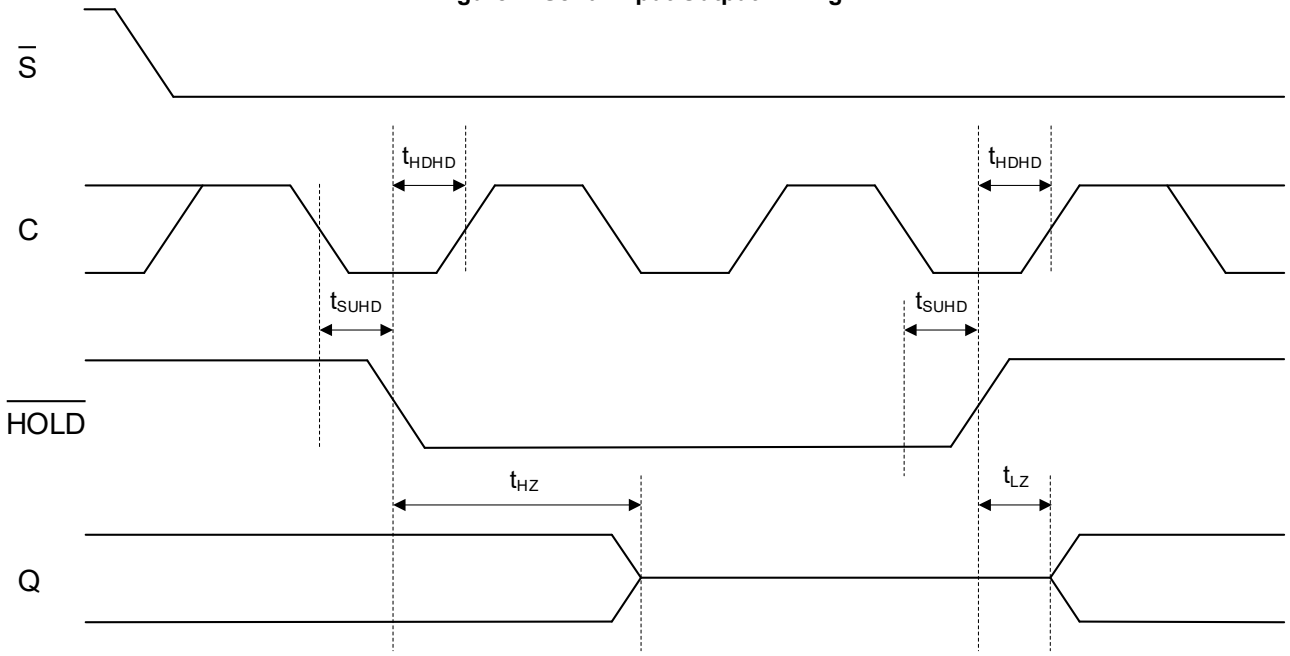


Figure 2. Hold Condition Timing

FUNCTIONAL BLOCK DIAGRAM

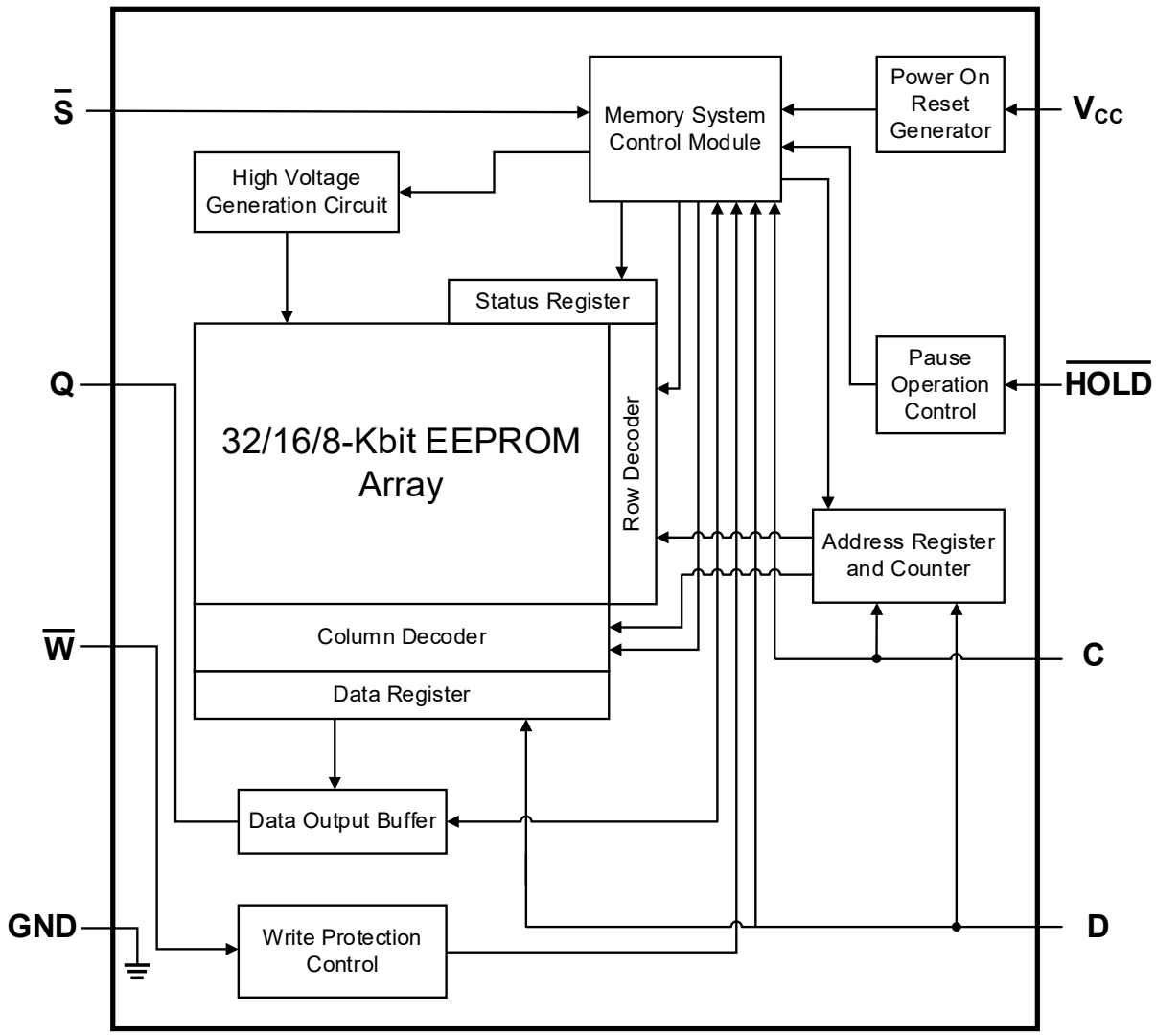


Figure 3. Block Diagram

DEVICE COMMUNICATION

SPI Mode

The TD25C320/160/080 is controlled by a set of instructions sent from a microcontroller, commonly referred to as the SPI Master. The SPI Master communicates with the device via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{S}$), Serial Clock (C), Serial Data Input (D) and Serial Data Output (Q).

The SPI protocol defines a total of four modes of operation (mode 0, 1, 2 or 3) with each mode differing in respect to Serial Clock (C) polarity (CPOL) and phase (CPHA) and how the polarity and phase control the flow of data on the SPI bus. The TD25C320/160/080 supports two most common modes: SPI mode 0 (CPOL = 0, CPHA = 0) and mode 3 (CPOL = 1, CPHA = 1). The rising edge of Serial Clock (C) captures data in SPI modes 0 and 3, while the falling edge makes output valid.

When the bus master is in Standby mode and not transferring data, the two modes differ in clock polarity (see Figure 4).

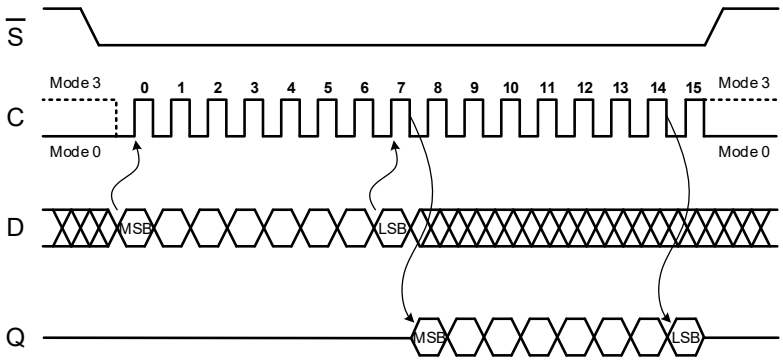


Figure 4. SPI Mode 0 and Mode 3

SPI Bus Connection

With the most significant bit transmitted first, the device accepts all instructions, addresses, and input bytes via serial shifting. Once Chip Select ($\overline{S}$) is pulled low, the first rising edge of C samples Serial Data Input (D).

The device shifts all output bytes out with the most significant bit first. The first falling edge of Serial Clock (C) after an instruction clock-in latches Serial Data Output (Q).

Figure 5 provides an example of four memory chips interfaced with an SPI bus master over the SPI bus. With only one memory device selected at a time, the Serial Data Output (Q) line is driven by just that one device. All unselected memory devices set their outputs to a high-impedance state.

The pull-up resistor R ensures the Chip Select ($\overline{S}$) line stays de-asserted to avoid accidental device selection if the bus master drives the line into a high-impedance state.

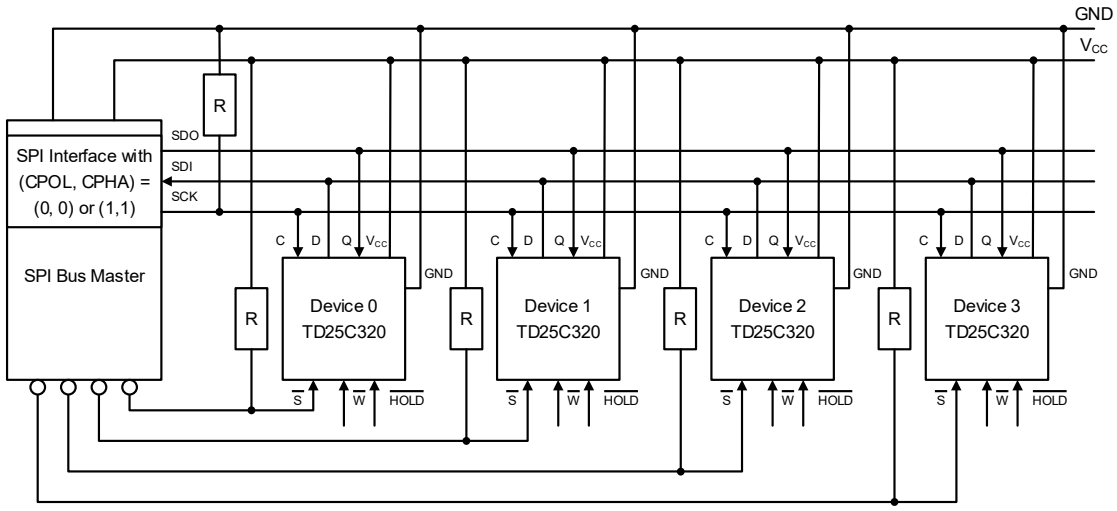


Figure 5. SPI Master and Memory Device Connections

DEVICE COMMUNICATION (continued)

Active and Standby Mode

The TD25C320/160/080 enters Active mode and becomes selected once Chip Select ($\overline{S}$) is driven low. The device consumes I_{CC}, refer to DC Characteristics table.

Driving Chip Select ($\overline{S}$) high deselects the TD25C320/160/080. When no internal write cycle is active, the device enters low-power Standby mode.

Device Reset and Initialization

The TD25C320/160/080 incorporates a Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal power-on reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC} (MIN). The Chip Select ($\overline{S}$) line should be connected to V_{CC} and must not float during this time. Therefore, it is recommended to connect the Chip Select ($\overline{S}$) line to V_{CC} via a pull-up resistor. Once the supply voltage passes V_{POR}, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT}. The supply voltage shall stay stable and valid until the completion of protocol transmission. For write commands, stable supply must be maintained through the entire internal write cycle (see Figure 6).

This POR behavior is bi-directional. It protects the TD25C320/160/080 against brown-out failure caused by a temporary loss of power. In a similar way, as soon as the supply voltage drops below the internal brown-out reset threshold voltage (V_{BOR}), the device is reset and stops responding to any instructions (see Figure 6). The V_{BOR} level is set below the V_{POR} level.

Parameters related to power-up and power-down conditions are listed in Table 1.

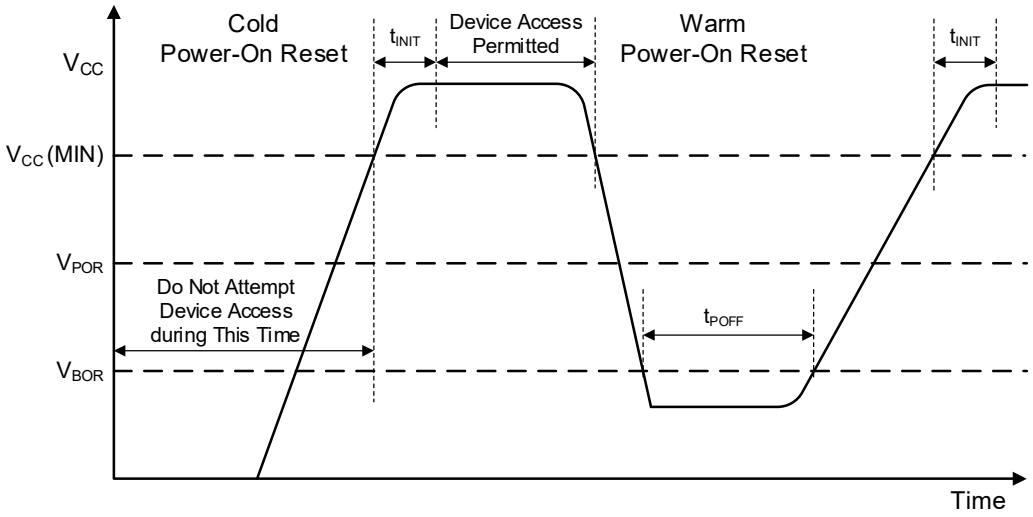


Figure 6. Power-Up and Power-Down Timing

Table 1. Power-Up and Power-Down Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power-On Reset Voltage	V_{POR}		1.5	V
Brown-Out Reset Voltage	V_{BOR}	1.2		
Time from Power-On to First Command	t_{INIT}	200		μs
Warm Power Cycle Off Time	t_{POFF}	200		

DEVICE COMMUNICATION (continued)

Hold Condition

The Hold ($\overline{HOLD}$) signal suspends serial communication without disturbing the ongoing clock sequence. However, the internal write cycle is unaffected by the Hold condition. Therefore, if a write cycle is in progress, driving the Hold ($\overline{HOLD}$) signal low will not pause the operation and the write cycle will continue to complete.

The Hold condition can only be enabled when the device is selected by pulling Chip Select ($\overline{S}$) to a low level. The Hold state is triggered when the Hold ($\overline{HOLD}$) signal is pulled low while the Serial Clock (C) is at a low logic level. When the Hold ($\overline{HOLD}$) signal is pulled low during the Serial Clock (C) high pulse, then the Hold condition will not be started until the beginning of the next Serial Clock (C) low pulse.

In the Hold state, Serial Data Output (Q) is high-impedance while Serial Data Input (D) and Serial Clock (C) are Don't Care.

The Hold state is terminated by driving the Hold ($\overline{HOLD}$) signal high while the Serial Clock (C) is at a low logic level. When the Hold ($\overline{HOLD}$) signal is pulled high during the Serial Clock (C) high pulse, then the Hold condition will not end until the beginning of the next Serial Clock (C) low pulse (see Figure 7).

In the Hold state, the device usually stays selected for its full duration. Deselecting the device when it is in the Hold state will reset the device internal state.

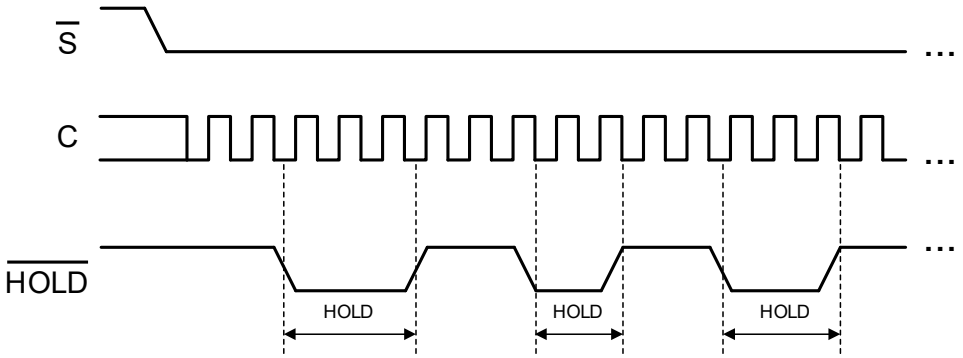


Figure 7. Hold Condition Activation

Data Protection

The TD25C320/160/080 integrates the following data protection functions:

- The Write Enable Latch (WEL) bit must be set by a WREN instruction before any instruction that modifies data is executed (see Write Enable (WREN) section for details).
- The Block Protect bits (BP1, BP0) within the Status Register are used to configure designated memory regions as Read-only (see Section Block Write Protection for details).
- The Write Protect (W) signal in accordance with the Status Register Write Protect (SRWR) bit in the Status Register is used to write protect the Status Register (see Section Status Register Write Protection for details).

INSTRUCTIONS

Each instruction is composed of bytes transmitted MSB first, beginning with an instruction byte (see Table 2), and is initiated by a falling edge on Chip Select ($\overline{S}$).

The device automatically holds a wait state until the chip is deselected when an invalid instruction is transmitted (an instruction not listed in Table 2).

Table 2. Instruction Set for the TD25C320/160/080

INSTRUCTION NAME	OPERATION DESCRIPTION	INSTRUCTION FORMAT
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from 32/16/8-Kbit Memory Array	0000 0011
WRITE	Write to 32/16/8-Kbit Memory Array	0000 0010
RDID	Read Identification Page	1000 0011
WRID	Write Identification Page	1000 0010
RDLS	Read Identification Page Lock Status	1000 0011
LID	Lock Identification Page in Read-only Mode	1000 0010
RDUID	Read Unique ID	1000 0001

INSTRUCTIONS (continued)

Write Enable (WREN)

Prior to issuing each WRITE and WRSR instruction, the Write Enable Latch (WEL) bit must be set. This bit can only be set by transmitting the Write Enable (WREN) instruction to the device.

To issue the WREN instruction to the device, pull Chip Select ($\overline{S}$) low first, and then shift the instruction byte (06h) in through Serial Data Input (D) (see Figure 8). The device will enter a wait state and hold this status until Chip Select ($\overline{S}$) is pulled high to deselect.

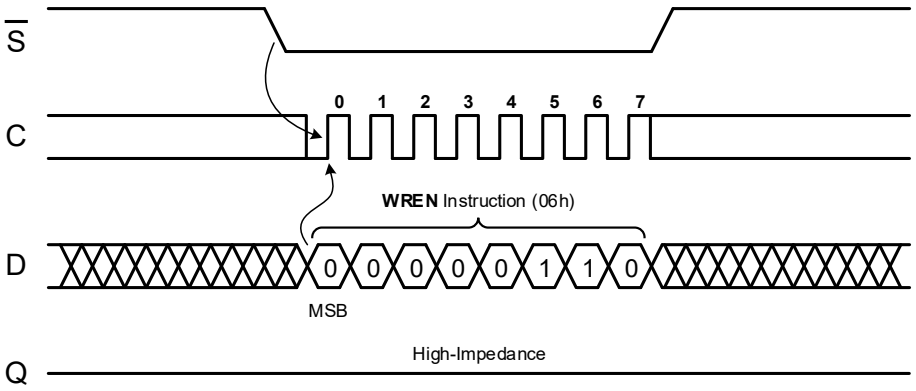


Figure 8. Write Enable

Write Disable (WRDI)

To reset the WEL bit, send a Write Disable (WRDI) instruction by driving Chip Select ($\overline{S}$) low and shifting in the instruction byte on Serial Data Input (D) (see Figure 9). The device then enters a Wait state and remains there until Chip Select ($\overline{S}$) is driven high to deselect it.

The following events will reset the WEL bit:

- Power-up;
- WRDI instruction execution;
- WRSR or WRITE (including WRID and LID) instruction completion;

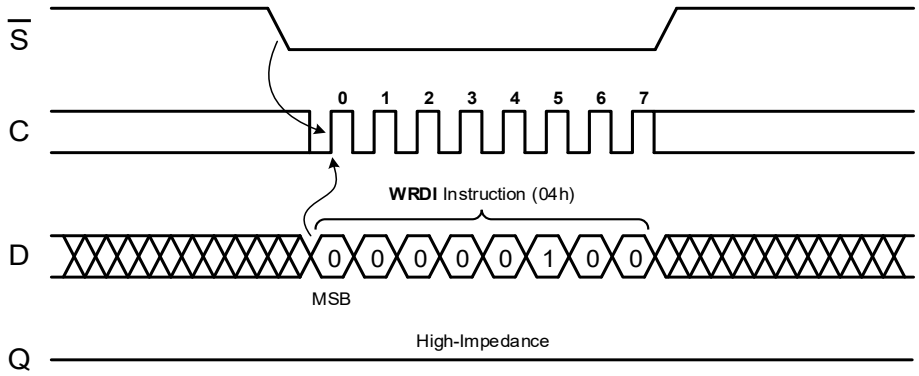


Figure 9. Write Disable

INSTRUCTIONS (continued)

Read Status Register (RDSR)

The TD25C320/160/080 includes an 8-bit Status Register. The Status Register bits modulate various features of the device as listed in Table 3.

Table 3. Status Register Bit Definition and Function

BIT	NAME	FUNCTION	DESCRIPTION	
D[7]	SRWD	Status Register Write Protect	0	Write Protect (W) pin is not enabled (Initial Delivery State)
			1	Write Protect (W) pin is enabled (see section Status Register Write Protection for detail)
D[6:4]	RFU	Reserved for Future Use	0	Read always as '000'
D[3]	BP1	Block Protect	00	No memory array write protection (Initial Delivery State)
			01	Quarter memory array write protection (see section Block Write Protection for detail)
D[2]	BP0		10	Half memory array write protection (see Block Write Protection for detail)
			11	Whole memory array write protection (see Block Write Protection for detail)
D[1]	WEL	Write Enable Latch	0	Device is not write enabled (Power-up state)
			1	Device is write enabled
D[0]	WIP	Write in Progress	0	No write cycle is in progress, device is ready for new instruction
			1	Device is busy with an internal write cycle

The Status Register is read via the Read Status Register (RDSR) instruction. This instruction begins with Chip Select ($\overline{S}$) driven low, after which the instruction byte (05h) is shifted on Serial Data Input (D). The device will return 8-bit Status Register value on Serial Data Output (Q). The Status Register value is output repeatedly while Chip Select ($\overline{S}$) remains low (see Figure 10).

Driving Chip Select ($\overline{S}$) high ends the RDSR instruction. The rising edge on Chip Select ($\overline{S}$) is valid at any point within the operation cycle.

Status Register read is available anytime, during internal write operation as well. While a write cycle is active, the Write in Progress (WIP) bit should be polled before issuing a new instruction.

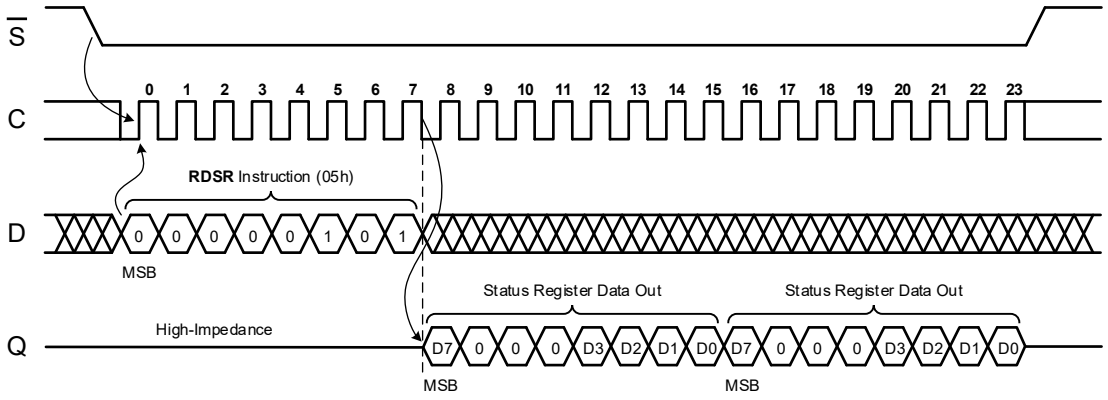


Figure 10. Read Status Register

INSTRUCTIONS (continued)

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction enables the SPI Master to change selected bits of the Status Register. Before a WRSR instruction being initiated, a WREN instruction must be executed to set the WEL bit to Logic '1'. To execute the WRSR instruction, drive Chip Select ($\overline{S}$) low, clock the instruction byte (01h) and data byte into the device via Serial Data Input (D), and then drive Chip Select ($\overline{S}$) high. After the rising edge of Serial Clock (C) that latches the 8th data bit, and before the next C rising edge, Chip Select ($\overline{S}$) must be driven high (see Figure 11). The WRSR instruction fails if this timing requirement is violated.

Pulling Chip Select ($\overline{S}$) high at the byte boundary initiates the self-timed write cycle, which requires a fixed duration t_{WC} to complete. During this cycle, the WIP bit in the Status Register is held high and can be polled to monitor write progress; it returns low when the cycle completes. After the completion of the write cycle, the WEL bit is also reset.

The WRSR instruction has no effect on the bit 6, bit 5, bit 4, bit 1 and bit 0 in the Status Register, but only enables the user to change the values of the SRWD, BP1 and BP0 bits. These three bits are non-volatile bits that have the same properties and functions as regular EEPROM cells.

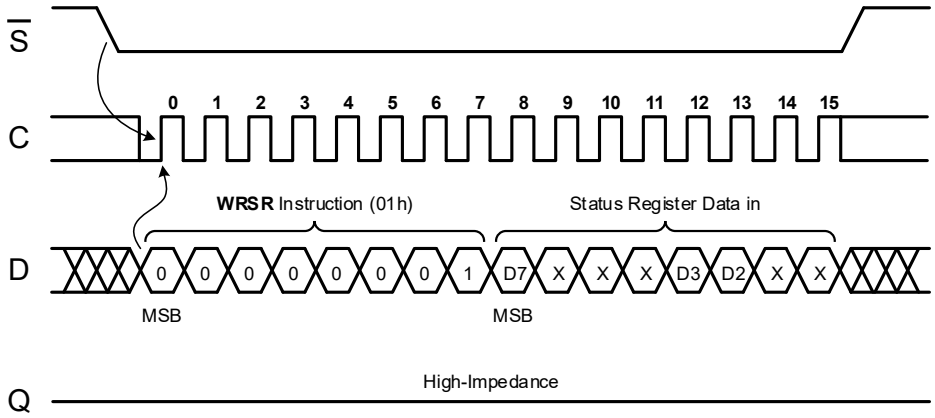


Figure 11. Write Status Register

Block Write Protection

The WRSR instruction enables the user to selectively write-protect the memory array by blocks through changing the Block Protect bits (BP1, BP0). The Write-Protected Block size and the corresponding Status Register control bits are shown in Table 4.

Table 4. Write-Protected Block Size

STATUS REGISTER BITS		PROTECTED BLOCK	PROTECTED ADDRESS RANGE		
BP1	BP0		TD25C320	TD25C160	TD25C080
0	0	None	None	None	None
0	1	Upper Quarter	0C00h to 0FFFh	0600h to 07FFh	0300h to 03FFh
1	0	Upper Half	0800h to 0FFFh	0400h to 07FFh	0200h to 03FFh
1	1	Whole Memory	0000h to 0FFFh	0000h to 07FFh	0000h to 03FFh

INSTRUCTIONS (continued)

Status Register Write Protection

The WRSR instruction allows the user to enable or disable the Status Register Write Protection mode through changing the Status Register Write Protect (SRWD) bit in accordance with the state of Write Protect ($\overline{W}$) pin.

When the SRWD bit is Logic '0', the user can write to the Status Register when the WEL bit has been set by a WREN instruction, regardless of the Write Protect ($\overline{W}$) pin state. When the SRWD bit is set to Logic '1', the Write Protect ($\overline{W}$) pin determines two possible scenarios:

- When Write Protect ($\overline{W}$) is high and the Write Enable Latch (WEL) bit has been set by a Write Enable (WREN) instruction, writing to the Status Register is permitted.
- With Write Protect ($\overline{W}$) low, Status Register writes are prohibited even when WREN has set the Write Enable Latch (WEL) bit. Thus, hardware write protection also covers the memory region defined by the Block Protect (BP1, BP0) bits in the Status Register.

The Hardware-Protected mode can be entered regardless of the sequence: either set the SRWD bit first then drive Write Protect ($\overline{W}$) low, or drive Write Protect ($\overline{W}$) low first then set the SRWD bit. Once entered, the only way to exit this mode is to drive the Write Protect ($\overline{W}$) pin high. Hardware-Protected mode cannot be activated when Write Protect ($\overline{W}$) is permanently tied high.

Table 5 summarizes the device protection features.

Table 5. SRWD Protection Modes

SRWD BIT	$\overline{W}$ PIN	WEL BIT	STATUS REGISTER	PROTECTED BLOCK	UNPROTECTED BLOCK
0	X	0	Protected	Protected	Protected
0	X	1	Writable	Protected	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Protected	Writable
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Writable	Protected	Writable

NOTE: X = Don't Care State.

INSTRUCTIONS (continued)

Read from Memory Array (READ)

Reading the TD25C320/160/080 memory array is achieved with the Read from Memory Array (READ) instruction. To issue the READ instruction, first drive Chip Select ($\overline{S}$) low, then clock in the instruction byte (03h) and two address bytes on Serial Data Input (D). For the 32/16/8-Kbit memory array, address bits A11:A0 are significant address bits and A15:A12 are Don't Care bits. For the 16-Kbit memory array, address bits A10:A0 are significant address bits and A15:A11 are Don't Care bits. For the 8-Kbit memory array, address bits A9:A0 are significant address bits and A15:A10 are Don't Care bits. An internal address counter receives the address, and the data byte at that location is output on Serial Data Output (Q). When Chip Select ($\overline{S}$) is held low, the counter auto-increments and shifts out the next data byte (see Figure 12). The read cycle can continue as the counter rolls over to the lowest address when the highest is reached. Therefore, a single READ instruction can read the whole memory.

Pull Chip Select ($\overline{S}$) high to end the read operation. During the read cycle, the Chip Select ($\overline{S}$) rising edge can happen at any moment.

The READ instruction is neither acknowledged nor executed when an internal write cycle is in progress.

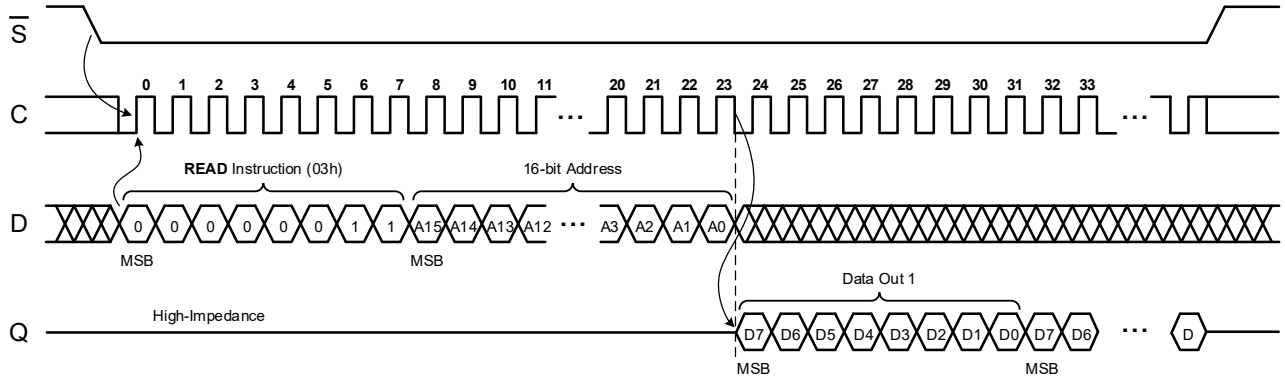


Figure 12. Read from Memory Array

INSTRUCTIONS (continued)

Write to Memory Array (WRITE)

In order to program the TD25C320/160/080 32/16/8-Kbit memory array, two separate instructions must be executed. First, a WREN instruction must be executed to set the device to write enable. Then, one of the two possible write sequences described below may be executed. The device will ignore the WRITE instruction if the device is not write enable, and return to the Standby mode when Chip Select ($\overline{S}$) is driven high.

Byte Write

To execute a Byte Write instruction, first drive Chip Select ($\overline{S}$) low, then clock in the WRITE instruction byte (02h), the address byte, and one data byte on Serial Data Input (D). For the 32/16/8-Kbit memory array, address bits A11:A0 are significant address bits and A15:A12 are Don't Care bits. For the 16-Kbit memory array, address bits A10:A0 are significant address bits and A15:A11 are Don't Care bits. For the 8-Kbit memory array, address bits A9:A0 are significant address bits and A15:A10 are Don't Care bits. After the C rising edge that captures the 8th data bit, and prior to the next C rising edge, take Chip Select ($\overline{S}$) high (see Figure 13).

When the addressed page is outside the Block Protect (BP1, BP0) region, driving Chip Select ($\overline{S}$) high at a byte boundary initiates the self-timed write cycle, which lasts for a fixed duration specified by t_{WC}. The TD25C320/160/080 will automatically return to the Write Disable state (WEL = 0) at the completion of a write cycle.

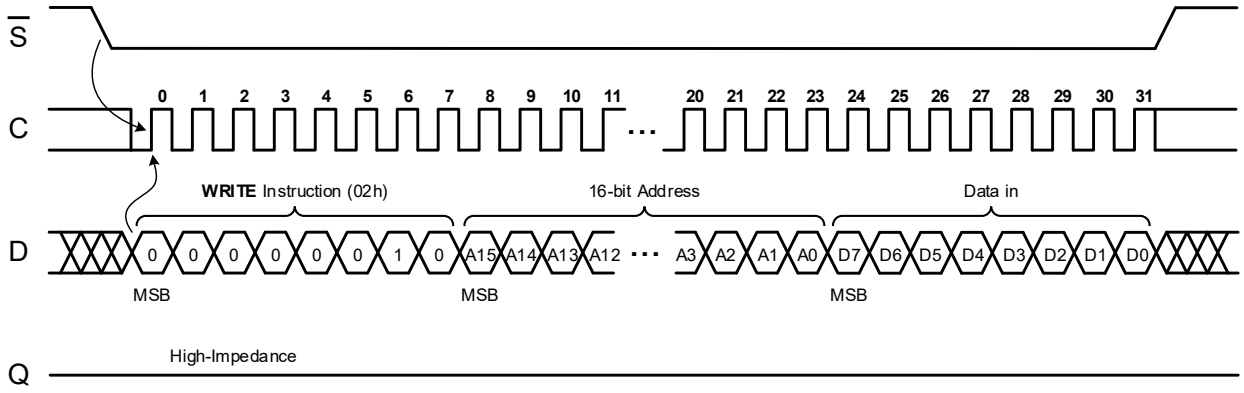


Figure 13. Byte Write

INSTRUCTIONS (continued)

Page Write

A page write sequence allows up to 32 bytes to be written in the same write cycle, provided that all bytes are in the same page of the memory array. Partial page write of less than 32 bytes is allowed. This is achieved by Chip Select ($\overline{S}$) continuing to be driven low after the receipt of each data byte, and the next byte of input data is shifted in (see Figure 14).

The five least significant bits of the internal address counter increment with each new data byte shifted in. The higher address bits are not incremented and retain the page location. When the internal address reaches the page boundary, the so-called "roll-over" condition occurs and the following data byte is placed at the beginning of the same page. When a roll-over occurs, transmission of over 32 bytes exceeding the page size to the device will overwrite the existing stored data

When the addressed page is outside the Block Protect (BP1, BP0) region, driving Chip Select ($\overline{S}$) high at a byte boundary initiates the self-timed write cycle, which lasts for a fixed duration specified by t_{WC}. The TD25C320/160/080 will automatically return to the Write Disable state (WEL = 0) at the completion of a write cycle.

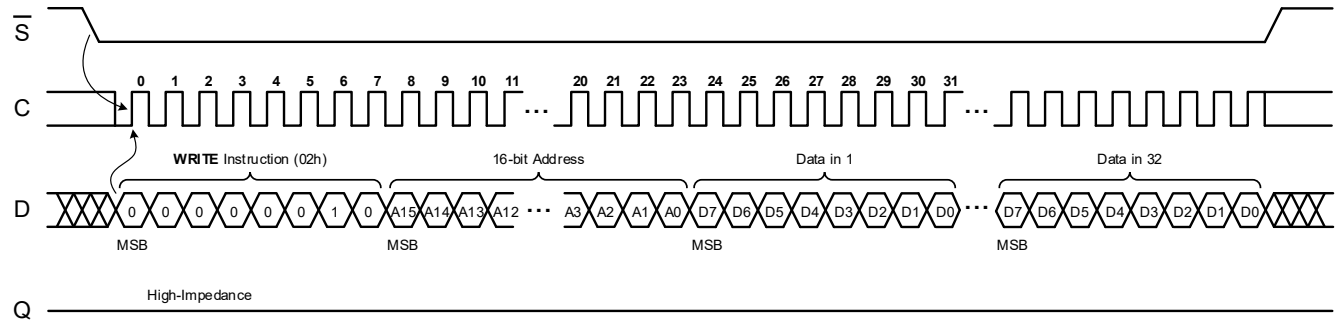


Figure 14. Page Write

Polling Routine

A polling routine can be implemented to optimize time-sensitive applications that would not prefer to wait the fixed maximum write cycle time (t_{WC}). This method allows the application to know immediately when the write cycle has completed to start a subsequent operation.

Once the internal write cycle has started, a polling routine can be initiated. This involves repeatedly sending RDSR instruction to determine if the device has completed its self-timed write cycle. If the WIP bit (bit 0 of the Status Register) = 1, the write cycle is still in progress; if the WIP bit = 0, the write cycle has ended. If the WIP bit = 1, repeated RDSR commands can be executed until the WIP bit = 0, indicating that the device is ready to execute a new instruction (see Figure 15).

Only the RDSR instruction is enabled during the write cycle.

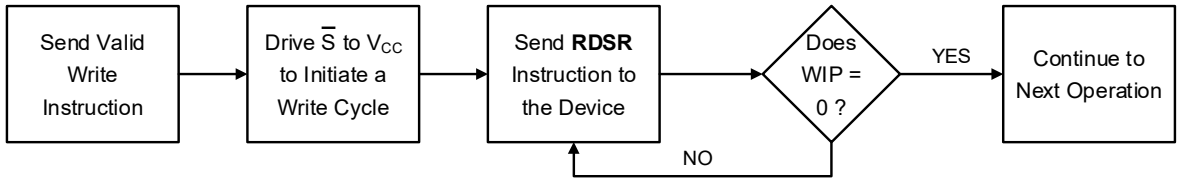


Figure 15. Polling Flow Chart

INSTRUCTIONS (continued)

Read Identification Page (RDID)

The TD25C320/160/080 offers a 32-byte Identification Page (ID Page) in addition to the 32/16/8-Kbit memory array for storage of specific application data. This Identification Page can be written and (later) permanently locked in Read-only mode.

The Identification Page is accessed via the Read Identification Page (RDID) instruction. Execution begins by asserting Chip Select ($\overline{S}$) low, followed by clocking in the instruction byte (83h) and address bytes through Serial Data Input (D). The state of address bit A10 must be logic '0'. Byte offset inside the Identification Page is specified by lower address bits (A4:A0), with upper address bits being Don't Care. The matching data byte is then output on Serial Data Output (Q). When Chip Select ($\overline{S}$) stays low, the internal counter auto-increments and shifts out the byte at the new address (see Figure 16). Upon reaching the end of the ID Page, the address counter rolls over to the start to enable continuous read operation.

Pull Chip Select ($\overline{S}$) high to end the read operation. During the read cycle, the Chip Select ($\overline{S}$) rising edge can happen at any moment.

The RDID instruction is neither acknowledged nor executed when an internal write cycle is in progress.

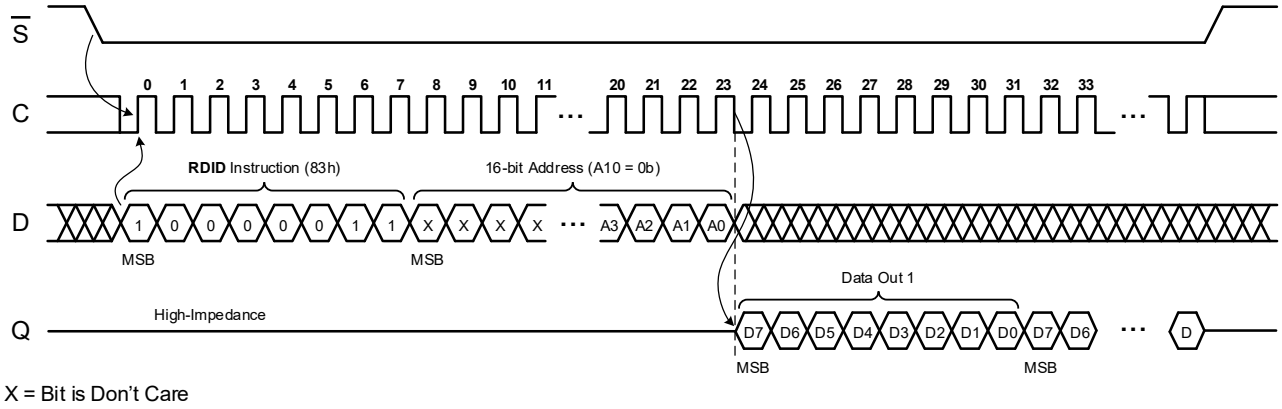


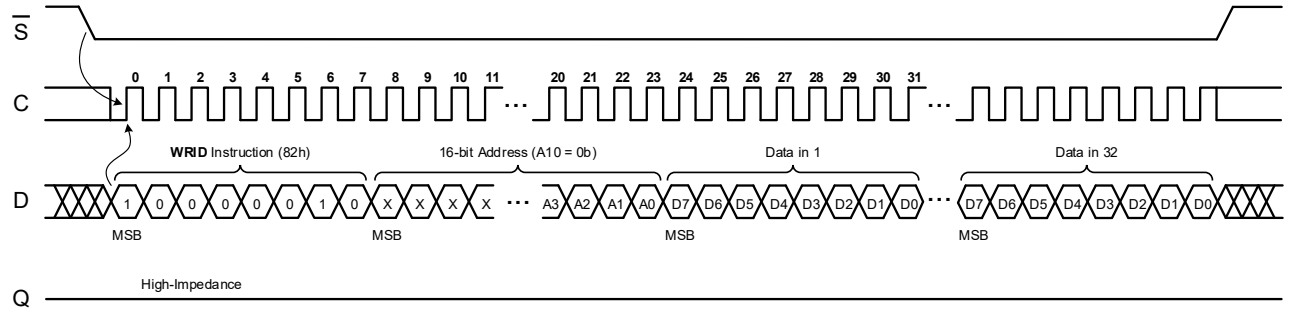
Figure 16. Read Identification Page

INSTRUCTIONS (continued)

Write Identification Page (WRID)

The Identification Page is programmed using the Write Identification Page (WRID) instruction. A prior WREN instruction is required to enable reception of the WRID instruction.

To send the WRID instruction, first drive Chip Select ($\overline{S}$) low. After that, shift the instruction byte (82h), address bytes, and a minimum of one data byte in via Serial Data Input (D). The state of address bit A10 must be logic '0'. The Identification Page byte address is defined by lower bits A4:A0, with upper bits being Don't Care. When Chip Select ($\overline{S}$) is driven high at the completion of a data byte, the instruction ends (see Figure 17). If the Identification Page has not been locked in Read-only mode, the Chip Select ($\overline{S}$) rising edge triggers the self-timed write cycle, which continues for a period of t_{WC}.



X = Bit is Don't Care

Figure 17. Write Identification Page

INSTRUCTIONS (continued)

Read Lock Status (RDLS)

The Read Lock Status (RDLS) instruction verifies the lock state of the Identification Page (locked Read-only or not). To issue the RDLS instruction, drive Chip Select ($\overline{S}$) low, then clock in the instruction byte (83h) and the address bytes on Serial Data Input (D). With A10 set to '1', all other address bits are Don't Care. The least significant bit (LSB) of the byte from Serial Data Output (Q) indicates the lock status. This bit is logic ‘1’ for active write lock and logic ‘0’ when the lock is inactive. All other bits are always read as ‘0’ (see Figure 18). The same data byte continues to be shifted out while Chip Select ($\overline{S}$) remains low.

Pull Chip Select ($\overline{S}$) high to end the read operation. During the read cycle, the Chip Select ($\overline{S}$) rising edge can happen at any moment.

The RDLS instruction is neither acknowledged nor executed when an internal write cycle is in progress.

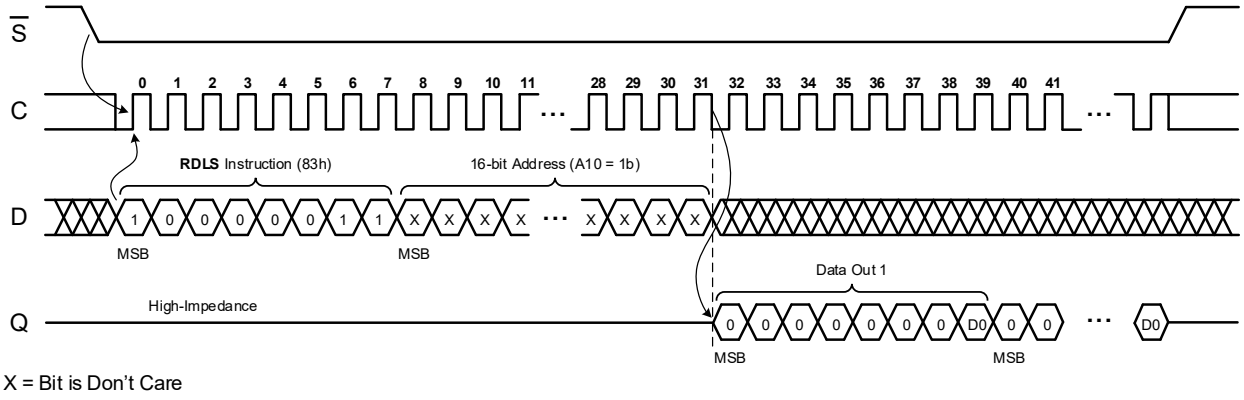


Figure 18. Read Lock Status

INSTRUCTIONS (continued)

Lock Identification Page (LID)

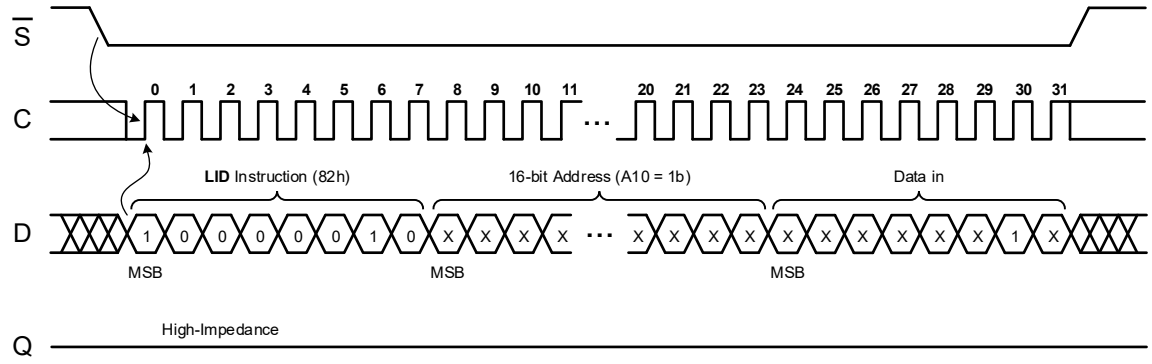
The Lock ID (LID) instruction permanently sets the Identification Page to Read-only mode. A prior WREN instruction is required for the LID command to be accepted.

The Lock ID (LID) instruction is sent by pulling Chip Select ($\overline{S}$) low, shifting the instruction byte (82h), the address bytes, and a data byte through Serial Data Input (D), and then taking Chip Select ($\overline{S}$) high. With A10 set to '1', all other address bits are Don't Care. The transmitted data byte must match the binary pattern xxxx_xx1x (where x = bit is Don't Care).

After the rising edge of Serial Clock (C) that captures the 8th data bit and prior to the next rising edge of Serial Clock (C), Chip Select ($\overline{S}$) must be pulled high. The LID instruction is not executed otherwise (see Figure 19). The self-timed write cycle is launched by taking Chip Select ($\overline{S}$) high at an input byte boundary and runs for t_{WC}.

Under the following conditions, the LID instruction is not executed:

- When the WEL bit is not configured to logic ‘1’;
- When a write operation is ongoing;
- When Chip Select ($\overline{S}$) is not driven high at a byte boundary to deselect the device;
- When the Block Protect bits (BP1, BP0) = (1, 1);



X = Bit is Don’t Care

Figure 19. Lock Identification Page

INSTRUCTIONS (continued)

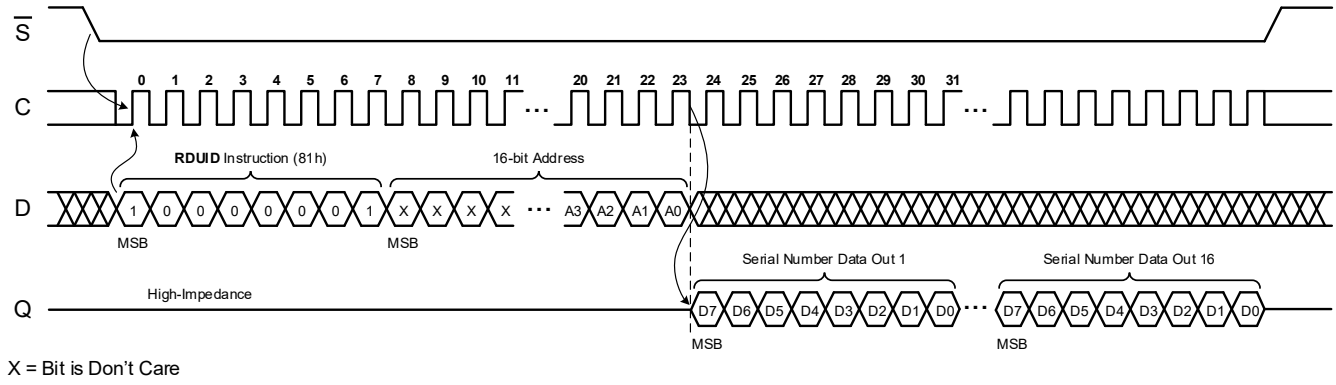
Read Unique ID (RDUID)

The TD25C320/160/080 offers a separate memory block containing a factory programmed 128-bit Unique ID (UID), or Serial Number. The Read Unique ID (RDUID) instruction is used to read this block. The instruction byte (81h) and address bytes are shifted on Serial Data Input (D) after Chip Select ($\overline{S}$) is first taken low. Byte locations inside the Unique ID block are defined by the lower address bits A3:A0, with upper address bits being Don't Care. The matching data byte for this address is then output on Serial Data Output (Q). If Chip Select ($\overline{S}$) is held low, the internal address counter auto-increments, and the byte at the updated address is output (see Figure 20).

In order to guarantee a unique number, the entire 128-bit value must be read from the starting address of the Serial Number block with the address bits A3:A0 to be '0000'. Reading from a location other than the first address of the block will not result in a unique Serial Number. Writing or altering the 128-bit Unique ID is not allowed. When the end of the 128-bit UID block is reached, the address counter will roll over to the beginning of this block to enable continuous read operation.

Pull Chip Select ($\overline{S}$) high to end the read operation. During the read cycle, the Chip Select ($\overline{S}$) rising edge can happen at any moment.

The RDUID instruction is neither acknowledged nor executed when an internal write cycle is in progress.



X = Bit is Don't Care

Figure 20. Read Unique ID

Power-up and Delivery State

Power-up State

The TD25C320/160/080 enters the following state after power-up:

- Standby mode.
- The device must be deselected (a falling edge of Chip Select ($\overline{S}$) is mandatory prior to initiating any new instruction).
- Hold condition is not active.
- The device clears the Write Enable Latch (WEL) bit to logic '0'.
- The device clears the Write in Progress (WIP) bit to logic '0'.
- The SRWD, BP1 and BP0 bits within the Status Register retain their states from the prior power-down period, as these are non-volatile bits.

Initial Delivery State

The TD25C320/160/080 serial EEPROM is delivered as follows:

- All bits in the memory array are set to ‘1’ (each byte contains FFh).
- All bits in the Identification Page are set to ‘1’ (each byte contains FFh).
- The SRWD, BP1 and BP0 flags inside the Status Register are preset to logic ‘0’.

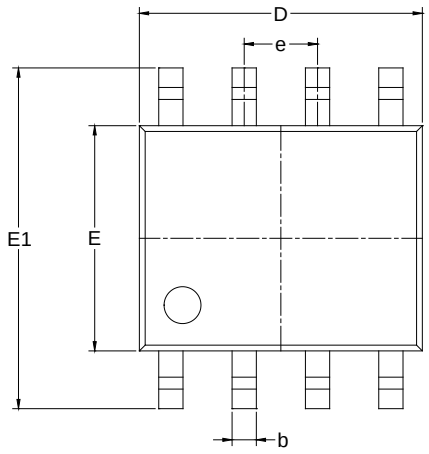
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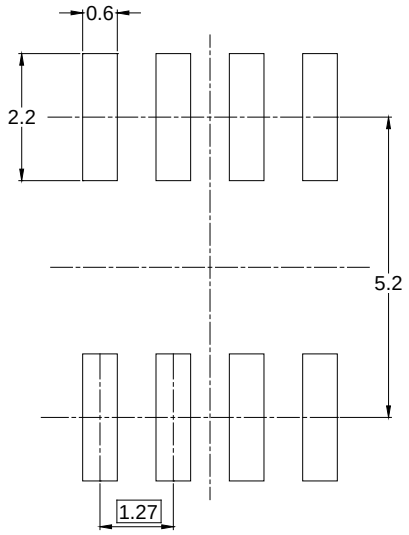
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

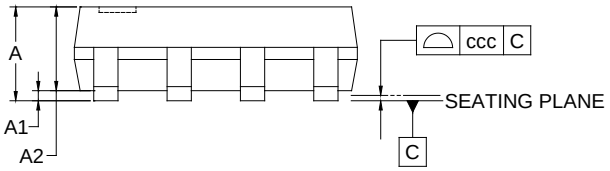
PACKAGE OUTLINE DIMENSIONS

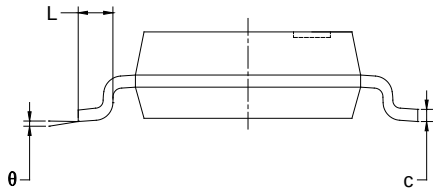
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



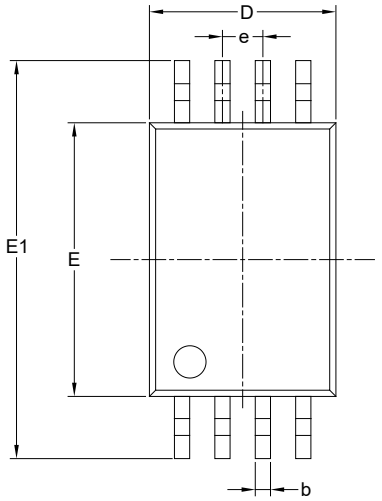


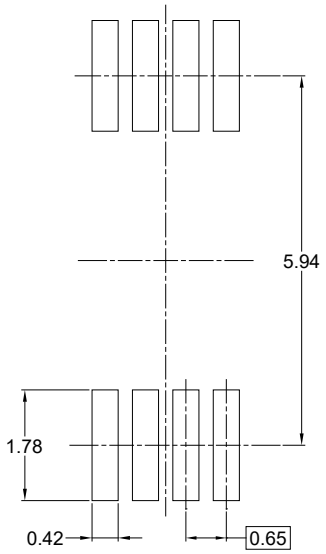
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	MIN	NOM	MAX
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.350	-	1.550
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Reference JEDEC MS-012.

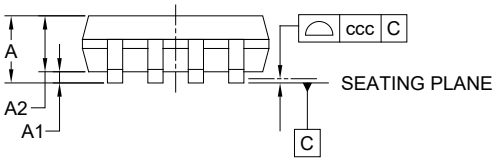
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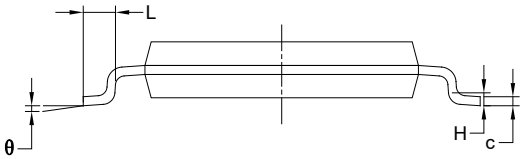
TSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



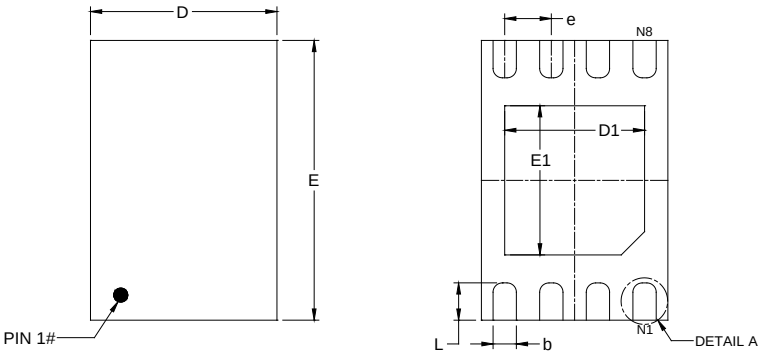


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
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A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	-	3.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

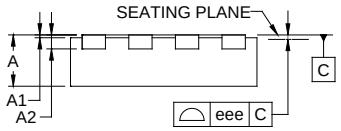
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

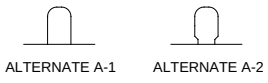
UTDFN-2×3-8AL



TOP VIEW **BOTTOM VIEW**

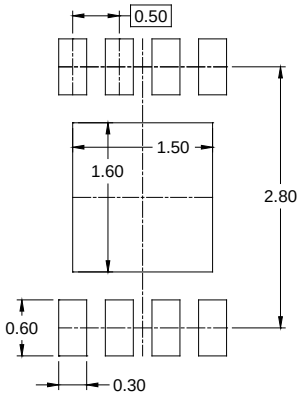


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



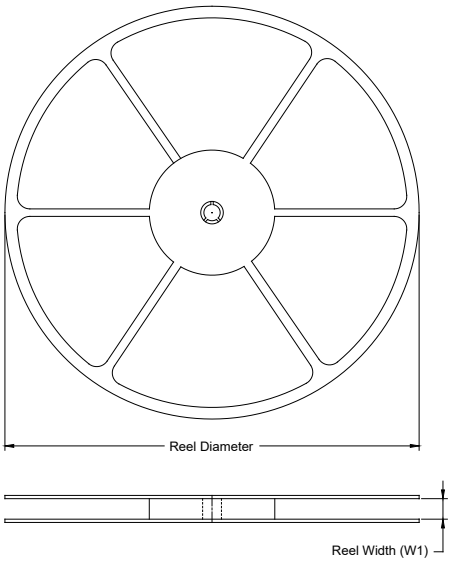
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
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A1	0.000	-	0.050
A2	0.150 REF		
b	0.180	-	0.300
D	1.900	-	2.100
D1	1.400	-	1.600
E	2.900	-	3.100
E1	1.500	-	1.700
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

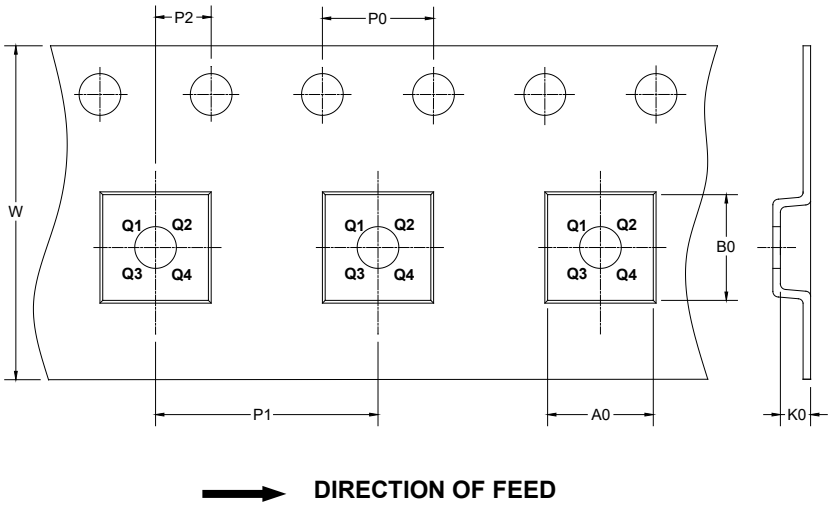
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



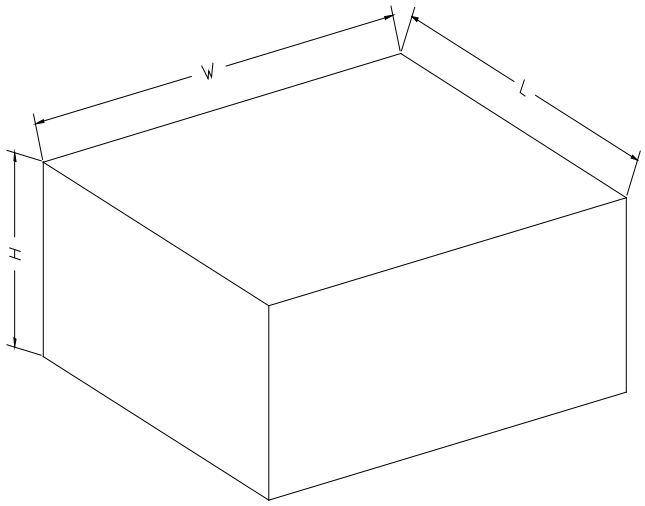
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TSSOP-8	13"	12.4	6.76	3.30	1.80	4.0	8.0	2.0	12.0	Q1
UTDFN-2×3-8AL	7"	9.5	2.30	3.30	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002