SGM838
85V, 16-Bit, High-Precision Power Monitor with I²C Interface

GENERAL DESCRIPTION

The SGM838 is a high-accuracy digital current sensor and power monitor with a 16-bit sigma-delta ADC inside. The device is capable of measuring a full-scale differential input of either ±163.84mV or ±40.96mV across a resistive shunt sense element, with -0.3V to +85V common mode voltage.

The SGM838 features current, bus voltage, temperature and power monitoring along with an alert capability. The built-in temperature sensor has an accuracy of ±1℃ for measuring the die temperature and is helpful in monitoring the ambient temperature of the system.

Targeted at precision measurement applications, the SGM838 features low offset and low gain drift to maintain accuracy across temperature. Additionally, for wide-range current applications, its low offset voltage and low noise enable measurements from A to kA while ensuring low power loss. Furthermore, the low input bias current facilitates the use of high resistance sensing resistors, ensuring precise micro-amp range measurements.

The ADC conversion time of the device can be selected from 150μs to 4.12ms and sample averaging can be selected from 1x to 1024x, which further contributes to reducing the noise.

The SGM838 is available in a Green MSOP-10 package and specified over the operating temperature range of -40℃ to +125℃.

TYPICAL APPLICATION

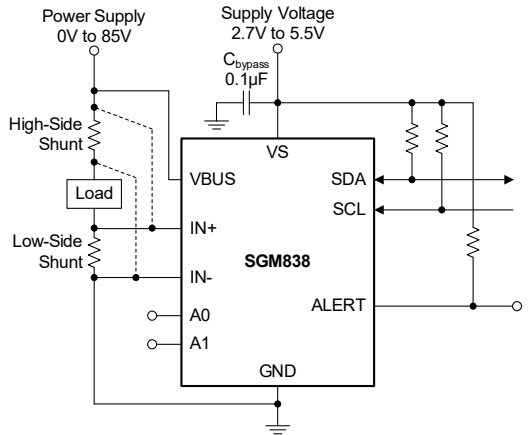


Figure 1. High-Side/Low-Side Sensing Application Circuit

FEATURES

- **High-Resolution, 16-Bit Sigma-Delta ADC**
- **Gain Accuracy:**
  - **Gain Error: ±0.35% (MAX)**
  - **Gain Drift: ±35ppm/℃ (MAX)**
- **Offset Accuracy:**
  - **Offset Voltage: ±30μV (MAX)**
  - **Offset Drift: ±300nV/℃ (MAX)**
- **Power Monitoring Accuracy:**
  - **1.3% (MAX) at -40℃ to +125℃**
- **Fast Alert Response: 275μs**
- **Input Common-Mode Voltage Range: -0.3V to +85V**
- **Sense Bus Voltage Range: 0V to 85V**
- **Excellent CMRR: 145dB (TYP)**
- **Supply Voltage Range: 2.7V to 5.5V**
- **Shutdown Current: 2.5μA (TYP)**
- **Shunt Full-Scale Differential Range:**
  - **±163.84mV/±40.96mV**
- **Input Bias Current: 8nA (MAX)**
- **Temperature Sensor: ±1℃ (TYP at +25℃)**
- **Selectable Averaging and Conversion Times**
- **3.4MHz High-Speed I²C Interface**
- **16 Pin-Selectable Addresses**
- **Available in a Green MSOP-10 package**

APPLICATIONS

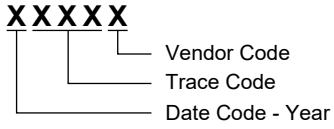
DC/DC Converters
Telecom Equipment Power Inverters
Industrial Battery Packs
Enterprise Servers
Power-over-Ethernet (PoE)

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM838	MSOP-10	-40℃ to +125℃	SGM838XMS10G/TR	SGM838 XMS10 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S 6V
Analog Inputs, IN+, IN-
Differential (V_{IN+} - V_{IN-}) ..... -40V to 40V
Common-Mode ..... -0.3V to 85V
VBUS Voltage, V_{BUS} ..... -0.3V to 85V
ALERT Voltage, V_{ALERT} ..... -0.3V to V_S + 0.3V
SDA, SCL Voltage, V_{SDA}, V_{SCL} ..... -0.3V to 6V
Input Current into Any Pin, I_{IN} 5mA
Digital Output Current, I_{OUT} 10mA
Package Thermal Resistance
MSOP-10, θ_{JA} ..... 132.4℃/W
MSOP-10, θ_{JB} ..... 79.5℃/W
MSOP-10, θ_{JC} ..... 43.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Common-Mode Input Voltage, V_{CM} ..... -0.3V to 85V
Operating Supply Voltage, V_S ..... 2.7V to 5.5V
Operating Ambient temperature, T_A ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

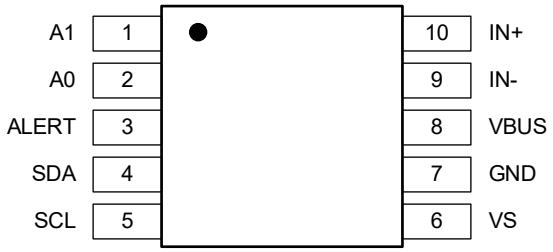
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



MSOP-10

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	A1	DI	Address Pin. Four options: GND, SCL, SDA, or VS with corresponding addresses.
2	A0	DI	Address Pin. Four options: GND, SCL, SDA, or VS with corresponding addresses.
3	ALERT	DO	Multi-Functional Alert Pin.
4	SDA	DI/DO	Data Input/Output Pin.
5	SCL	DI	Clock Input Pin.
6	VS	P	Power Supply Pin.
7	GND	G	Ground.
8	VBUS	AI	Bus Voltage Input.
9	IN-	AI	Negative Input of the Device. Connect this pin to the low-voltage side of the sense resistor when positive current flows through it.
10	IN+	AI	Positive Input of the Device. Connect this pin to the high-voltage side of the sense resistor when positive current flows through it.

NOTE: AI: analog input, DI: digital input, DO: digital output, P: power, G: ground.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV and V_{CM} = V_{IN-} = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Common-Mode Input Range	V_{CM}	T_A = -40℃ to +125℃	-0.3		85	V
Bus Voltage Input Range	V_{BUS}		0		85	V
Common-Mode Rejection	CMRR	-0.3V < V_{CM} < 85V, T_A = -40℃ to +125℃	120	145		dB
Shunt Voltage Input Range	V_{DIFF}	T_A = -40℃ to +125℃, ADCRANGE = 0	-163.84		163.84	mV
		T_A = -40℃ to +125℃, ADCRANGE = 1	-40.96		40.96	mV
Shunt Offset Voltage	V_{OS}	V_{CM} = 48V		±5	±30	μV
		V_{CM} = 0V		±5	±30	μV
Shunt Offset Voltage Drift	dV_{OS}/dT	T_A = -40℃ to +125℃		±100	±300	nV/℃
Shunt Offset Voltage vs. Power Supply	PSRR	V_S = 2.7V to 5.5V		±3.5		μV/V
VBUS Offset Voltage	V_{OS_BUS}	V_{BUS} = 200mV		±3.125	±15	mV
VBUS Offset Voltage Drift	dV_{OS}/dT	T_A = -40℃ to +125℃		50	100	μV/℃
VBUS Offset Voltage vs. Power Supply	PSRR	V_S = 2.7V to 5.5V		±1		mV/V
Input Bias Current	I_B	Either IN+ or IN- input, V_{CM} = 30V		1.5	8	nA
VBUS Pin Input Impedance	Z_{VBUS}	Active mode		1	1.2	MΩ
VBUS Pin Leakage Current	I_{VBUS}	Shutdown mode, V_{BUS} = 85V		85		μA
Input Differential Impedance	R_{DIFF}	Active mode, V_{IN+} - V_{IN-} < 164mV		284		kΩ
DC ACCURACY						
Shunt Voltage Gain Error	G_{SERR}			±0.03	±0.35	%
Shunt Voltage Gain Error Drift	G_{S_DRFT}	T_A = -40℃ to +125℃		15	35	ppm/℃
VBUS Voltage Gain Error	G_{BERR}			±0.03	±0.35	%
VBUS Voltage Gain Error Drift	G_{B_DRFT}	T_A = -40℃ to +125℃		30	80	ppm/℃
Power Total Measurement Error (TME)	P_{TME}	T_A = -40℃ to +125℃, at full scale		±0.1	±1.3	%
ADC Native Resolution				16		Bits
1 LSB Step Size		Shunt voltage, ADCRANGE = 0		5		μV
		Shunt voltage, ADCRANGE = 1		1.25		μV
		Bus voltage		3.125		mV
		Temperature		125		m℃
ADC Conversion-Time (1)	t_{CT}	Conversion time field = 0h		150		μs
		Conversion time field = 1h		150		
		Conversion time field = 2h		280		
		Conversion time field = 3h		280		
		Conversion time field = 4h		540		
		Conversion time field = 5h		1052		
		Conversion time field = 6h		2074		
		Conversion time field = 7h		4120		
Integral Non-Linearity	INL			±6		m%
Differential Non-Linearity	DNL			0.2		LSB

NOTE: Subject to oscillator accuracy and drift.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV and V_{CM} = V_{IN-} = 48V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Source						
Internal Oscillator Frequency	F_{OSC}			1.66		MHz
Internal Oscillator Frequency Tolerance	F_{OSC_TOL}	T_A = +25℃		±1	±5	%
		T_A = -40℃ to +125℃			±10	%
Temperature Sensor						
Measurement Range			-40		+125	℃
Temperature Accuracy		T_A = +25℃		±1		℃
		T_A = -40℃ to +125℃		±2		℃
Power Supply						
Supply Voltage	V_S		2.7		5.5	V
Quiescent Current	I_Q	V_{SENSE} = 0V		2000	2500	μA
		V_{SENSE} = 0V, T_A = -40℃ to +125℃			2700	μA
Quiescent Current, Shutdown	I_{QSD}	Shutdown mode		2.5	5.0	μA
Device Start-Up Time	t_{POR}	Power-up (NPOR)		462		μs
		From shutdown mode		303		
Digital Input/Output						
Logic Input Level, High	V_{IH}	SDA, SCL	1.2			V
Logic Input Level, Low	V_{IL}				0.4	V
Logic Output Level, Low	V_{OL}	I_{OL} = 3mA		0.3	0.4	V
Digital Leakage Input Current	I_{IO_LEAK}	V_{IN} = 0V to V_S		0.05	0.2	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	FAST MODE			HIGH-SPEED MODE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
I^2C Clock Frequency	f_{SCL}	1		400	10		3400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}	600			160			ns
Hold Time after a Repeated START Condition (After this period, the first clock is generated.)	t_{HDSTA}	100			100			ns
Repeated START Condition Setup Time	t_{SUSTA}	100			100			ns
STOP Condition Setup Time	t_{SUSTO}	100			100			ns
Data Hold Time	t_{HDDAT}	10		900	10		70	ns
Data Setup Time	t_{SUDAT}	100			20			ns
SCL Clock Low Period	t_{LOW}	1300			160			ns
SCL Clock High Period	t_{HIGH}	600			60			ns
Data Fall Time	t_F			300			80	ns
Clock Fall Time	t_F			300			40	ns
Clock Rise Time	t_R			300			40	ns

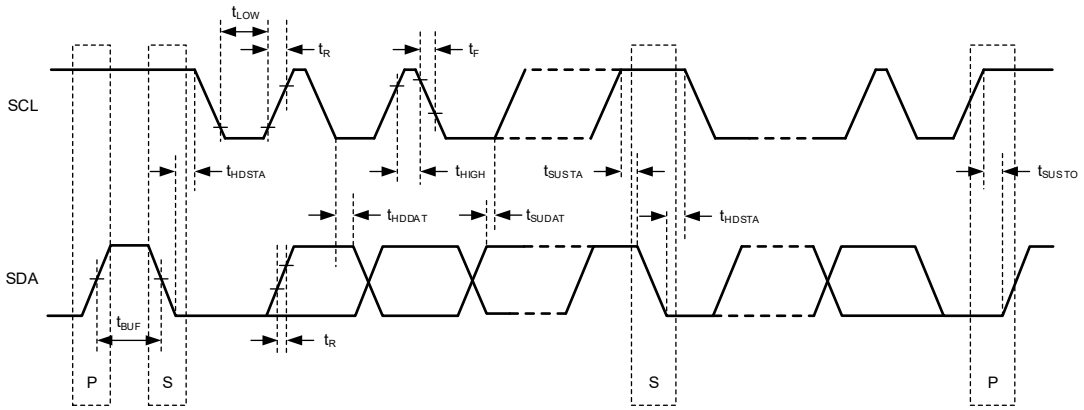
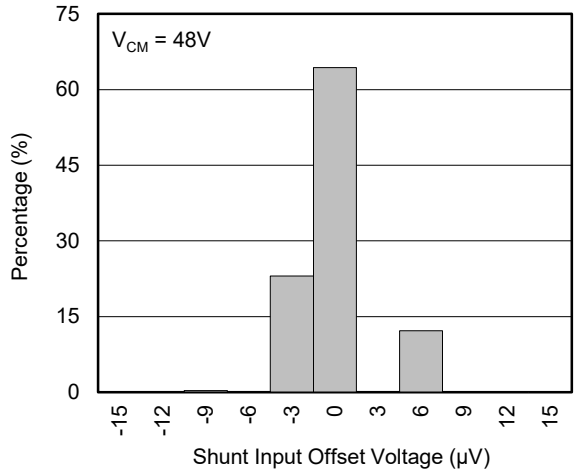


Figure 2. Bus Timing Diagram

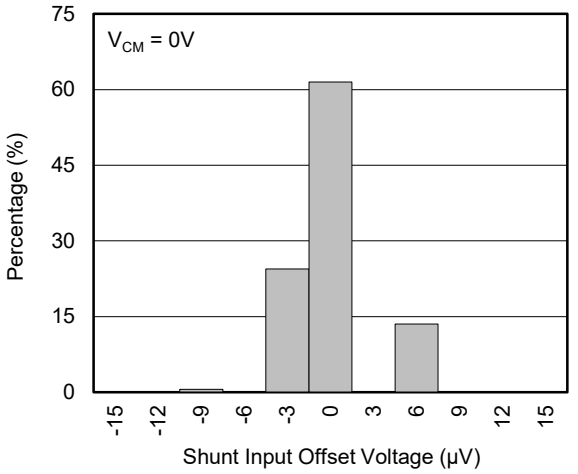
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{BUS} = 48V unless otherwise noted.

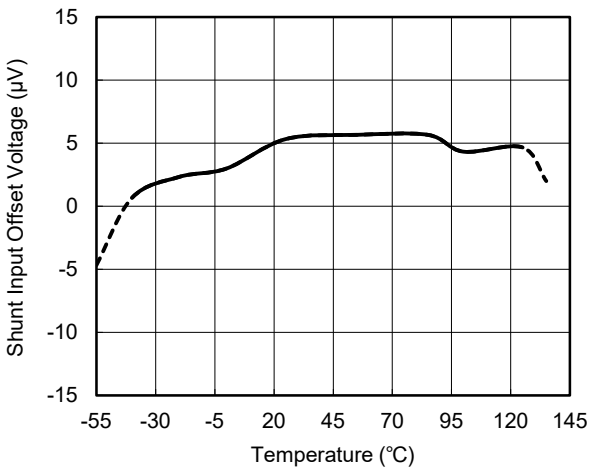
Shunt Input Offset Voltage Production Distribution



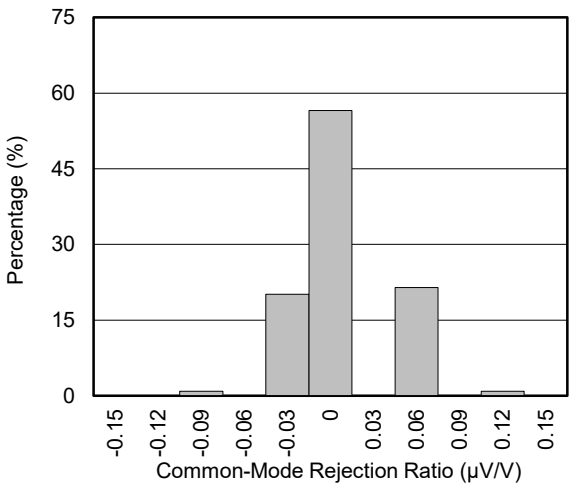
Shunt Input Offset Voltage Production Distribution



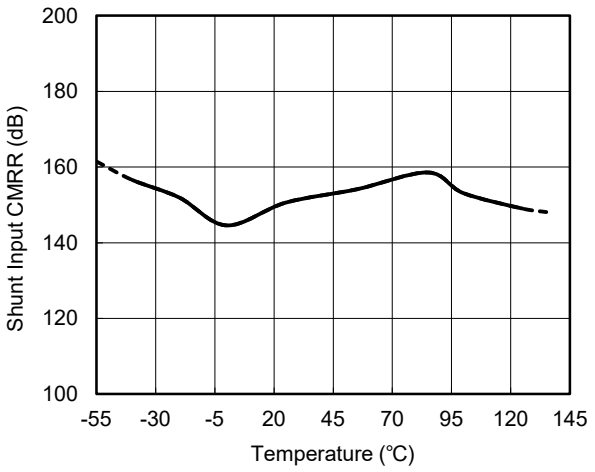
Shunt Input Offset Voltage vs. Temperature



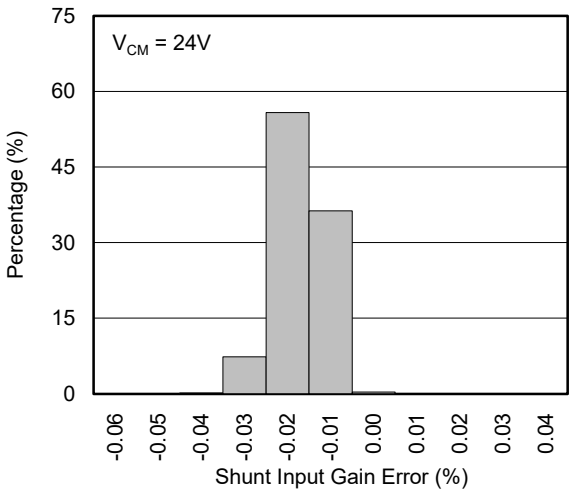
Common-Mode Rejection Ratio Production Distribution



Shunt Input Common-Mode Rejection Ratio vs. Temperature



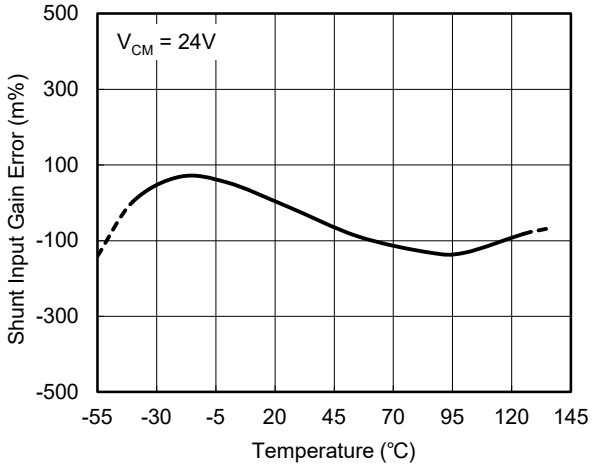
Shunt Input Gain Error Production Distribution



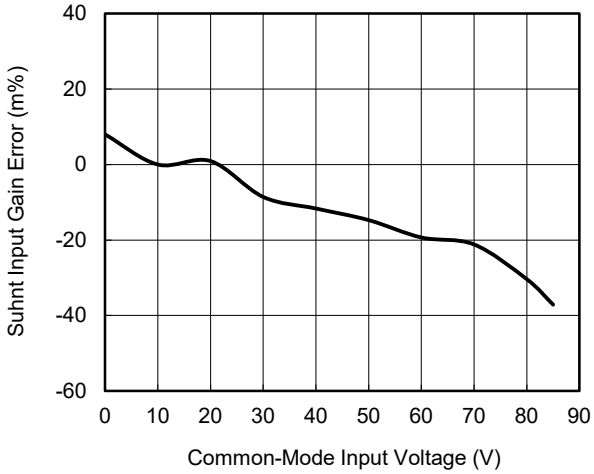
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{BUS} = 48V unless otherwise noted.

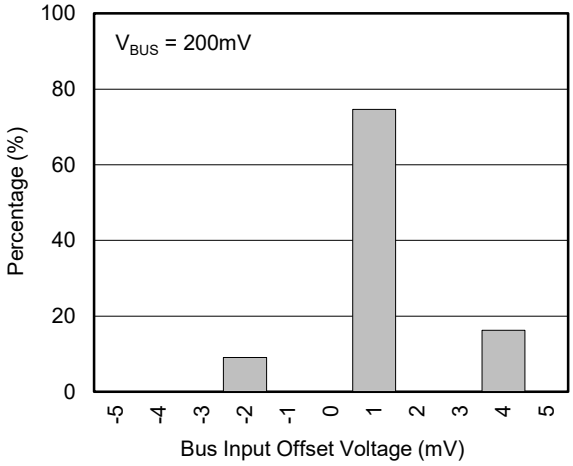
Shunt Input Gain Error vs. Temperature



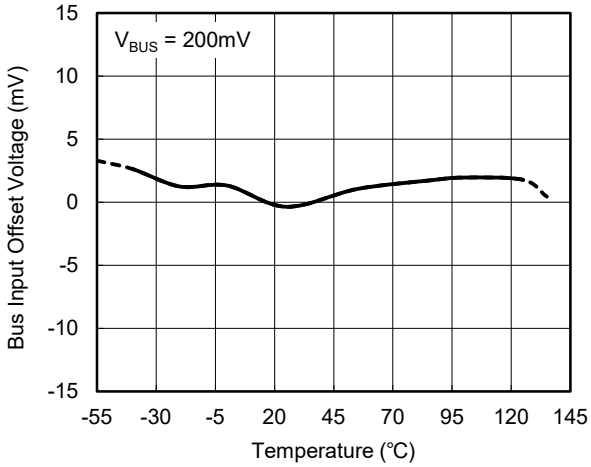
Shunt Input Gain Error vs. Common-Mode Voltage



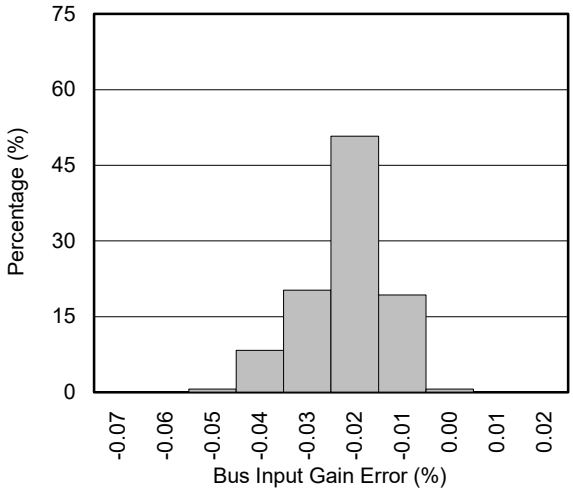
Bus Input Offset Voltage Production Distribution



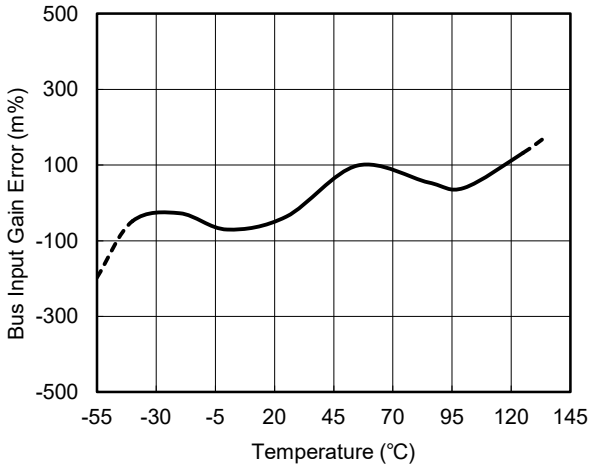
Bus Input Offset Voltage vs. Temperature



Bus Input Gain Error Production Distribution



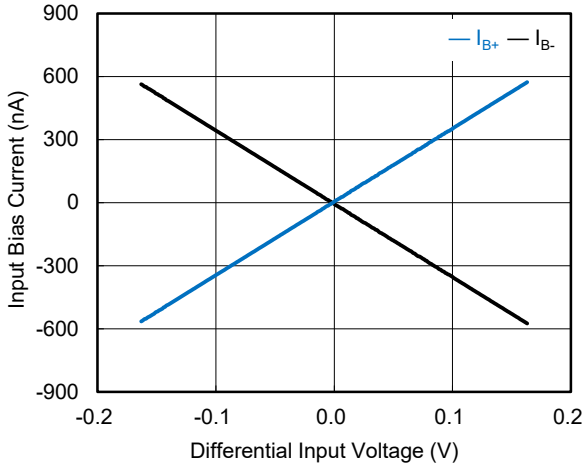
Bus Input Gain Error vs. Temperature



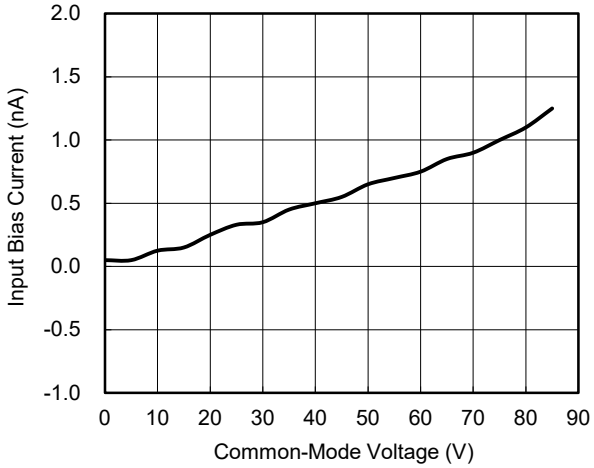
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{BUS} = 48V unless otherwise noted.

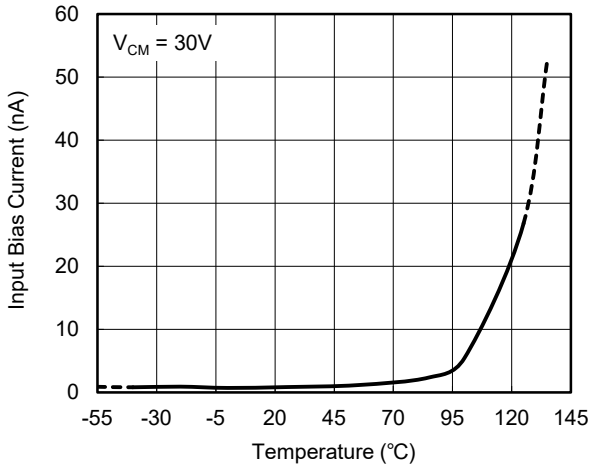
Input Bias Current vs. Differential Input Voltage



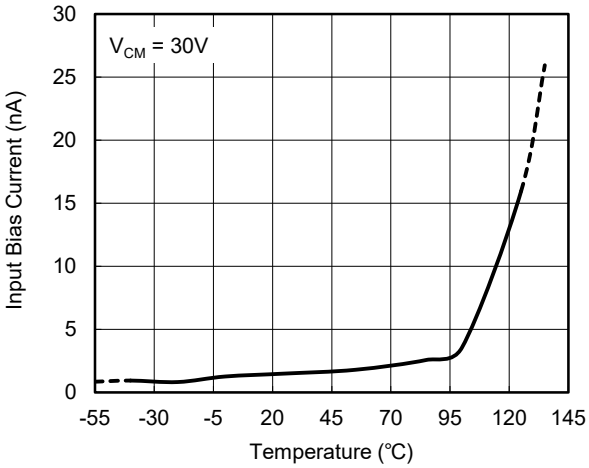
Input Bias Current (I_{B+} or I_{B-}) vs. Common-Mode Voltage



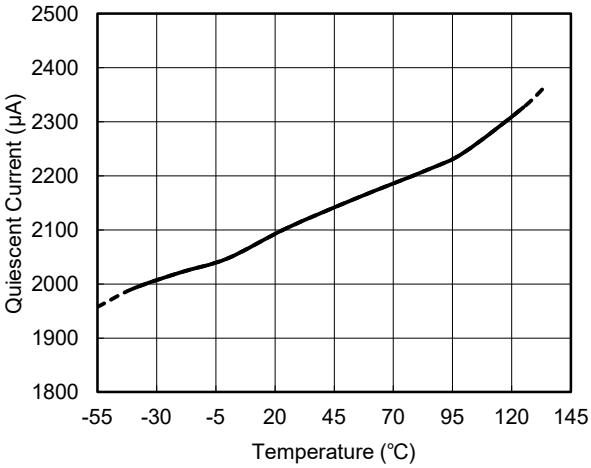
Input Bias Current vs. Temperature



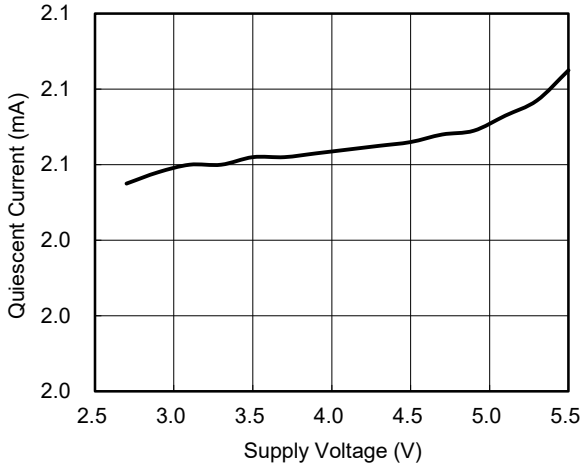
Input Bias Current vs. Temperature, Shutdown



Quiescent Current vs. Temperature



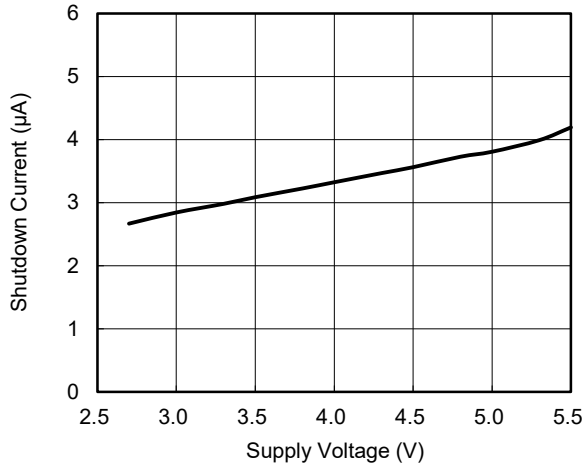
Quiescent Current vs. Supply Voltage



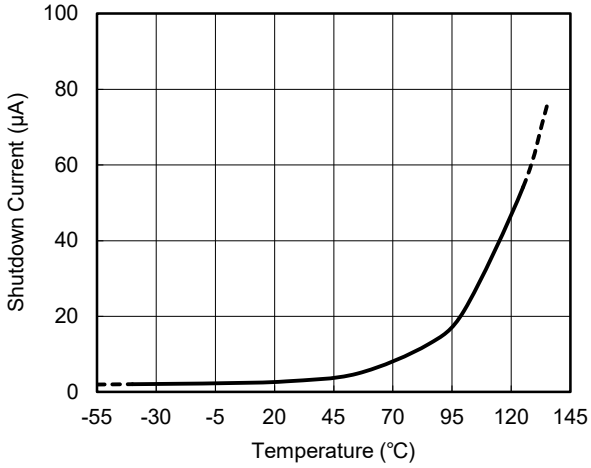
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{CM} = 48V, V_{SENSE} = 0V, and V_{BUS} = 48V unless otherwise noted.

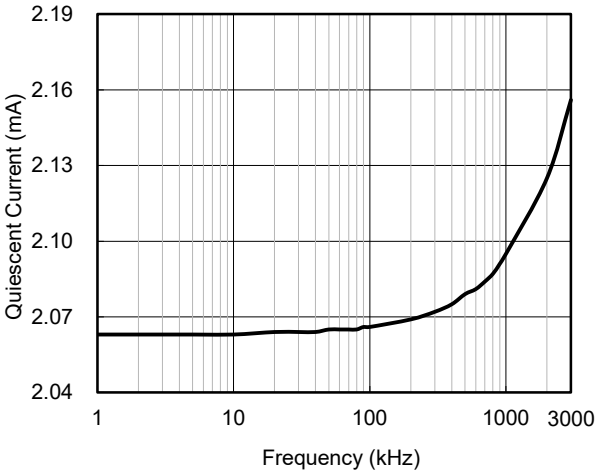
Shutdown Current vs. Supply Voltage



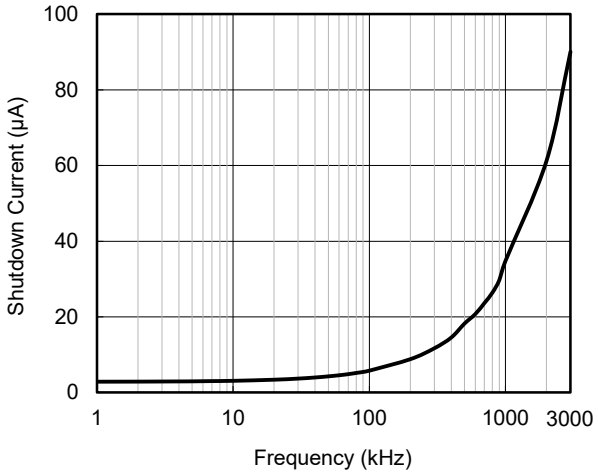
Shutdown Current vs. Temperature



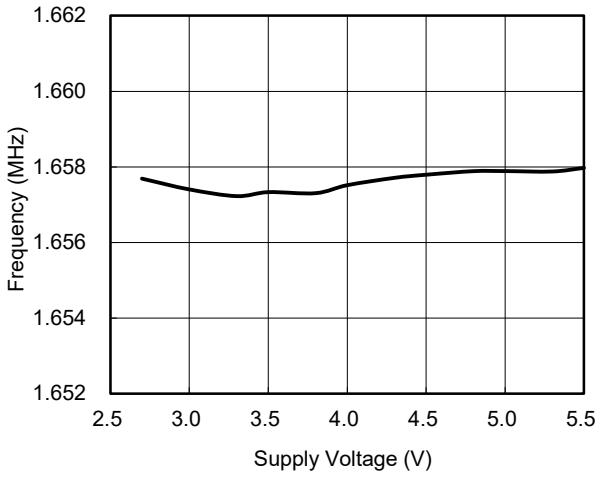
Quiescent Current vs. Clock Frequency



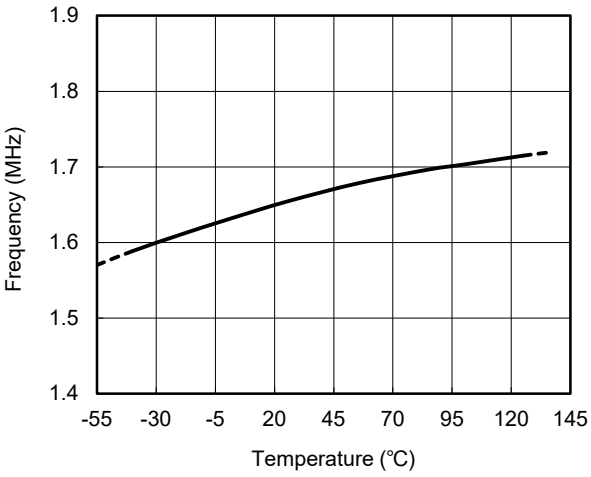
Shutdown Current vs. Clock Frequency



Internal Clock Frequency vs. Power Supply



Internal Clock Frequency vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

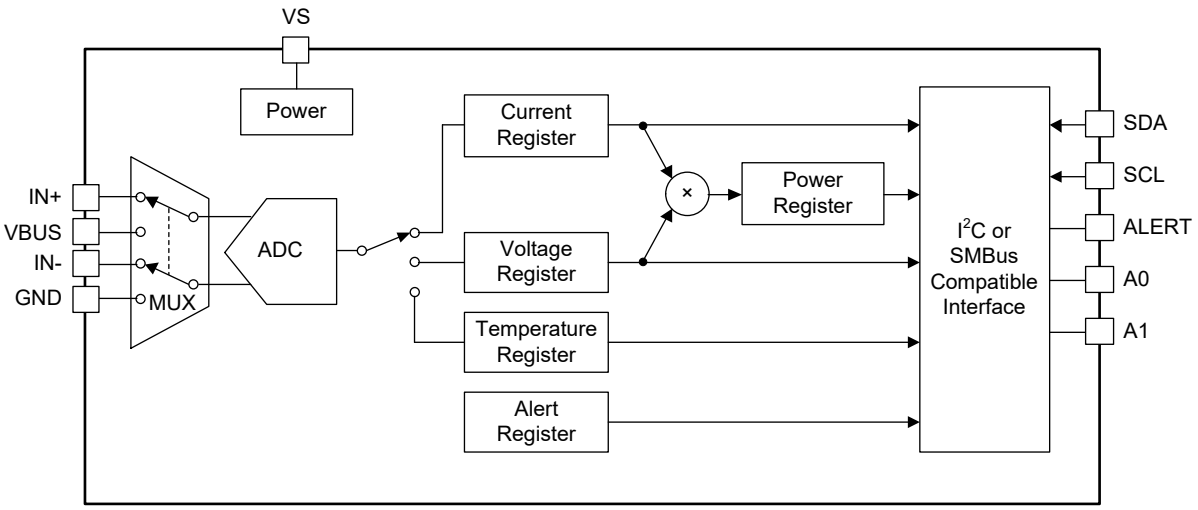


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM838 is a 16-bit ultra-precision I²C interface, current, voltage, temperature and power monitor. The device senses both shunt and bus voltages, and provides digital voltages, current, power and internal temperature readings in the data registers. In addition, it provides programmable registers to flexibly configure the device such as operating modes, conversion time, averaging times and alert functions.

Versatile High-Voltage Measurement Capability

The SGM838 measures two voltages at the input terminals, namely the voltage between the IN+ and IN- pins, and the voltage between VBUS and GND pins. Operating from 2.7V to 5.5V, the SGM838 supports current and bus voltage measurements on rails up to 85V. The SGM838's input common-mode voltage can exceed its supply voltage, as the input stage operates independently of the device power supply. The voltage monitored on the VBUS pin (typically the bus voltage) ranges from 0V to 85V. Since the power supply of the device is independent of the input voltage, the power-up sequence does not need special attention. Therefore, the bus and shunt voltages can be applied on the input pins when the device is powered off.

In typical applications, a current sense resistor (shunt resistor) is connected to the IN+ and IN- pins. When load current flows through the resistor, the shunt voltage developed is measured. The bus voltage with respect to the ground is measured by connecting to the VBUS pin. The SGM838 features a temperature sensor monitoring from -40°C to +125°C.

Figure 4 shows the multiplexed measurement scheme for shunt voltage, bus voltage and internal temperature.

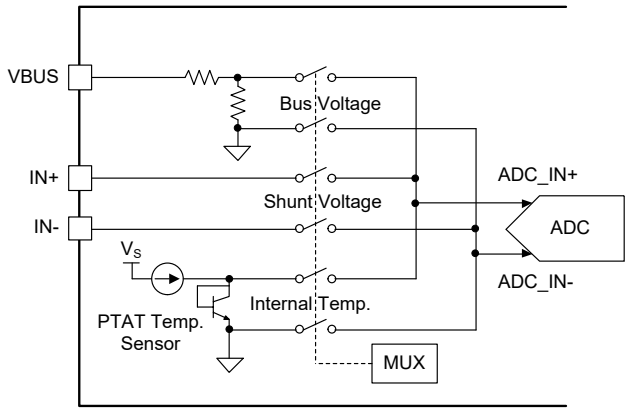
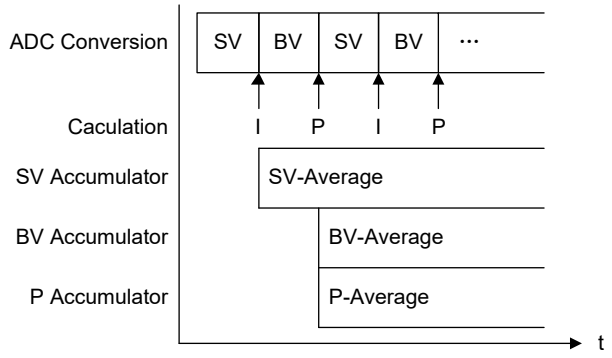


Figure 4. High-Voltage Input Multiplexer

Power Calculation

Following each shunt voltage and bus voltage measurement, the current and power are calculated, as shown in Figure 5. Following a shunt voltage measurement, the current is calculated according to the value set in the SHUNT_CAL register. If no value is written to the SHUNT_CAL register, the current value in the CURRENT register is '0'. Following a bus voltage measurement, the power is calculated based on the measured bus voltage and the calculated current value. Also, if no value is written to the SHUNT_CAL Resister, the power value in the POWER register is '0'. The current and power values are regarded as intermediate results (unless the average time is set to '1'), and are stored in an accumulator rather than the output data registers. Following each conversion sequence, the calculated current and power values are added to the previously accumulated values until the number of sequences reaches the average times. After that, the accumulated values are averaged, and the final current and power values are updated in the corresponding registers.

Similar to the current and power values, the shunt and bus voltage values are also collected and accumulated following each measurement sequence. After the number of sequences reaches the average, the accumulated values are averaged and the final shunt and bus voltage values are updated in the corresponding registers.



Note: SV: Shunt Voltage; BV: Bus Voltage; I: Current; P: Power.

Figure 5. Power Calculation Scheme

DETAILED DESCRIPTION (continued)

Low Bias Current

The SGM838 has a very low input bias current, which is beneficial for reducing power loss of the device in both active and shutdown states. Another advantage brought by low input bias current is that filters can be used at the front end of the digital current sensing amplifier, where the filters can filter out high-frequency noise and minimize the accuracy reduction. Besides, the low input bias current makes the device capable of applying a larger sensing resistor, so as to ensure the accuracy of current detection within sub-mA range. When the sensed current is zero, the input bias current of SGM838 is the smallest. When the detection current increases and the differential voltage drop on the sense resistor becomes larger, the input bias current will gradually increase.

High-Precision Sigma-Delta ADC

The SGM838 employs a sigma-delta ADC architecture enabling bidirectional current measurement at the input stage. An internal multiplexer routes measurement signals, including shunt voltage, bus voltage, and die temperature to the ADC inputs. This architecture minimizes temperature-induced drift while maintaining stable offset performance across common-mode voltage variations, temperature fluctuations, and supply disturbances, thereby maximizing dynamic range utilization.

The SGM838's MODE bits in the ADC_CONFIG register enable flexible selection of shunt voltage, bus voltage, and temperature measurement combinations to accommodate diverse applications. When averaging is set to 1, the device performs ADC conversion sequence, updates corresponding registers upon completion, and makes data readable via the digital I²C interface. Programmable measurement inputs conversion times (8 settings from 150μs to 4.12ms) are individually configurable for each input in the ADC_CONFIG register, with total conversion time depending on enabled channels and their respective timing settings. When averages exceed 1, converted values for shunt voltage, bus voltage, current, and power are stored in internal accumulators, the conversion sequence repeats until the repeat times reach the average value set in the ADC Configuration Register. Following each sequence, the measured and calculated values are added to the previously accumulated values. When the number of sequence reaches the averages, the average calculations are performed on all the accumulated values, and the final average value of shunt voltage, bus voltage, current and power are updated in the corresponding data registers which can be read. These values in the data registers remain readable until the next full conversion cycle is completed. The ongoing conversion is not affected by the data registers reading.

Continuous mode and triggered mode are two operating modes of the device. For the continuous mode, the SGM838 perpetually performs conversions and updates the respective output registers in the manner detailed above. For the triggered mode, the device is triggered to perform a single-shot measurement/ conversion by writing any of the triggered control modes to the ADC_CONFIG Register. This action controls the device to perform a single measurement/conversion. Therefore, to trigger another single conversion, the ADC Configuration Register must be written again, even though the operation mode does not change.

The device provides a conversion ready flag bit (DIAG_ALRT Register, CNVRF bit) to help coordinate one-shot or trigger conversions. The CNVRF bit is set after all the conversions, multiplication and averaging are completed.

The CNVRF bit clears under the conditions of writing to the ADC_CONFIG register (except for selecting shutdown mode) or reading the DIAG_ALRT Register.

The SGM838 enables system synchronization through its CONVDLY register bit, providing programmable conversion delays from 0ms to 510ms with 2ms resolution to align measurements with external components. The default delay setting is 0ms. Note that while the ADC's internal time base maintains high precision, extended delays may cause synchronization drift due to discrepancies between internal and external timing references.

DETAILED DESCRIPTION (continued)

Low Latency Digital Filter

An internally integrated low-pass digital filter performs decimation and noise reduction on ADC output data. This filter dynamically adjusts to varying output data rates, achieving signal settling within a single conversion cycle. Users select output conversion periods (t_{CT}) from 150μs to 4.12ms. The primary amplitude notch automatically aligns with the Nyquist frequency (f_{NOTCH} = 1/(2 × t_{CT})), causing filter cutoff frequency to scale proportionally with the output data rate. Figure 6 illustrates the response profile at t_{CT} = 1.052ms.

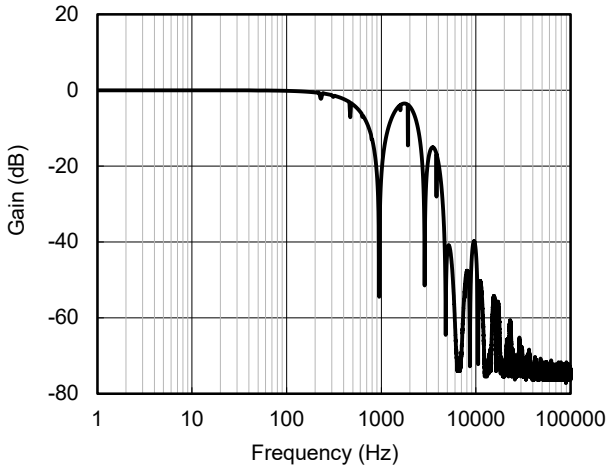


Figure 6. ADC Frequency Response

Flexible Conversion Times and Averaging

The averaging and conversion times are programmed via the ADC Configuration Register. Eight levels of conversion time from 150μs to 4.12ms are available. The programmable conversion and average times allow the device to match different time requirements in real applications. For example, if a system requires reading the shunt voltage and bus voltage every 5ms, the conversion time for shunt and bus voltage measurement can be set to 540μs, with the average time set to 4. With this configuration, the shunt and bus voltage values are updated approximately every 4.32ms. Also, the conversion time for shunt and bus voltage measurement can be different, which allows the device to focus on one of the two voltages. Suppose the system desires more conversion time for shunt voltage, a 4.12ms conversion time can be set for shunt voltage, with 540μs of conversion time for bus voltage and single conversion (average time set to '1'). With this configuration, the shunt and bus voltage values are updated approximately every 4.66ms.

There are trade-offs between the conversion times and average times used. The averaging can filter the input signal, thus effectively improving the measurement accuracy. With more average times, the device would reduce the noise of the input signal more effectively.

Similarly, the conversion time also affects the measurement accuracy. A longer conversion time results in better measurement accuracy. Therefore, to achieve the highest measurement accuracy, use the longest conversion time with the most average times, provided that the time requirements of the system are met. The impact of conversion time and averaging on an input signal is demonstrated in Figure 7 and Figure 8 below.

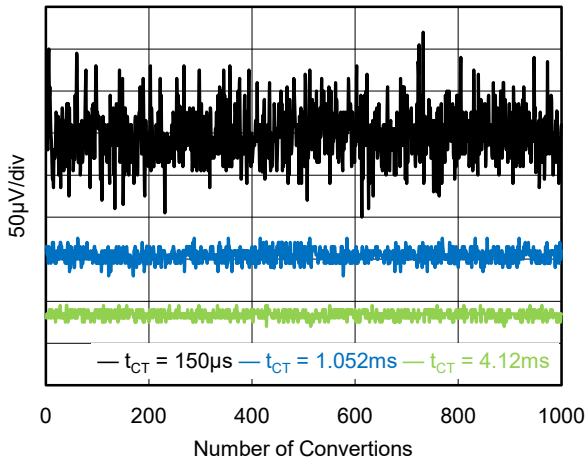


Figure 7. Noise vs. Conversion Time (Averaging = 1)

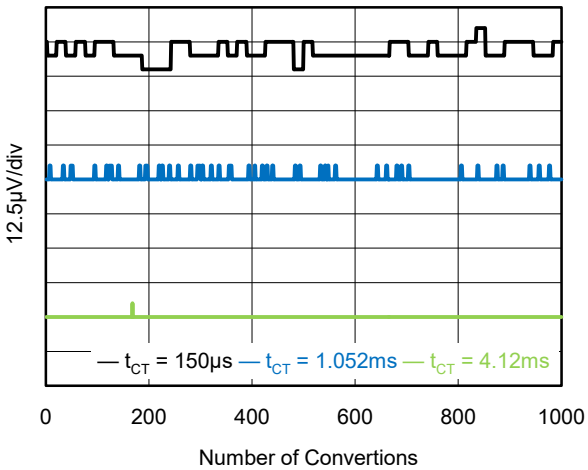


Figure 8. Noise vs. Conversion Time (Averaging = 128)

DETAILED DESCRIPTION (continued)

Multi-Alert Monitoring and Fault Detection

The SGM838 provides an open-drain alert pin to respond to one of the six available alert functions or to a conversion ready event. They are shunt voltage over-limit (SHNTOL), shunt voltage under-limit (SHNTUL), bus voltage over-limit (BUSOL), bus voltage under-limit (BUSUL), power over-limit (POL) and temperature over-limit (TMPOL). The alert functions and the conversion ready event can be enabled through the corresponding register. The SGM838 is equipped with six corresponding threshold registers for setting comparison reference values. When an alert event occurs, the ALERT pin will be asserted.

This DIAG_ALRT register provides event indication functionality for the ALERT pin, configures additional alert functionalities, and can be read to identify specific fault conditions in the system.

The device features an alert latching function, enabled by setting the ALATCH bit in the DIAG_ALRT register. This function maintains the ALERT pin in a latched asserted state after being triggered. The latched state is cleared only by reading the DIAG_ALRT register.

The ALERT pin can also be configured to monitor the conversion ready state through setting the CNVR bit of the DIAG_ALRT Register. The ALERT pin is asserted when the device has finished the previous conversions and the conversion ready flag is set.

The device implements an averaged-comparison alert function by setting the SLOWALERT bit. This feature mitigates false triggering of the ALERT pin caused by system noise by comparing averaged output data against programmed thresholds. When enabled, intrinsic processing latency occurs for fault reporting due to the averaging calculation.

The SGM838 provides configurable alert polarity. Setting the APOL bit configures the ALERT pin as active-high when asserted, and its open-drain output requires an external pull-up resistor to the supply voltage.

The DIAG_ALRT register provides non-alert functions: the MATHOF bit flags arithmetic overflow exceeding register bit width, and the MEMSTAT bit monitors non-volatile trim memory integrity (normally 1) and sets upon operational anomaly detection.

Table 1. ALERT Diagnostics Description

Diagnostic	Status Bit in DIAG_ALRT Register (R)	Out-of-Range Threshold Register (R/$\overline{W}$)	Register Default Value
Shunt Under-Voltage Limit	SHNTUL	SUVL	0x8000h (two's complement)
Shunt Over-Voltage Limit	SHNTOL	SOVL	0x7FFFh (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFFh (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0x7FF0h (two's complement)
Power Over-Limit	POL	PWR_LIMIT	0xFFFFh (two's complement, positive values only)

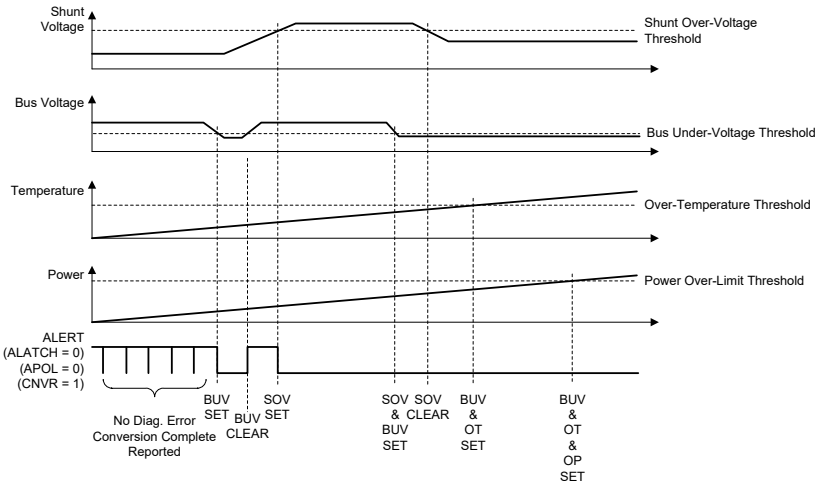


Figure 9. Multi-Alert Configuration

DETAILED DESCRIPTION (continued)

Device Functional Modes

Shutdown Mode

The SGM838 features a shutdown mode enabled through the MODE bit in the ADC_CONFIG register. In shutdown mode, the quiescent current drops below 5μA, significantly reducing power consumption. Register access via I²C remains operational during shutdown. ADC conversions resume only after reconfiguring the MODE bit to an active state. Note that the shutdown current is specified with an inactive communications bus. This current increases with rising bus frequency as shown in Shutdown Current vs. Clock Frequency curve.

Power-On Reset

The device initiates a power-on reset (POR) when the supply voltage drops below 2.17V (TYP), restoring all registers to default values. Alternatively, initiate a manual register reset by asserting the RST bit in the CONFIG register. Default register values are provided in the Register Maps section.

Bus Overview

The SGM838 provides compatibility with I^2C and SMBus interfaces. I^2C and SMBus are essentially compatible. In this manual, the I^2C interface is used as an example, and the SMBus interface will only be mentioned unless there is a difference between the SMBus interface and the I^2C interface. SCL and SDA connect the device to the bus, and SDA is open-drain connection.

The device which can send the command to the target register is called master and the device which can be controlled by the master is called slave. The master device can generate the clock signal to the slave in order to control it with SCL and SDA lines.

Send a specific address to start the slave, then the SDA signal will be pulled from high to low while SCL is still in high state. For the slaves connected to the bus, at the CLK rising edge, the slaves start to be addressed by the master, and followed by a READ or WRITE bit. For the ninth bit of the transmission signal, if SDA is pulled low, the slave acknowledges the transmission, in which case the slave is being addressed.

In one word, for the data transfer process, the initial signal will indicate a start state, and then followed by eight clock pulses and an acknowledge signal. However, the stability of SDA signal should be guaranteed when SCL is high, otherwise it will be mistaken for START or STOP mode. After the transmission completes, the signal of SDA will change from low to high when SCL is high. The device provides a 35ms timeout action logic on its interface to avoid the bus being locked up.

Serial Bus Address

For the definition of I^2C communication, before sending data, the master device should address the specified slave device. There are seven bits for the address of the slave device and another one bit is for the command of reading or writing.

A0 and A1 are used to determine the address of the device. As shown in Table 2, if these two pins are at different logic levels, the device will have different addresses. The device will sample the state of A0 and A1 pins before each communication, so it is necessary to ensure the stability of the states of A0 and A1 pins before any actions are taken on the interface.

Table 2. Address Pins and Slave Addresses

A1	A0	Slave Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

On the I^2C bus or SMBus, the SGM838 can be operated as a slave device, which is controlled by the master. When connecting to the bus, SDA is connected through the topology of open-drain. In addition, in order to improve the performance of slave devices under the condition of input spikes and noise bus, filter and Schmitt flip-flop are adopted. Although the device has integrated tip suppression in the digital I/O lines, it is recommended that proper layout be used to minimize coupling in the communication lines.

DETAILED DESCRIPTION (continued)

Noise in communication lines mainly comes from two sources: capacitive coupling generated at the signal edges between two communication lines, or switching noise generated by other parts of the system. Keeping lines parallel to ground when routing can reduce coupling effects between communication lines. In addition, note that digital I/O is susceptible to unintended noise coupling. Shielding signal lines prevents erroneous commands caused by noise.

There are two modes of transmission protocol: fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 3.4MHz). MSB is the first bit to be transferred when transmitting a byte.

Writing and Reading Operation

In order to access the specified pointer register of SGM838, it is necessary to send the values of the desired pointer register after addressing the slave device. As already illustrated in Figure 10, the values of pointer register are required after each write command.

The first byte written to a register is the address of the slave device, and R/$\overline{W}$ bit is low, then the device acknowledges receipt of a valid address. The second byte sent by the host is the address of the register to be written, which updates the register pointer to the desired register. The following two bytes are written to the register addressed by the register pointer, and the device then acknowledges receipt of each byte. Finally, the master generates a START or STOP condition to terminate data transfer (Figure 11).

If the master device desires to read the information of the specified register, a write command must be sent by the master at first to indicate which pointer register is needed. First, the slave address should be sent with the low state of R/$\overline{W}$, followed by the address of the pointer address (Figure 10). Second, the START command should be sent by the master, the slave address of the specified SGM838, and then followed with the high state of R/$\overline{W}$ to indicate a read command (Figure 12). The slave transmits the next byte, which is the most significant byte of the register indicated by the register pointer. For the condition of repeated reading, it is not required to send the bytes of pointer register again, unless the device is reset or the address of pointer register is altered by the write command.

High-Speed (HS) I²C Mode

The SGM838 also supports high-speed (HS) I²C mode whose data rate speeds up to 3.4MHz. To enable this mode, the master device sends a START condition. After the START, a master code is transmitted '00001XXX', followed by a mandatory Not Acknowledge (NACK) condition. Note that the master code is sent in fast mode or standard mode, which is at most 400kHz.

The three lowest bits of the master code are used to identify different I²C masters on the same bus. The user should guarantee that each master device has its unique identifier.

After the NACK condition, the high-speed transfer begins. At the master device side, the master device sends a REPEATED START condition followed by the slave address and the remaining data, the same as the frame in fast mode or standard mode, just at a higher speed. At the slave device side, the SGM838 switches the internal circuit to support HS mode. To keep the bus in HS mode, the user should avoid using the STOP condition and use the REPEATED START condition instead. A STOP condition makes the SGM838 switch back to support fast mode or standard mode.

SMBus Alert Response

The SGM838 has the ability to respond to the SMBus alert response that has the ability to identify a quick fault for simple slaves. The master broadcasts the alert response slave address (0001100) and the R/$\overline{W}$ bit is high. The slave that generates the ALERT signal will send its own address through the bus after recognizing the alert response. The host can identify the slave that generates the alert after receiving the slave address (Figure 13).

The alert response is similar to the I²C broadcast call, which may cause multiple slave devices to respond at the same time, and the bus arbitration rules are applied at this time. The losing device will not generate an Acknowledge but continue to pull the Alert line low until it is the device's turn to complete the Acknowledge. Cleared Alert pin asserts again until alert event removes.

DETAILED DESCRIPTION (continued)

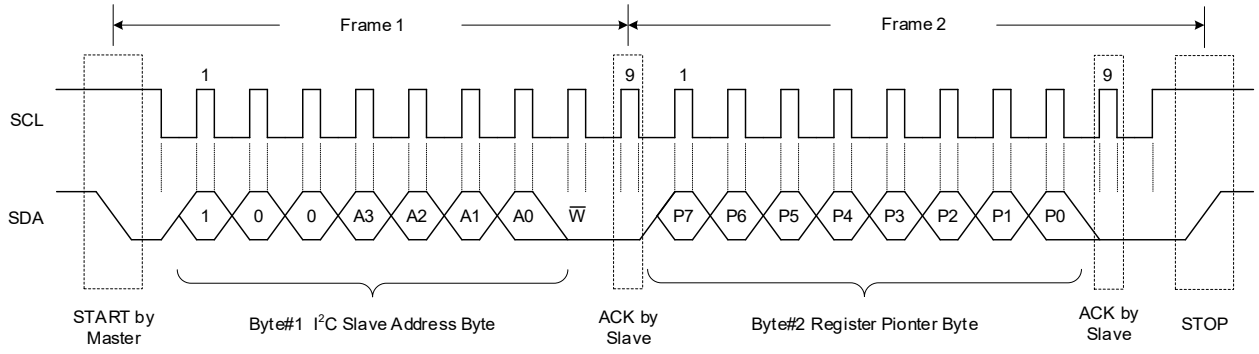
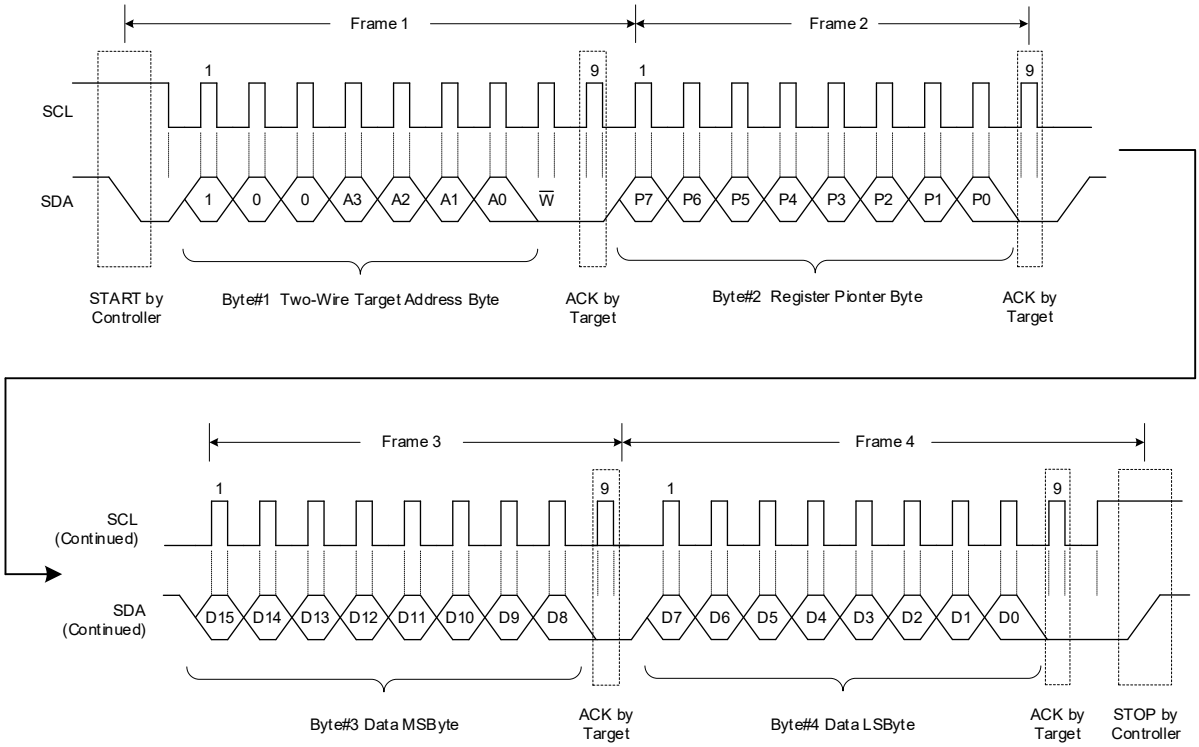


Figure 10. Typical Register Pointer Set

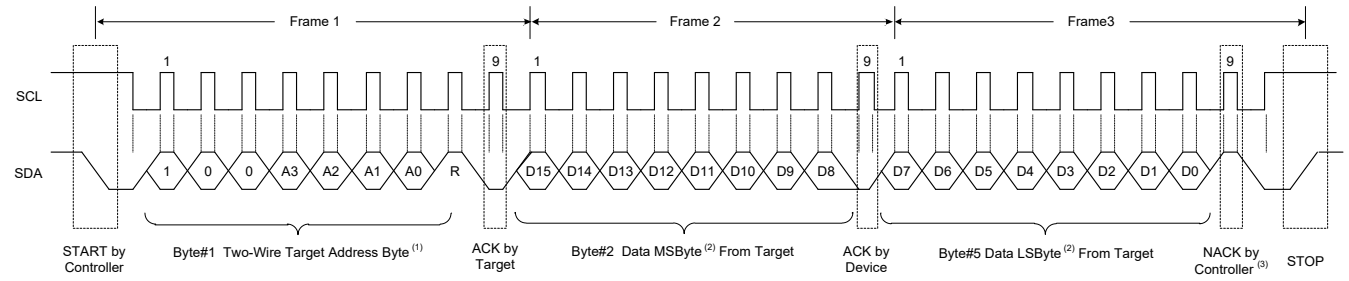


NOTES:

1. The relationship between the slave device address and pins A0 and A1 is shown in Table 2.
2. Packet error checking (PEC) and clock stretching are not supported.

Figure 11. Register Write Word Format

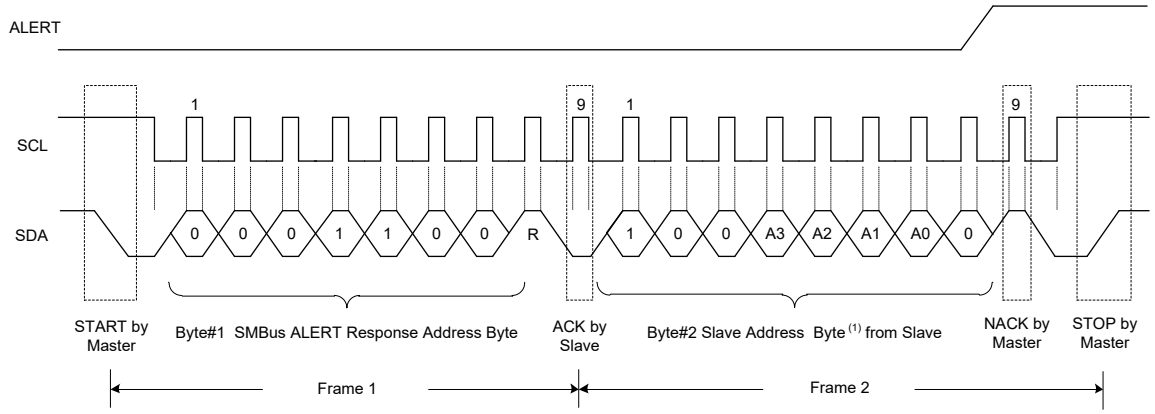
DETAILED DESCRIPTION (continued)



NOTES:

1. The relationship between the slave device address and pins A0 and A1 is shown in Table 2.
2. To read data from a new register, update the register pointer first. Otherwise, it reads from the last accessed location.
3. The master device can also sent an ACK signal.
4. Packet error checking (PEC) and clock stretching are not supported.

Figure 12. Register Read Word Format



NOTE: The relationship between the slave device address and pins A0 and A1 is shown in Table 2.

Figure 13. SMBus ALERT

REGISTER MAPS

I²C Register Set Summary

POINTER ADDRESS	REGISTER NAME	ACRONYM	REGISTER SIZE (BITS)
0h	Configuration	CONFIG	16
1h	ADC Configuration	ADC_CONFIG	16
2h	Shunt Calibration	SHUNT_CAL	16
4h	Shunt Voltage Measurement	VSHUNT	16
5h	Bus Voltage Measurement	VBUS	16
6h	Temperature Measurement	DIETEMP	16
7h	Current Result	CURRENT	16
8h	Power Result	POWER	24
Bh	Diagnostic Flags and Alert	DIAG_ALRT	16
Ch	Shunt Over-Voltage Threshold	SOVL	16
Dh	Shunt Under-Voltage Threshold	SUVL	16
Eh	Bus Over-Voltage Threshold	BOVL	16
Fh	Bus Under-Voltage Threshold	BUVL	16
10h	Temperature Over-Limit Threshold	TEMP_LIMIT	16
11h	Power Over-Limit Threshold	PWR_LIMIT	16
3Eh	General Code	GCO	16
3Fh	Device ID	DEVICE_ID	16

NOTES:

1. Type: R = Read-Only, R/W = Read/Write. -n: Value after reset or the default value

0h: Configuration (CONFIG) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RST	0h	R/W	Reset Bit. Writing 1 to this bit initiates a manual system reset and resets all registers to default values. 0h = Normal Operation 1h = All registers reset to default values. This bit self-clears.
D[14]	RESERVED	0h	R	Reserved.
D[13:6]	CONVDLY	0h	R/W	Set the Delay for initial ADC conversion in steps of 2ms. 0h = 0ms 1h = 2ms FFh = 510ms
D[5]	RESERVED	0h	R	Reserved.
D[4]	ADCRANGE	0h	R/W	Shunt Full Scale Range Selection across IN+ and IN- Pins. 0h = ±163.84mV 1h = ± 40.96mV
D[3:0]	RESERVED	0h	R	Reserved.

REGISTER MAPS (continued)

1h: ADC Configuration (ADC_CONFIG) Register [reset = FB68h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:12]	MODE	Fh	R/W	Mode Selection Bits. 0h = Shutdown 1h = Bus voltage, single shot 2h = Shunt voltage, single shot 3h = Shunt voltage and bus voltage, single shot 4h = Temperature, single shot 5h = Temperature and bus voltage, single shot 6h = Temperature and shunt voltage, single shot 7h = Bus voltage, shunt voltage and temperature, single shot 8h = Shutdown 9h = Bus voltage only, continuous Ah = Shunt voltage only, continuous Bh = Shunt and bus voltage, continuous Ch = Temperature only, continuous Dh = Bus voltage and temperature, continuous Eh = Temperature and shunt voltage, continuous Fh = Bus voltage, shunt voltage and temperature, continuous
D[11:9]	VBUSCT	5h	R/W	Bus Voltage Conversion Time Setting Bits. 0h = 150μs 1h = 150μs 2h = 280μs 3h = 280μs 4h = 540μs 5h = 1052μs 6h = 2074μs 7h = 4120μs
D[8:6]	VSHCT	5h	R/W	Shunt Voltage Conversion Time Setting Bits. 0h = 150μs 1h = 150μs 2h = 280μs 3h = 280μs 4h = 540μs 5h = 1052μs 6h = 2074μs 7h = 4120μs
D[5:3]	VTCT	5h	R/W	Temperature Conversion Time Setting Bits. 0h = 150μs 1h = 150μs 2h = 280μs 3h = 280μs 4h = 540μs 5h = 1052μs 6h = 2074μs 7h = 4120μs
D[2:0]	AVG	0h	R/W	ADC Sample Averaging Count Selection Bits. Set the ADC sample averaging count for all active inputs. If the count is greater than 0h, output registers update after averaging completes. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

REGISTER MAPS (continued)

2h: Shunt Calibration (SHUNT_CAL) Register [reset = 1000h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RESERVED	0h	R	Reserved.
D[14:0]	SHUNT_CAL	1000h	R/W	The register sets a conversion constant for the shunt resistance, used to calculate the current in amperes and determine the resolution of the CURRENT register.

4h: Shunt Voltage Measurement (VSHUNT) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	VSHUNT	0h	R	Differential Voltage Measured Across the Shunt Output. Two's complement value. Conversion factor: 5μV/LSB when ADCRANGE = 0 1.25μV/LSB when ADCRANGE = 1

5h: Bus Voltage Measurement (VBUS) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	VBUS	0h	R	Bus Voltage Output. Two's complement value, however always positive. Conversion factor: 3.125mV/LSB

6h: Temperature Measurement (DIETEMP) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	DIETEMP	0h	R	Internal Die Temperature Measurement. Two's complement value. Conversion factor: 125 m℃/LSB
D[14:0]	RESERVED	0h	R	Reserved. Always reads 0.

7h: Current Result (CURRENT) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	CURRENT	0h	R	Calculated Current Output in Amperes. Two's complement value.

8h: Power Result (POWER) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[23:0]	POWER	0h	R	Calculated Power Output in Watts. Unsigned representation. Always positive.

REGISTER MAPS (continued)

Bh: Diagnostic Flags and Alert (DIAG_ALRT) Register [reset = 0001h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	ALATCH	0h	R/W	0h = Transparent Mode The ALERT pin and flag bit return to idle once the fault is cleared. 1h = Latched Mode The ALERT pin and flag bit stay active after a fault until the DIAG_ALRT Register is read.
D[14]	CNVR	0h	R/W	Setting this bit to 1 enables the conversion-ready alert function. The ALERT pin is set high upon completion of a conversion cycle. 0h = Disable conversion ready flag on ALERT pin 1h = Enable conversion ready flag on ALERT pin
D[13]	SLOWALERT	0h	R/W	When enabled, the ALERT function triggers after the averaged value is completed, allowing for delayed alerting. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
D[12]	APOL	0h	R/W	Alert Pin Polarity Setting Bit. 0h = Normal (Active-low, open-drain) 1h = Inverted (active-high, open-drain)
D[11:10]	RESERVED	0h	R	Reserved.
D[9]	MATHOF	0h	R	Read 1 if an arithmetic operation resulted in an overflow error, indicating invalid current and power data. 0h = Normal 1h = Overflow Manually cleared by triggering the next conversion.
D[8]	RESERVED	0h	R	Reserved.
D[7]	TMPOL	0h	R	Read 1 if the measured temperature is higher than the threshold limit in the TEMP_LIMIT register. 0h = Normal 1h = Over-Temperature Event When ALATCH = 1, this bit is cleared by reading this register.
D[6]	SHNTOL	0h	R	Read 1 if the measured shunt voltage is higher than the threshold limit in the SOVL register. 0h = Normal 1h = Over Shunt Voltage Event This bit will be cleared by reading this register if ALATCH = 1.
D[5]	SHNTUL	0h	R	Read 1 if the measured shunt voltage is lower than the threshold limit in the SUVL register. 0h = Normal 1h = Shunt Under-Limit Event This bit will be cleared by reading this register if ALATCH = 1.
D[4]	BUSOL	0h	R	Read 1 if the measured bus voltage is higher than the threshold limit in the BOVL register. 0h = Normal 1h = Bus Over-Limit Event This bit will be cleared by reading this register if ALATCH = 1.
D[3]	BUSUL	0h	R	Read 1 if the measured bus voltage is lower than the threshold limit in the BUVL register. 0h = Normal 1h = Bus Under-Limit Event This bit will be cleared by reading this register if ALATCH = 1.
D[2]	POL	0h	R	Read 1 if the measured power is higher than the threshold limit in the PWR_LIMIT register. 0h = Normal 1h = Power Over-Limit Event This bit will be cleared by reading this register if ALATCH = 1.
D[1]	CNVRF	0h	R	Read 1 if the conversion is completed. 0h = Normal 1h = Conversion is completed If ALATCH = 1, clear this bit via register read or new conversion trigger.
D[0]	MEMSTAT	1h	R	Read 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

REGISTER MAPS (continued)

Ch: Shunt Over-Voltage Threshold (SOVL) Register [reset = 7FFFh]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	SOVL	7FFFh	R/W	Shunt over-voltage (over-current protection) threshold value in two's complement. Conversion Factor: 5μV/LSB when ADCRANGE = 0 1.25μV/LSB when ADCRANGE = 1.

Dh: Shunt Under-Voltage Threshold (SUVL) Register [reset = 8000h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	SUVL	8000h	R/W	Shunt under-voltage (under-current protection) threshold value in two's complement. Conversion Factor: 5μV/LSB when ADCRANGE = 0, 1.25μV/LSB when ADCRANGE = 1.

Eh: Bus Over-Voltage Threshold (BOVL) Register [reset = 7FFFh]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RESERVED	0h	R	Reserved. Always reads 0.
D[14:0]	BOVL	7FFFh	R/W	Bus over-voltage (over-voltage protection) threshold value in unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

Fh: Bus Under-Voltage Threshold (BUVL) Register [reset = 0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RESERVED	0h	R	Reserved. Always reads 0.
D[14:0]	BUVL	0h	R/W	Bus under-voltage (under-voltage protection) threshold value in unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

10h: Temperature Over-Limit Threshold (TEMP_LIMIT) Register [reset = 7FF0h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:4]	TOL	7FFh	R/W	Over-temperature threshold value in two's complement. The value in this field is compared directly with the DIETEMP register value to identify whether the temperature exceeds its limit. Conversion factor: 125m℃/LSB.
D[3:0]	RESERVED	0h	R	Reserved, always reads 0.

11h: Power Over-Limit Threshold (PWR_LIMIT) Register [reset = FFFFh]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	POL	FFFFh	R/W	Power over-limit threshold value Setting Bits. Unsigned representation, positive value only. The value in this field is compared directly with the POWER register value to identify whether the power exceeds its limit. Conversion factor: 256 × Power LSB.

3Eh: General Code (GCO) Register [reset = 5449h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	MANFID	5449h	R	General Code Bits, Fixed Value.

3Fh: Device ID (DEVICE_ID) Register [reset = 2381h]

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:4]	DIEID	238h	R	Device ID Bits.
D[3:0]	REV_ID	1h	R	Device Revision ID Bits.

APPLICATION INFORMATION

Device Measurement Range and Resolution

The current-sense amplifier provides two configurable shunt voltage measurement ranges: ±163.84mV and ±40.96mV. Selection between these ranges is accomplished by setting the ADCRANGE bit in the CONFIG register to match specific current-sensing requirements. Integrated monitoring capabilities include bus voltage measurement across 0V to 85V and on-die temperature sensing from -40℃ to +125℃. All measurement ranges, resolution steps, and accuracy specifications are described in Table 3.

Table 3. ADC Full Scale Values

Parameter	Full Scale Value	Resolution
Shunt Voltage	±163.84mV (ADCRANGE = 0)	5μV/LSB
	±40.96mV (ADCRANGE = 1)	1.25μV/LSB
Bus Voltage	0V to 85V	3.125mV/LSB
Temperature	-40℃ to +125℃	125m℃/LSB

The device provides dedicated read-only measurement registers: VSHUNT for shunt voltage, VBUS for bus voltage, and DIETEMP for die temperature. VSHUNT and VBUS are 16-bit registers, while DIETEMP delivers valid data only in its higher 12 bits.

Both VSHUNT and DIETEMP may return negative values, indicating reverse current flow and sub-zero temperatures respectively. Measured values are calculated by multiplying register readings by their parameter-specific LSB resolutions.

Current and Power Calculations

The SGM838 does not need to measure current and power directly, it realizes the calculation of current and power by measuring the differential voltage between IN+ and IN- pins and the voltage on VBUS pin. To obtain the correct current and power values, users need to program the resolution of the CURRENT Register (CURRENT_LSB) and the value of the sampling resistor applied between the IN+ and IN- pins. The SHUNT_CAL register provides a calibration coefficient to enable the CURRENT register to output accurate current measurements. The determination of the SHUNT_CAL Register value requires the value of Current_LSB and the sampling resistor as shown in Equation 1.

$$SHUNT\_CAL = 819.2 \times 10^6 \times CURRENT\_LSB \times R_{SHUNT} \quad (1)$$

Note that the value of SHUNT_CAL must be multiplied by 4 for ADCRANGE = 1.

Users can convert the value in CURRENT Register to the actual current value in amperes through Current_LSB. According to Equation 2, the minimum Current_LSB can be obtained to realize the highest resolution of the CURRENT Register, which needs to determine an estimated maximum current first. In order to simplify the calculation process of converting the CURRENT Register and POWER Register into the corresponding amperes and watts, the smallest Current_LSB is generally rounded up to an integer (no higher than 8x) .

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

The device calculates current by applying the calibration coefficient from the SHUNT_CAL register to the measured shunt voltage value read from the VSHUNT register. This computed current value populates the CURRENT register and is scaled to the final measured current through multiplication with the Current_LSB parameter by using Equation 3:

$$Current\ (A) = CURRENT\_LSB \times CURRENT \quad (3)$$

The system power is determined by multiplying the POWER register value by the Current_LSB, then multiplying the product by a fixed scaling factor of 0.2, as defined by Equation 4:

$$Power\ (W) = 0.2 \times CURRENT\_LSB \times POWER \quad (4)$$

ADC Output Data Rate and Noise Performance

The noise performance and effective resolution of the SGM838 are determined by the ADC's conversion time and averaging configuration. There are trade-offs between the conversion times and average times used. The averaging can filter the input signal, thus effectively improving the measurement accuracy. With more average times, the device would reduce the noise of the input signal more effectively. Similarly, the conversion time also affects the measurement accuracy. A longer conversion time results in better measurement accuracy. Therefore, to achieve the highest measurement accuracy, use the longest conversion time with the most average times, provided that the time requirements of the system are met.

APPLICATION INFORMATION (continued)

Table 4 presents the typical effective number of bits (ENOB) for the SGM838 across various conversion time and averaging configurations, where ENOB is calculated from peak-to-peak noise measurements.

Table 4. Noise Performance

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (±163.84mV) (ADCRANGE = 0)	Noise-Free ENOB (±40.96mV) (ADCRANGE = 1)
150	1	0.15	10.48	8.31
150		0.15	10.48	8.31
280		0.28	11.68	9.68
280		0.28	11.68	9.68
540		0.54	12.42	10.33
1052		1.052	12.68	10.83
2074		2.074	13.42	11.14
4120		4.12	14.00	11.61
150	4	0.6	11.54	9.73
150		0.6	11.54	9.73
280		1.12	12.54	10.61
280		1.12	12.54	10.61
540		2.16	13.19	11.05
1052		4.208	14.00	11.61
2074		8.296	14.42	12.19
4120		16.48	14.42	13.00
150	16	2.4	12.54	10.71
150		2.4	12.54	10.71
280		4.48	14.00	11.68
280		4.48	14.00	11.68
540		8.64	14.42	12.30
1052		16.832	15.00	12.68
2074		33.184	15.00	13.00
4120		65.92	16.00	13.68
150	64	9.6	13.68	11.61
150		9.6	13.68	11.61
280		17.92	15.00	12.68
280		17.92	15.00	12.68
540		34.56	16.00	13.19
1052		67.328	16.00	13.68
2074		132.736	16.00	14.00
4120		263.68	16.00	15.00

APPLICATION INFORMATION (continued)

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (±163.84mV) (ADCRANGE = 0)	Noise-Free ENOB (±40.96mV) (ADCRANGE = 1)
150	128	19.2	14.42	12.09
150		19.2	14.42	12.09
280		35.84	16.00	13.19
280		35.84	16.00	13.19
540		69.12	16.00	13.68
1052		134.656	16.00	14.00
2074		265.472	16.00	14.42
4120		527.36	16.00	15.00
150	256	38.4	15.00	12.68
150		38.4	15.00	12.68
280		71.68	16.00	13.68
280		71.68	16.00	13.68
540		138.24	16.00	14.00
1052		269.312	16.00	15.00
2074		530.944	16.00	15.00
4120		1054.72	16.00	15.00
150	512	76.8	16.00	13.19
150		76.8	16.00	13.19
280		143.36	16.00	14.00
280		143.36	16.00	14.00
540		276.48	16.00	15.00
1052		538.624	16.00	15.00
2074		1061.888	16.00	16.00
4120		2109.44	16.00	16.00
150	1024	153.6	16.00	13.68
150		153.6	16.00	13.68
280		286.72	16.00	14.42
280		286.72	16.00	14.42
540		552.96	16.00	15.00
1052		1077.248	16.00	16.00
2074		2123.776	16.00	16.00
4120		4218.88	16.00	16.00

APPLICATION INFORMATION (continued)

Input Filtering Considerations

In real applications, the current measurement usually introduces undesirable noise. The SGM838 provides different noise filtering capabilities by configuring the conversion and average times independently in the ADC_CONFIG Register. The conversion time for shunt and bus voltage can be set independently, while the average times are the same.

The ADC of SGM838 is a sigma-delta (Σ-Δ) structure with typical sampling rates of 1.66MHz. The sigma-delta structure has good noise suppression capability. However, if there are transients at or near the sampling frequency (greater than 3.32MHz), it will affect the measurement accuracy which needs to be handled. By placing low-value resistors in series with a ceramic capacitor at the IN+ and IN- pins, these high-frequency signals can be effectively filtered. Figure 14 shows the filter setup, where the recommended resistor value is less than 100Ω and the recommended capacitor value is between 0.1μF and 1μF. Both resistor values should be consistent to avoid offset due to I_{BIAS}.

Besides the transients, the input overload conditions should also be well addressed. The inputs of the device can tolerate ±40V differential voltage. During a load short-circuit, the load current flows, and the shunt resistor increases sharply. When the short-circuit fault is removed, the parasitic inductance in the power loop could induce kickback voltages on the inputs which may exceed the voltage ratings. Such kickback voltages can be well suppressed using zener-type devices.

In some applications, an over-stress condition may occur as a result of an excessive dV/dt caused by event such as input hard short. The over-stress occurs due to the activation of the internal ESD protection with large available currents. The test results show that adding the 100Ω resistors at the inputs can sufficiently protect the devices from dV/dt induced fault event.

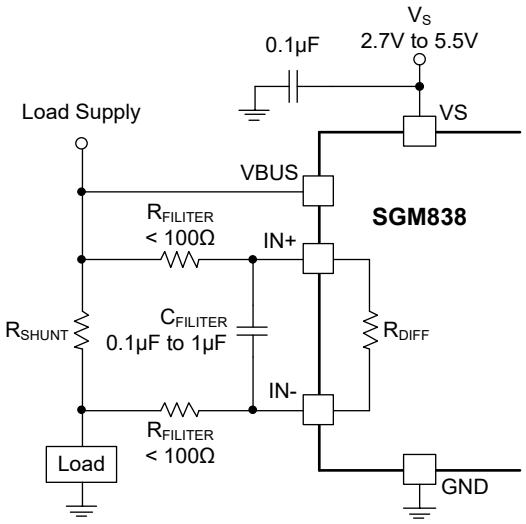


Figure 14. Input Filtering

Typical Application

The SGM838 features low offset voltage and low input bias current, enabling accurate current measurements over a wide range. The differential input voltage range can be freely configured to ±163.84mV or ±40.96mV. Since the device can monitor the shunt voltages, bus voltages and die temperature, the current in amperes and power in watts readings can be directly obtained through the internal multiplier by setting the correct calibration value, conversion time and average mode.

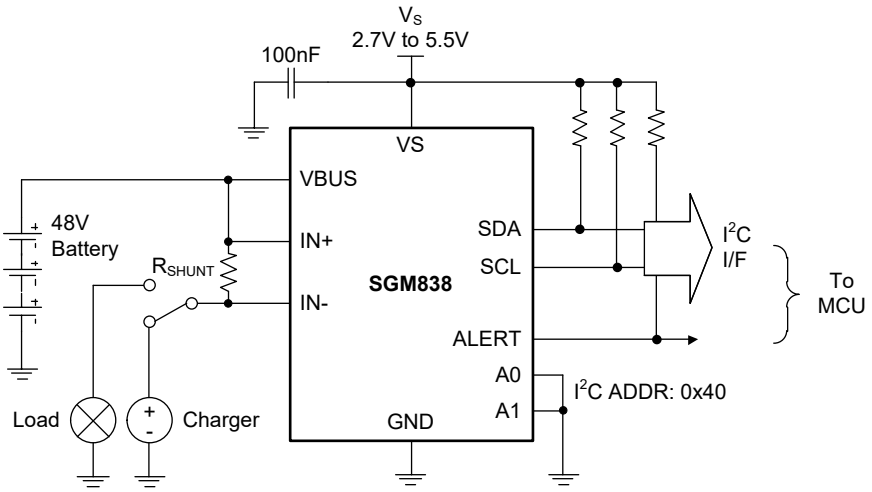


Figure 15. High-Side Sensing Application Diagram

APPLICATION INFORMATION (continued)

Design Requirements

The SGM838 characterizes current by the voltage drop across the shunt resistor. The device can also measure the bus voltage, and then calculate the corresponding power by programming the SHUNT_CAL Register. It has a programmable alert function, which can respond to user-defined fault or conversion completion events. In addition, users can also customize the specific threshold that triggers alert. Table 5 lists the design requirements for the SGM838.

Table 5. Design Parameters

Design Parameter	Example Value
Power Supply Voltage (V_S)	5V
Bus Supply Rail (V_{CM})	48V
Bus Supply Rail Over-Voltage Fault Threshold	52V
Average Current	6A
Over-Current Fault Threshold (I_{MAX})	10A
ADC Range Selection (V_{SENSE_MAX})	±163.84mV
Temperature	+25℃

Select the Shunt Resistor

Based on the above design requirements, the ADC's maximum range of ±163.84mV is selected. The shunt resistor (R_{SHUNT}) selection requires consideration of the maximum current (I_{MAX}) and the maximum shunt voltage (V_{SENSE_MAX}). During device operation at maximum current, the sense voltage must be kept below the full-scale voltage V_{SENSE_MAX}. The maximum allowable value for R_{SHUNT} is calculated using Equation 5, yielding a maximum value of 16.38mΩ. A standard resistance value of 16.2mΩ is selected as the sense resistor value.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (5)$$

Configure the Device

The device resets all registers to their default values upon every power-up. Therefore, the registers must be configured correctly during the initial power-up sequence. In the default state, the device continuously converts the shunt voltage, bus voltage, and die temperature according to the default settings. Registers can be configured as needed.

Program the Shunt Calibration Register

To ensure accurate current measurement, first calculate the current LSB (CURRENT_LSB) using Equation 2. With a maximum expected current of 10A, this yields a CURRENT_LSB of 305.1758μA/bit. The SHUNT_CAL register is then set to 4050d (FD2h) based on the CURRENT_LSB value and the selected R_{SHUNT} resistance.

Set Desired Fault Thresholds

The device provides six types of fault detection. Setting the threshold levels requires configuration of the corresponding registers. With the over-current fault threshold specified as 10A and the R_{SHUNT} resistance of 16.2mΩ, the maximum shunt voltage is calculated as 162mV. This threshold voltage determines the required setting for the shunt over-voltage limit (SOVL) register. Based on the shunt voltage register LSB of 5μV, the value for the SOVL register is calculated as: 162mV/5μV = 32400d (7E90h).

Configuring the bus over-voltage limit (BOVL) register is required for bus over-voltage fault detection. Based on the bus voltage threshold of 52V and the LSB of the bus fault limit register (3.125mV), the BOVL register setting is calculated as: 52V/3.125mV = 16640d (4100h).

When setting the power threshold, note that the Power Over-Limit Threshold register is 16 bits wide while the Power Result register is 24 bits. Consequently, the effective LSB required for the Power Over-Limit Threshold register calculation is 256 times the LSB of the Power Result register.

Calculate Returned Values

To obtain the actual parameter value, multiply the register reading by its corresponding LSB. Table 6 provides the register return values in decimal format.

Table 6. Calculating Returned Values

Parameter	Returned Value	LSB Value	Calculated Value
Shunt Voltage (V)	19440d	5μV/LSB	0.0972V
Current (A)	19660d	$10A/2^{15}$ = 305.176μA/LSB	5.9997A
Bus Voltage (V)	15360d	3.125mV/LSB	48V
Power (W)	4718604d	Current_LSB × 0.2 = 61.035156μW/LSB	288W
Temperature (℃)	200d	125m℃/LSB	+25℃

The readings for shunt voltage, current, bus voltage (positive values only), and die temperature are returned in two's complement format. A value is negative when its most significant bit (MSB) is 1, and is positive when the MSB is 0. To interpret negative values: first complement (invert) all bits of the reading, then add 1 to the result. Convert this resulting unsigned binary number to decimal and assign a negative sign.

APPLICATION INFORMATION (continued)

For example, a shunt voltage reading of 1011 0100 0001 0000 has MSB = 1 indicating a negative value. After complementing all bits (0100 1011 1110 1111) and adding 1 (0100 1011 1111 0000), the decimal equivalent is 19440. Applying the negative sign yields -19440 as the raw register value. Multiplying by the Shunt Voltage LSB (5μV) gives -97.2mV as the actual voltage measurement.

Application Curves

Figure 16 and Figure 17 demonstrate the fast response of the ALERT pin during a bus over-voltage fault when configured with a 150μs conversion time and averaging setting of 1. To visualize the ALERT pin response time under different conditions, the oscilloscope was set to persistence mode. When the fault exceeds the threshold significantly, the ALERT response can reach speeds as fast as 1/6 of the conversion time, as shown in Figure 16. Conversely, when the fault marginally exceeds the threshold (Figure 17), the ALERT response time extends to approximately 0.8 to 1.8 conversion periods. This variation primarily results from the relative timing between fault occurrence and ADC sampling instants. For applications sensitive to alert response time, when monitoring only shunt voltage or bus voltage conversions, the alert response time should be designed to accommodate up to 1.8 times the conversion period.

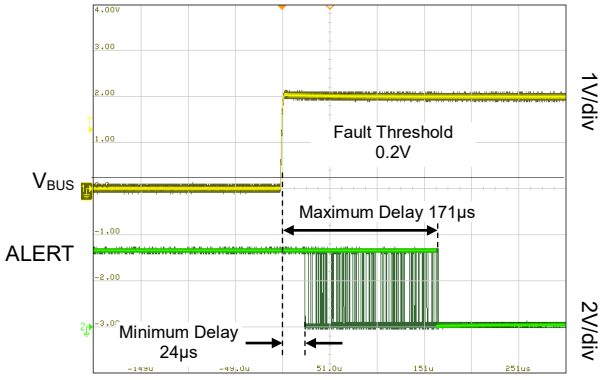


Figure 16. Alert Response Time (Sampled Values Significantly Above Threshold)

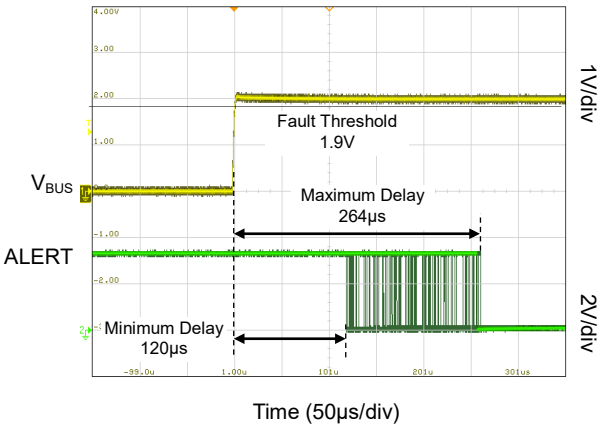


Figure 17. Alert Response Time (Sampled Values Slightly Above Threshold)

Power Supply Recommendations

The device can accurately measure the common-mode voltages applied to power supply terminals, which may be beyond its supply voltage, V_S. For example, the power supply voltage of the device is 5V, while the monitored load voltage can be as high as 85V. Regardless of whether the device is powered or not, the input terminal of the device can withstand a voltage of 0V to 85V.

The bypass capacitors should be placed as close to input and GND pins of the device as possible to ensure the stability of the power supply. A bypass capacitor of 0.1μF is recommended. For noisy or high-impedance power supplies, the device requires additional decoupling capacitors to filter power supply noise.

Layout Guidelines

A Kelvin connection or a 4-wire connection is recommended to be made between the input pins (IN+ and IN-) and the sensing resistor. These connection techniques avoid introducing additional impedance between the input pins. Considering that the resistance of the sensing resistor is very small, the additional high current-carrying impedance will result in considerable measurement errors.

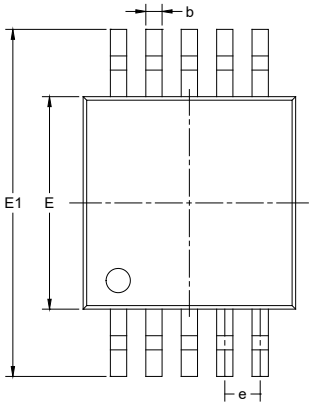
REVISION HISTORY

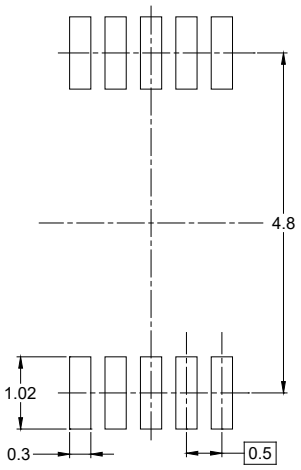
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JULY 2025)	Page
Changed from product preview to production data	All

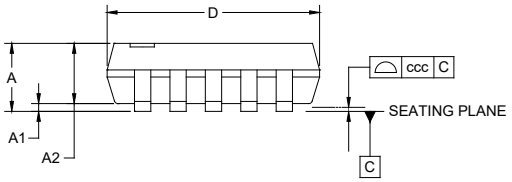
PACKAGE OUTLINE DIMENSIONS

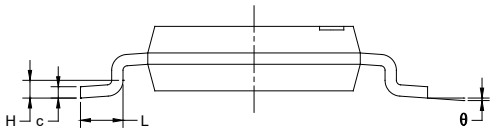
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



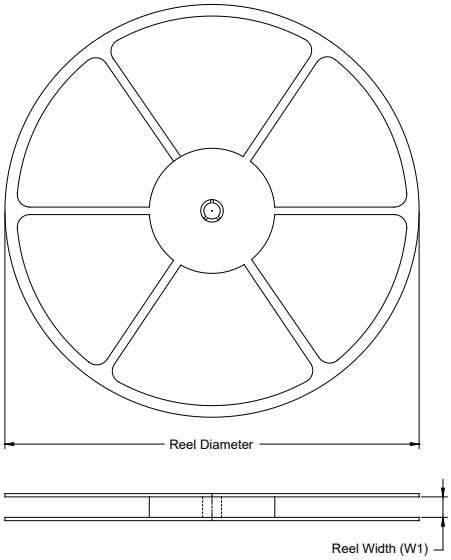


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

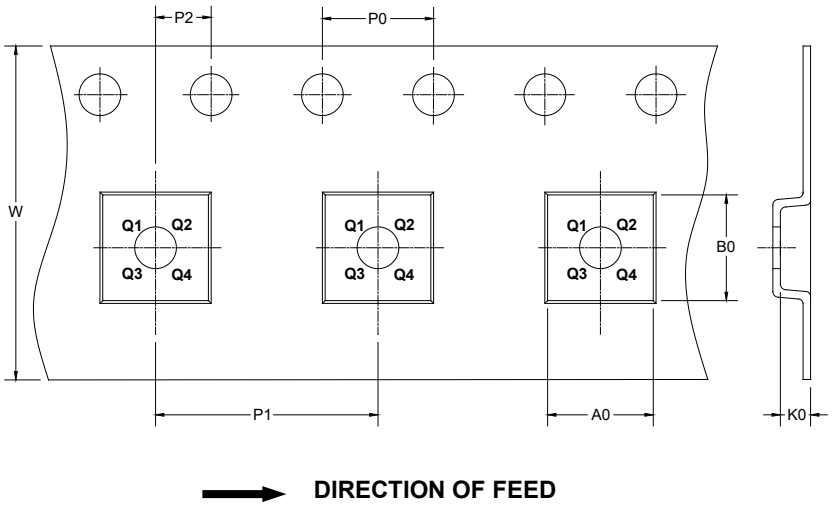
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



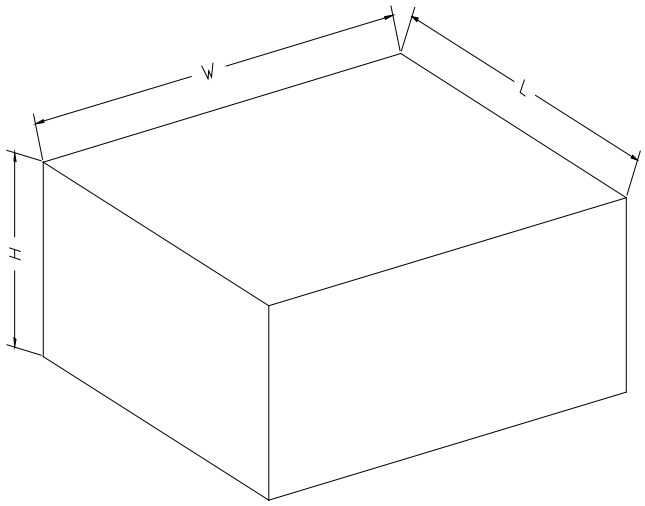
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002