SGM611A17
16V, 12A, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM611A17 is a high-efficiency high-frequency synchronous Buck DC/DC converter with a wide input voltage range and 12A output current, optimized for compact solutions. With an internally compensated adaptive constant on-time (ACOT) control architecture, ultra-fast dynamic response is achieved, and loop stabilization is guaranteed with ease.

The SGM611A17 provides multiple configurable functions: internal LDO or external VCC bias, three switching frequencies 600kHz, 800kHz and 1000kHz, PSM or FCCM operating mode at light load, internal fixed or external adjustable soft-start time, internal reference or external trackable reference input, and programmed current limit with R_{CS} resistor.

The device integrates comprehensive protection features to ensure reliable operation, such as output over-voltage protection (OVP), output under-voltage protection (UVP), output overshoot reducing mode (ORM), over-current protection (OCP), input under-voltage lockout (UVLO), VCC UVLO and thermal shutdown.

The SGM611A17 is available in a Green TQFN-3×4-21L package.

APPLICATIONS

Server, Computing, Storage
Telecom, Base Stations
SSD
Optical Module
General Purpose Point-of-Load

FEATURES

- **ACOT Control for Ultra-Fast Transient Response Stable with Low-ESR Output Capacitor**
- **Wide Input Voltage Range**
  - **2.7V to 16V with External 3.3V VCC Bias**
  - **4V to 16V with Internal Bias or External 3.3V VCC Bias**
- **Wide Output Adjustable Voltage Range: 0.6V to 5.5V**
- **Output Current: 12A**
- **Integrated Low R_{DSON} Power FETs: 7.2mΩ/2.2mΩ**
- **Selectable Switching Frequency: 600kHz, 800kHz and 1000kHz**
- **Remote Differential Sense of Output Voltage**
- **Adjustable Current Limit Level**
- **Selectable Pulse Skip Mode (PSM) and Forced Continuous Conduction Mode (FCCM)**
- **Outstanding Load Regulation**
- **PG Open-Drain Output**
- **PG Active Low Clamping at Power Failure**
- **Support External Reference and Tracking**
- **Output Discharge Function**
- **Internal Fixed 1.5ms or External Adjustable Soft-Start Time**
- **Pre-Bias Startup Capability**
- **Protections:**
  - **Latch-Off: Output OVP**
  - **Non-Latch: OCP, Output UVP, VIN UVLO, VCC UVLO and Thermal Shutdown**
- **Available in a Green TQFN-3×4-21L Package**

SIMPLIFIED SCHEMATIC

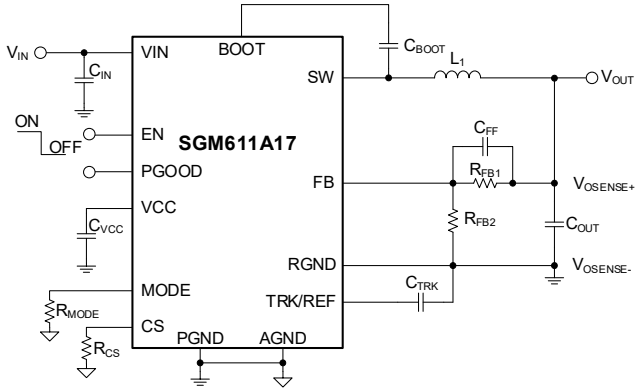


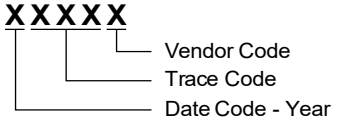
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM611A17	TQFN-3×4-21L	-40℃ to +150℃	SGM611A17TTWD21G/TR	SGM 3CLTWD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{IN} 18V
SW Voltage (DC) ..... -0.3V to V_{IN} + 0.3V
SW Voltage (15ns) (1) ..... -5V to 25V
BOOT Voltage ..... V_{SW} + 4V
VCC Voltage 4V
All Other Pins ..... -0.3V to 4.3V
Package Thermal Resistance
TQFN-3×4-21L, θ_{JA} ..... 43.9℃/W
TQFN-3×4-21L, θ_{JB} ..... 2.5℃/W
TQFN-3×4-21L, θ_{JC} ..... 24.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:
1. When the input voltage is 16V, the rated voltage is in the range of -5V to 25V for a period shorter than 15ns, and the maximum repetition frequency is 1000kHz.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 4V to 16V
Output Voltage Range, V_{OUT} ..... 0.6V to 5.5V
External VCC Bias, V_{CC_EXT} ..... 3.15V to 3.6V
Maximum Output Current, I_{OUT_MAX} 12A
EN Voltage, V_{EN} 3.6V
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

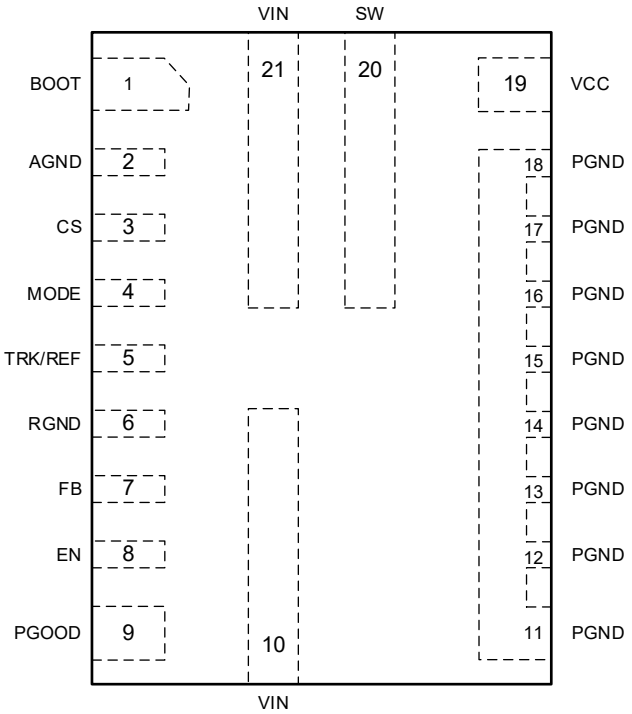
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×4-21L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	P	Bootstrap Supply for the High-side Gate Driver. A bootstrap capacitor should be connected between SW and BOOT pins.
2	AGND	P	Analog Ground. Select AGND as the internal circuit reference point of the analog circuits. Connect to PGND with PCB trace and avoid introducing noise from the power circuit.
3	CS	AI	Current Limit Adjust and Current Sense Input. Connect a resistor from this pin to AGND to set the current limit.
4	MODE	AI	Mode Selection. Connect a different resistor to select FCCM or PSM operation mode, and switching frequency 600kHz, 800kHz, or 1000kHz.
5	TRK/REF	AI	External Reference and Tracking Input. This pin has two functions. Connecting an external reference to this pin can override the internal reference. Connecting a capacitor between TRK/REF and AGND can set the soft-start time.
6	RGND	AI	This pin provides the return path for remote voltage sensing. It also serves as the ground for the internal reference. Tie this pin to AGND when operating in single-ended sense mode.
7	FB	AI	Feedback of Output Voltage. Connect an external resistor divider from the output to this pin to adjust output voltage.
8	EN	AI	Enable Input. This pin is pulled low by an internally 7MΩ resistor. Do not leave EN floating.
9	PGOOD	DO	Open-Drain Power-Good Output. A pull-up resistor is needed if this feature is used.
10, 21	VIN	P	Supply Input of the Device. Connect low ESR ceramic capacitors from this pin to PGND.
11-18	PGND	P	Power Ground. System Power Ground.
19	VCC	P	Internal LDO Output. A recommended 2.2μF decoupling ceramic capacitor with X5R or X7R dielectrics must be placed as close to VCC pin as possible.
20	SW	P	Switching Node. Connect it to the power inductor and bootstrap capacitor.

NOTE: AI = analog input, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40℃ to +150℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
VIN Supply Current (Shutdown)	I_{SD}	V_{EN} = 0V, no external bias on VCC pin, T_J = +25℃		13	18	μA
VCC Supply Current (Shutdown)		V_{EN} = 0V, V_{IN} = 0V, 3.3V external bias on VCC pin, T_J = +25℃		42	52	
VIN Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V (non-switching), no external bias on VCC pin, T_J = +25℃		710	850	μA
VCC Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 0.65V (non-switching), 3.3V external bias on VCC pin, T_J = +25℃		680	820	
MOSFET						
HS On-State Resistance	R_{DSON_HS}	V_{EN} = 2V		7.2		mΩ
LS On-State Resistance	R_{DSON_LS}	V_{EN} = 2V		2.2		mΩ
BOOT Circuit						
BOOT Leakage Current	I_{BOOT_LKG}	T_J = +25℃, $V_{BOOT-SW}$ = 3.3V		27	38	μA
BOOT-SW UVLO Falling Threshold	$V_{BOOT-SW_UV_F}$	T_J = +25℃, $V_{BOOT-SW}$ falling		2.15		V
Current Limit						
Constant for R_{CS} Equation				78		A×kΩ
Initial Current Limit Threshold	L_{OCL_VALLEY}	Valley current on LS FET, R_{CS} = AGND, T_J = +25℃	12.3	15	18.4	A
		Valley current on LS FET, R_{CS} = 5.23kΩ, T_J = +25℃	12.3	15	18.4	
Low-side Negative Current Limit	I_{LIM_NEG}			11.8		A
Zero-Cross Detection Current Threshold Open Loop	I_{ZCD}			70		mA
Switching Frequency						
Switching Frequency	f_{SW}	MODE = 0Ω, I_{OUT} = 10A, V_{OUT} = 2.5V		600		kHz
		MODE = 30.1kΩ, I_{OUT} = 10A, V_{OUT} = 2.5V		800		
		MODE = 60.4kΩ, I_{OUT} = 10A, V_{OUT} = 2.5V		1000		
Minimum On Time	t_{ON_MIN}			80		ns
Minimum Off Time	t_{OFF_MIN}			200		ns
Over-Voltage and Under-Voltage Protection						
OVP Threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP Threshold	V_{UVP}		77%	80%	83%	V_{REF}
Output UVP Filter Delay	t_{UVP_DELAY}			70		μs
Overshoot Reducing Mode Threshold	V_{ORM}		102%	105%	108%	V_{REF}
Feedback Voltage and Soft-Start						
Feedback Voltage	V_{INTREF}	T_J = +25℃	597	600	603	mV
		T_J = 0℃ to +85℃	596	600	604	mV
		T_J = -40℃ to +150℃	594	600	606	mV
TRK/REF Sourcing Current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		37	50	μA
TRK/REF Sinking Current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		12	18	μA
Soft-Start Time	t_{SS}	C_{TRACK} = 50nF, T_J = +25℃, first switching to 95% V_{OUT} delay		1.5		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, T_J = -40℃ to +150℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

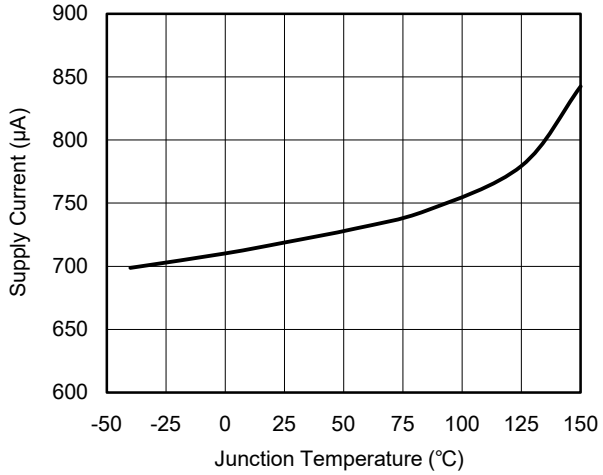
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN to First Switching Delay, Internal LDO				1.25	2	ms
EN to First Switching Delay, External VCC Bias				0.87	1.5	ms
Error Amplifier						
Error Amplifier Offset	V_{OS}		-4.5		4.5	mV
Feedback Leakage Current	I_{FB_LEK}	V_{FB} = V_{INTREF}			50	nA
Enable and UVLO						
Enable Input Rising Threshold	V_{IH_EN}		1.15	1.23	1.31	V
Enable Hysteresis	V_{EN_HYS}			200		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0.3	0.6	μA
Soft Shutdown Discharge FET	R_{ON_DISCH}	V_{EN} = 0V, V_{SW} = 0.5V		70	140	Ω
EN Internal Pull-Down Resistance				7		MΩ
VIN UVLO						
VIN Under-Voltage Lockout Threshold Rising	$V_{IN_UVLO_R}$	V_{CC} = 3.3V	2.2	2.4	2.6	V
VIN Under-Voltage Lockout Threshold Falling	$V_{IN_UVLO_F}$		1.65	1.85	2.05	V
VCC Regulator						
VCC Under-Voltage Lockout Threshold Rising	$V_{CC_UVLO_R}$		2.7	2.9	3.1	V
VCC Under-Voltage Lockout Threshold Hysteresis	$V_{CC_UVLO_HYS}$			200		mV
VCC Regulator	V_{CC}	I_{VCC_LOAD} = 2mA	2.95	3.05	3.15	V
VCC Load Regulation		Percentage change of VCC with I_{VCC_LOAD} from 2mA to 25mA		0.2		%
VCC LDO Dropout Voltage		V_{IN} = 4.0V, I_{VCC_LOAD} = 20mA		0.95	1.2	V
VCC LDO Short-Circuit Current Limit		V_{CC} = 2.6V, external bias on VCC pin		130		mA
FB Threshold to Turn-Off VCC LDO				90	220	mV
Power-Good						
Power-Good High Threshold	$V_{PG_H_R}$	FB from low to high	89%	92%	95%	V_{REF}
Power-Good Low Threshold	$V_{PG_L_R}$	FB from low to high	113%	116%	119%	V_{REF}
	$V_{PG_L_F}$	FB from high to low	77%	80%	83%	
Power-Good Low to High Delay	t_{PG}			1.08		ms
Power-Good Sink Current Capability	V_{PG}	I_{PG} = 10mA		0.4	0.6	V
Power-Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		1.3	2.1	μA
Power-Good Low-Level Output Voltage	V_{OL_100}	V_{IN} = 0V, V_{CC} = 0V, Pull PGOOD up to 3.3V through a 100kΩ resistor at +25℃		0.78	1.2	V
	V_{OL_10}	V_{IN} = 0V, V_{CC} = 0V, Pull PGOOD up to 3.3V through a 10kΩ resistor at +25℃		0.90	1.4	
Thermal Protection						
Thermal Shutdown (1)	T_{SD}			170		℃
Thermal Shutdown Hysteresis (1)	T_{HYS}			30		℃

NOTE:
1. Guaranteed by design not tested in production.

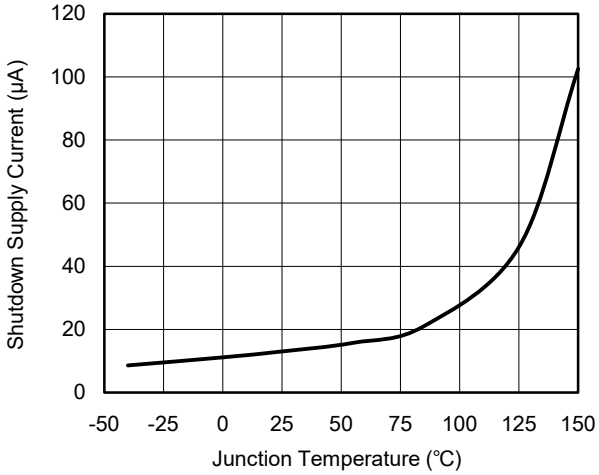
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

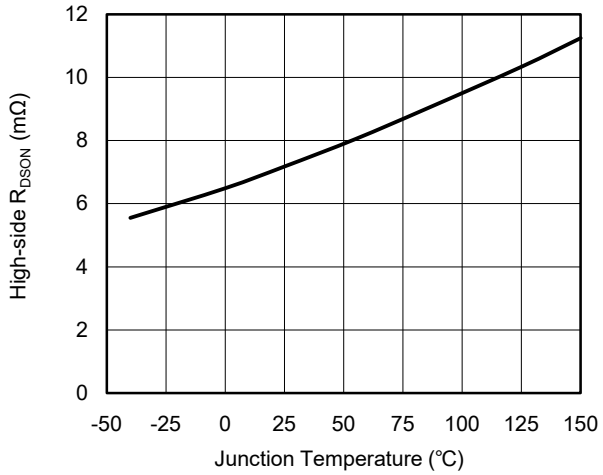
Supply Current vs. Temperature



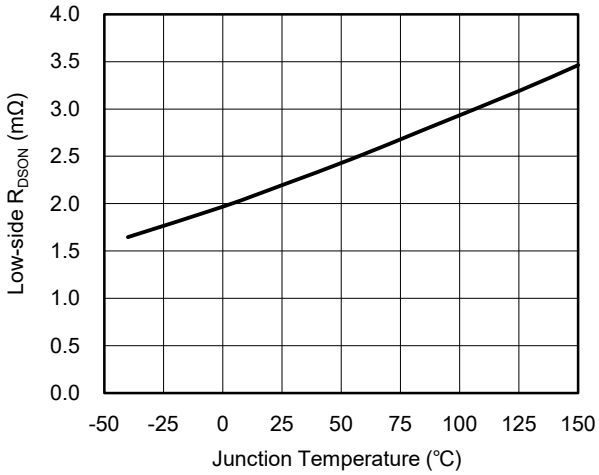
Shutdown Supply Current vs. Temperature



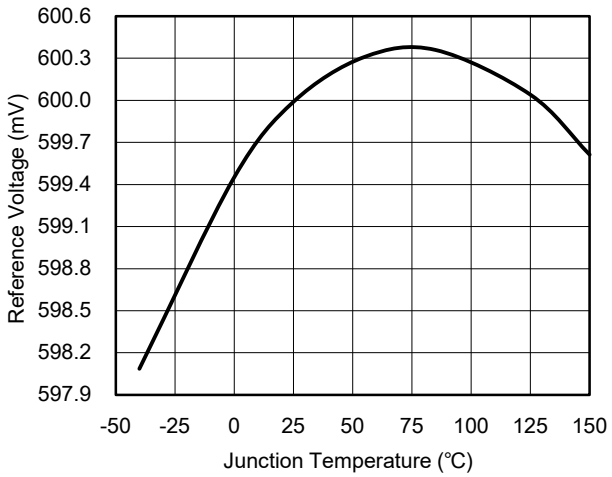
High-side R_{DSON} vs. Temperature



Low-side R_{DSON} vs. Temperature



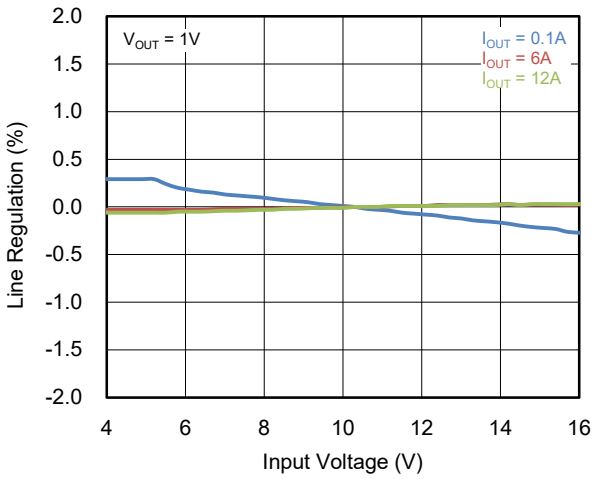
Reference Voltage vs. Temperature



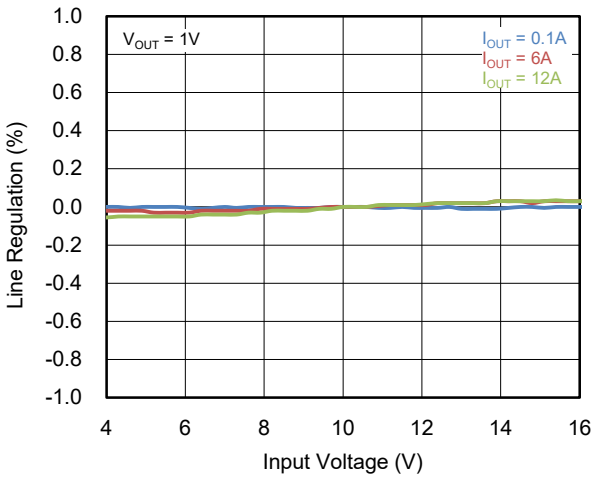
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, T_A = +25℃, L_1 = 0.33μH, DCR = 1.5mΩ, f_{SW} = 800kHz, unless otherwise noted.

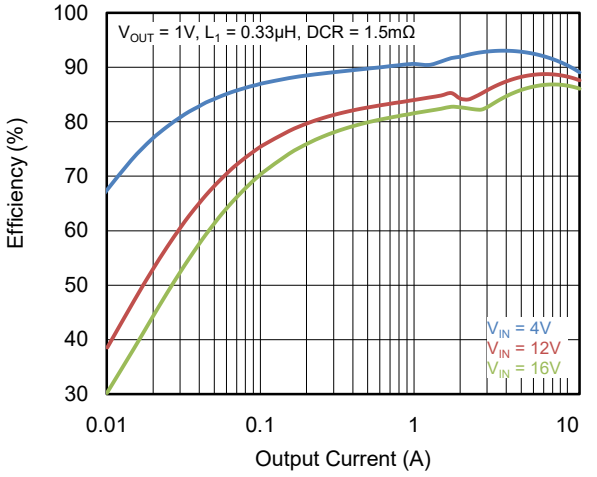
Line Regulation vs. Input Voltage (PSM)



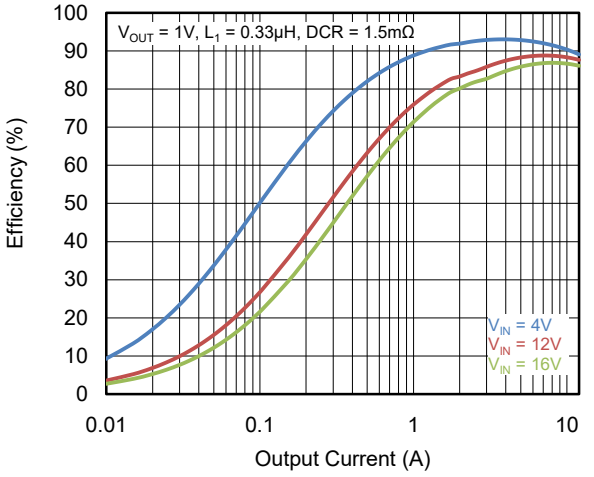
Line Regulation vs. Input Voltage (FCCM)



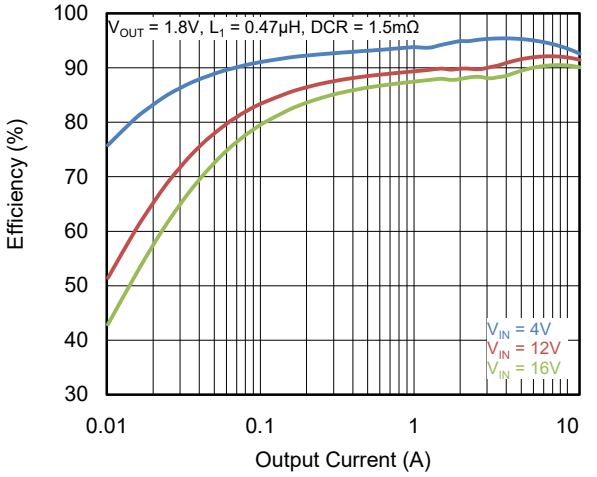
Efficiency vs. Output Current (PSM)



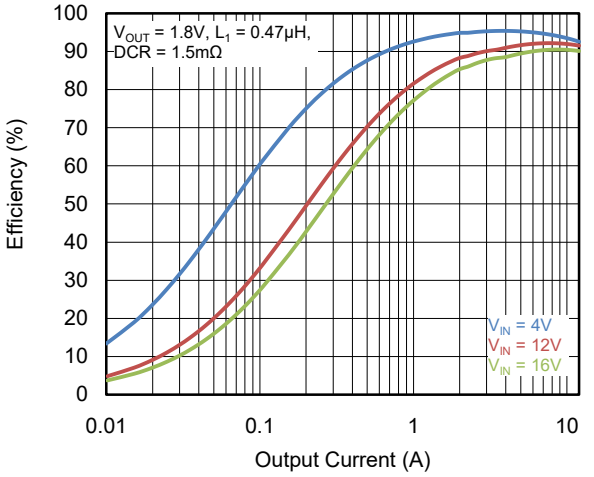
Efficiency vs. Output Current (FCCM)



Efficiency vs. Output Current (PSM)



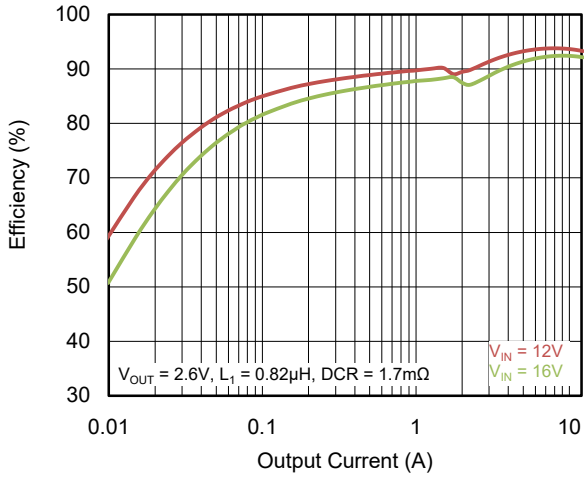
Efficiency vs. Output Current (FCCM)



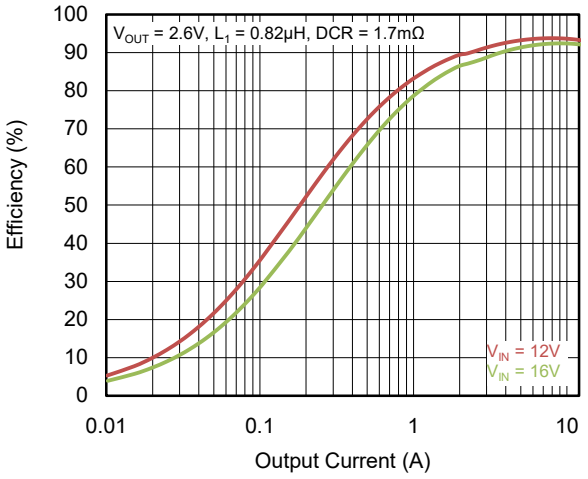
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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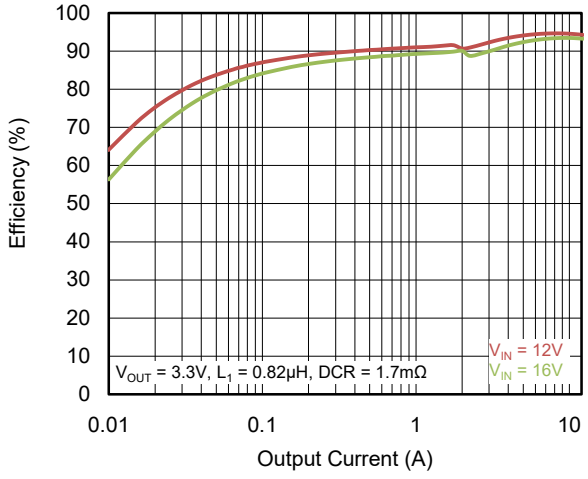
Efficiency vs. Output Current (PSM)



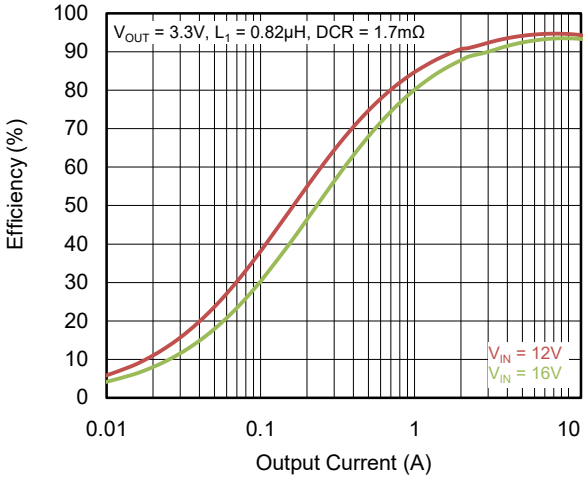
Efficiency vs. Output Current (FCCM)



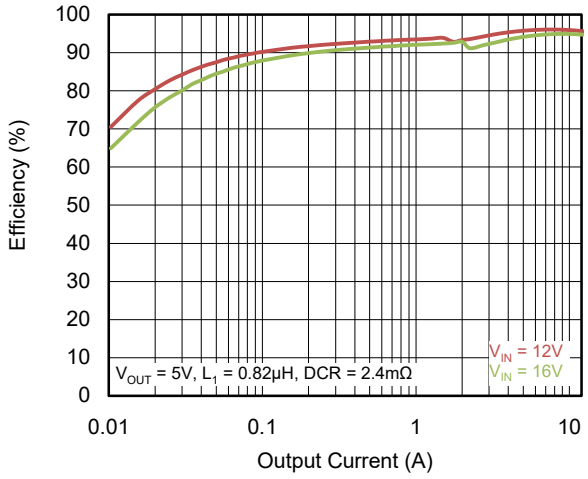
Efficiency vs. Output Current (PSM)



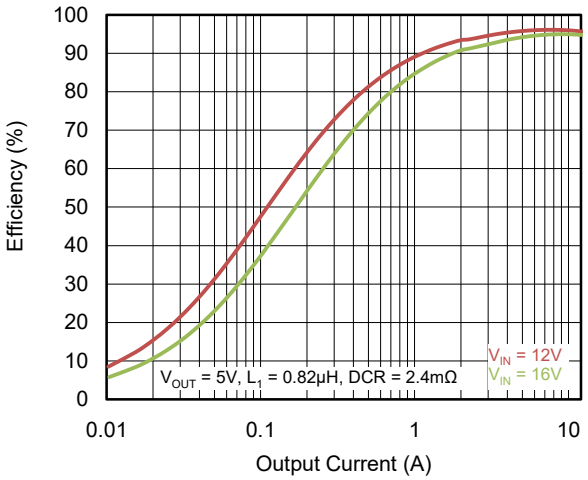
Efficiency vs. Output Current (FCCM)



Efficiency vs. Output Current (PSM)



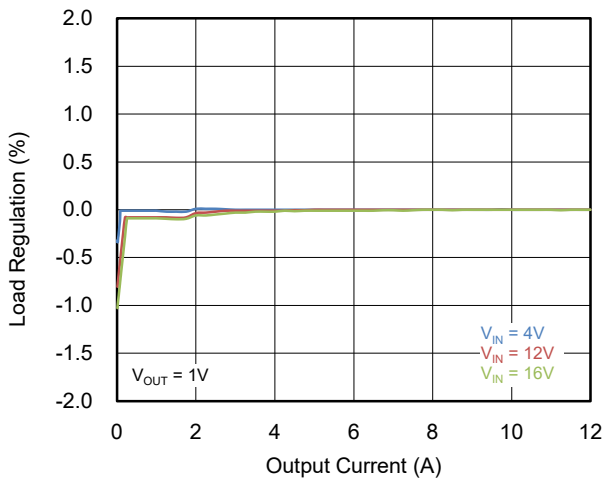
Efficiency vs. Output Current (FCCM)



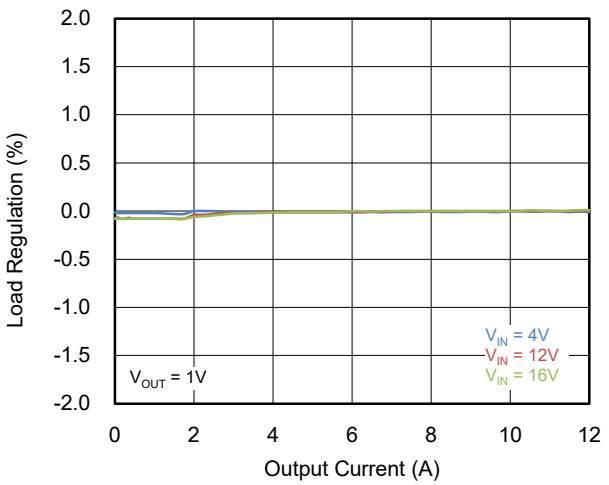
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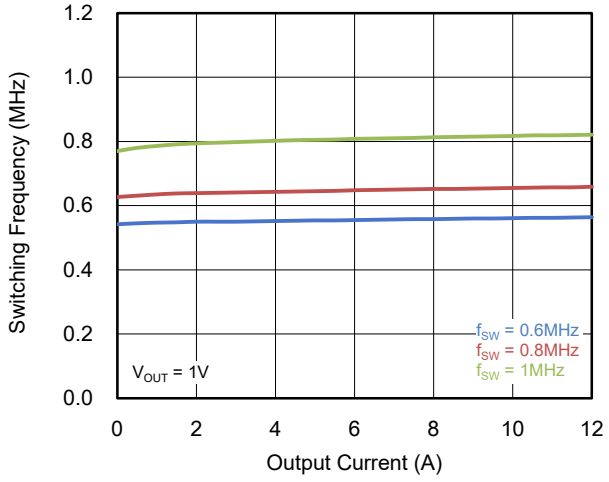
Load Regulation vs. Output Current (PSM)



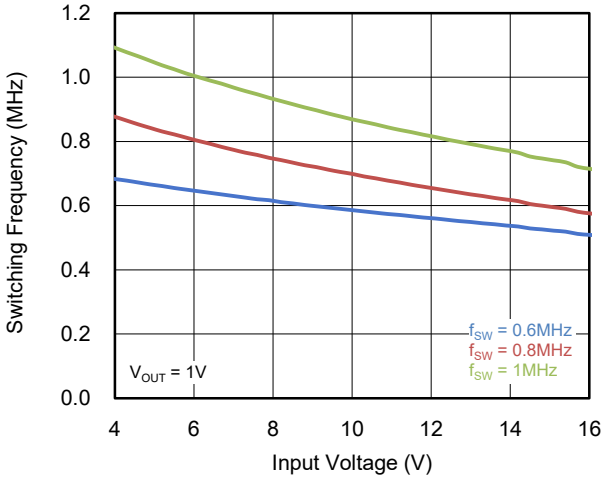
Load Regulation vs. Output Current (FCCM)



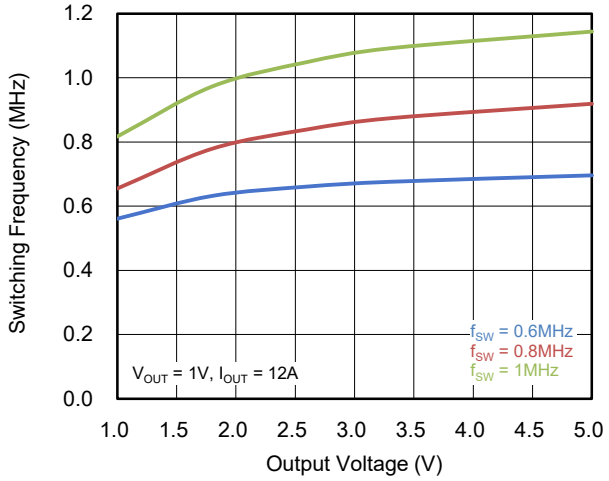
Switching Frequency vs. Output Current (FCCM)



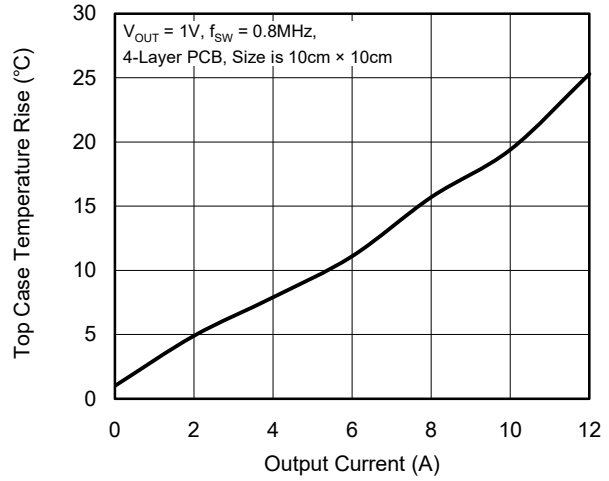
Switching Frequency vs. Input Voltage (FCCM)



Switching Frequency vs. Output Voltage



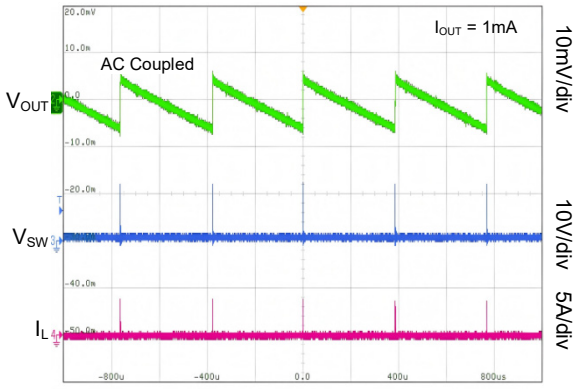
Top Case Temperature Rise vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

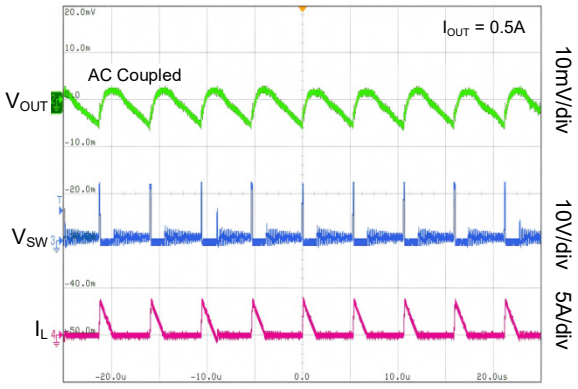
V_{IN} = 12V, T_A = +25℃, L_1 = 0.33μH, DCR = 1.5mΩ, f_{SW} = 800kHz, unless otherwise noted.

Output Ripple (PSM)



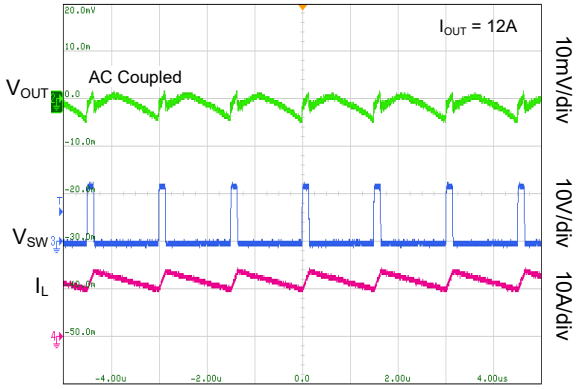
Time (200μs/div)

Output Ripple (PSM)



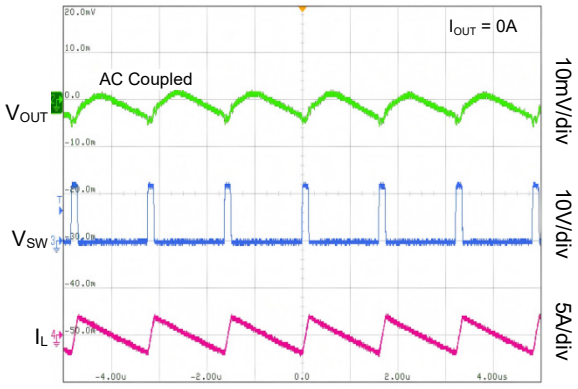
Time (5μs/div)

Output Ripple (PSM)



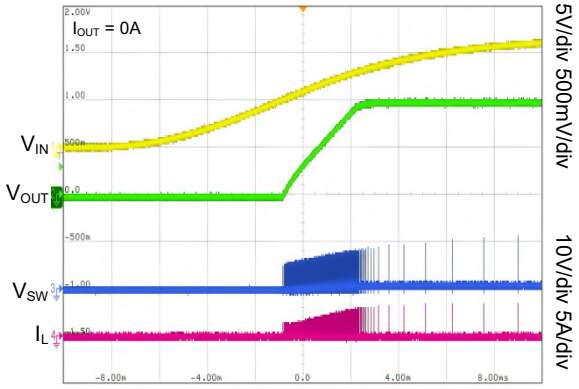
Time (1μs/div)

Output Ripple (FCCM)



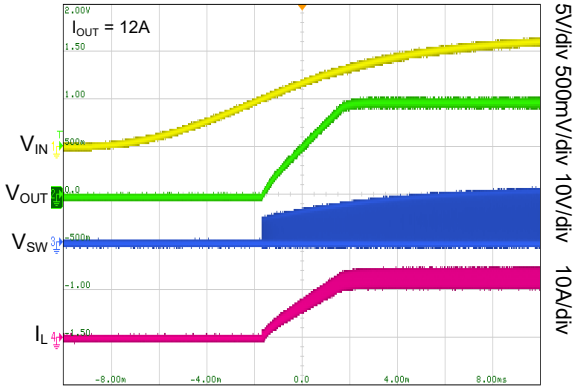
Time (1μs/div)

Startup through Input Voltage (PSM)



Time (2ms/div)

Startup through Input Voltage (PSM)

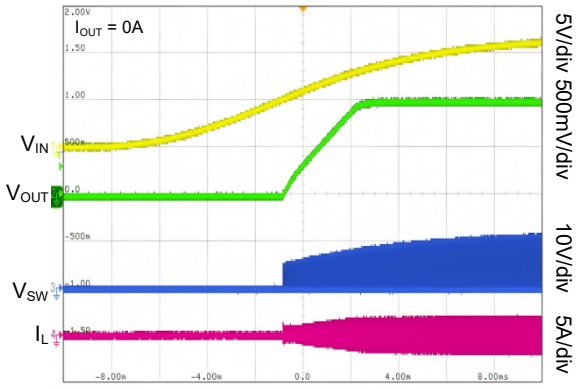


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

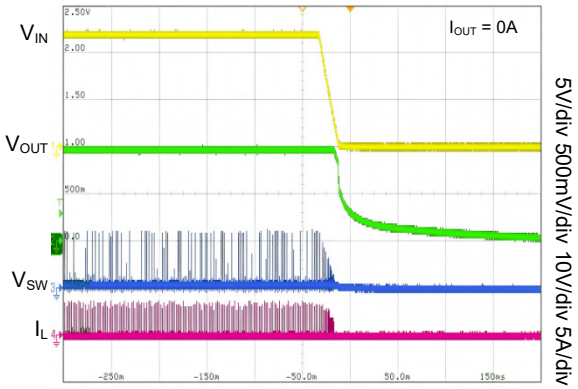
V_{IN} = 12V, T_A = +25℃, L_1 = 0.33μH, DCR = 1.5mΩ, f_{SW} = 800kHz, unless otherwise noted.

Startup through Input Voltage (FCCM)



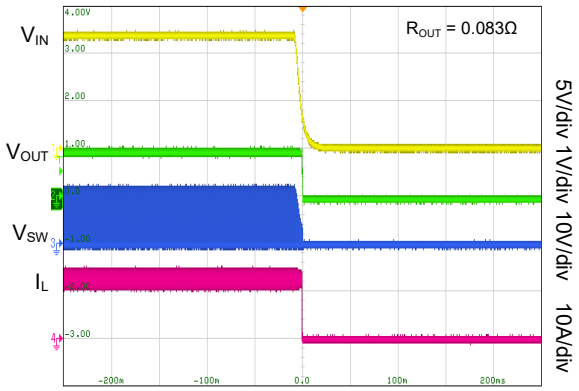
Time (2ms/div)

Shutdown through Input Voltage (PSM)



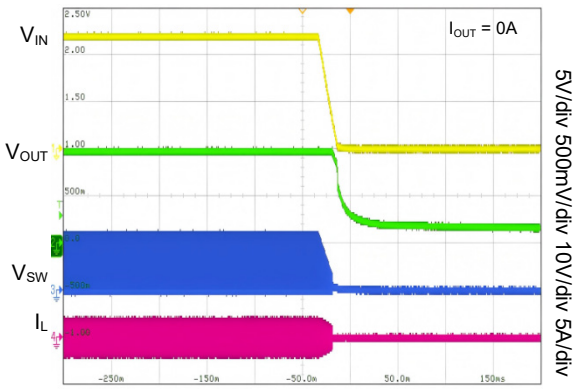
Time (50ms/div)

Shutdown through Input Voltage (PSM)



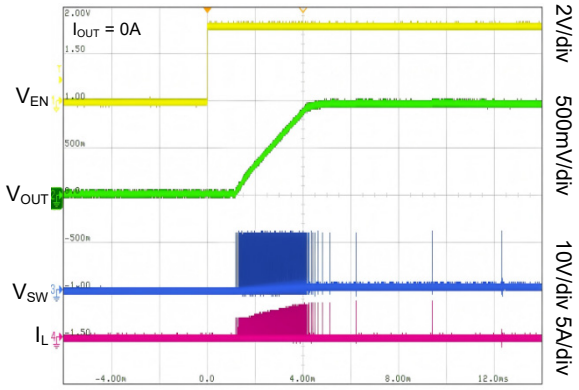
Time (50ms/div)

Shutdown through Input Voltage (FCCM)



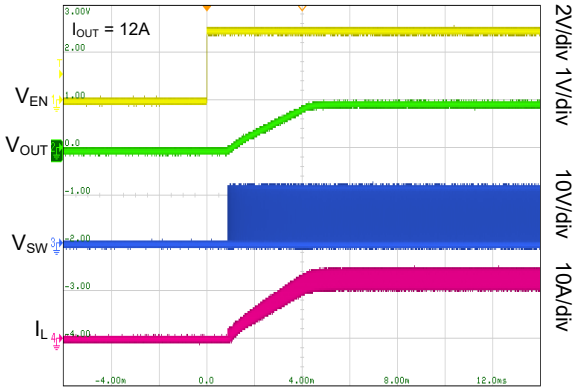
Time (50ms/div)

Startup through EN (PSM)



Time (2ms/div)

Startup through EN (PSM)

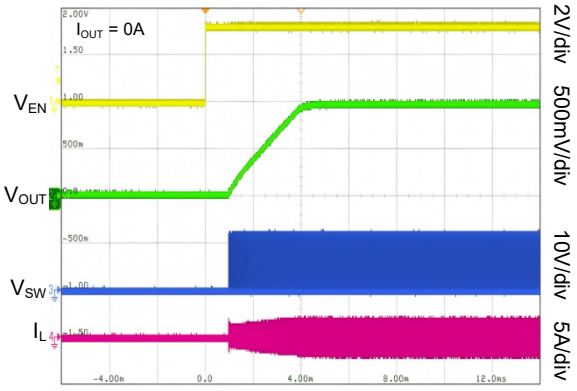


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

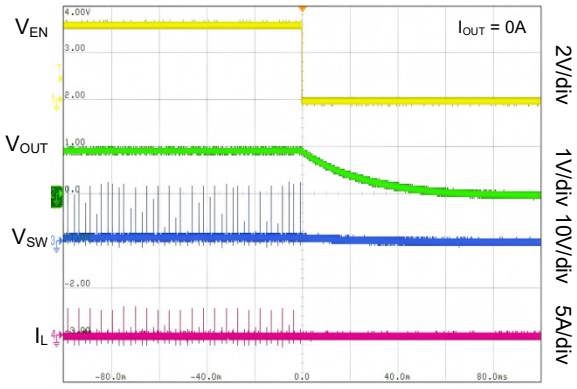
V_{IN} = 12V, T_A = +25℃, L_1 = 0.33μH, DCR = 1.5mΩ, f_{SW} = 800kHz, unless otherwise noted.

Startup through EN (FCCM)



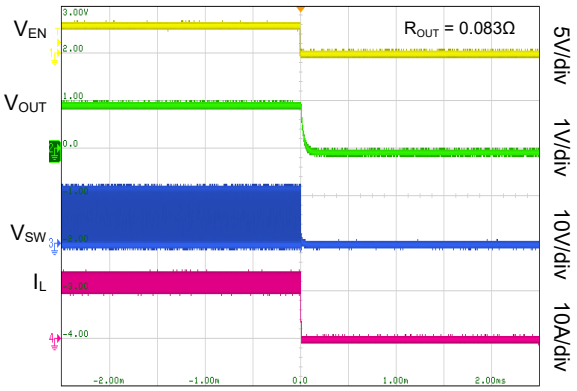
Time (2ms/div)

Shutdown through EN (PSM)



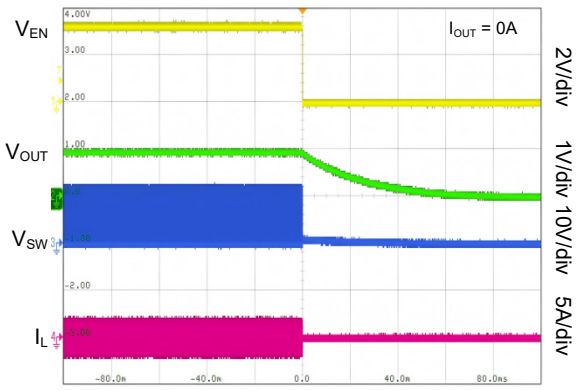
Time (20ms/div)

Shutdown through EN (PSM)



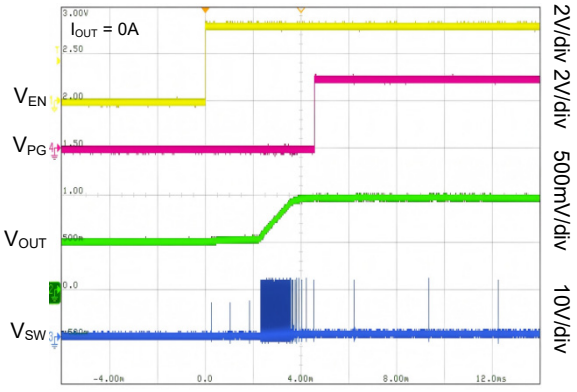
Time (500μs/div)

Shutdown through EN (FCCM)



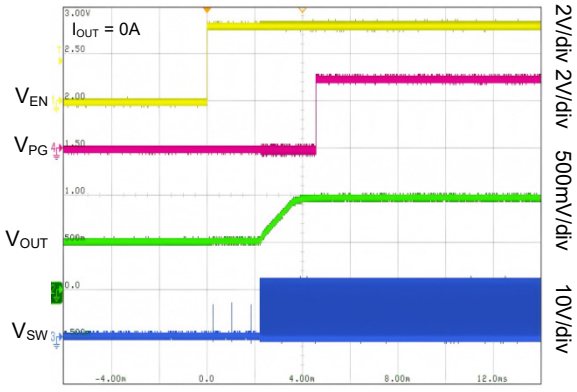
Time (20ms/div)

Pre-Bias Power On (PSM)



Time (2ms/div)

Pre-Bias Power On (FCCM)

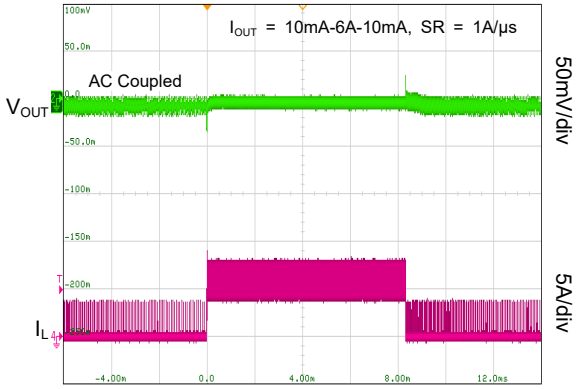


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

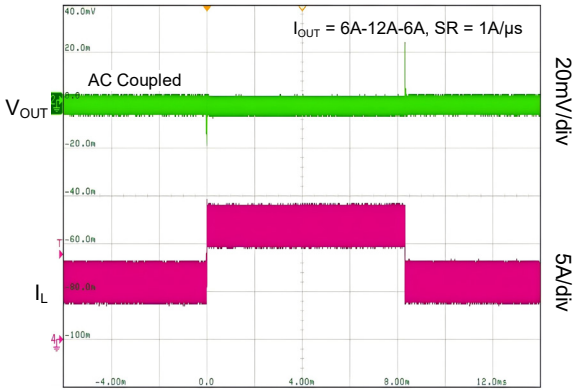
V_{IN} = 12V, T_A = +25℃, L_1 = 0.33μH, DCR = 1.5mΩ, f_{SW} = 800kHz, unless otherwise noted.

Load Transient (PSM)



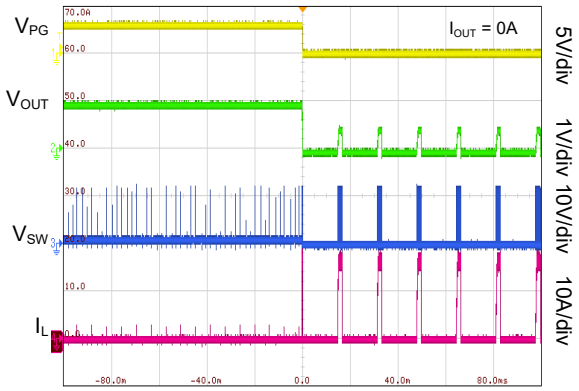
Time (2ms/div)

Load Transient (PSM)



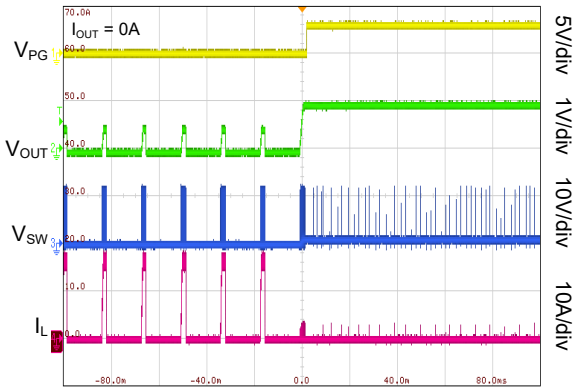
Time (2ms/div)

Short-Circuit Protection Entry (PSM)



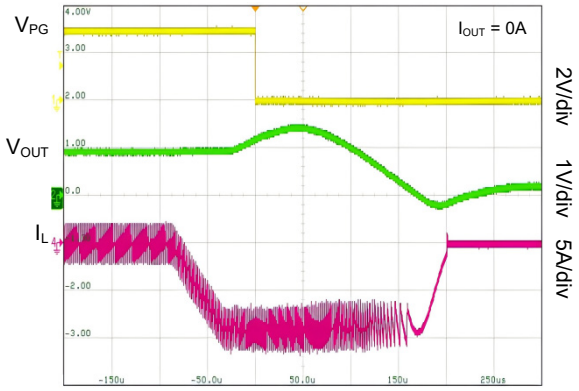
Time (20ms/div)

Short-Circuit Protection Recovery (PSM)



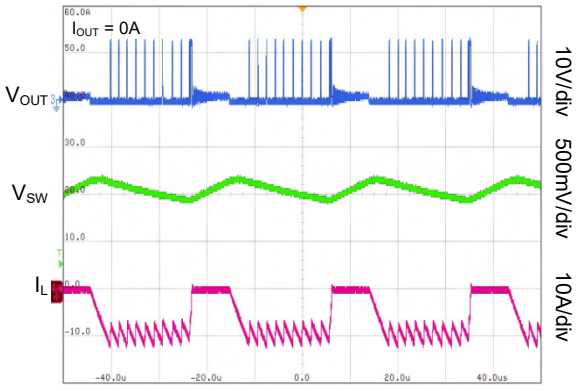
Time (20ms/div)

Over-Voltage Protection (FCCM)



Time (50μs/div)

ORM Operation (PSM)



Time (10μs/div)

FUNCTIONAL BLOCK DIAGRAM

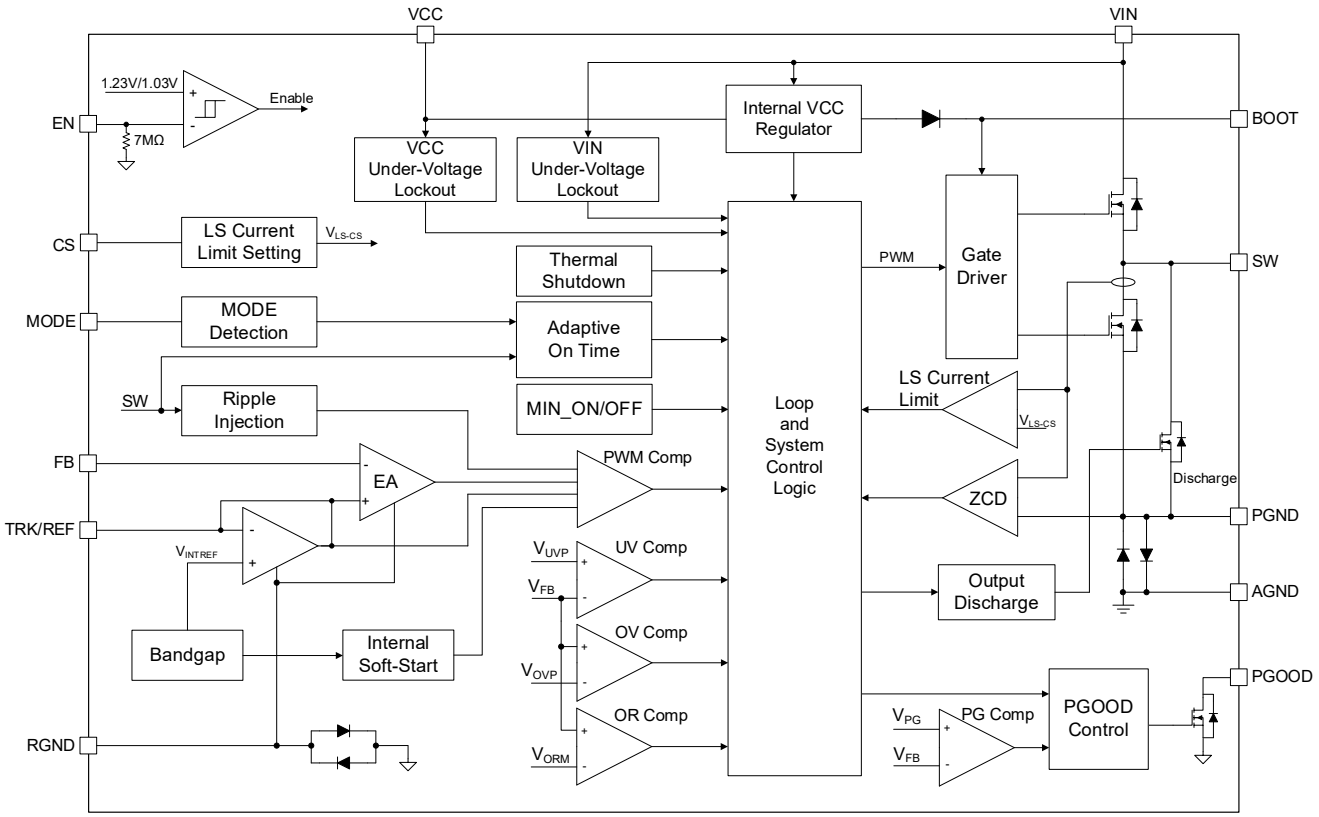


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

SGM611A17 is a high-efficiency, compact synchronous Buck converter designed for point-of-load power applications requiring up to 12A output current in computing systems such as servers and storage equipment. The SGM611A17 supports output voltages from 0.6V to 5.5V. The power input accepts a supply ranging from 2.7V to 16V, with the dedicated VCC bias supply operates from 3.15V to 3.6V.

The device incorporates an adaptive constant on-time control (ACOT), enabling optimal performance in low-duty-cycle applications while delivering ultra-rapid response to load transients. Internal loop compensation simplifies design implementation and reduces the number of external components. Furthermore, this control technique ensures stable operation with low-ESR output ceramic capacitors.

Internal VCC LDO and External Bias

The SGM611A17 integrates an internal 3.05V low-dropout regulator (LDO) powered from the VIN pin, with its output connected to VCC. When the voltage applied to the EN pin exceeds the enable threshold, the internal low-dropout regulator activates and initiates regulation of the VCC pin voltage. This VCC voltage supplies bias to the internal analog circuits and also powers the gate driver. A 2.2μF ceramic capacitor with a voltage rating of at least 6.3V must be connected to VCC for decoupling.

If an external bias voltage higher than the internal LDO output is applied, it overrides the internal LDO. This configuration improves overall power efficiency by sourcing the VCC current directly from the external bias supply rather than relying on the internal linear regulator. An under-voltage lockout (UVLO) circuit monitors the VCC voltage and shuts down the converter when the level falls beneath its specified falling threshold. A well-regulated and low-noise VCC voltage is critical for ensuring reliable operation of the device. If an external V_{CC} bias voltage is used, please pay attention to the following three points.

• Applying an external bias to the VCC pin before EN signal forces the internal LDO to remain disabled.

• When using an external VCC, the recommended startup sequence requires that the VCC UVLO rising threshold be met first, followed by satisfying the VIN UVLO rising threshold, and lastly meeting the EN rising threshold.

• (Not Recommended) If external bias voltage is supplied to the VCC pin after the EN signal becomes active, the power-up and power-down sequence may be freely implemented provided that no excessive current is drawn from the VCC pin. Note that any external discharge path connected to this pin may draw current beyond the current limit of the internal LDO, potentially causing the LDO to shut down and disable the converter output.

Enable

EN has precise rising and falling threshold values. When the voltage on the EN pin exceeds the rising threshold (TYP 1.23V) and the input voltage rises above the VIN under-voltage lockout rising threshold, the device initiates its internal startup sequence.

When operating with the internal VCC LDO, the startup procedure consists of three consecutive phases. In the first phase, a constant current source charges the VCC decouple capacitor. The charging period depends on the capacitance connected to the VCC pin. If the input voltage rises very gradually, the LDO output may be constrained by the input voltage, potentially extending the LDO startup interval. This extended charging period allows sufficient time for the internal reference (V_{INTREF}) to stabilize. Once the VCC voltage exceeds the VCC UVLO rising threshold, the device proceeds to the second phase, a power-on initialization. During this interval, the MODE pin configuration is read, the TRK/REF pin status is detected, and the control loop is initialized. After the initialization phase is completed, soft-start ramp begins to rise.

DETAILED DESCRIPTION (continued)

Figure 3 illustrates a case in which the VIN under-voltage lockout rising threshold is met before the EN rising threshold. The VCC UVLO rising threshold serves as the trigger to initiate the internal power-up sequence. The typical delay time between EN and the first switching is about 1.25ms (TYP). The soft-start circuit is internally set with a 50mV offset to avoid uncertainty in the initial state during startup, so the first switch pulse will not be emitted until the TRK/REF voltage rises over the offset.

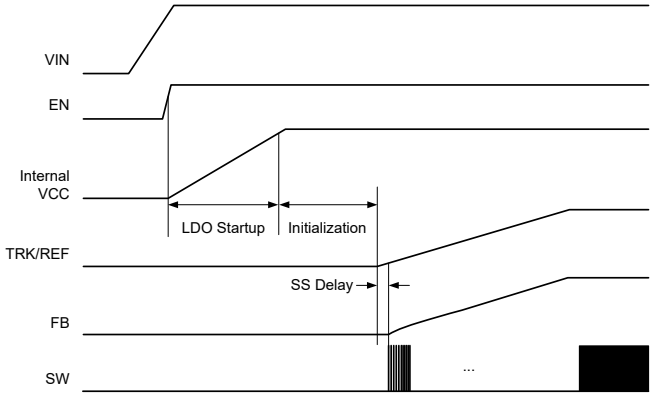


Figure 3. Power-up Sequence with Internal VCC

When operating with the external VCC bias, the startup procedure also consists of three consecutive phases as shown in Figure 4. The difference from using internal LDO is that since VCC has already been established, the first period of time will be much shorter, and only used for internal V_{INTREF} build-up. The other phases are the same as that of internal LDO.

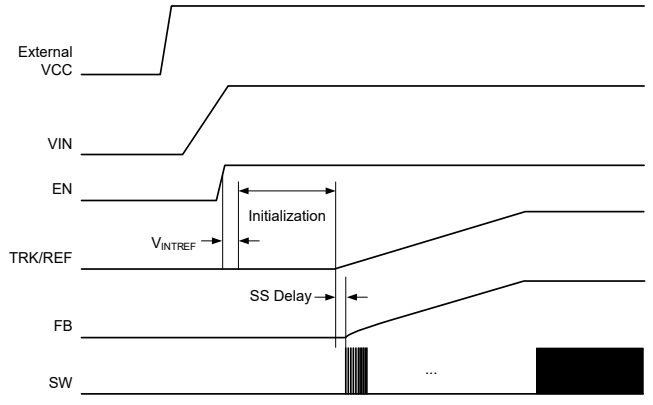


Figure 4. Power-up Sequence with External VCC

The EN pin incorporates an internal filter to prevent unintended activation or deactivation caused by minor disturbances. This RC filter has a time constant of 3μs (TYP). An internal pull-down resistor connects the EN pin to AGND. To prevent affecting the EN rising/falling thresholds, this resistor is configured at 7MΩ. With this pull-down implemented, leaving the EN pin floating before startup ensures the device remains disabled. However, during normal switching operation, this high-value resistor offers insufficient noise immunity to maintain a low state on the EN pin. The maximum voltage rating for the EN pin is 3.6V. Avoid direct connection between the EN and VIN pins.

Internal and External Soft-Start

The device features both an internal fixed soft-start time (TYP 1.5ms) and an externally adjustable soft-start time.

When the internal fixed 1.5ms soft-start time is used, a minimum capacitance of 50nF between TRK/REF and RGND is required for noise filtering.

If a longer external soft-start time is required, connect a larger capacitor between TRK/REF and RGND, per Equation 1. The total soft-start time is governed by the longer of the two: the internal fixed soft-start time or the time set by the external capacitor.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 36(\mu A)}{V_{INTREF}(V)} \quad (1)$$

When the FB voltage goes above V_{INTREF} - 50mV, the external soft-start is done. After both the internal and external soft-start sequences complete, the device's overall soft-start operation is finished.

The TRK/REF pin is also used as the external reference input, causing the FB voltage to track this external signal precisely. When an active external reference is applied to this pin and detected by the SGM611A17, the internal fixed soft-start circuitry controls the output voltage ramp-up. In this case, the capacitance between TRK/REF and RGND is not limited, and larger capacitor can be used to obtain a more stable and lower noisy reference voltage.

DETAILED DESCRIPTION (continued)

When driving the TRK/REF pin via a resistor divider, the divider-output impedance must be low enough so that the external voltage can dominate over the internal current-source effect.

External Reference and Tracking

The SGM611A17 features an analog input (TRK/REF) that accepts an external DC voltage reference. The control loop continuously uses the voltage present on the TRK/REF pin as its reference signal. When an external reference is connected between the TRK/REF and RGND pins, the feedback voltage precisely tracks this external signal.

Before the internal soft-start process, monitoring circuitry checks the TRK/REF pin voltage to determine whether a valid DC source is present. Firstly, the TRK/REF pin is discharged to RGND by an internal 110Ω resistor. Subsequently, the pin voltage is compared to 89% (TYP) of the internal V_{INTREF} value. This discharge sequence prevents misinterpretation of residual energy in an SS capacitor as an external voltage reference.

If the external voltage reference is unable to deliver adequate current to maintain a level above 89% of V_{INTREF} (indicating no external reference), the device defaults to the internal fixed V_{INTREF} for setting the PG, OVP, and UVP thresholds. In this case, the soft-start time is determined with the capacitance between TRK/REF and RGND, which is detailed at soft-start description.

If the detected voltage remains above 89% of V_{INTREF} (indicating an active external DC reference), the TRK/REF voltage is used as the reference instead of V_{INTREF}. In this case, the startup process is managed by the internal fixed 1.5ms soft-start circuitry. It is recommended to apply a stable DC reference to the TRK/REF pin before the EN signal is driven high. During the internal power-on delay period, the external reference must maintain the TRK/REF pin voltage at or above 89% of V_{INTREF} to ensure proper detection.

After soft-start, the external reference voltage can be configured within the 0.5V to 1.2V range. During normal operation, the external reference must sink over 37μA if its voltage is below the internal V_{INTREF} level, or supply more than 12μA if its voltage exceeds the internal V_{INTREF}. The slew rate of an external voltage source must not exceed 1mV/μs when ramping between different voltage levels.

If the detected voltage remains above 89% of $V_{INTRREF}$ (confirming an active external DC reference), the TRK/REF voltage is used as the reference for all three thresholds instead of $V_{INTRREF}$. In this configuration, as only a DC voltage is detected with no soft-start ramp, the startup process is managed by the internal fixed soft-start circuitry.

Power-Good

The power-good indicator is implemented with an open-drain structure with a maximum sinking capacity of 10mA, and requires an external pull-up resistor (TYP 30.1kΩ) connected to either the VCC rail or an external supply not exceeding 4V. If PG function is not used, connect the pin to AGND or keep it floating.

After the total soft-start is completed, PG becomes high impedance if output voltage is in regulated window and no EN shutdown, UVLO, or thermal shutdown events occur. PG is driven low once FB voltage falls below typically 80% of the reference voltage, or FB voltage goes higher than 116% of the reference voltage.

If the VCC supply is unable to power the device, for instance VCC remains at 0V, an internal low clamping circuit can ensure the PG stays at low state even with external pull-up resistor and pull-up power rail in place.

The PG signal may be used for multi-rail sequencing by connecting it to the EN pin of other converters. A 1.08ms delay is incurred when the PG pin asserts high upon satisfying its level-change criteria.

DETAILED DESCRIPTION (continued)

Output Voltage Setting

The output voltage of the device can be adjusted by resistors R_{FB1} and R_{FB2} which are connected to the FB pin. Use resistors with 1% tolerance or better for good output accuracy. Equation 2 can be used to calculate the R_{FB1} and R_{FB2} values based on the desired output voltage (V_{OUT}) and V_{REF}. Do not choose so large resistors that may cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{FB1}(k\Omega) \quad (2)$$

Remote Sense

The device supports remote output voltage sensing through the FB and RGND pins. This feature compensates for voltage drops across PCB traces, helping maintain output voltage accuracy during both steady-state operation and transient load events.

The traces running from the FB feedback divider to the remote load shall form a Kelvin-sense pair. The remote-sense ground return shall be tied to the RGND pin. The V_{OUT} sense line shall feed into the feedback divider network, with the lower feedback resistor R_{FB2} terminated at the RGND pin.

To maintain output voltage stability and minimize ripple, route remote-sense traces clear of noise sources including inductor, switching nodes, and high-frequency clock lines. Ground-plane shielding on both sides of these traces is recommended.

If remote sensing is not implemented, short the RGND pin to AGND.

Mode Selection

The SGM611A17 supports two operation modes: pulse skip mode (PSM) and forced continuous conduction mode (FCCM) under light load conditions. The device also provides three switching frequencies: 600kHz, 800kHz and 1000kHz. Configuration of the switching frequency and operational mode is accomplished by placing a resistor between the MODE pin and AGND. The combination is dictated by the resistance value applied, as detailed in Table 1. It is advised to utilize resistors with a ±1% tolerance.

Table 1. MODE Pin Selection

Mode Pin Connections	Operation Mode Under Light Load	Switching Frequency (f_{SW}) (kHz) (1)
Short to VCC or Open	PSM	600
243kΩ ± 10% to AGND		800
121kΩ ± 10% to AGND		1000
60.4kΩ ±10% to AGND	FCCM	1000
30.1kΩ ±10% to AGND		800
Short to AGND		600

NOTE: 1. The operating frequency is specified with a 2.5V output. Actual frequency becomes dependent on the output voltage setting.

The operational configuration is established and stored internally throughout the power-up initialization sequence. Subsequent modifications to the MODE terminal's resistance value following this initialization phase will not alter the converter's configured behavior. If the MODE terminal remains unconnected during the critical power-on interval, the internal logic will default to a 600kHz switching frequency with PSM operation.

For reliable recognition of the intended configuration, avoid installing any capacitive elements on the MODE terminal.

Pulse Skip Mode

If PSM is selected, the device can move to discontinuous conduction mode (DCM) at light load. A zero-crossing detection circuit works during PSM to determine the inductor current zero point. By setting a positive zero-crossing threshold, the device prevents negative inductor current flow. The conduction time (t_{ON}) is approximately the same as that of CCM, therefore, the switching frequency will gradually decrease as the load decreases. This design approach enhances efficiency under light-load conditions.

Forced Continuous Conduction Mode

If FCCM is selected, the device operates at a fixed frequency across all load conditions, making it suitable for applications requiring a stable switching frequency at the cost of reduced light-load efficiency.

DETAILED DESCRIPTION (continued)

Positive Over-Current Protection and Current Limit Setting

The SGM611A17 employs cycle-by-cycle valley current detection to implement over-current protection. During the low-side FET conduction interval, the current of low-side FET is monitored. If the sensed current exceeds the setting limit, the low-side FET remains conducting until the current drops below the limit threshold. This mechanism reduces the average current delivered to the output. Under output over-current conditions, the load demand surpasses the current supplied to the output capacitors, resulting in a decreasing output voltage. When the FB voltage drops below the UVP threshold (TYP 80% of V_{REF}), and lasts for 70μs. The device subsequently stops switching and enters a 14ms (TYP) hiccup mode before attempting to restart.

During startup, if an over-current condition is detected, the device continues to enforce cycle-by-cycle current regulation based on the low-side valley current setting. After soft-start completion, an under-voltage event triggered by the over-current condition will stop switching the converter and activate hiccup mode.

The current limit threshold is set by a resistor (R_{CS}) connected between the CS pin and AGND. Resistors with ±1% tolerance should be used, as resistors with wider tolerance may significantly reduce the accuracy of the over-current limit setting. Equation 3 defines the relationship between the valley-current-limit threshold and R_{CS}. To simplify calculations, a constant term K_{OCL} may be used in place of the numerical factor 78×10^3 (TYP). The tolerance of K_{OCL}, specified in Electrical Characteristics, facilitates analysis of the overall variation in the current limit threshold.

An integrated fixed maximum over-current clamp circuit safeguards the device against fault conditions on the CS pin, such as too small R_{CS} resistance or an accidental short to ground.

$$L_{OCL_VALLEY} = \frac{K_{OCL}}{R_{CS}} \quad (3)$$

where

L_{OCL_VALLEY} is valley-current-limit threshold in A

R_{CS} is CS resistor value in Ω

K_{OCL} is a constant for the calculation

Negative Current Limit

The device also incorporates a negative cycle-by-cycle current limit. Mirroring the approach used for positive over-current limit, the inductor current is observed throughout the low-side FET's conduction period. To prevent excessive negative current through the low-side FET, the device turns it off when a current of 11.8A (TYP) is detected. The high-side FET is then turned on for a duration determined by the instantaneous input-output voltages and switching frequency. Once this on-time expires, the low-side FET is enabled again. Once this on-time expires, the low-side FET is enabled again.

Under normal operating conditions, the 11.8A negative current limit should not be triggered. This negative current protection is primarily used to discharge the output capacitor during output OVP.

Output Over-Voltage and Under-Voltage Protection

The device continuously checks the feedback voltage to identify over-voltage and under-voltage conditions. If the FB voltage falls below 80% of the V_{REF}, the output UVP comparator triggers and initiates an internal timer. Once the 70μs (TYP) UVP timer ends, the system enters hiccup mode and initiates a restart following a 14ms (TYP) interval. Note that UVP protection is only active after the soft-start phase has completed.

During the 70μs (TYP) UVP timer period, if the output voltage rises above the UV threshold and therefore no longer meets the criteria for a UV event, the timer will be reset.

When the FB voltage exceeds 116% (TYP) of the V_{REF} level, the output OVP comparator triggers, causing the circuit to turn off the high-side MOSFET and turn on the low-side MOSFET until the negative current limit (I_{LIM_NEG}) is reached. Once this current threshold is detected, the low-side FET is turned off and the high-side FET is then turned on for a duration determined by the instantaneous input-output voltages and switching frequency. The converter continues operating in this manner until the output voltage stays below 80% of the target value. Then both the high-side and low-side FETs are turned off. The latch-off state can only be exited by re-powering the device or asserting the EN enable pin, to resume chip operation.

DETAILED DESCRIPTION (continued)

Overshoot Reducing Mode

The device supports an overshoot reducing mode (ORM) to protect the output load, which serves as an early non-latch over-voltage protection. When the output voltage is greater than 105% of the reference voltage and OVP is not triggered, it enters ORM. The low-side FET is turned on until the negative current limit is triggered (TYP 11.8A). Then the low-side FET is turned off and the high-side FET is then turned on for a duration determined by the instantaneous input-output voltages and switching frequency. This rapidly discharge of the output capacitor helps V_{OUT} quickly return to its target value.

The converter operates in this state repeatedly until the FB voltage falls below 102% (TYP) of the V_{REF} level.

Output Voltage Discharge

When the device is disabled via the EN pin, it enters an output discharge state. In this mode, both the high-side and low-side FETs are maintained off, while a dedicated discharge FET (connected between SW and PGND) is activated to dissipate output energy. The discharge FET deactivates once the FB voltage falls below 90mV (TYP).

This discharge mode can be triggered by any of the following fault conditions:

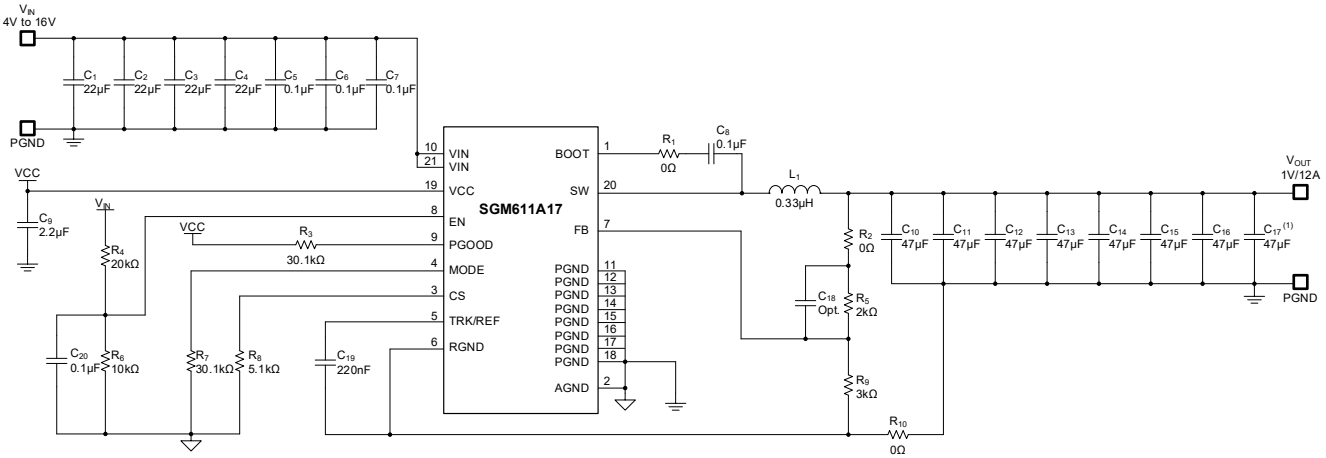
- EN Shutdown
- OTP
- VIN UVLO
- VCC UVLO

Thermal Shutdown

When the junction temperature exceeds the trigger threshold (TYP 170℃), the device stops switching and discharges the TRK/REF pin. Once the junction temperature cools by approximately 30℃ below the threshold, the device automatically restarts and initiates a new soft-start sequence. This thermal shutdown feature operates as a non-latching protection mechanism.

APPLICATION INFORMATION

In this section, power supply design with the SGM611A17 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.



NOTE: 1. When employing remote sensing with a distant load, all output capacitors must be placed in the vicinity of the sense point.

Figure 5. Application Circuit

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 5. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	4V to 16V
Output Voltage	1V
Maximum Output Current	12A
Switching Frequency	800kHz

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1-C_4	Ceramic Capacitor, 22μF, 25V, X7S, Size1206, P/N: GRM31CC71E226ME15	muRata
C_5-C_8, C_{20}	Ceramic Capacitor, 0.1μF, 25V, X7R, Size 0603, P/N: GRM188R71E104KA01	muRata
C_9	Ceramic Capacitor, 2.2μF, 6.3V, X7R, Size 0603	Standard
C_{10}-C_{17}	Ceramic Capacitor, 47μF, 6.3V, X7U, Size 1206, P/N: GRM31CE70J476ME15L	muRata
C_{18}	Option	Standard
C_{19}	Ceramic Capacitor, 220nF, 10V, X7R, Size 0603	Standard
L_1	0.33μH, Power Inductor, DCR_{MAX} = 1.5mΩ, $I_{SAT(10\%)}$ = 56.7A, $I_{RP(40K)}$ = 48.2A, P/N: 7443320033	Wurth
R_1, R_2, R_{10}	0Ω, Chip Resistor, 1%, Size 0603	Standard
R_3, R_7	30.1kΩ, Chip Resistor, 1%, Size 0603	Standard
R_4	20kΩ, Chip Resistor, 1%, Size 0603	Standard
R_5	2kΩ, Chip Resistor, 1%, Size 0603	Standard
R_6	10kΩ, Chip Resistor, 1%, Size 0603	Standard
R_8	5.1kΩ, Chip Resistor, 1%, Size 0603	Standard
R_9	3kΩ, Chip Resistor, 1%, Size 0603	Standard

Table 4. SGM611A17 Suggested Component Selections

V_{OUT}	R_{FB_UP}	R_{FB_DOWN}	Frequency Set	L_1	Normal C_{OUT}	Effective C_{OUT}	C_{FF}
1V	2kΩ	3kΩ	600kHz	0.47μH	8x47μF	261.04μF	NC
			800kHz	0.33μH	8x47μF	261.04μF	NC
1.8V	2kΩ	1kΩ	600kHz	0.68μH	6x47μF	182.82μF	820pF
			800kHz	0.47μH	6x47μF	182.82μF	820pF
			1000kHz	0.33μH	6x47μF	182.82μF	820pF
2.6V	10kΩ	3kΩ	600kHz	0.82μH	8x47μF	217.28μF	820pF
			800kHz	0.82μH	6x47μF	162.96μF	820pF
			1000kHz	0.82μH	6x47μF	162.96μF	820pF
3.3V	10kΩ	2.2kΩ	600kHz	0.82μH	8x47μF	196.48μF	820pF
			800kHz	0.82μH	6x47μF	147.36μF	820pF
			1000kHz	0.82μH	5x47μF	122.8μF	820pF
5V	10kΩ	1.37kΩ	600kHz	1μH	6x47μF	108μF	820pF
			800kHz	0.82μH	6x47μF	108μF	820pF
			1000kHz	0.82μH	5x47μF	90μF	820pF

NOTE: 1. Ceramic Capacitor, 47μF, 6.3V, X7U, Size 1206, GRM31CE70J476ME15L.

APPLICATION INFORMATION (continued)

Input Capacitor Selection

Use ceramic capacitors (X7S, X7R, or equivalent types) for decoupling between the VIN and PGND pins. These capacitors must be placed as close as possible to the device. For typical applications, it is recommended to use 22μF × 4 ceramic capacitors. Applications with long input traces or transient load demands may need additional input bulk capacitance. For high-frequency noise suppression, 0.1μF capacitors must be positioned directly adjacent to critical VIN pin and PGND pin on the same board layer as the device. The capacitor's voltage rating must exceed the maximum input voltage and leave enough margin. The total ripple current rating of capacitors must exceed the calculated maximum RMS capacitor current, derived from the regulator's operating parameters (e.g., duty cycle, load current), which can be calculated by Equation 4. Ceramic capacitance decreases under DC bias. The input ripple voltage depends on the input capacitance, switching frequency, and duty cycle. Worst-case ripple occurs near 50% duty cycle. It can be calculated by Equation 5.

$$I_{C_RMS} = I_{OUT_MAX} \times \sqrt{\frac{V_{OUT}}{V_{IN_MIN}} \times \frac{V_{IN_MIN} - V_{OUT}}{V_{IN_MIN}}} \quad (4)$$

where:

I_{C_RMS} is the maximum RMS current of capacitor.

I_{OUT_MAX} is the maximum output DC current.

V_{IN_MIN} is minimum input voltage.

$$\Delta V_{IN} = \frac{I_{OUT_MAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times f_{SW}} \quad (5)$$

where:

ΔV_{IN} is the input ripple voltage peak-to-peak.

I_{OUT_MAX} is the maximum output DC current.

C_{IN} is the effective input capacitance value (μF).

f_{SW} is switching frequency (MHz).

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 6 and Equation 7 can be used to choose the inductance value based on ΔI_L.

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2} \quad (6)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (7)$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

Output Capacitor Selection

The architecture of the SGM611A17 allows use of ceramic-type output capacitors with low equivalent series resistance (ESR). To keep the capacitance up to high-frequency and to achieve narrow capacitance variation with temperature, it is recommended to use X7U dielectric. The bias voltage can cause the capacitance of the ceramic capacitor to decrease significantly, and the degree of decrease depends on the specification of the capacitor (size, nominal voltage, temperature standard). The effective deviation of a ceramic capacitor can be as high as -20% to +20% of the nominal value.

Steady-state output ripple voltage depends on inductor current ripple and capacitor impedance. The minimum capacitance requirement is:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right) \quad (8)$$

where:

ΔV_{OUT} is the output ripple voltage (peak-to-peak).

L is the inductance value (μH).

f_{SW} is switching frequency (MHz).

R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

C_{OUT} is the output capacitance value (μF).

If the switching frequency is seriously reduced due to the decrease of the input voltage, it is recommended to increase the output capacitance to ensure system stability.

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 9 for selecting the feedback resistors (R_5 and R_9) in Figure 5 to set the desired output voltage (V_{OUT}):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_5}{R_9}\right) \quad (9)$$

To avoid high noise sensitivity on the FB pin, the resistance value of R_9 is recommended not to exceed 200kΩ. The smaller the R_9 resistance value is, the stronger the anti-noise ability will be, but at the same time, the loss on the voltage divider will also be greater.

Bootstrap Capacitor

To maintain stable switching behavior, implement a 100nF ceramic capacitor across the BOOT-SW pins, prioritizing components with minimal DC voltage dependency.

Controlled MOSFET activation and transient suppression can be achieved by inserting a current-limiting resistor in the bootstrap path. While this configuration tempers switching-edge overshoot, it introduces switching efficiency degradation due to increased conduction losses. Prototype designs should integrate a default short-circuit (0Ω) path for bootstrap circuits, allowing subsequent impedance adjustment if PCB-induced parasitic effects amplify switching spikes beyond component tolerances.

Layout Guidelines

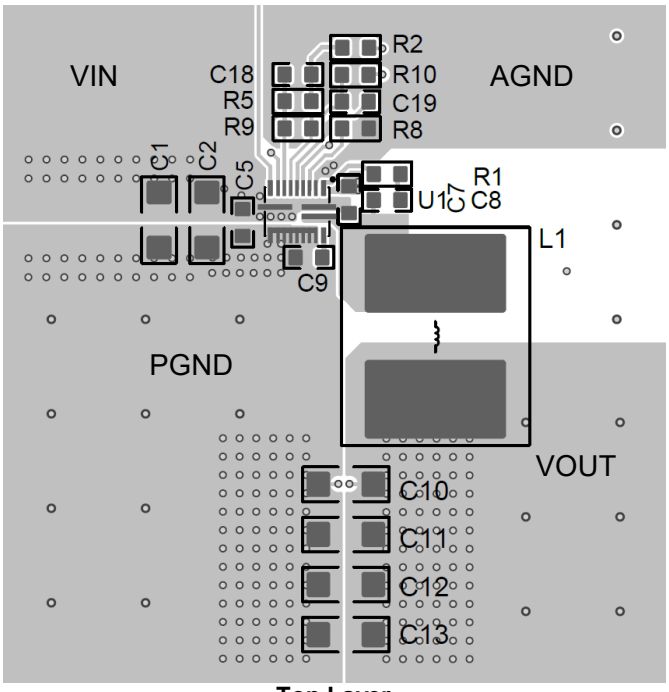
A critical component of a high-frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM611A17.

- Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- For better thermal performance, the VIN and PGND networks should be arranged in at least two layers.
- To achieve the best power integrity, place the 100nF low ESR decoupling capacitor as close as possible to the VIN-PGND pins. Place the remaining input capacitors closer to them. It is not recommended to place the remaining input capacitors on another layer of PCB. If such a situation occurs, it is suggested to use sufficient vias near them to reduce the impedance between them and the IC.
- Place the inductor as close as possible to SW pin to reduce the length of the SW node route and thereby improve EMI performance.
- Connect the ground returns of the input and output capacitors close to the PGND pin and at the same point to avoid a ground potential shift and to minimize high-frequency current path.
- Keep RGND pin and FB pin connections away from the high-frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.
- Place the output voltage divider near the FB pin and on the same layer as the IC.
- Use as many vias as possible near the PGND pin to connect the PGND copper-clad networks of each layer directly beneath the chip together to facilitate noise reduction and heat dissipation.
- The AGND pin must be connected to the PGND network only through a few relatively concentrated vias. These vias cannot be too far from the AGND pin.
- Place the BOOT-SW capacitor as close as possible to the BOOT (pin 1) and SW (pin 20).
- For remote-load sensing, the traces from the FB divider to the load must form a Kelvin-sense pair. The remote-sense ground return shall be tied to the RGND pin. The V_{OUT} sense line shall feed into the feedback divider network, with the lower feedback resistor R_{FB2} terminated at the RGND pin.

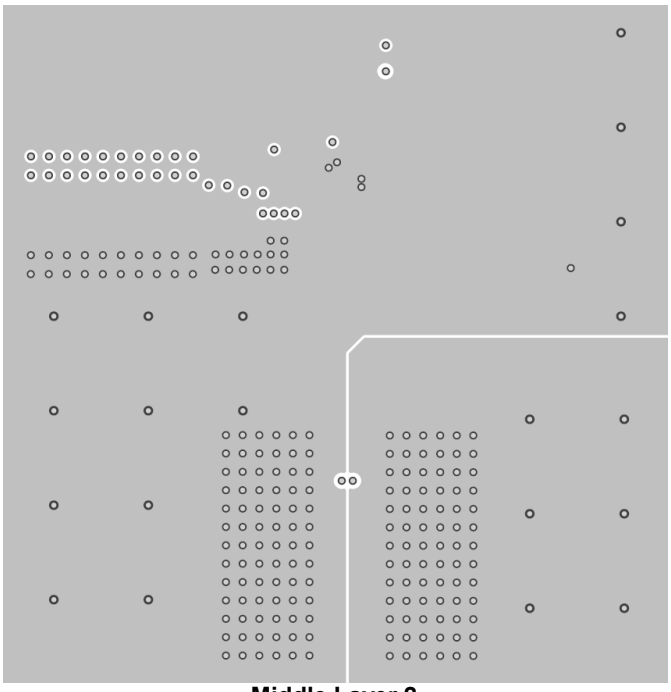
  Keep remote-sense traces away from inductor, switching nodes and high-frequency clock lines to preserve output-voltage stability and reduce ripple. Ground-plane shielding on both sides of the sense traces is recommended.
- The lower resistor of EN, the CS resistor, and the MODE resistor need to be connected with AGND island.

  Refer to Figure 6 for a recommended PCB layout.

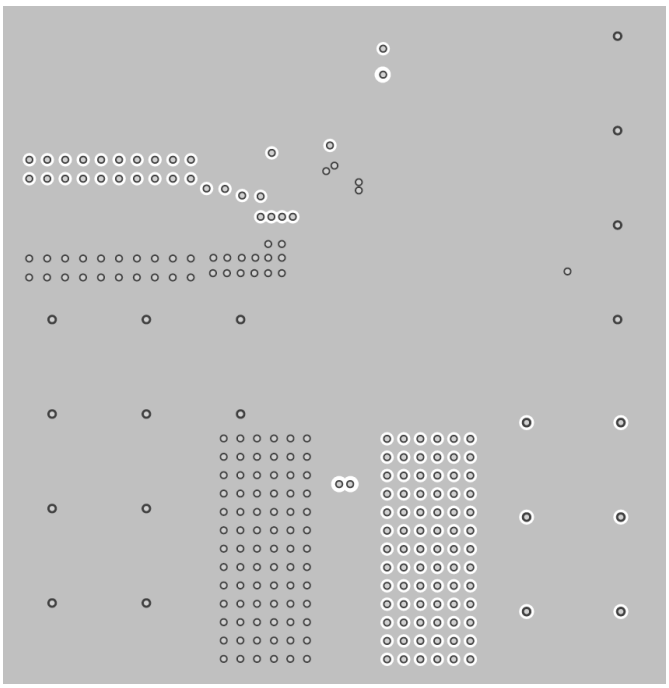
APPLICATION INFORMATION (continued)



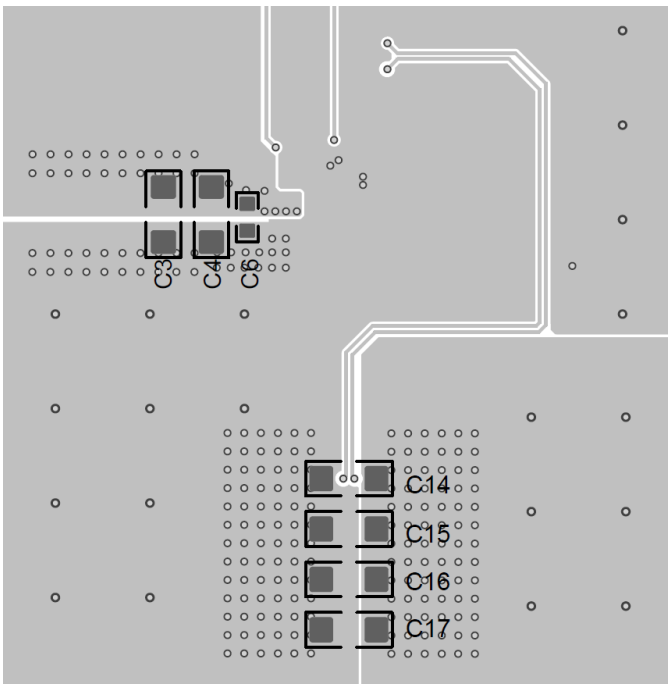
Top Layer



Middle Layer 2



Middle Layer 1



Bottom Layer

Figure 6. PCB Layout

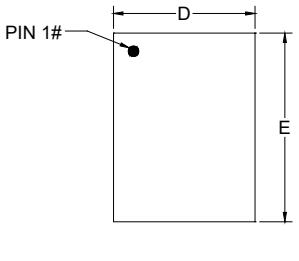
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

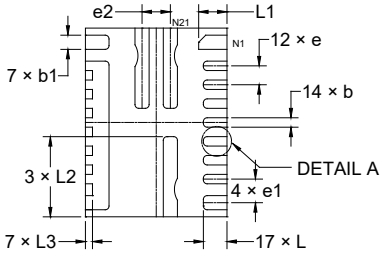
Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

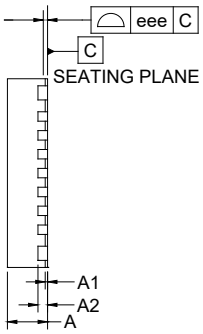
TQFN-3×4-21L



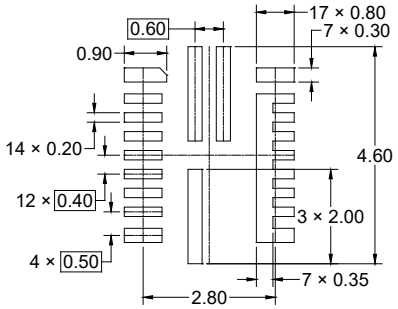
TOP VIEW



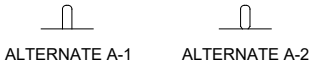
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



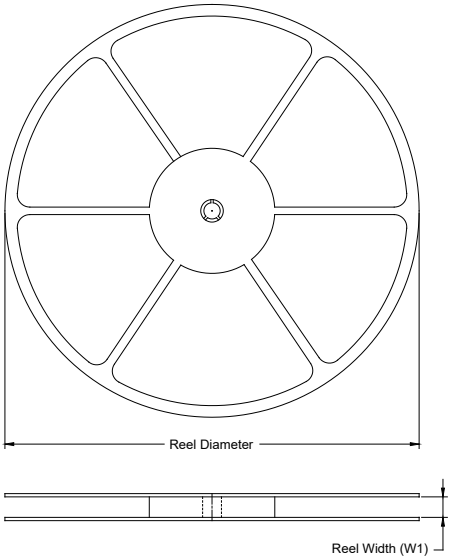
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
b1	0.250	-	0.350
D	2.900	-	3.100
E	3.900	-	4.100
e	0.400 BSC		
e1	0.500 BSC		
e2	0.600 BSC		
L	0.400	-	0.600
L1	0.500	-	0.700
L2	1.600	-	1.800
L3	0.150 REF		
eee	0.080		

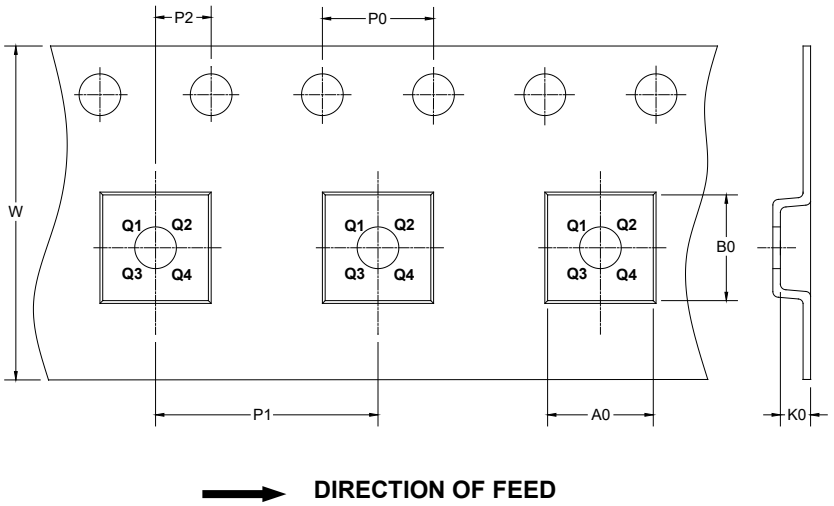
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



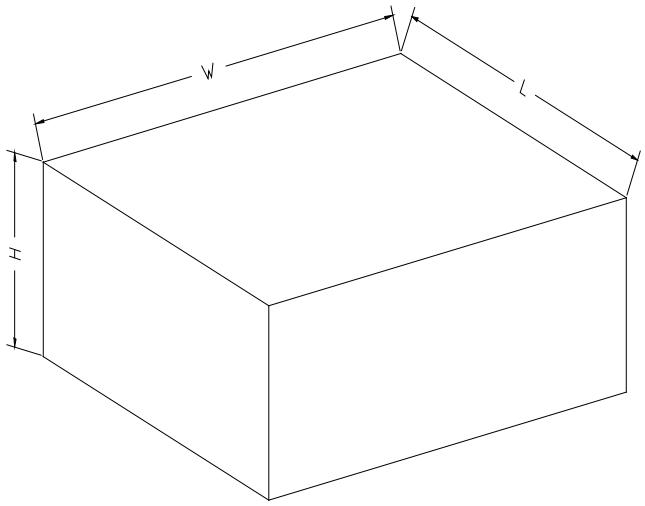
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-21L	13"	12.4	3.30	4.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002