SGM61023
2.5V to 5.5V Input, 2A Output, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61023 is a series of high-efficiency high-frequency synchronous Buck converters with an input voltage range of 2.5V to 5.5V and a wide output current range optimized for compact solutions. SGM61023A works in PWM mode under heavy load and automatically enter power-save mode to maintain high efficiency under light load. SGM61023B works in forced PWM mode over entire load range to maintain low output voltage ripple and good load regulation.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

SGM61023 is available in a Green WLCSP-0.9×1.2-6B-A package.

APPLICATIONS

Video Surveillance
Portable Electronics
Solid State Drive
Multi Function Printers
Generic Point of Loads
Industrial PC

FEATURES

- **AHP-COT Architecture for Fast Transient Regulation**
- **2.5V to 5.5V Input Voltage Range**
- **Wide Output Voltage Range: 0.6V to 4V**
- **Output Current: 2A**
- **Quiescent Current:**
  - **Power-Save Mode: 20μA**
  - **Force PWM Mode: 465μA**
- **100% Duty Cycle for Lowest Dropout**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown**
- **1% Feedback Accuracy**
- **4MHz Switching Frequency**
- **Power-Save Mode at Light Loads (SGM61023A)**
- **Force PWM Mode (SGM61023B)**
- **Hiccup Short-Circuit Protection**
- **Available in a Green WLCSP-0.9×1.2-6B-A Package**

TYPICAL APPLICATION

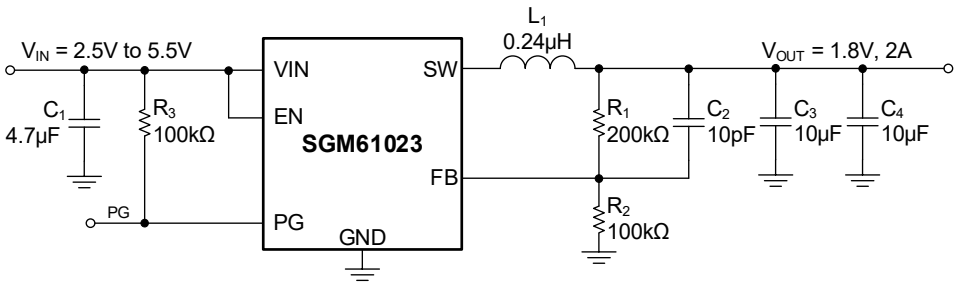


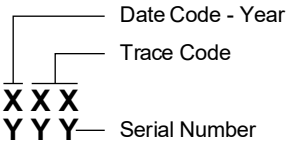
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61023A-ADJ	WLCSP-0.9×1.2-6B-A	-40℃ to +125℃	SGM61023A-ADJXG/TR	XXX 09N	Tape and Reel, 4000
SGM61023B-ADJ	WLCSP-0.9×1.2-6B-A	-40℃ to +125℃	SGM61023B-ADJXG/TR	XXX 09P	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, FB, EN, PG ..... -0.3V to 6V
SW (DC) ..... -0.3V to V_{IN} + 0.3V
SW (AC, Less than 1ns) ..... -2V to 7V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
Package Thermal Resistance
WLCSP-0.9×1.2-6B, θ_{JA} ..... 174.8℃/W
WLCSP-0.9×1.2-6B, θ_{JB} ..... 57℃/W
WLCSP-0.9×1.2-6B, θ_{JC} ..... 54.8℃/W
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.5V to 5.5V
Output Voltage Range, V_{OUT} ..... 0.6V to 4.0V
Output Current Range, I_{OUT} ..... 0A to 2A
Sink Current at PG Pin, I_{SINK_PG} 1mA
Pull-Up Resistor Voltage, V_{PG} 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

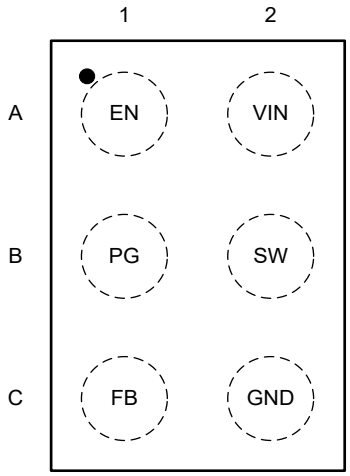
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-0.9×1.2-6B-A

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	EN	I	Active High Enable Input. Logic high sets the device active, logic low disables and turns it into shutdown mode. It can connect a 10kΩ resistor to VIN pin if it is needed. Do not leave this pin floating.
B1	PG	O	Power Good Open-Drain Output. Pull this pin up with a resistor to a voltage below 5.5V. Leave this pin floating when it is not in use.
C1	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
C2	GND	G	Power and Signal Ground.
B2	SW	P	Converter Switching Node Output Pin. Connect to the switching terminal of the output inductor.
A2	VIN	P	Power Supply Voltage Input.

NOTE: O = output, I = input, P = power, G = ground.

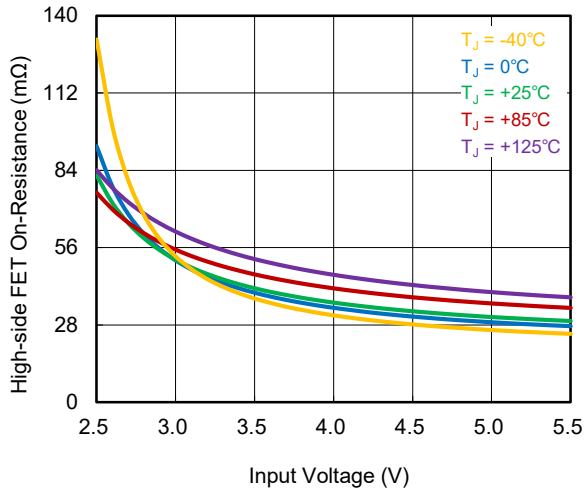
ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃ and V_{IN} = 2.5V to 5.5V. Typical values are at T_J = +25℃ and V_{IN} = 5V, unless otherwise noted.)

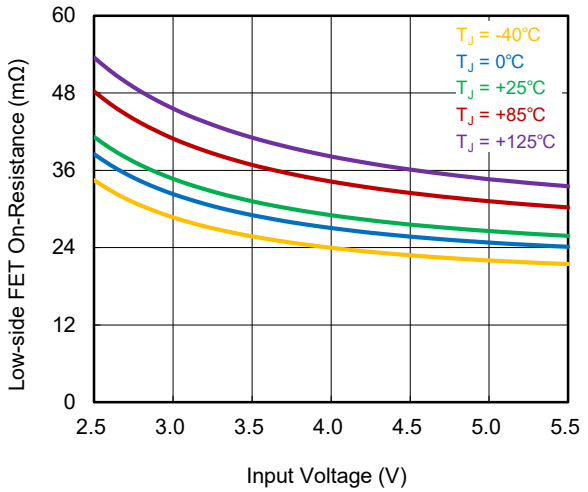
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Quiescent Current	I_Q	Power-save mode, not switching		20	30	μA
		Force PWM mode, not switching		465	600	
Shutdown Current	I_{SD}	EN = Low, T_J = -40℃ to +85℃		0.05	0.5	μA
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	V
Under Voltage Lockout Hysteresis		V_{IN} rising		160		mV
Thermal Shutdown Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling		20		
Logic Interface EN						
High-Level Threshold Voltage	V_{IH}		1.05			V
Low-Level Threshold Voltage	V_{IL}				0.35	V
Input Leakage Current into EN Pin	I_{EN_LKG}	EN = High		0.01	0.05	μA
Soft-Start, Power Good						
Soft-Start Time	t_{SS}	Time from EN high to 95% of V_{OUT} nominal		1.4		ms
Power Good Lower Threshold	V_{PG}	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	93	96	99	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	89	92	95	
Power Good Upper Threshold		V_{PG} rising, V_{FB} referenced to V_{FB} nominal	102	105	108	
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	107	110	113	
Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA			0.3	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01	0.1	μA
Power Good Deglitch Delay	t_{PG_DLY}	PG rising edge		92		μs
		PG falling edge, exclude shutdown by EN or V_{UVLO}		13		
Output						
Feedback Regulation Voltage	V_{FB}	PWM mode, T_J = +25℃	594	600	606	mV
		PWM mode	591		609	
Feedback Input Leakage Current	I_{FB_LKG}	V_{FB} = 0.6V		0.01	0.05	μA
Output Discharge Current	I_{DIS}	V_{SW} = 0.4V; EN = low	25	88		mA
Power Switch						
High-side FET On-Resistance	R_{DSON}	V_{IN} = 2.5V		80		mΩ
		V_{IN} = 5.0V		29	58	
Low-side FET On-Resistance		V_{IN} = 2.5V		40		
		V_{IN} = 5.0V		25	45	
High-side FET Switch Current Limit, DC	I_{LIM_H}			5.5		A
Low-side FET Switch Current Limit, DC	I_{LIM_L}			3.7		A
Low-side FET Negative Current Limit, DC	I_{LIM_LN}			-2.4		A
Switching Frequency	f_{SW}	I_{OUT} = 1A, V_{OUT} = 1.8V		4		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

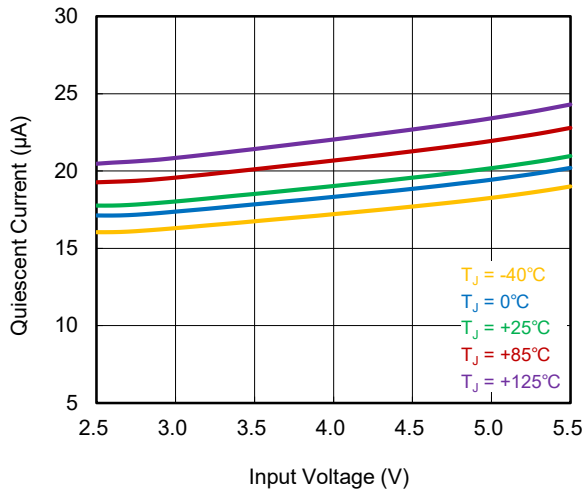
High-side FET On-Resistance vs. Input Voltage



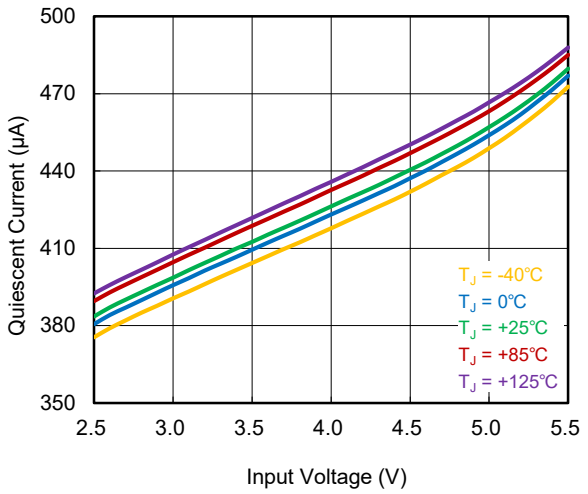
Low-side FET On-Resistance vs. Input Voltage



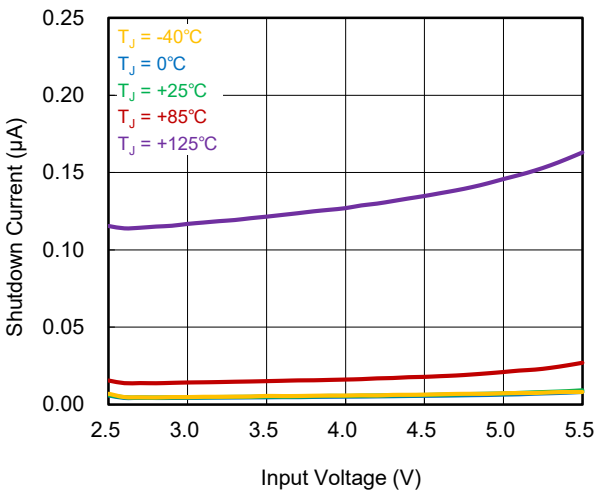
Quiescent Current vs. Input Voltage (SGM61023A)



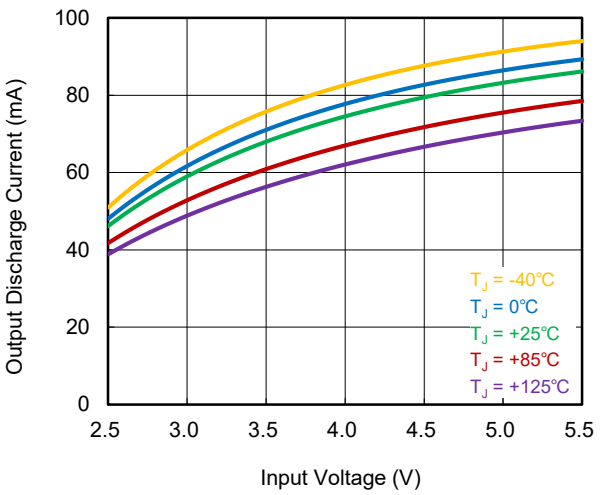
Quiescent Current vs. Input Voltage (SGM61023B)



Shutdown Current vs. Input Voltage



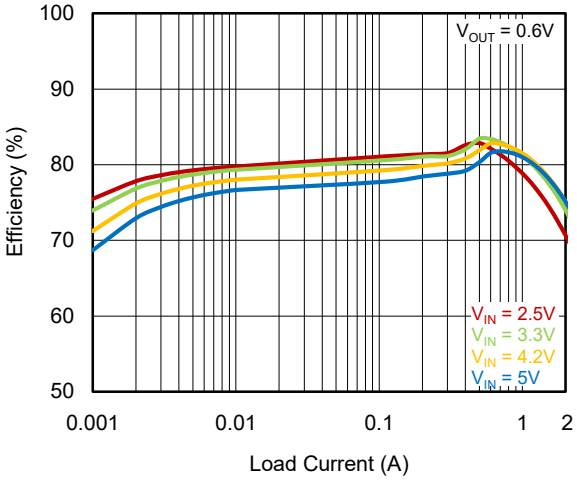
Output Discharge Current vs. Input Voltage



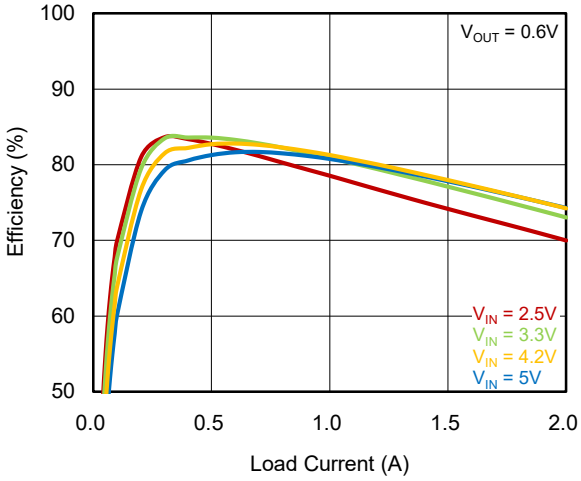
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

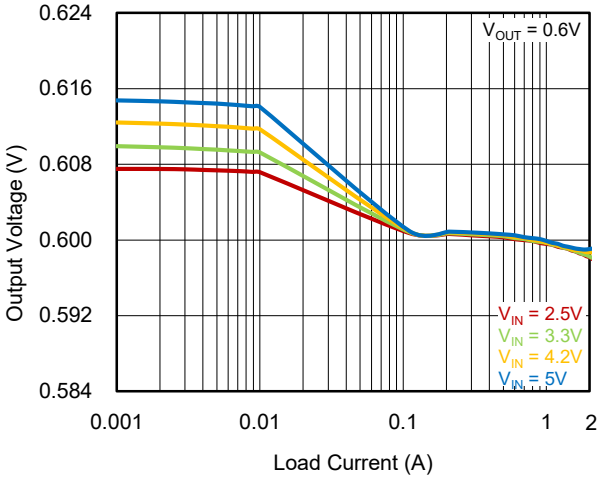
Efficiency vs. Load Current (SGM61023A)



Efficiency vs. Load Current (SGM61023B)



Load Regulation (SGM61023A)



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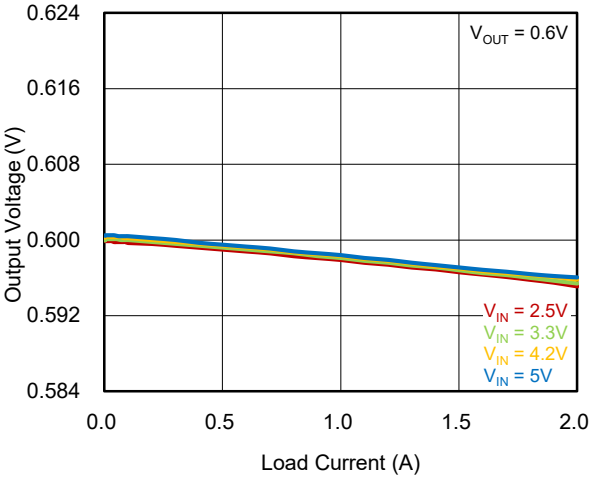

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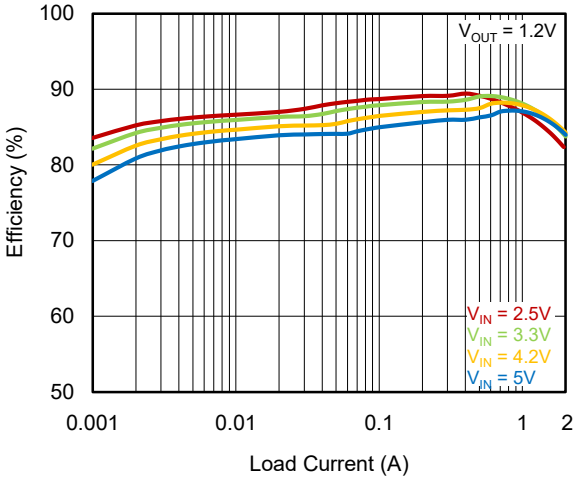

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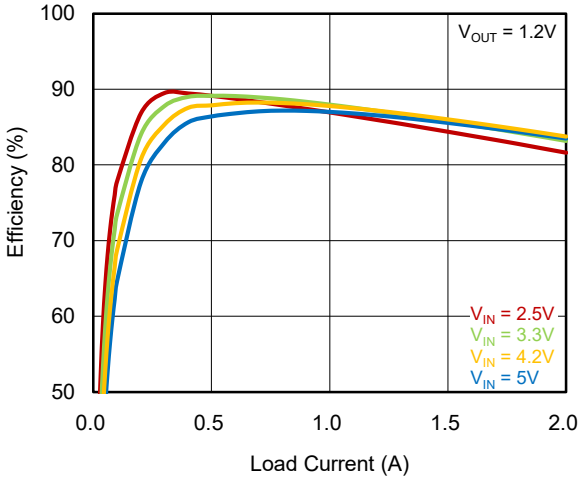
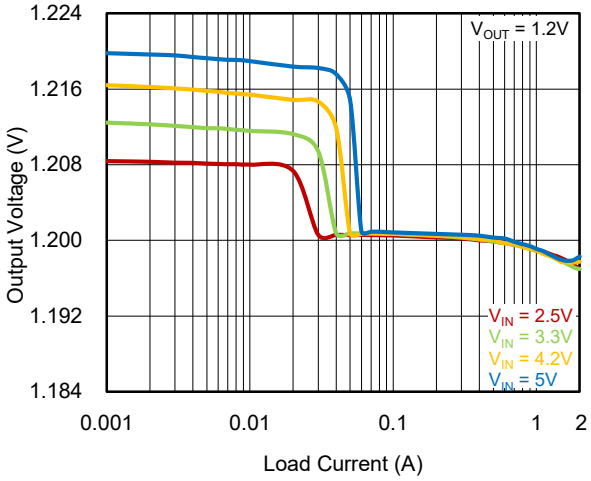


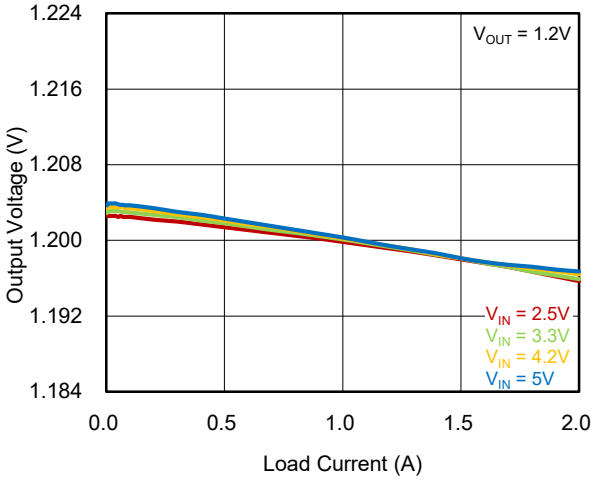
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

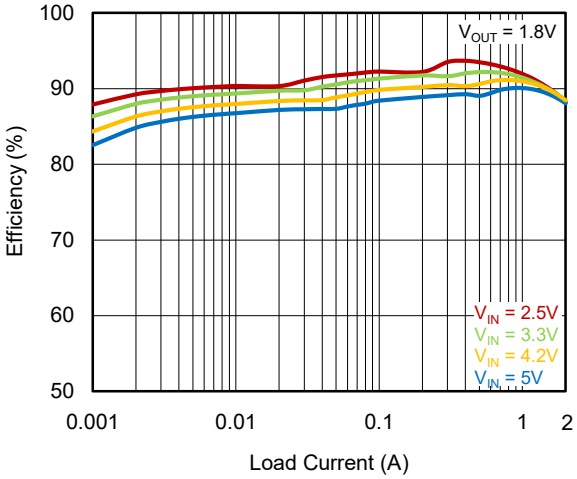
Load Regulation (SGM61023A)



Load Regulation (SGM61023B)



Efficiency vs. Load Current (SGM61023A)



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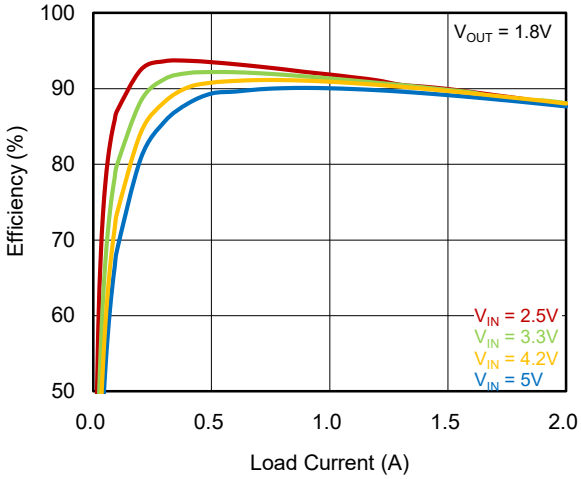

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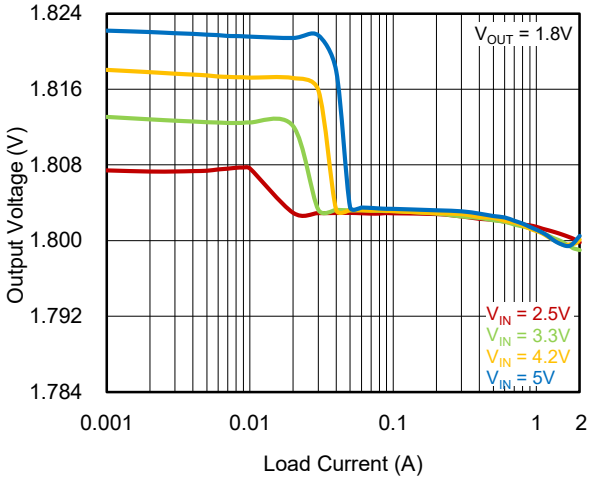

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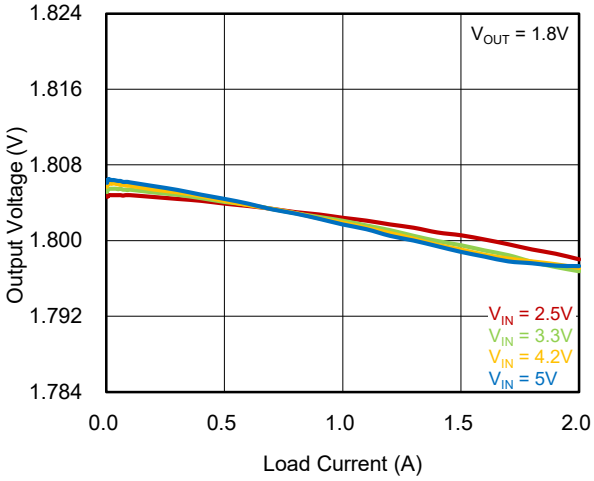
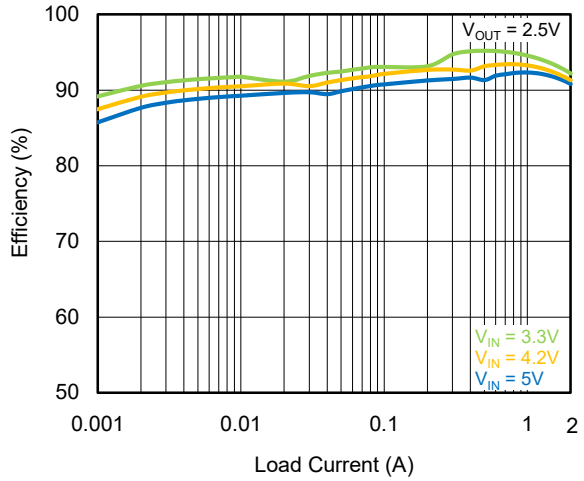


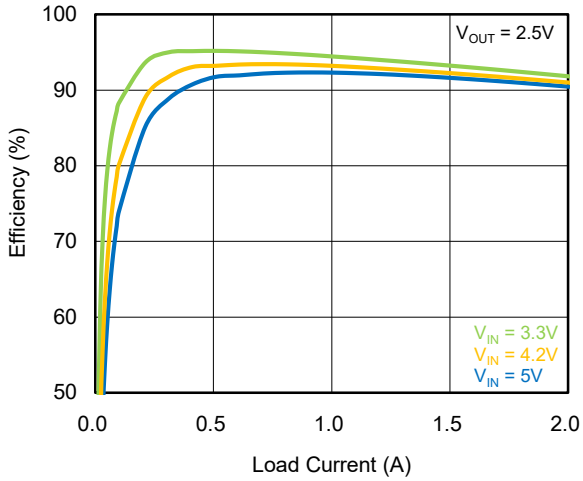
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

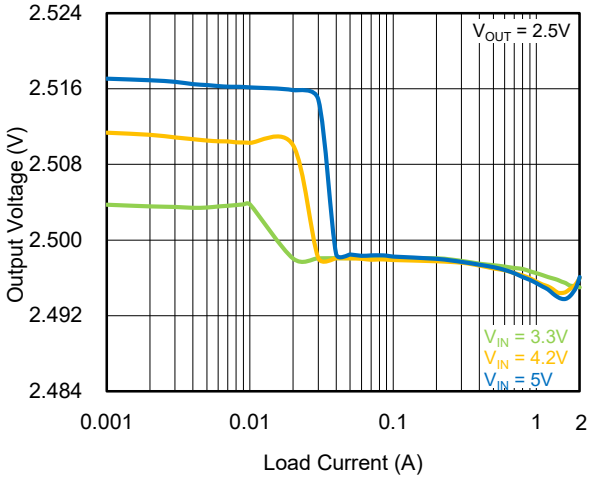
Efficiency vs. Load Current (SGM61023A)



Efficiency vs. Load Current (SGM61023B)



Load Regulation (SGM61023A)



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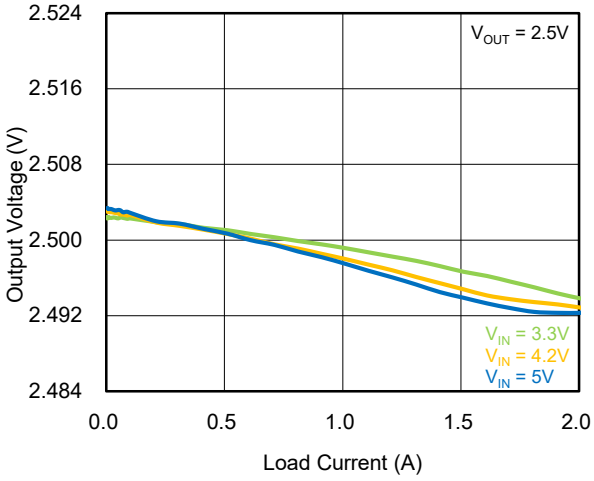
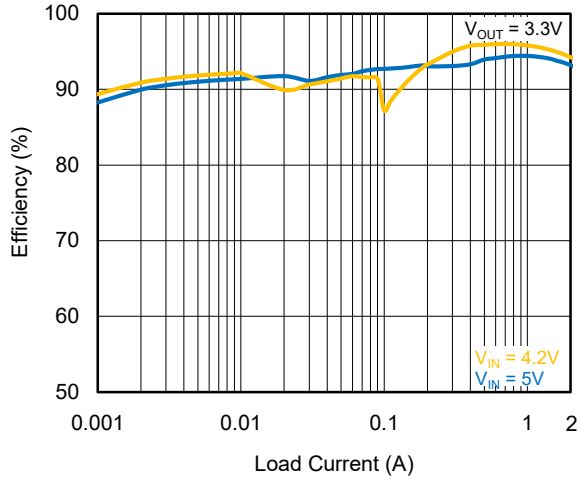
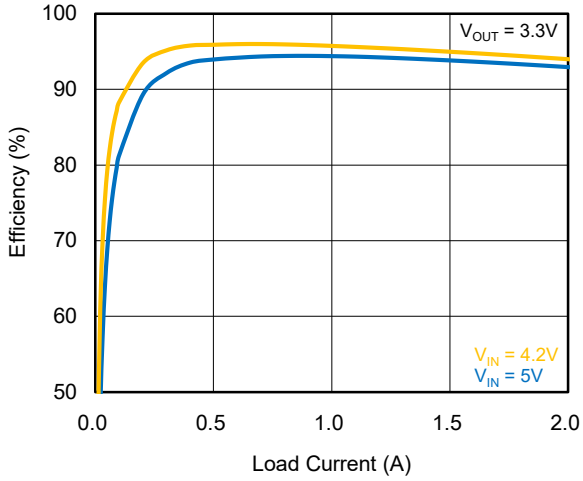


Efficiency vs. Load Current (SGM61023A)



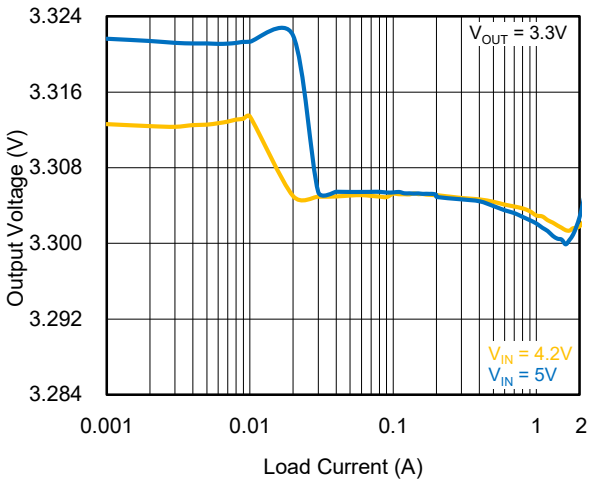
Efficiency vs. Load Current (SGM61023B)



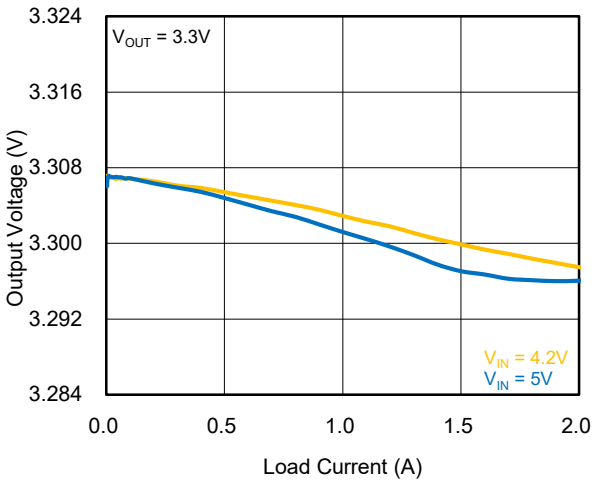
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

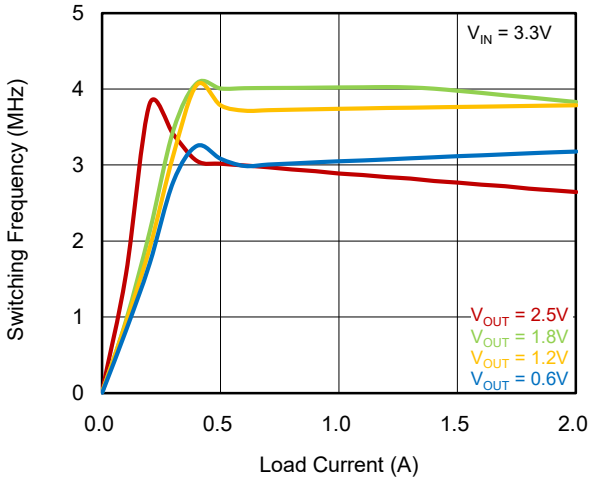
Load Regulation (SGM61023A)



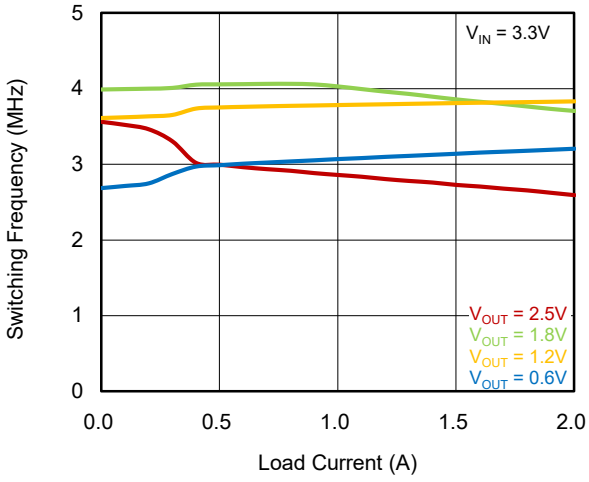
Load Regulation (SGM61023B)



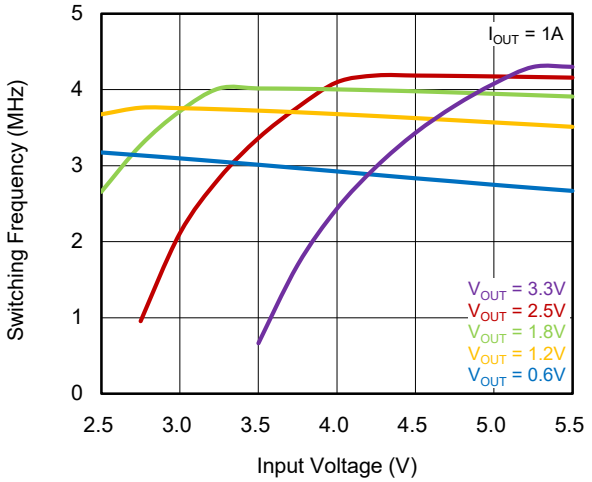
Switching Frequency vs. Load Current (SGM61023A)



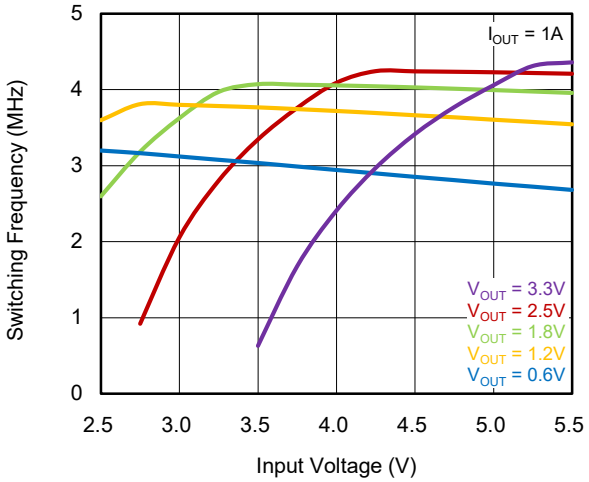
Switching Frequency vs. Load Current (SGM61023B)



Switching Frequency vs. Input Voltage (SGM61023A)



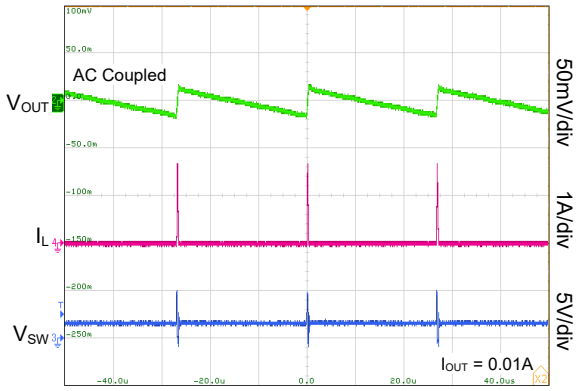
Switching Frequency vs. Input Voltage (SGM61023B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

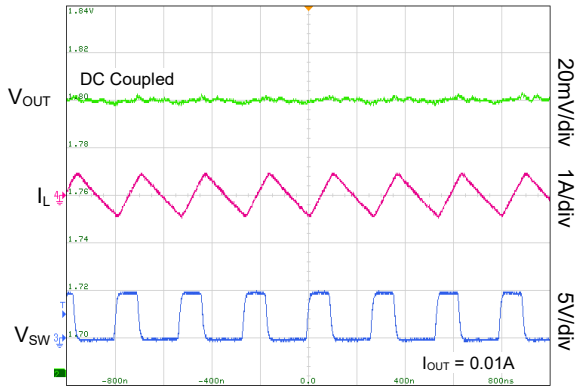
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

PSM Operation (SGM61023A)



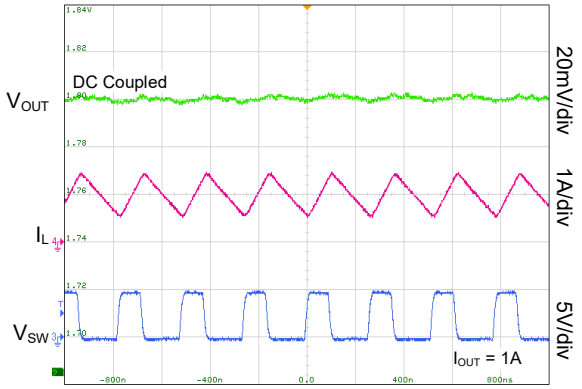
Time (10μs/div)

FPWM Operation (SGM61023B)



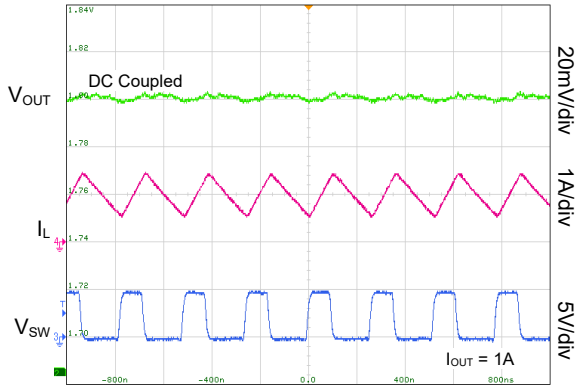
Time (200ns/div)

PWM Operation (SGM61023A)



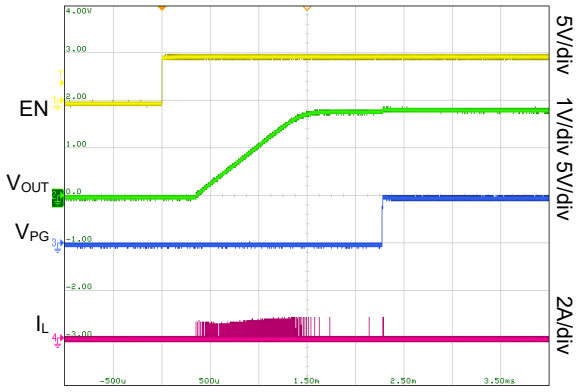
Time (200ns/div)

FPWM Operation (SGM61023B)



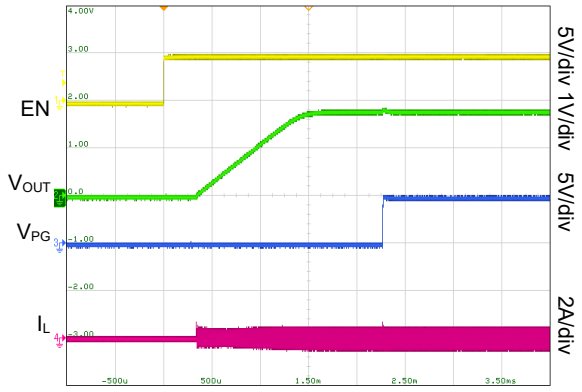
Time (200ns/div)

EN On without Load (SGM61023A)



Time (500μs/div)

EN On without Load (SGM61023B)

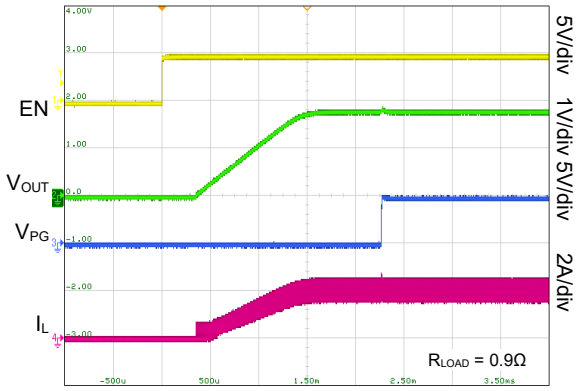


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

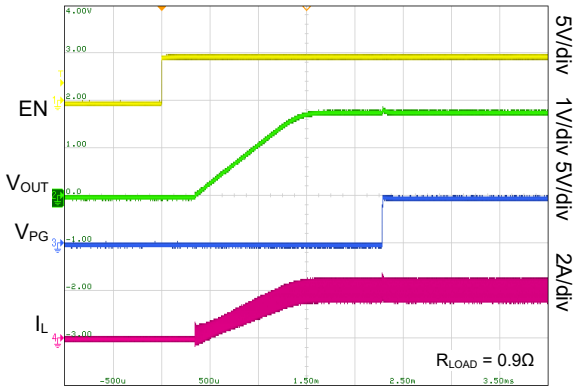
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

EN On with Load (SGM61023A)



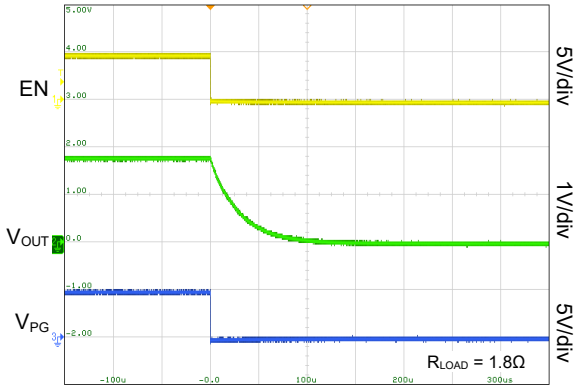
Time (500μs/div)

EN On with Load (SGM61023B)



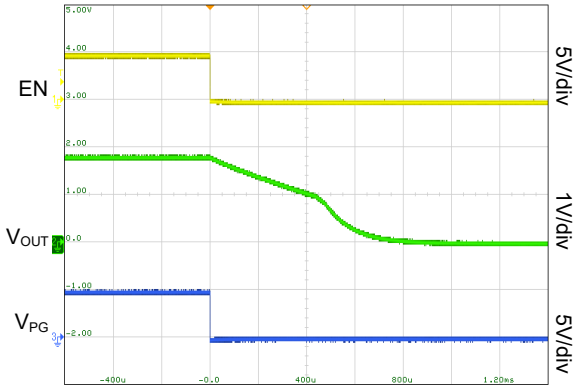
Time (500μs/div)

EN Off with Load (SGM61023A/B)



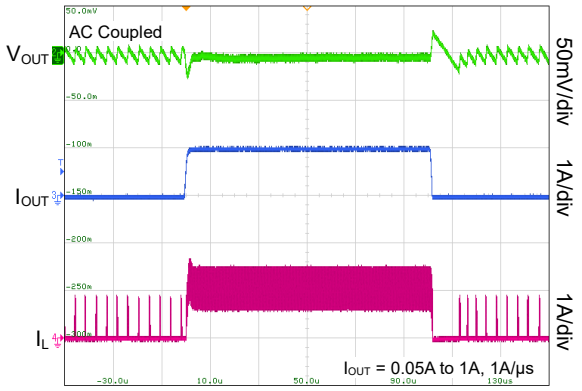
Time (50μs/div)

EN Off without Load (SGM61023A/B)



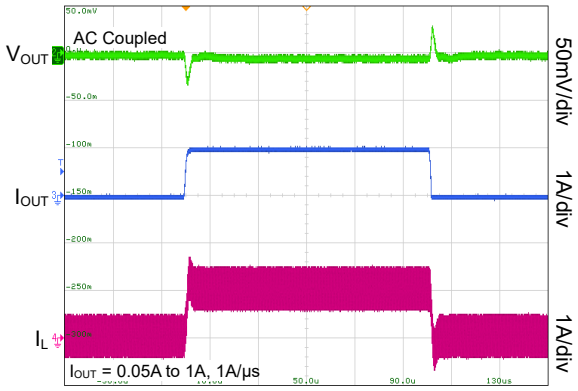
Time (200μs/div)

Load Transient (SGM61023A)



Time (20μs/div)

Load Transient (SGM61023B)

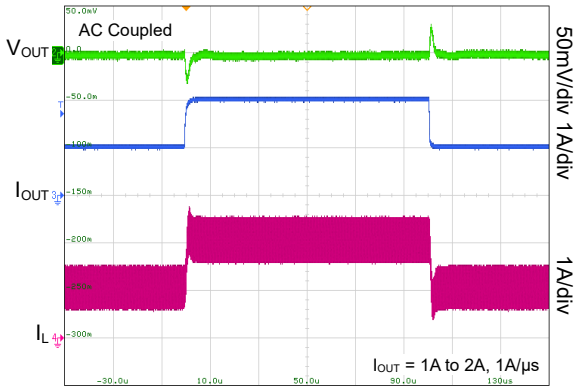


Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

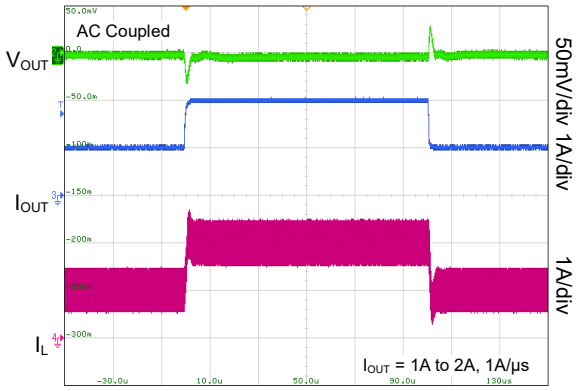
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 0.24μH (DCR = 25mΩ), and C_{OUT} = 2 × 10μF, unless otherwise noted.

Load Transient (SGM61023A)



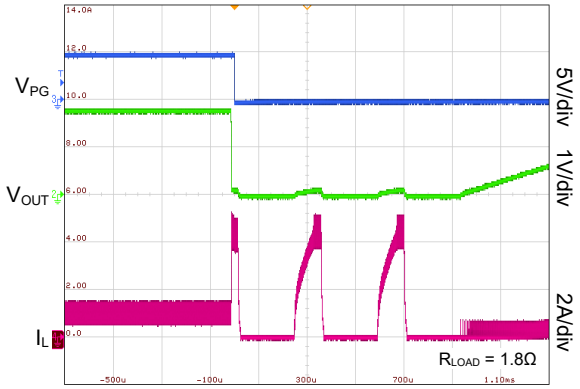
Time (20μs/div)

Load Transient (SGM61023B)



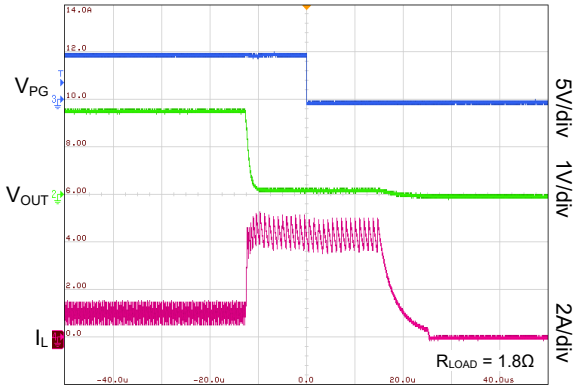
Time (20μs/div)

Hiccup Short-Circuit Protection



Time (200μs/div)

Hiccup Short-Circuit Protection (Zoom-In)



Time (10μs/div)

FUNCTIONAL BLOCK DIAGRAM

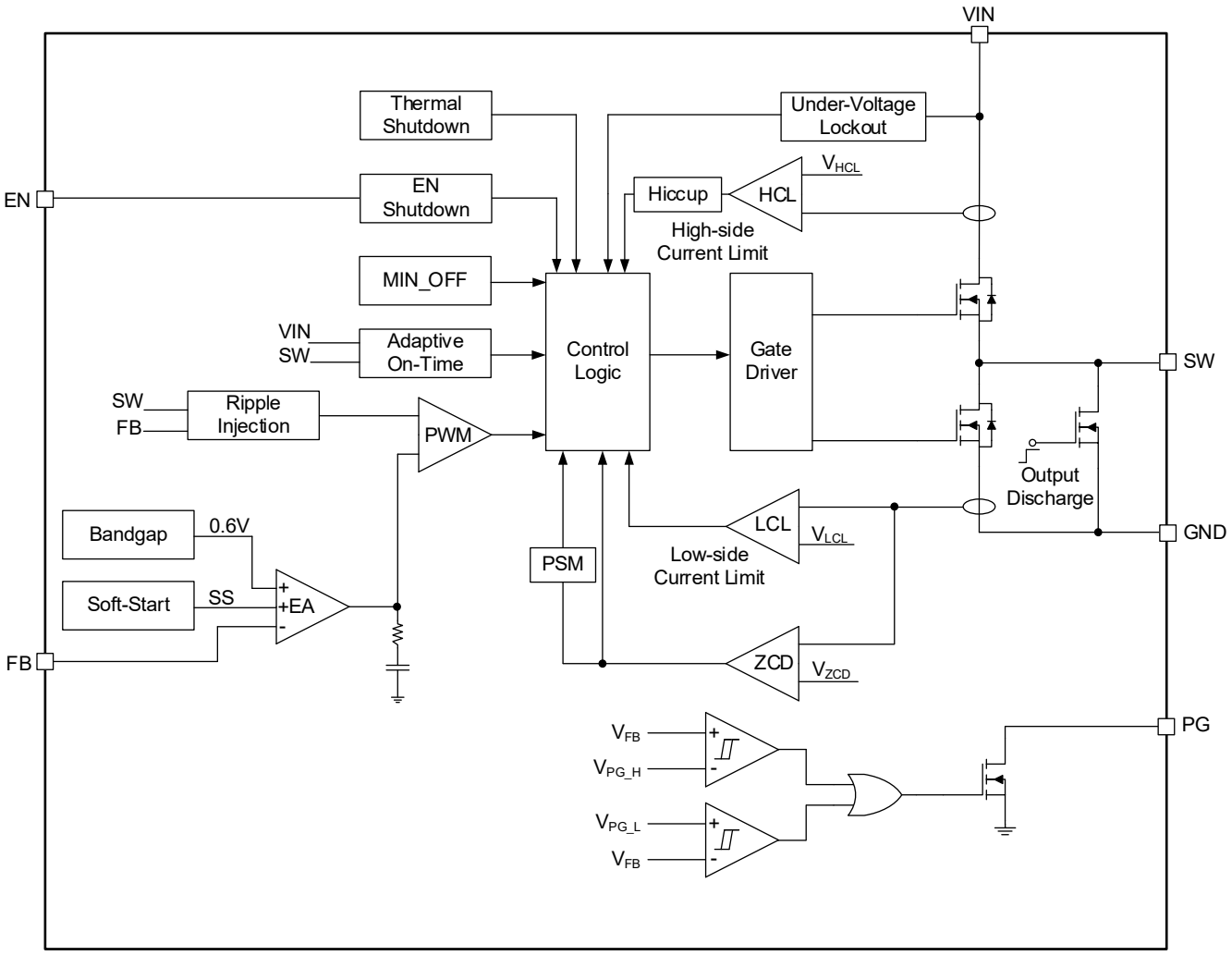


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGM61023 is a series of high-frequency synchronous Buck converter with AHP-COT architecture and advanced regulation topology.

For SGM61023A, the device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. For SGM61023B, the device works in force PWM mode at full load range. In PWM mode, the device works with a nominal switching frequency of 4MHz.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 160mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.05μA (TYP). During shutdown, an internal FET is turned on and connects the SW pin to the GND for smooth discharge of the output.

Power Good (PG)

There is the PG function inside the device. PG is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail which is no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. Table 1 shows how the PG state is changed in different conditions. PG remains low until V_{OUT} comes up to 96% or down to 105% of its nominal (set) value. PG function has hysteresis effect. When PG is high, it will go low if V_{OUT} changes down to 92% or up to 110% of its nominal (set) value. When the device is disabled, under-voltage lockout or in thermal shutdown, the PG pin is driven to low.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing. If not used, the PG pin needs to keep float. When the device is enabled and operates, the transition of the PG state from Low to Hi-Z requires continuous fulfillment of the conditions in Table 1 for 92μs. Conversely, the transition from Hi-Z to Low requires continuous fulfillment of the conditions for 13μs. However if it is disabled by EN or V_{UVLO}, PG will turn to low immediately.

Table 1. PG Output State in Different Conditions

Device Information		PG State	
		Hi-Z	Low
Enable (EN = High)	V_{FB} ≥ 0.576V	√	
	V_{FB} ≤ 0.552V		√
	V_{FB} ≤ 0.63V	√	
	V_{FB} ≥ 0.66V		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	V_{IN} < 1.4V	Uncertain	

Soft-Start and Pre-biased Startup

When EN is set to logic high and after internal delay, the device starts switching and V_{OUT} increases with 1.4ms (TYP) internal soft-start circuit. The soft-start is critical to prevent excessive inrush currents and to avoid triggering of the over-current protection to provide a smooth output rise. It also prevents extreme input voltage drops due to large inrush current over the high-impedance batteries and input sources that can interrupt the power-up. The device is also capable of starting with a pre-biased output capacitor when it is powered up or enabled.

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM), which occurs at medium to heavy load or the force PWM mode, the device works in pulse width modulation (PWM) operation. Then a fixed on-time architecture is activated and the typical on-time is t_{ON} = 250ns × (V_{OUT}/V_{IN}).

Power-Save Mode (PSM)

Once the load current decreases, the SGM61023A will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous and the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor. In PSM mode, the switching frequency is greatly reduced with the decrease of load current.

DETAILED DESCRIPTION (continued)

Minimum Duty Cycle and 100% Duty Cycle

Due to the reduction of the switching frequency for regulation, the device has no minimum duty cycle set. When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

• V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.
• I_{OUT_MAX} is maximum output current.
• R_{DSON} is high-side MOSFET on-resistance.
• R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection (Hiccup)

Limiting the switch current protects the switch itself and also prevents over-current of the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak current.

If 32 cycles consecutive repetition of this event occurs, the device stops switching and turns the output discharge circuit on. A new startup is initiated automatically (hiccup) after 220μs (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 20℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGM61023 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

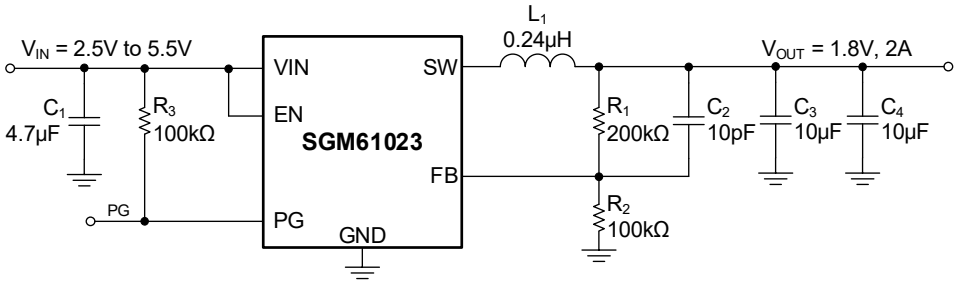


Figure 3. 1.8V Output Voltage Application

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.8V
Output Ripple Voltage	< 20mV (CCM)
Maximum Output Current	2A

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	4.7μF, Ceramic Capacitor, 6.3V, X7R, Size 0603	Standard
C_2	10pF, Ceramic Capacitor, 50V, Size 0603	Standard
C_3, C_4	10μF, Ceramic Capacitor, 10V, X5R, Size 0603	Standard
L_1	0.24μH, Power Inductor, DCR = 25mΩ, Size 0603	Standard
R_1	200kΩ, Chip Resistor, 1/16W,1%, Size 0603	Standard
R_2	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Input and Output Capacitor Selection

The high frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 4.7μF ceramic capacitor with X7R and 0603 size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

For output capacitor design, output ripple, transient response and loop stability should be considered. Choosing ceramic capacitor with X5R or better dielectric is very important for temperature characteristics.

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 2 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where:

- I_{OUT_MAX} is the maximum output DC current.
- ΔI_L is the inductor current ripple (peak-to-peak).
- f_{SW} is switching frequency (MHz).
- L is the inductance value (μH).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 3 to set the desired output voltage. First choose R_2 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_2 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (3)$$

A feedforward capacitor improves transient response to the load steps and reduces the output ripple in PSM.

LC Filter

The inductor (L) and the output capacitor (C) form a low-pass filter for removing switching AC components and passing the DC voltage to the output. Note that variations are as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the C_{OUT}, due to tolerances and bias voltage derating, the effective capacitance can vary by +20% to -35%.

Thermal Considerations

Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGM61023 is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself plays a significant role in helping to transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61023.

- Place the input/output capacitors and the inductor as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.
- Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

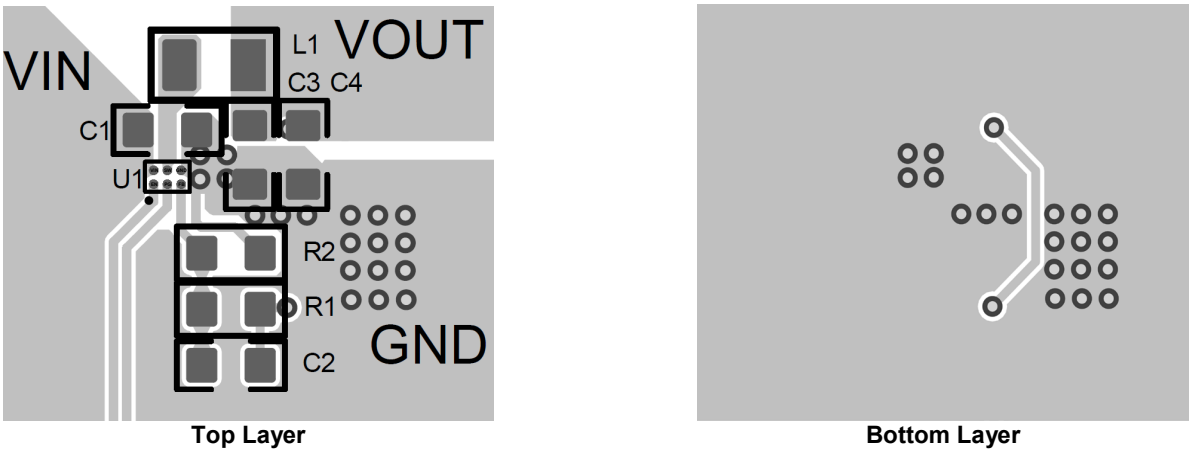


Figure 4. PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

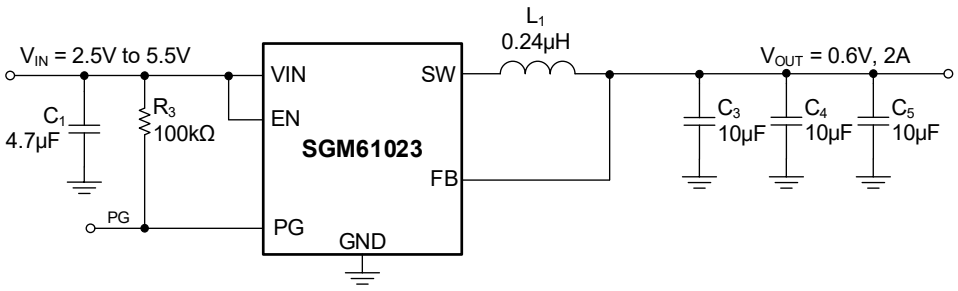


Figure 5. 0.6V Output Voltage Application

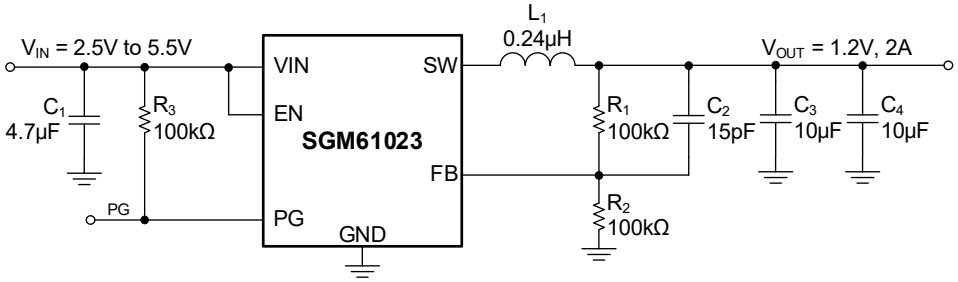


Figure 6. 1.2V Output Voltage Application

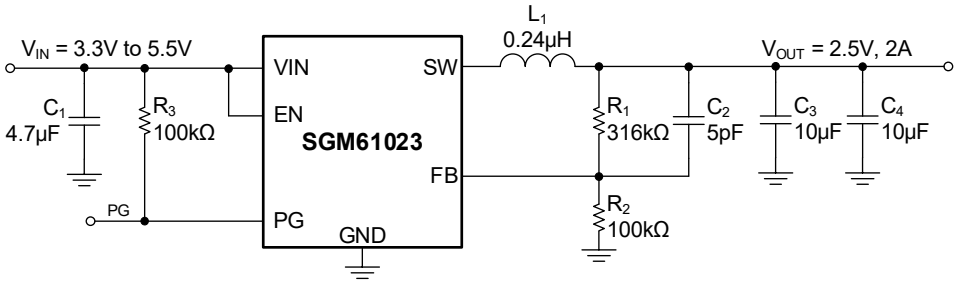


Figure 7. 2.5V Output Voltage Application

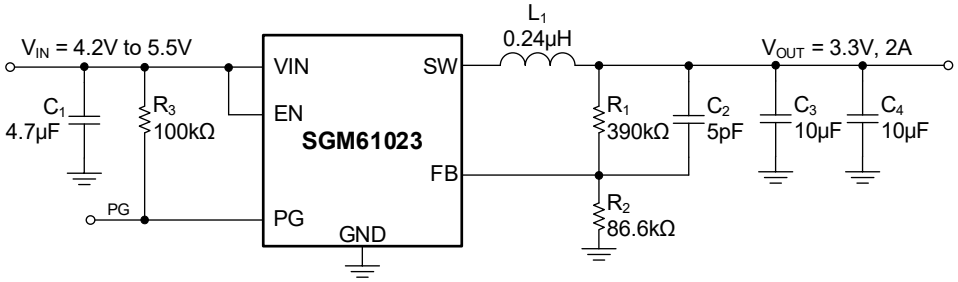


Figure 8. 3.3V Output Voltage Application

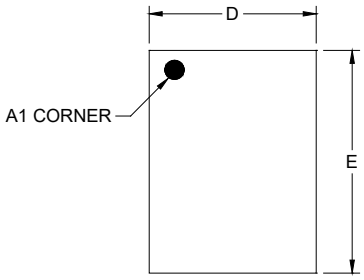
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

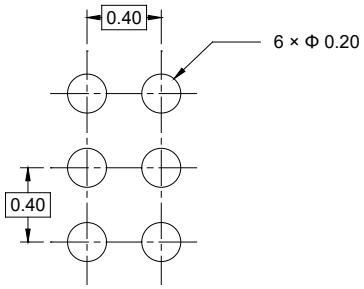
Changes from Original to REV.A (JULY 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

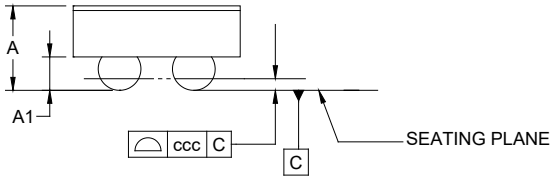
WLCSP-0.9×1.2-6B-A



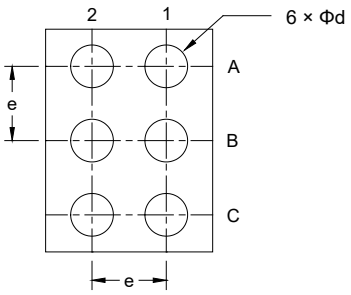
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



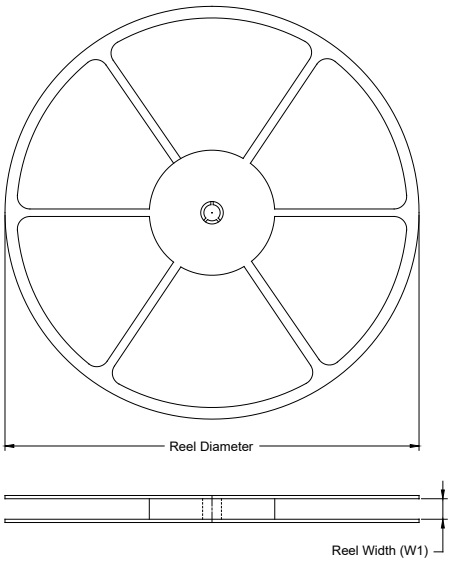
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.500
A1	0.160	-	0.200
D	0.870	-	0.930
E	1.170	-	1.230
d	0.200	-	0.260
e	0.400 BSC		
ccc	0.050		

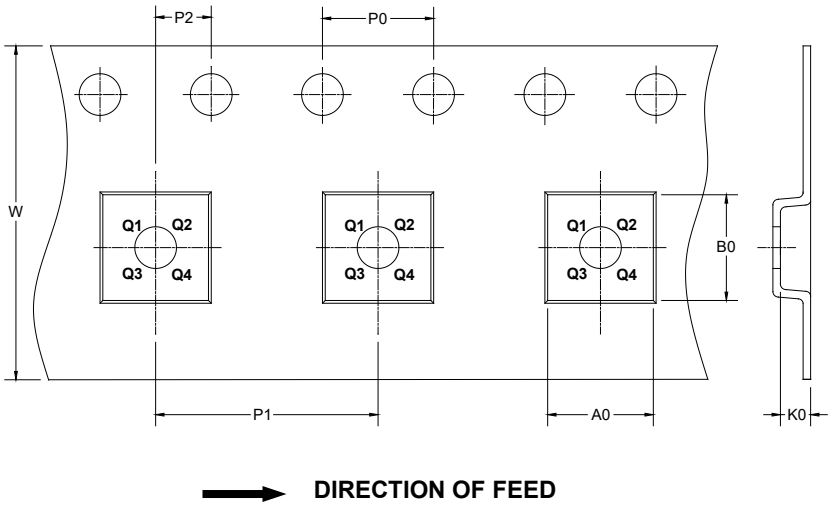
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



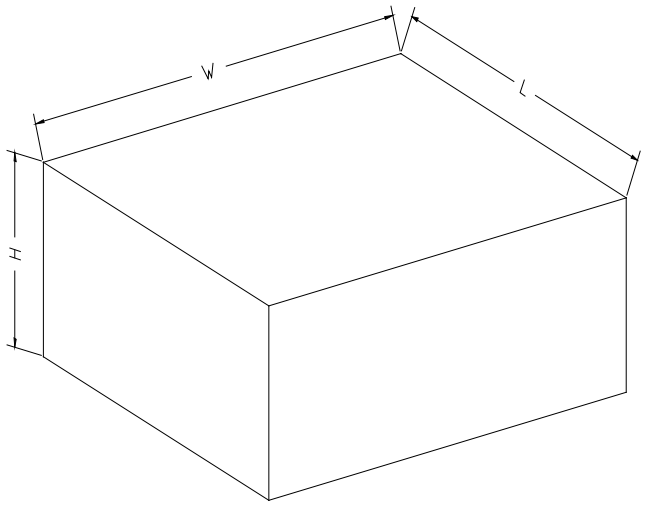
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.9×1.2-6B-A	7"	9.5	1.00	1.30	0.56	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002