

GENERAL DESCRIPTION

The SGM2538 series of eFuses feature comprehensive protection functions, robust operation, accurate limit threshold and compact package which are very suitable for various system applications.

The SGM2538 provides fixed over-voltage clamp (OVC), adjustable over-current protection (OCP) and fast short-circuit protection (SCP). The device also provides adjustable soft-start (SS) function to manage inrush current through external resistor. When the device junction temperature exceeds +155 °C, the thermal shutdown function works and turns off the device. Once in thermal shutdown, the latch-off and auto-retry options are available.

Besides the above features, the SGM2538 has additional configurable functions using the BFET pin. The BFET pin can be used to drive an external N-FET connected back to back with the internal pass FET to provide reverse current block (RCB) function. It can also be used as fault event indicator through an external transistor.

The SGM2538 is available in a Green TDFN-3×3-10AL package.

FEATURES

- Wide Input Voltage Range from 4.5V to 13.8V with Surge up to 20V
- On-Resistance: 27mΩ (TYP)
- Programmable Current Limit: 1A to 5A
- ±8% I_{LIMIT} Accuracy at 3.7A
- Reverse Current Blocking Support
- Programmable OUT Slew Rate, UVLO
- Built-in Thermal Shutdown
- Fixed Over-Voltage Clamp
 - ♦ 6.1V: SGM2538Ax
 - ♦ 15V: SGM2538Bx
- Fault Response
 - ♦ Auto-Retry: SGM2538xA
 - ♦ Latch-Off: SGM2538xL
- UL Recognized Component (File No. E532373*)
- Available in a Green TDFN-3×3-10AL Package

APPLICATIONS

PCI-E SSD
Servers and Block Supplies
Motherboard Power Management

TYPICAL APPLICATION

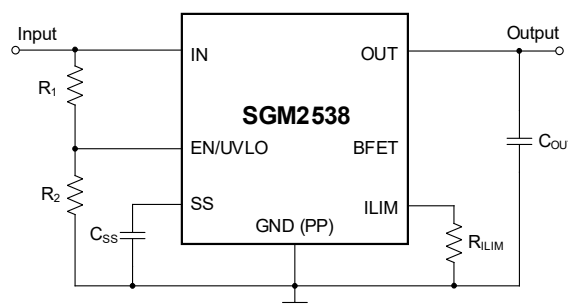


Figure 1. Typical Application Circuit

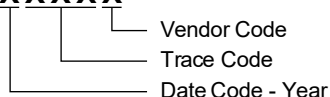
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2538AA	TDFN-3×3-10AL	-40°C to +125°C	SGM2538AAXTGZ10G/TR	SGM 0NKGZ XXXXX	Tape and Reel, 4000
SGM2538AL	TDFN-3×3-10AL	-40°C to +125°C	SGM2538ALXTGZ10G/TR	SGM 0NLGZ XXXXX	Tape and Reel, 4000
SGM2538BA	TDFN-3×3-10AL	-40°C to +125°C	SGM2538BAXTGZ10G/TR	SGM 0NMGZ XXXXX	Tape and Reel, 4000
SGM2538BL	TDFN-3×3-10AL	-40°C to +125°C	SGM2538BLXTGZ10G/TR	SGM 0D8GZ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

IN -0.3V to 20V

IN (10ms Transient) 22V

Output Voltage

OUT -0.3V to $V_{IN} + 0.3V$

OUT (transient < 1μs) -1.2V

Voltage

ILIM -0.3V to 7V

EN/UVLO -0.3V to 7V

SS -0.3V to 7V

BFET -0.3V to 30V

Package Thermal Resistance

TDFN-3×3-10AL, θ_{JA} 45°C/W

TDFN-3×3-10AL, θ_{JB} 16.7°C/W

TDFN-3×3-10AL, $\theta_{JC (TOP)}$ 43.1°C/W

TDFN-3×3-10AL, $\theta_{JC (BOT)}$ 6.9°C/W

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10s) +260°C

ESD Susceptibility

HBM 2000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range

IN (SGM2538Ax) 4.5V to 5.5V

IN (SGM2538Bx) 4.5V to 13.8V

BFET 0V to $V_{IN} + 6V$

EN/UVLO, SS 0V to 6V

ILIM 0V to 3V

Continuous Output Current, I_{OUT} 0A to 5A

Resistance, ILIM 10kΩ to 162kΩ

External Capacitance

OUT 0.1μF to 1000μF

SS < 1000nF

Operating Junction Temperature Range, T_J -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

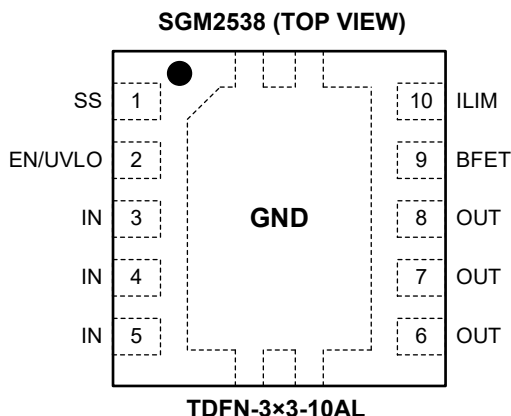
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

NAME	PIN	FUNCTION
1	SS	Soft-Start Pin. The capacitor between SS and GND pins sets the slew rate of output voltage.
2	EN/UVLO	Enable Input or Under-Voltage Lockout. As an enable pin, setting EN/UVLO pin high activates the device. As an UVLO pin, the UVLO threshold can be programmed through an external resistor divider.
3, 4, 5	IN	Power Input Pin. Power input and supply voltage of the device.
6, 7, 8	OUT	Power Output Pin.
9	BFET	N-FET Driver. Connect this pin to the gate of a blocking N-FET. This pin can be left floating if it is not used.
10	ILIM	Current Limit Programming Pin. A resistor between ILIM and GND pins sets the overload and short-circuit limit levels.
Exposed Pad	GND	Ground.

ELECTRICAL CHARACTERISTICS

($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{ILIM} = 100\text{k}\Omega$, $C_{SS} = \text{open}$, typical values are at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage and Under-Voltage Lockout							
UVLO Threshold	V _{UVR}	Rising		4.15	4.3	4.45	V
UVLO Hysteresis	V _{UVR_HYS}				170		mV
Supply Current, Enabled	I _{Q_ON}	V _{EN/UVLO} = 2V		150	210	270	μA
Supply Current, Disabled	I _{Q_OFF}	V _{EN/UVLO} = 0V			1.1	3.5	μA
Over-Voltage Clamp	V _{OVC}	SGM2538Ax	V _{IN} > 6.75V, I _{OUT} = 10mA	5.7	6.1	6.6	V
		SGM2538Bx	V _{IN} > 16.5V, I _{OUT} = 10mA	13.9	15	16.1	
Enable and Under-Voltage Lockout (EN/UVLO)							
EN/UVLO Threshold Voltage	V _{ENR}	Rising		1.35	1.41	1.48	V
	V _{ENF}	Falling		1.29	1.35	1.41	V
EN Input Leakage Current	I _{EN}	0V ≤ V _{EN/UVLO} ≤ 5V		-500	0	500	nA
Output Ramp Control (SS)							
SS Charging Current ⁽¹⁾	I _{SS}	V _{SS} = 0V			200		nA
SS Discharging Resistance	R _{SS}	V _{EN/UVLO} = 0V, I _{SS} = 10mA sinking		45	75	110	Ω
SS Max Capacitor Voltage ⁽¹⁾	V _{SSMAX}				5		V
SS to OUT gain ⁽¹⁾	GAIN _{SS}	ΔV _{SS}			4.88		V/V
Current Limit Programming (ILIM)							
ILIM Bias Current ⁽¹⁾	I _{ILIM}				10		μA
Overload Current Limit ⁽²⁾	I _{OL}	R _{ILIM} = 10kΩ, V _{IN-OUT} = 1V			1.2		A
		R _{ILIM} = 45.3kΩ, V _{IN-OUT} = 1V		1.99	2.2	2.42	
		R _{ILIM} = 100kΩ, V _{IN-OUT} = 1V		3.43	3.72	4.01	
		R _{ILIM} = 150kΩ, V _{IN-OUT} = 1V		4.70	5.13	5.57	
		Shorted or open resistor current limit			0.92		
Short-Circuit Current Limit ⁽²⁾	I _{SC}	SGM2538Ax	R _{ILIM} = 10kΩ, V _{IN-OUT} = 5V		0.96		A
			R _{ILIM} = 45.3kΩ, V _{IN-OUT} = 5V	1.45	1.80	2.16	
			R _{ILIM} = 100kΩ, V _{IN-OUT} = 5V	2.68	3.20	3.61	
			R _{ILIM} = 150kΩ, V _{IN-OUT} = 5V	3.72	4.40	5.06	
		SGM2538Bx	R _{ILIM} = 10kΩ, V _{IN-OUT} = 12V		0.97		
			R _{ILIM} = 45.3kΩ, V _{IN-OUT} = 12V	1.35	1.79	2.22	
			R _{ILIM} = 100kΩ, V _{IN-OUT} = 12V	1.18	1.84	2.51	
			R _{ILIM} = 150kΩ, V _{IN-OUT} = 12V	1.18	1.85	2.51	
Fast-Trip Comparator Level W.R.T. Overload Current Limit ⁽¹⁾	RATIO _{FASTRIP}	I _{FASTRIP} : I _{OL}			160%		
ILIM Open Resistor Detect Threshold ⁽¹⁾	V _{ILIM_OPEN}	V _{ILIM} rising, R _{ILIM} = open			3		V

ELECTRICAL CHARACTERISTICS

($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{ILIM} = 100\text{k}\Omega$, $C_{SS} = \text{open}$, typical values are at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pass FET Output (OUT)						
FET On-Resistance	R _{DS(on)}	T _J = +25°C	20	27	36	mΩ
		T _J = +125°C		37	46	
Out Bias Current in Off-State	I _{OUT-LKG}	V _{EN/UVLO} = 0V, V _{OUT} = 0V (sourcing)	-3	0	3	μA
	I _{OUT-SINK}	V _{EN/UVLO} = 0V, V _{OUT} = 300mV (sinking)	-3	0.2	20	
Blocking FET Gate Driver (BFET)						
BFET Charging Current ⁽¹⁾	I _{BFET}	V _{BFET} = V _{OUT}		2		μA
BFET Clamp Voltage ⁽¹⁾	V _{BFETmax}			V _{IN} + 6.2		V
BFET Discharging Resistance to GND	R _{BFETdisch}	V _{EN/UVLO} = 0V, I _{BFET} = 100mA		30		Ω
Thermal Shutdown (TSD)						
Thermal Shutdown Temperature ⁽¹⁾	T _{SD}	T _J rising		155		°C
Thermal Shutdown Hysteresis ⁽¹⁾	T _{HYS}			20		°C

TIMING REQUIREMENTS

($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{ILIM} = 100\text{k}\Omega$, $C_{SS} = \text{open}$, typical values are at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Delay Time ⁽¹⁾	t _{D_ON}	EN/UVLO↑ to I _{IN} = 100mA, 1A resistive load at OUT			120		μs
Turn-Off Delay Time ⁽¹⁾	t _{D_OFF}	EN/UVLO↓ to BFET↓, C _{BFET} = 0			370		ns
Output Ramp Control (SS)							
Output Ramp Time	t _{SS}	SGM2538Ax	EN/UVLO↑ to V _{OUT} = 4.7V, C _{SS} = 0nF	0.2	0.4	0.6	ms
			EN/UVLO↑ to V _{OUT} = 4.7V, C _{SS} = 1nF ⁽¹⁾		5.5		
		SGM2538Bx	EN/UVLO↑ to V _{OUT} = 11.7V, C _{SS} = 0nF	0.4	0.8	1.3	
			EN/UVLO↑ to V _{OUT} = 11.7V, C _{SS} = 1nF ⁽¹⁾		13		
Current Limit Programming (ILIM)							
Fast-Trip Comparator Delay ⁽¹⁾	t _{FAST-TRIP_DLY}	I _{OUT} > I _{FAST-TRIP} to switch off			300		ns
Blocking FET Gate Driver (BFET)							
BFET Turn-On Duration ⁽¹⁾	t _{BFET-ON}	SGM2538Ax	EN/UVLO↑ to V _{BFET} = 5V, C _{BFET} = 1nF		1.5		ms
			EN/UVLO↑ to V _{BFET} = 5V, C _{BFET} = 10nF		14		
		SGM2538Bx	EN/UVLO↑ to V _{BFET} = 12V, C _{BFET} = 1nF		5.5		
			EN/UVLO↑ to V _{BFET} = 12V, C _{BFET} = 10nF		52		
BFET Turn-Off Duration ⁽¹⁾	t _{BFET-OFF}	SGM2538Ax	EN/UVLO↓ to V _{BFET} = 1V, C _{BFET} = 1nF		0.4		μs
			EN/UVLO↓ to V _{BFET} = 1V, C _{BFET} = 10nF		1.8		
		SGM2538Bx	EN/UVLO↓ to V _{BFET} = 1V, C _{BFET} = 1nF		0.4		
			EN/UVLO↓ to V _{BFET} = 1V, C _{BFET} = 10nF		1.6		
Thermal Shutdown (TSD)							
Retry Delay after T _{SD} Recovery ⁽¹⁾	t _{TSD_RST}	SGM2538xA, T _J < T _{SD} - 20°C			170		ms

NOTES:

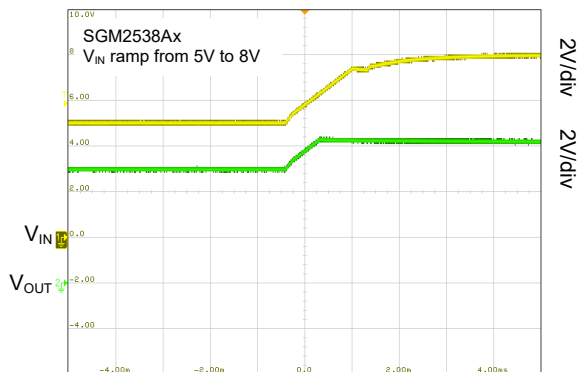
1. These parameters are for informational purposes only and do not form part of published device specifications for purposes of product warranty.
2. The pulse test technique used in this test keeps the junction temperature approximately equal to the ambient temperature.

SGM2538 5V/12V Electronic Fuses (eFuses) with OVP Function and Blocking FET Control

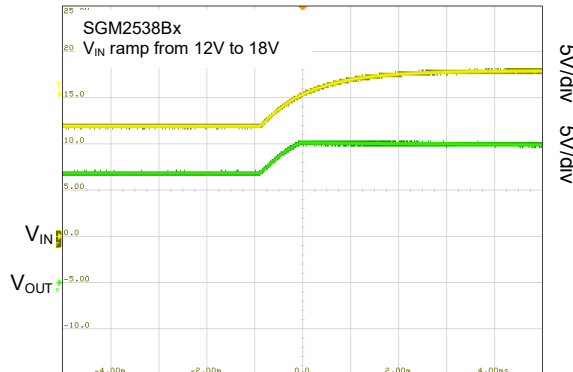
TYPICAL PERFORMANCE CHARACTERISTICS

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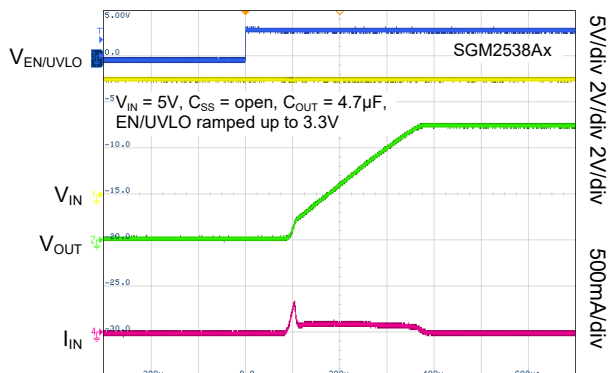
Transient: Over-Voltage Clamp



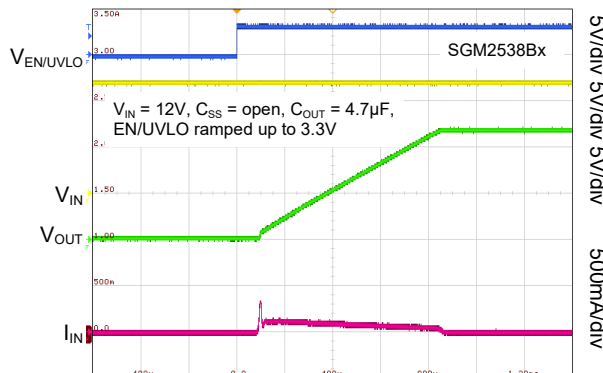
Transient: Over-Voltage Clamp



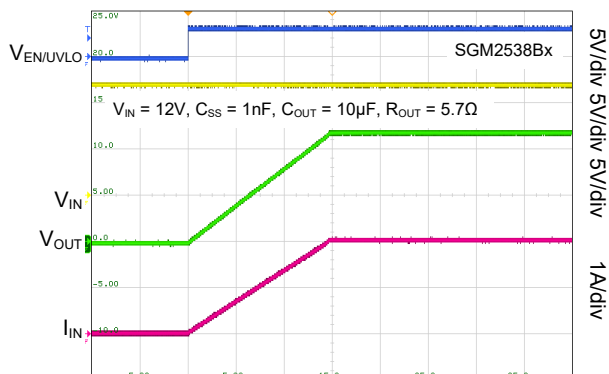
Transient: Output Ramp



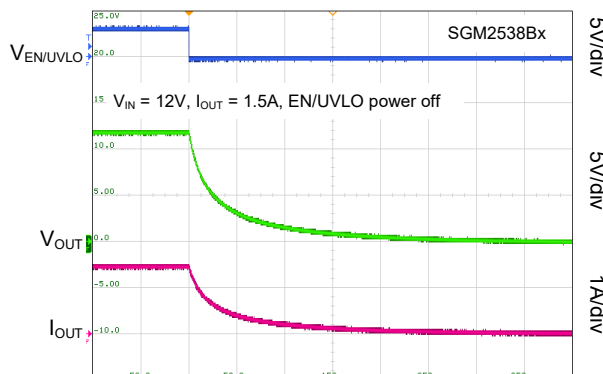
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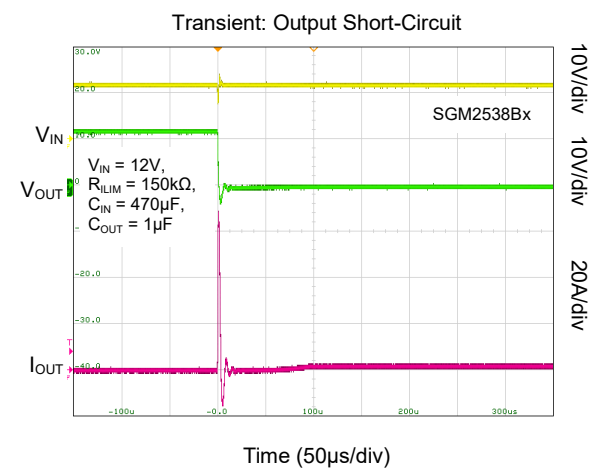
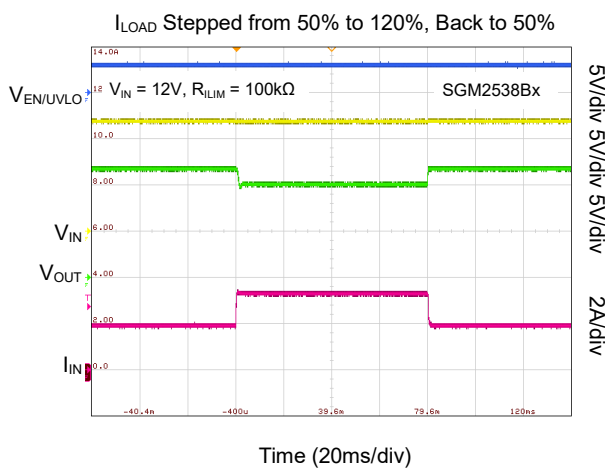
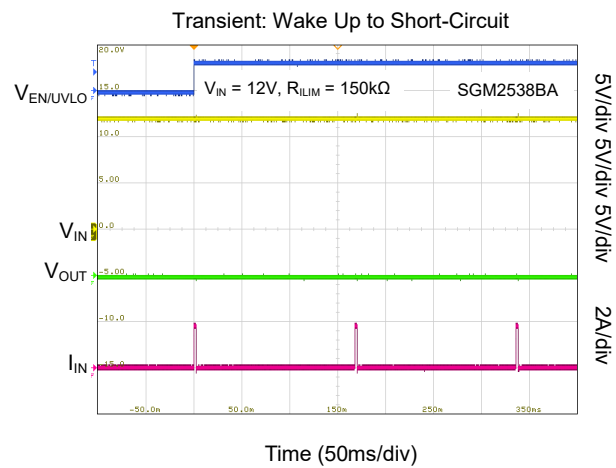
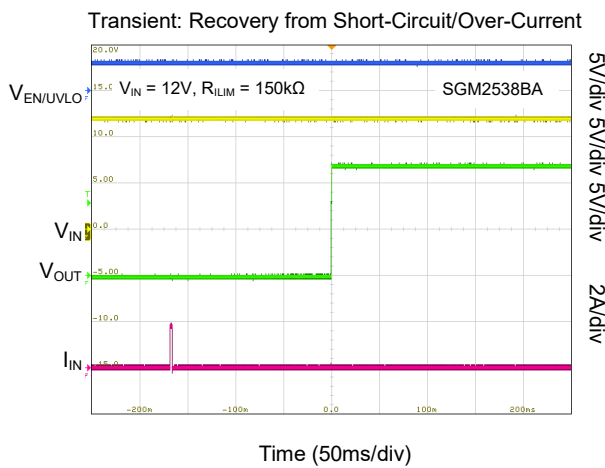
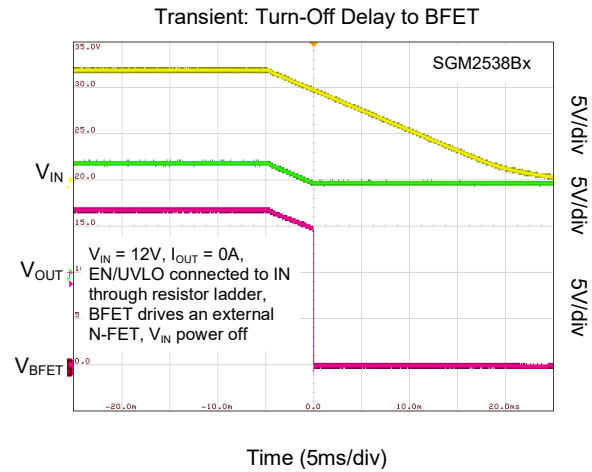
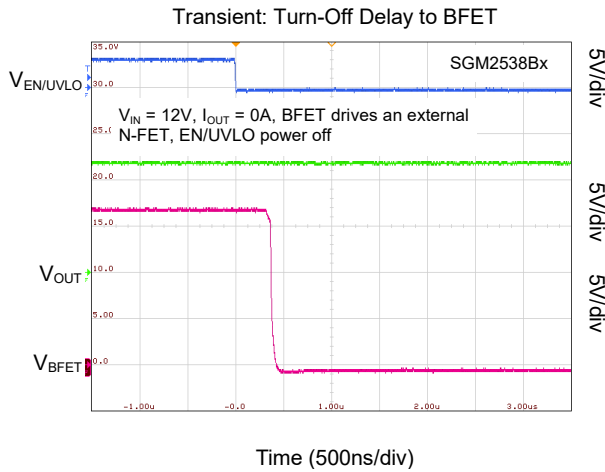


Transient: Turn-Off Delay



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

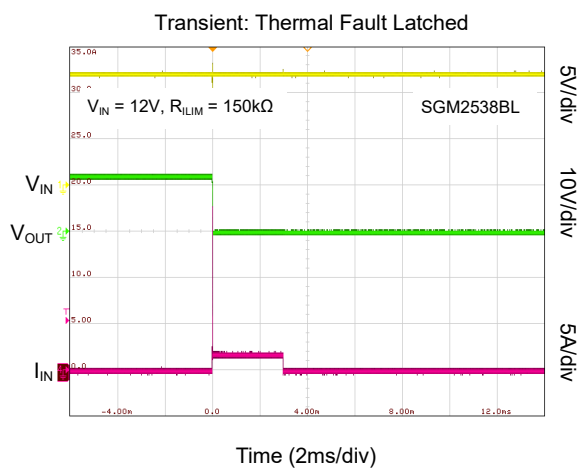
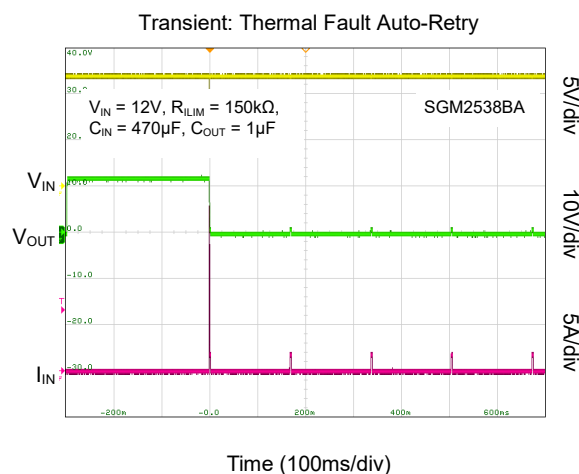
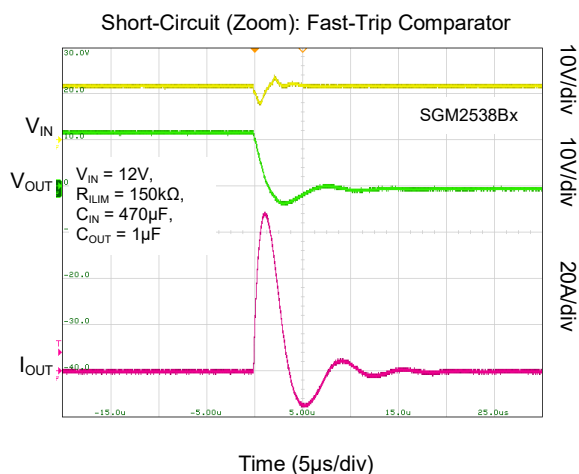
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SGM2538 5V/12V Electronic Fuses (eFuses) with OVP Function and Blocking FET Control

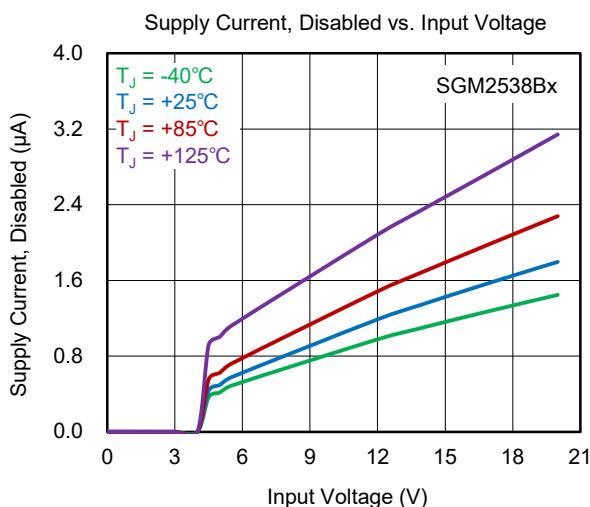
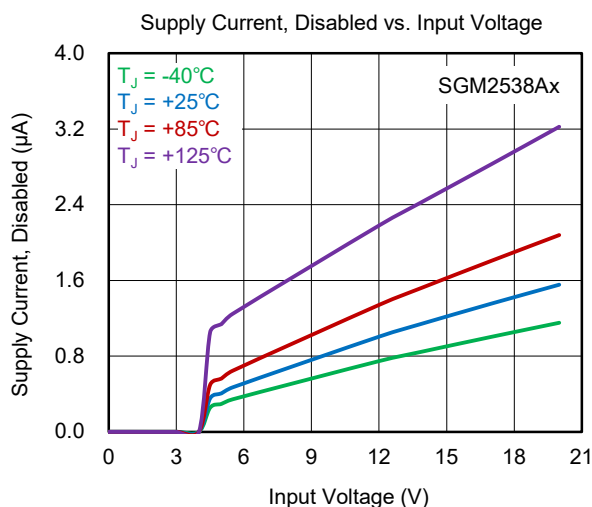
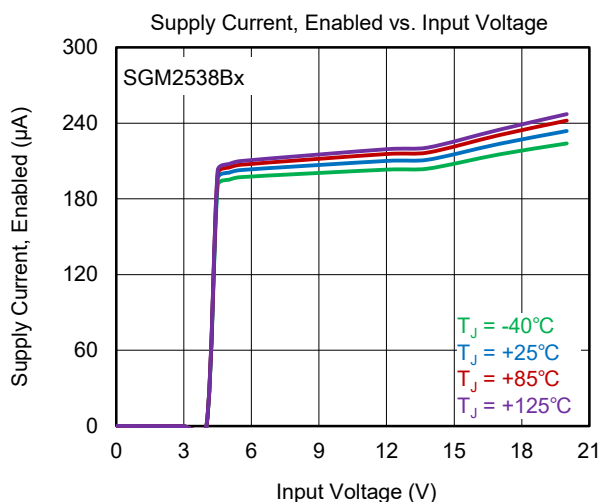
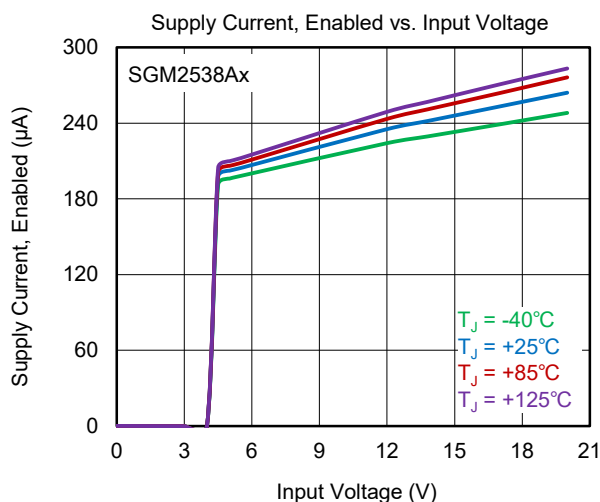
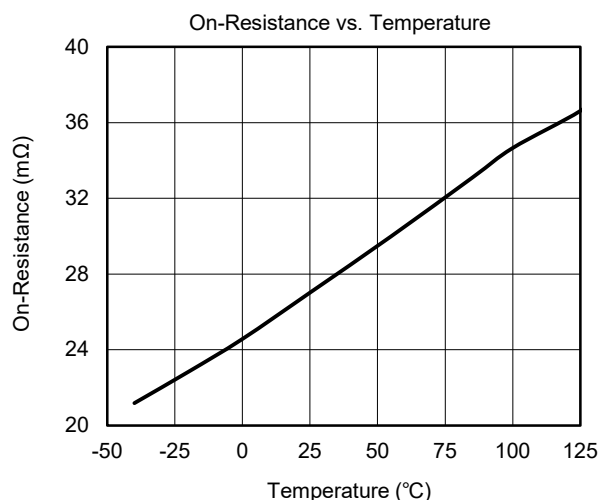
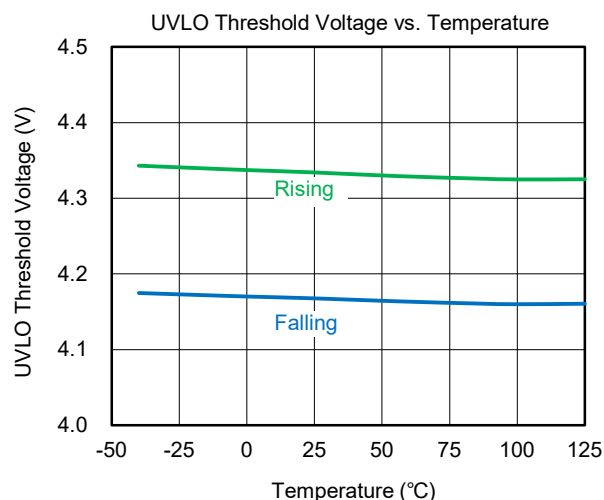
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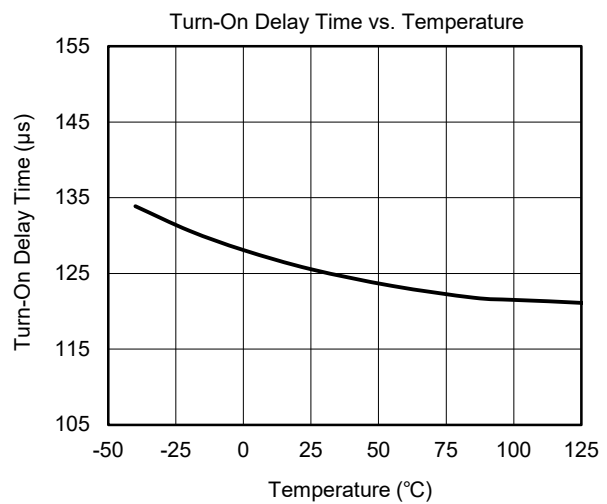
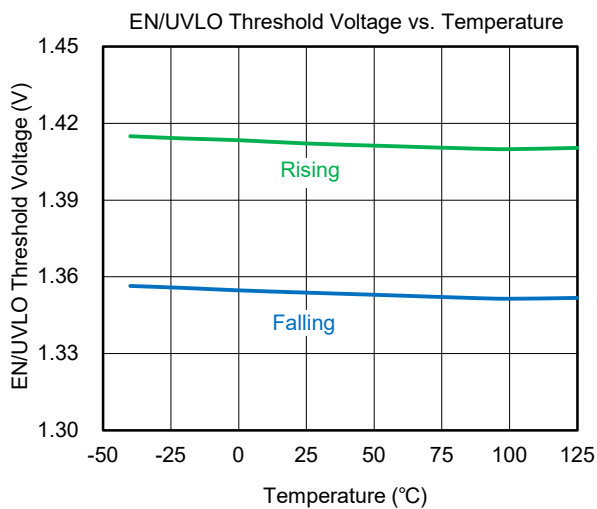
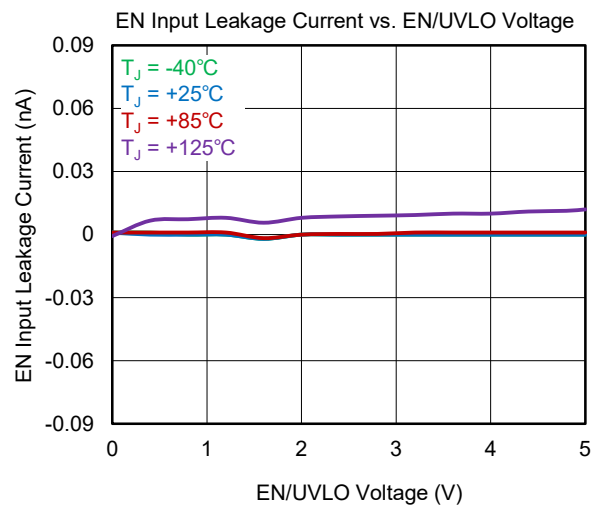
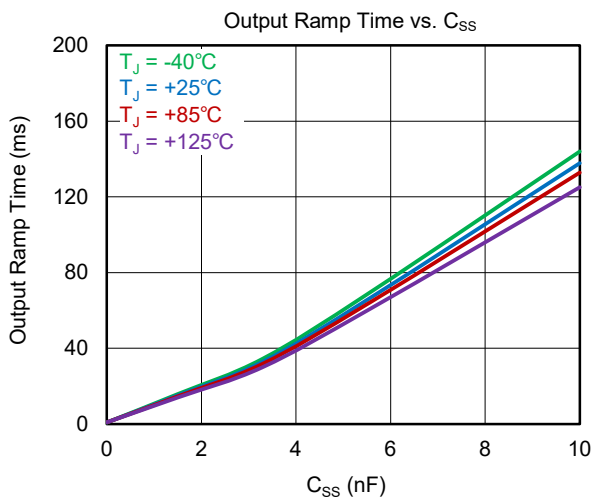
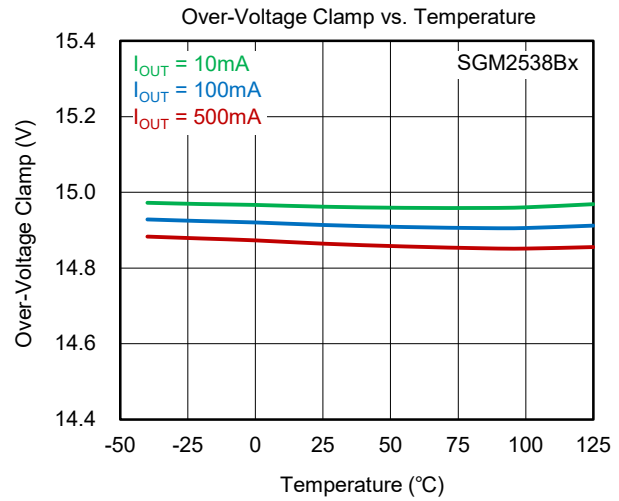
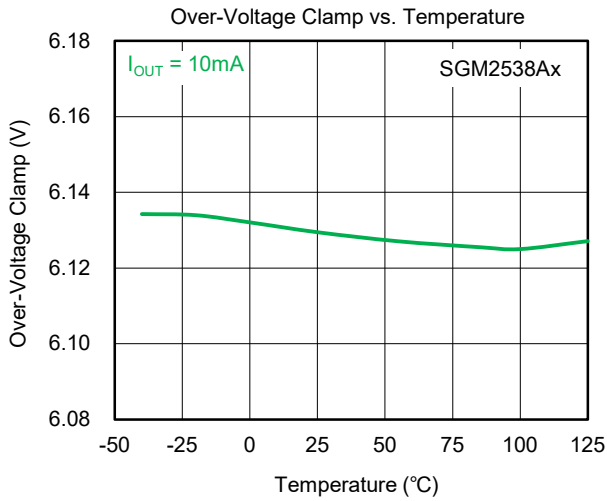
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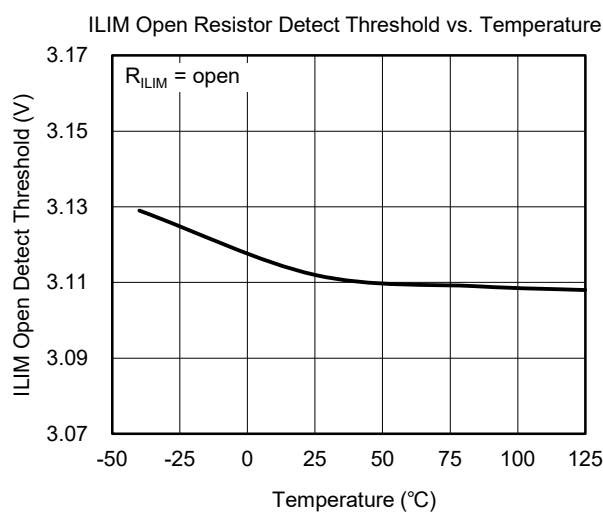
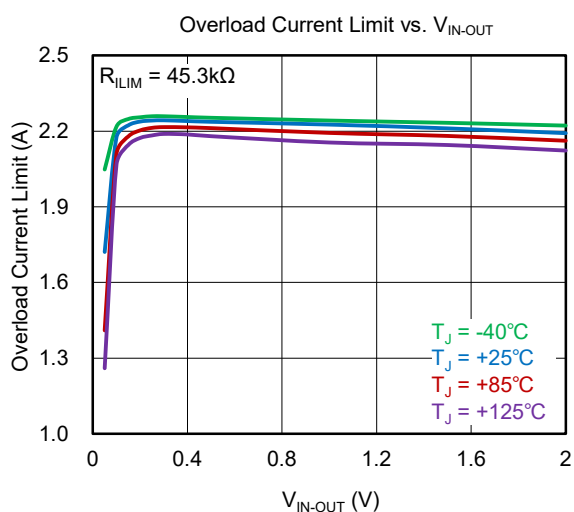
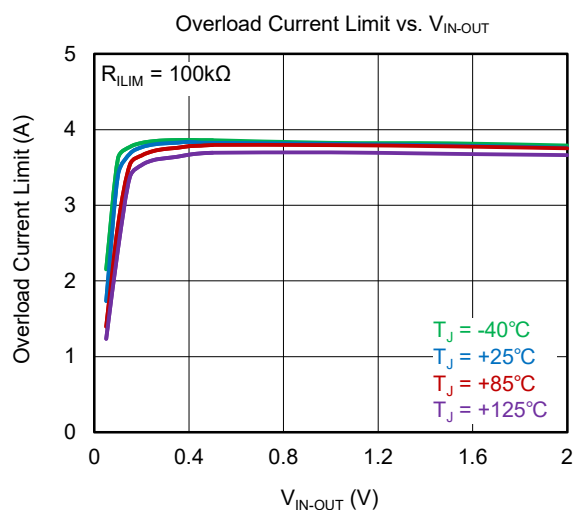
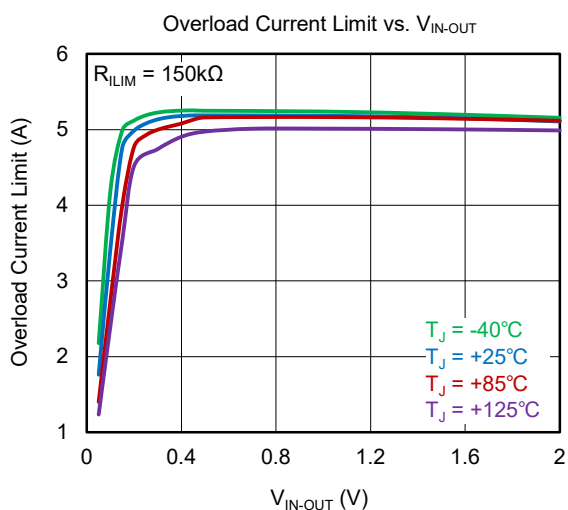
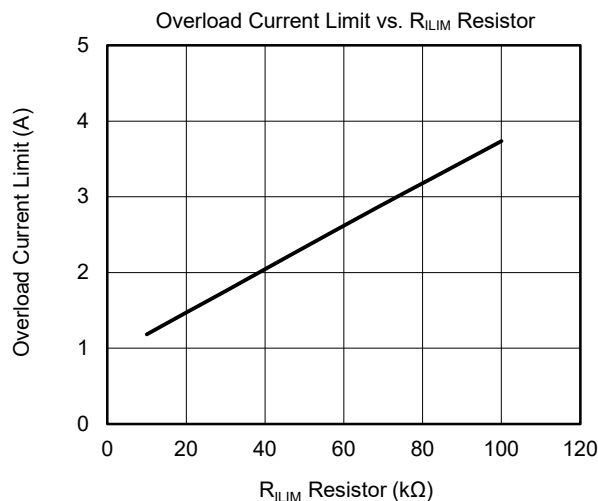
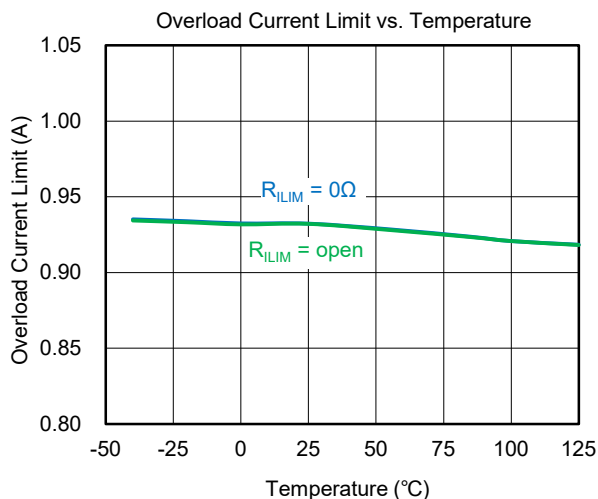
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_J = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{LIM} = 100\text{k}\Omega$, $C_{IN} = 0.1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, and $C_{SS} = \text{open}$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

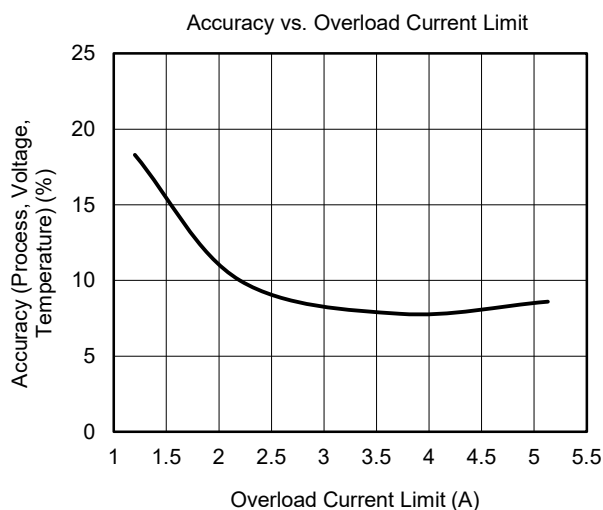
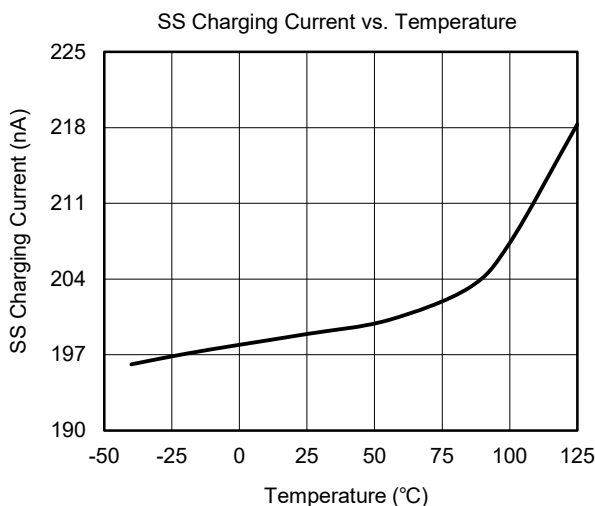
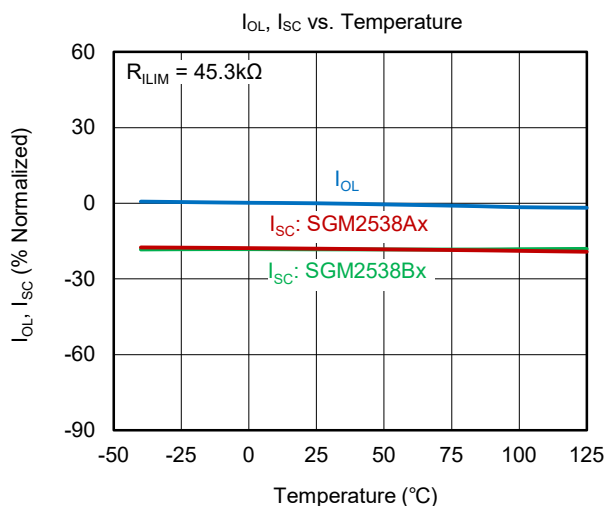
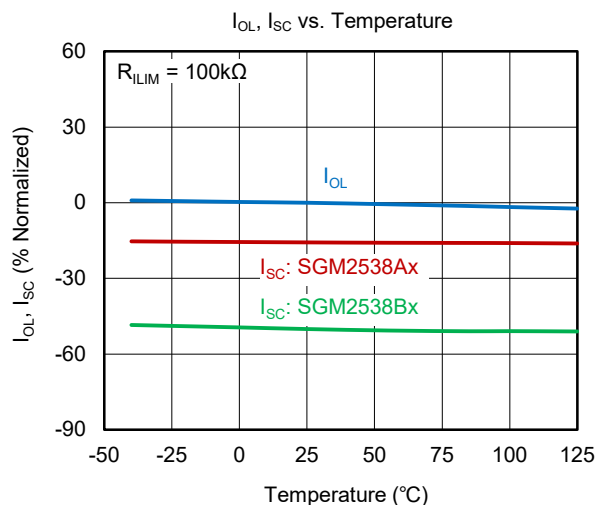
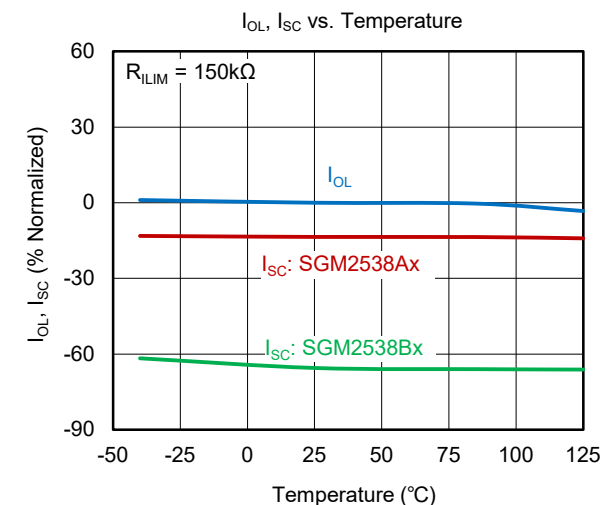
$T_J = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{ILIM} = 100\text{k}\Omega$, $C_{IN} = 0.1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, and $C_{SS} = \text{open}$, unless otherwise noted.



SGM2538 5V/12V Electronic Fuses (eFuses) with OVP Function and Blocking FET Control

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_J = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$ for SGM2538Ax, $V_{IN} = 12\text{V}$ for SGM2538Bx, $V_{EN/UVLO} = 2\text{V}$, $R_{ILIM} = 100\text{k}\Omega$, $C_{IN} = 0.1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, and $C_{SS} = \text{open}$, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

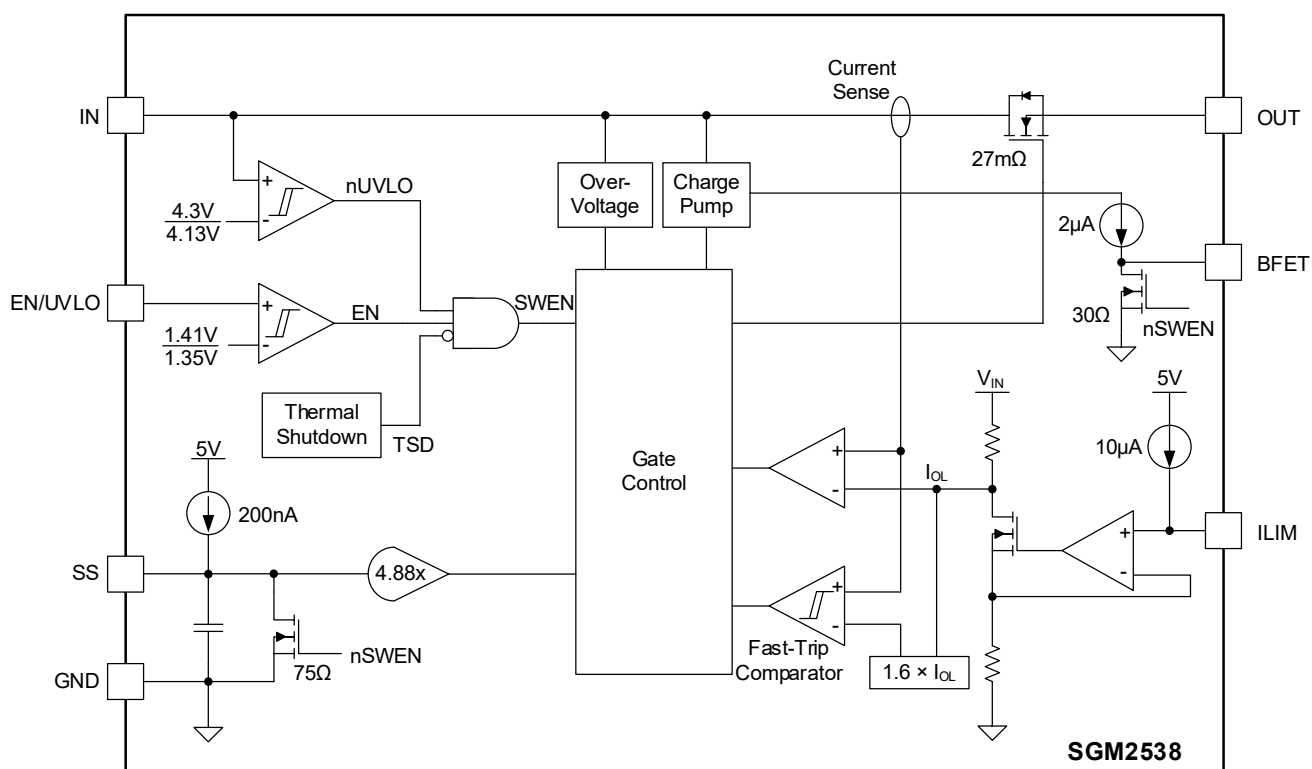


Figure 2. SGM2538 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM2538 is intelligent eFuse with comprehensive built-in protection and regulation functions. The device is enabled and the internal pass FET is turned on when voltages on the both IN (V_{IN}) and EN/UVLO ($V_{EN/UVLO}$) pins exceed their UVLO thresholds. During the start-up process, the output voltage rises with the slew rate programmed through the external capacitor on the SS pin. The device is disabled and the pass FET is turned off when V_{IN} or $V_{EN/UVLO}$ drops to their UVLO thresholds or other fault events occur.

During the steady operation, the SGM2538 is continuously protected from various fault events. The over-voltage clamp (OVC) ensures the input voltage clamped to V_{OVC} once voltage spikes occur. The over-current protection (OCP) function limits the output current to preset level accurately. When the current rises very rapidly under short-circuit condition, the short-circuit protection (SCP) works and turns off the device quickly. The above fault events may bring accumulated heat and cause the device temperature increase. To avoid over-temperature, the SGM2538 is integrated with thermal shutdown function. Once the junction temperature T_J exceeds the maximum level T_{SD} (+155°C), the thermal shutdown is activated and the device is turned off. For SGM2538xL, the device remains turned-off until the power supply or EN/UVLO pin is reset (pulled low and then pulled up). For SGM2538xA, the device is designed with 170ms auto-retry after the T_J drops to $T_{SD} - 20^\circ\text{C}$. The auto-retry will repeat until the fault is removed.

GND

The GND pin is the common ground of the device. All the voltages are referenced to this pin.

IN

The IN pin is the input of the device which should be connected to the power source. It is recommended to place a ceramic bypass capacitor close to the IN pin to reduce bus transient. The maximum input voltage of SGM2538 is 20V. For SGM2538Ax, the recommended input voltage is 4.5V to 5.5V. For SGM2538Bx, the recommended range is 4.5V to 13.8V. If the input voltage exceeds the maximum recommended operating voltage, the over-voltage clamp (OVC) function will work and clamp the output voltage at V_{OVC} . Under this condition, the device may heat up due to

more power dissipation, which eventually activates thermal shutdown.

SS

The SS pin is designed to regulate the output slew rate during start-up process. Place a capacitor between SS and GND pins will set the ramp-up time according to the application requirements. This pin can be float, and the output obtains the default value (minimum t_{SS}) under this condition. Equation 1 shows the calculation process.

$$\frac{dV_{OUT}}{dt} = \frac{I_{SS} \times GAIN_{SS}}{C_{SS}} \quad (1)$$

where:

- dV_{OUT}/dt = Desired output slew rate
- $I_{SS} = 200\text{nA}$ (TYP)
- $GAIN_{SS} = 4.88$

Equation 2 shows how to calculate the total ramp time (t_{SS}) when the output rises from 0V to V_{IN} :

$$t_{SS} = 1.02 \times 10^6 \times V_{IN} \times C_{SS} \quad (2)$$

When C_{SS} is open, there is a 70pF capacitor (C_{INT}) inside.

BFET

The BFET pin features gate driver ability. When this pin is used to drive an external N-FET connected back to back with the internal pass FET, the system provides reverse current block (RCB) function. Both voltages on the IN (V_{IN}) and EN/UVLO ($V_{EN/UVLO}$) pins control the BFET pin. Table 1 shows the control logic where V_{UVR} and V_{ENR} are the UVLO thresholds of V_{IN} and $V_{EN/UVLO}$ respectively. The BFET pin provides 2μA charging current and fast discharging speed (typically < 1μs) through the internal 30Ω resistor. High-impedance probe (> 10MΩ) should be used when measuring this pin.

Table 1. BFET

$V_{EN/UVLO} > V_{ENR}$	$V_{IN} > V_{UVR}$	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

DETAILED DESCRIPTION (continued)**EN/UVLO**

The EN/UVLO pin has two functions, namely enable and under-voltage lockout. When used as an enable pin, it controls the active and shutdown states of the internal pass FET and external blocking FET. Logic high (exceed V_{ENR}) enables the internal pass FET and controls BFET pin to charge the external N-FET. Logic low (below V_{ENF}) disables the internal pass FET and controls BFET pin to discharge the external N-MOSFET. The EN/UVLO levels are designed with hysteresis as specified in the electrical characteristic table.

When used as a UVLO pin by connecting resistor divider from IN to EN/UVLO to GND, it can program different input voltage UVLO thresholds.

The internal EN/UVLO falling edge de-glitch delay is $1\mu\text{s}$ (TYP). If a higher de-glitch delay is desired, it is recommended to add an external bypass capacitor between EN/UVLO and GND pins.

ILIM

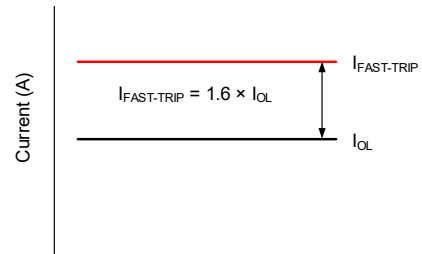
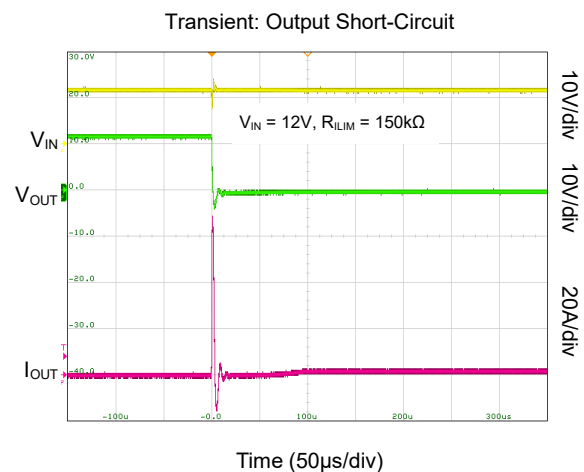
At all times, the load current is monitored by directly sensing the current flowing through the internal pass FET. The maximum power dissipation of device is restricted to constant 30W. During over-current event, the current is limited to the over-current limit (I_{OL}) programmed by R_{ILIM} as shown in Equation 3.

$$I_{OL} = (0.92 + 2.8 \times 10^{-5} \times R_{ILIM}) \quad (3)$$

Power dissipation of the internal MOSFET is calculated by $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. If it is set to constant 30W, the continue overload state will cause thermal shutdown.

When a transient short-circuit is happened, due to the limited bandwidth of the current limit amplifier, it cannot respond quickly to this event, so the SGM2538 contains a fast-trip comparator with a threshold ($I_{FAST-TRIP}$). If $I_{OUT} > I_{FAST-TRIP}$, the comparator turns off the power FET and terminates the short-circuit peak current cross the power FET rapidly. The fast-trip threshold is 1.6 times of the overload current limit. The

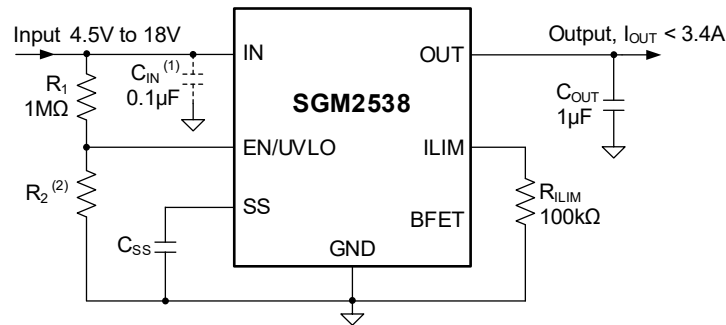
fast-trip comparator can terminate the transient short-circuit peak current, and then the current limit function limits the output current to I_{OL} .

**Figure 3. Fast-Trip Current****Figure 4. Fast-Trip and Current Limit Amplifier Response for Short-Circuit****Output Discharge**

The SGM2538 provides an internal two-level output discharge when the device is disabled through EN/UVLO pin. When the initial output voltage is above 7.5V, the output capacitor would be quickly discharged to 7.5V, and then slowly discharged to 0V. When the initial output voltage is below 7.5V, it will be slowly discharged to 0V.

APPLICATION INFORMATION

Simple 3.72A eFuse Protection for Set-Top Boxes



NOTES:

1. C_{IN} is optional and $0.1\mu F$ is recommended to suppress transients due to the inductance of PCB routing or from input wiring.
2. Optional and only needed for external UVLO.

Figure 5. Simple 3.72A eFuse for Set-Top Boxes

Design Requirements

Table 2 lists the typical application circuit requirements of SGM2538.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage, V_{IN}	12V
Under-Voltage Lockout Set Point, V_{UV}	Default: $V_{UVR} = 4.3V$
Over-Voltage Protection Set Point, V_{OV}	Default: $V_{OVC} = 15V$
Load at Start-Up, $R_{L(SU)}$	4Ω
Current Limit, $I_{OL} = I_{ILIM}$	3.72A
Load Capacitance, C_{OUT}	$1\mu F$
Maximum Ambient Temperature, T_A	$+85^\circ C$

Input Capacitor

It is recommended to use a capacitor ($0.001\mu F$ to $0.1\mu F$) between IN and GND close to the device pins. It can limit the voltage drop on the input supply.

Power Supply

The power supply range is 4.5V to 13.8V for SGM2538. If the distance between the power supply and the device is more than a few inches, it is recommended to use a higher than $0.1\mu F$ input bypass capacitor.

Programmable Current Limit

The overload current limit is programmed by the R_{ILIM} resistor with Equation 4.

$$R_{ILIM} = \frac{I_{OL} - 0.92}{2.8 \times 10^{-5}} \quad (4)$$

Assuming $I_{OL} = 3.72A$, R_{ILIM} is calculated as $100k\Omega$, select the resistor with 1% closest to the standard value.

APPLICATION INFORMATION (continued)

Set Point for Under-Voltage Lockout

Setting the external voltage divider of R_1 and R_2 will adjust the under-voltage lockout (UVLO) point of the device. The R_1 and R_2 resistors are placed among IN, EN/UVLO and GND pins. Equation 5 shows how to calculate these resistor values:

$$V_{UV} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

When V_{ENR} exceeds the threshold (1.41V), the device is turned on.

The values of R_1 and R_2 should be selected properly. If R_1 and R_2 are too small, it will cause considerable power loss from V_{IN} . If R_1 and R_2 are too large, it will cause undesirable current leaked into the device pins. In this design, the default UVLO $V_{UVR} = 4.3V$. Select $R_1 = 1M\Omega$ and $R_2 = 510k\Omega$.

The falling edge of power supply is set to detect for power failure, and the threshold V_{PFail} is usually 4% lower than the V_{UVR} . Equation 6 shows the calculation.

$$V_{PFail} = 0.96 \times V_{UVR} \quad (6)$$

where V_{UVR} is 4.3V, power fail threshold is 4.13V.

It should be noted that the EN/UVLO pin can only sustain voltage up to 7V. Therefore, if V_{IN} is less than 7V, the EN/UVLO can be connected to V_{IN} directly. If V_{IN} is greater than 7V, this pin must be connected to V_{IN} and GND through the resistors divider (R_1 and R_2).

Setting Output Ramp Time (t_{ss})

The SGM2538 is designed to control the inrush current when the device is enabled or powered-on. The slew rate of the output voltage can be set by an external capacitor between the SS pin and GND defined at power-on. Calculating the C_{SS} requires consideration of the two possible cases.

Start-Up without Load: Only Charge the C_{OUT}

Once the device starts up, the current flows through the device charges the output capacitor. This process causes the inrush current, and it can be calculated by Equation 7. Combining the voltage difference and the load current, the power is dissipated across the internal pass FET. Equation 8 shows how to calculate the average power dissipation during start-up:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{ss}} \quad (7)$$

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (8)$$

Start-Up with Load: C_{OUT} and Load Draws Current

During start-up, the load ($R_{L(SU)}$) current ramps up proportionally with the increase of output voltage. The average power dissipation in the internal pass FET during charging time is shown in Equation 9 to Equation 12.

$$P_{D(LOAD)} = \left(\frac{1}{6} \times \frac{V_{IN}^2}{R_{L(SU)}} \right) \quad (9)$$

$$P_{D(START_UP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

$$I_{START_UP} = I_{INRUSH} + I_L(t) \quad (11)$$

where:

$P_{D(START_UP)}$ is the total power dissipation during start-up.

I_{START_UP} is the total current during start-up.

At the initial start-up stage, I_{START_UP} is less than the overload limit level I_{OL} . With the resistor load drawing more current, I_{START_UP} increases continuously. Once $I_{START_UP} > I_{OL}$, the device limits the current to I_{OL} and the total start-up time is determined by:

$$t_{ss} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{INRUSH}} - 1 + \ln \left(\frac{I_{INRUSH}}{I_{OL} - \frac{V_{IN}}{R_{L(SU)}}} \right) \right] \quad (12)$$

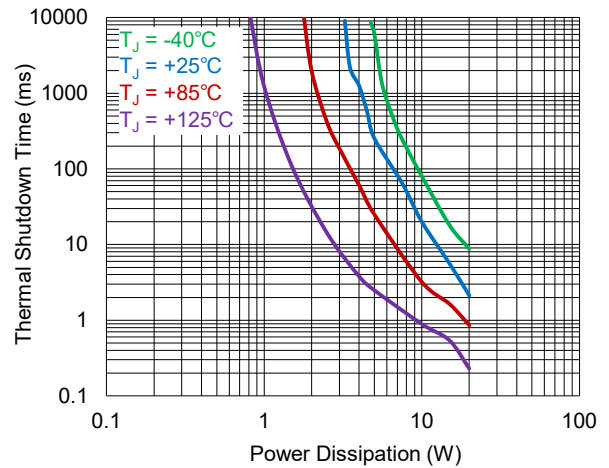


Figure 6. Thermal Shutdown Limit Plot

APPLICATION INFORMATION (continued)

For the design example with C_{SS} = open.

$$t_{SS} = 1.02 \times 10^6 \times 12V \times 70pF = 857\mu s \quad (13)$$

$$I_{INRUSH} = 1\mu F \times \frac{12}{857\mu s} = 14mA \quad (14)$$

$$P_{D(INRUSH)} = 0.5 \times 12 \times 14mA = 84mW \quad (15)$$

For a certain power loss during start-up, the thermal shutdown time must be greater than the ramp-up time t_{SS} . As shown in Figure 6, when $T_J = +85^\circ C$, the thermal shutdown time is infinite. Therefore, it is safe to use $857\mu s$ as start-up time without any load on output.

Considering the start-up event with a 4Ω load, the additional power dissipation on the load is calculated using Equation 9.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6W \quad (16)$$

$$P_{D(STARTUP)} = 6W + 84mW = 6.08W \quad (17)$$

Form Figure 6, the thermal shutdown time for power loss of $6.08W$ when $T_J = +85^\circ C$ is $10ms$ which is much more than t_{SS} . Therefore, it is still safe to use $857\mu s$ as start-up time with a 4Ω load.

Application Curves

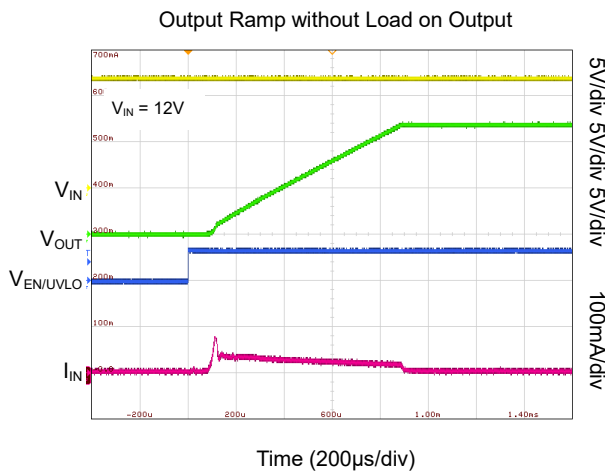
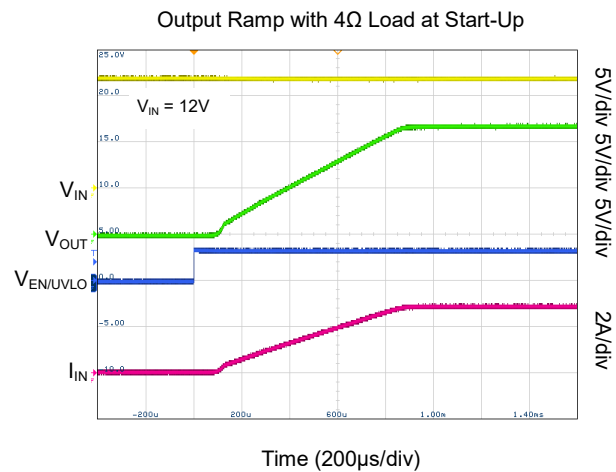
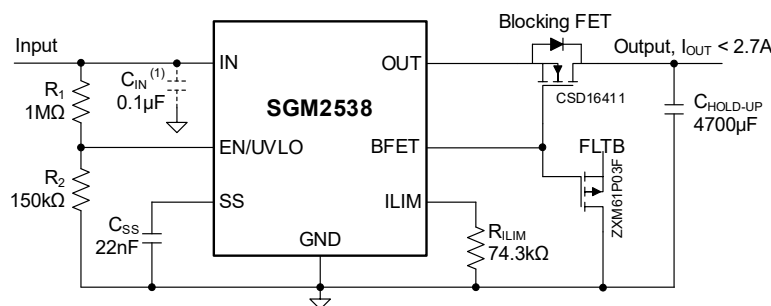


Figure 7. Output Ramp without Load on Output

Figure 8. Output Ramp with 4Ω Load at Start-Up

Inrush and RCP for Hold-Up Capacitor Application (SSD)



NOTE:

1. C_{IN} is optional and $0.1\mu F$ is recommended to suppress transients due to the inductance of PCB routing or from input wiring.

Figure 9. Inrush and RCP for Hold-Up Capacitor Application (SSD)

APPLICATION INFORMATION (continued)

Design Requirements

Table 2 lists the typical application circuit requirements of SGM2538.

Table 3. Design Parameters

Design Parameter	Example Value
Input Voltage, V_{IN}	12V
Under-Voltage Lockout Set Point, V_{UV}	10.8V
Over-Voltage Protection Set Point, V_{OV}	Default: $V_{OVC} = 15V$
Load at Start-Up, $R_{L(SU)}$	1000 Ω
Current Limit, $I_{OL} = I_{ILIM}$	3A
Load Capacitance, C_{OUT}	4700 μF
Maximum Ambient Temperature, T_A	+85 $^{\circ}C$

Programmable Current Limit

Assuming $I_{OL} = 3A$, R_{ILIM} is calculated as 74.3k Ω from Equation 4. Select the resistor with 1% closest to the standard value.

Set Point for Under-Voltage Lockout

The resistor divider R_1 and R_2 can be calculated by Equation 6. In this example, the UVLO set point is 10.8V. Therefore, $R_1 = 1M\Omega$ and $R_2 = 150k\Omega$ can be selected, and the rising threshold V_{UV} is 10.81V.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than

V_{UV} . For $V_{UV} = 10.81V$, the power fail threshold V_{PFAIL} is 10.38V.

Setting Output Ramp Time (t_{SS})

For the design example, C_{SS} is designed to be 22nF, and the parameters are calculated as follows:

$$t_{SS} = 1.02 \times 10^6 \times 12V \times (22nF + 70pF) = 270ms \quad (18)$$

$$I_{INRUSH} = 4700\mu F \times \frac{12}{270ms} = 209mA \quad (19)$$

$$P_{D(INRUSH)} = 0.5 \times 12 \times 209mA = 1254mW \quad (20)$$

Considering the start-up event with a 1000 Ω load, the additional power dissipation on the load is calculated using Equation 9.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 1000} = 24mW \quad (21)$$

$$P_{D(STARTUP)} = 1254mW + 24mW = 1278mW \quad (22)$$

Form Figure 6, the thermal shutdown time for power loss of 1.3W when $T_J = +85^{\circ}C$ is infinite. Therefore, it is safe to start the device.

Application Curves

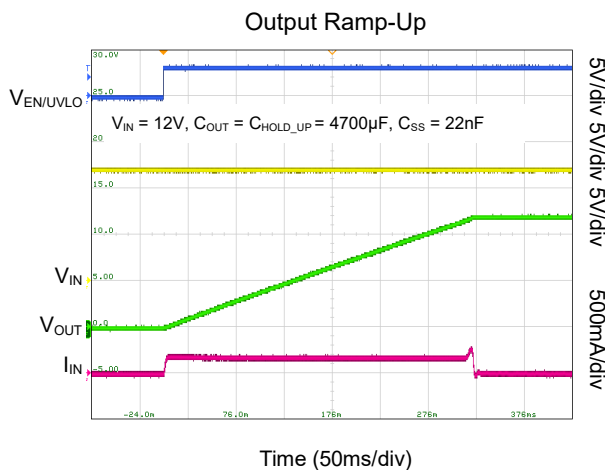
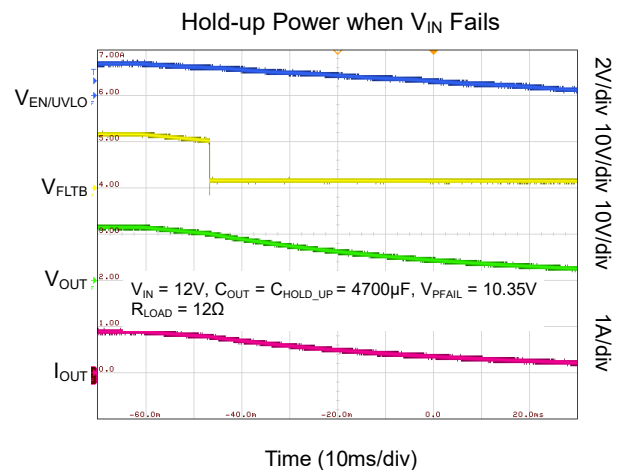
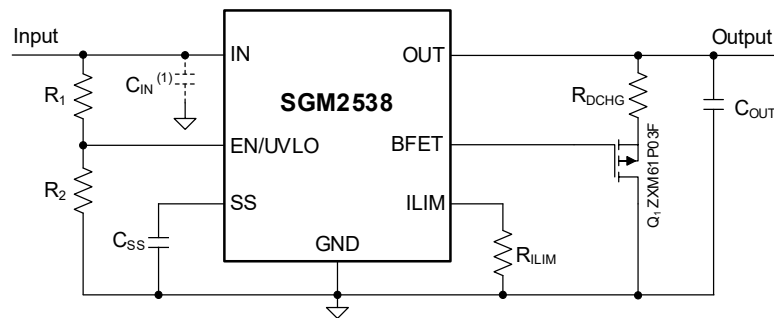


Figure 10. Output Ramp-Up

Figure 11. Hold-up Power when V_{IN} Fails

APPLICATION INFORMATION (continued)

Controlled Power-Down Using SGM2538



NOTE:

1. C_{IN} is optional and $0.1\mu F$ is recommended to suppress transients due to the inductance of PCB routing or from input wiring.

Figure 12. Circuit Implementation with Quick Output Discharge Function

For some applications, it is necessary to power down the load to a defined state to avoid undesirable events. The BFET pin of SGM2538 can be used to drive an external P-MOSFET to achieve quick output discharge function (see Figure 12). When the device is disabled, the BFET pin is pulled low, which turns on the Q_1 to discharge the output voltage. The output discharge rate is determined by the product of the output capacitor and discharge resistance, namely C_{OUT} and R_{DCHG} .

Power Supply Recommendations

The power supply range is 4.5V to 13.8V for SGM2538Bx. If the distance between the power supply and the device is more than a few inches, it is recommended to use a higher than $0.1\mu F$ input bypass capacitor.

Transient Protection

In case of turning off the internal MOSFET, such as V_{OUT} hard short, thermal shutdown, etc., the current flow path is cut off. The energy stored in parasitic inductance generates voltage spike. The input inductance produces a positive voltage spike on the input, while the output inductance produces a negative

voltage spike on the output. The voltage spike can exceed the absolute maximum ratings of the device if the following steps are not taken:

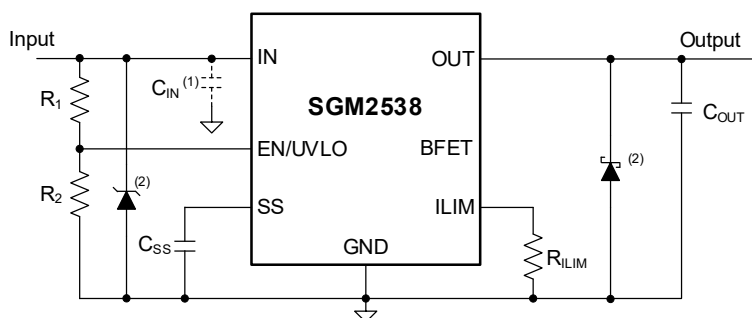
- ♦ Minimizing lead length and inductance into and OUT of the device, including GND connection.
- ♦ Schottky diode across the output to absorb negative spikes.
- ♦ A low value ceramic capacitor ($C_{IN} = 0.001\mu F$ to $0.1\mu F$) to absorb the energy. The approximate value of C_{IN} can be calculated with Equation 23.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (23)$$

where:

- ♦ V_{IN} is the supply voltage.
- ♦ I_{LOAD} is the load current.
- ♦ L_{IN} equals the effective inductance seen looking into the source.
- ♦ C_{IN} is the input capacitance.

APPLICATION INFORMATION (continued)



NOTES:

1. C_{IN} is optional and $0.1\mu F$ is recommended to suppress transients due to the inductance of PCB routing or from input wiring.
2. Optional components for transient suppression.

Figure 13. Circuit Implementation with Optional Protection Components

Some applications may require the addition of a transient voltage suppressor (TVS) across the IN pin and GND to prevent transients from exceeding the absolute maximum ratings of the device.

Ceramic capacitors, TVS and Schottky diodes are optional protection components. Optional components can be used to suppress transients as shown in Figure 13.

Layout Guidelines

- ♦ It is recommended to use a $0.01\mu F$ or larger ceramic decoupling capacitor between IN and GND pins. When the input power path inductance is too low to ignore in hot plug applications, the capacitor can be minimized.
- ♦ The path of high current carrying power should be as short as possible, which must size to withstand twice the load current.
- ♦ The GND pin must be connected to the PCB ground as short as possible.
- ♦ Connect the terminal of the R_{ILIM} , C_{SS} and resistors for EN/UVLO to the GND pin with the shortest trace. These paths and switching signals should not have any coupling.
- ♦ The ceramic capacitors, TVS and Schottky diodes must be placed as close to the device as possible.

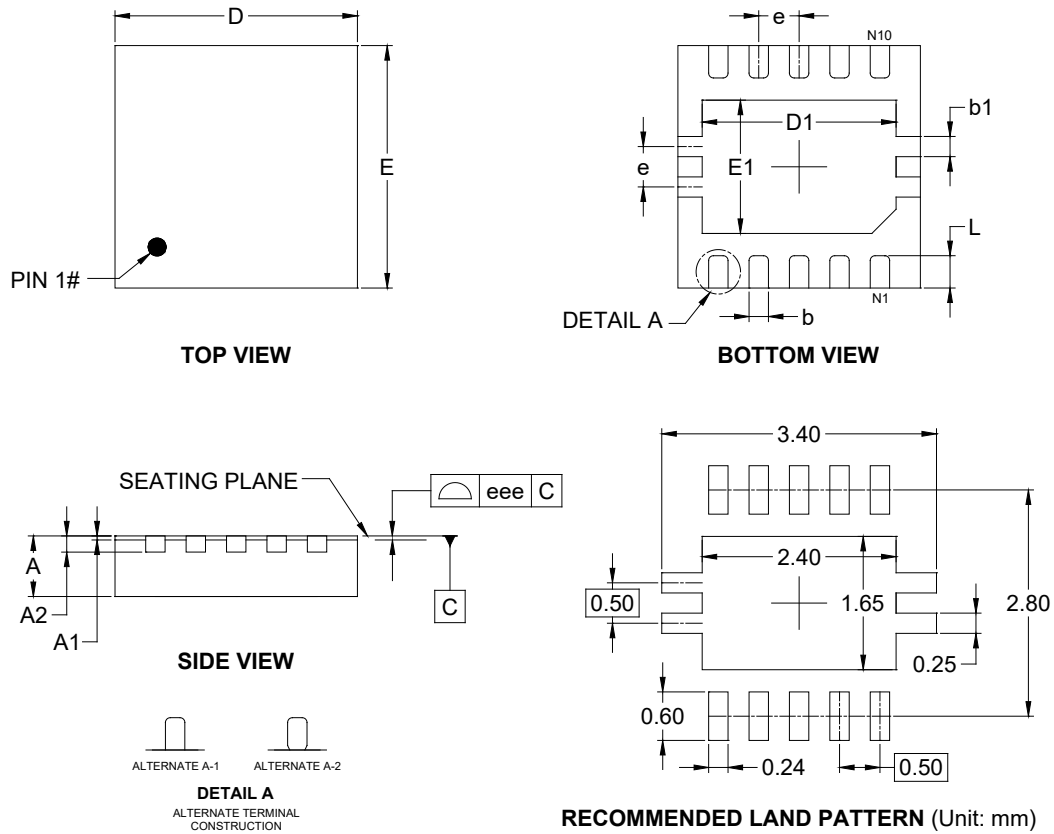
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2024 – REV.A.1 to REV.A.2		Page
Added UL Recognized Component (File No. E532373*)		1
APRIL 2024 – REV.A to REV.A.1		Page
Added SGM2538AA, SGM2538AL and SGM2538BL Models		All
Changes from Original (DECEMBER 2023) to REV.A		Page
Changed from product preview to production data		All

PACKAGE OUTLINE DIMENSIONS

TDFN-3×3-10AL



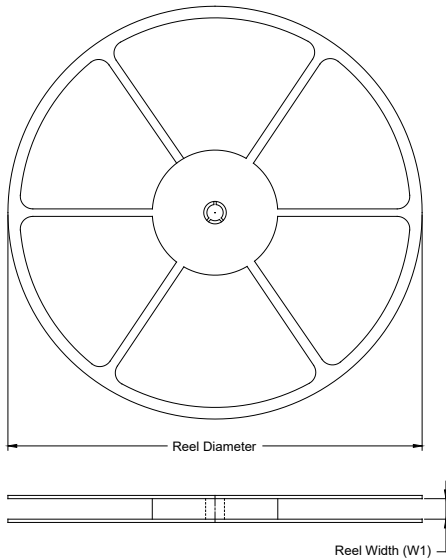
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
b1	0.250 REF		
D	2.900	-	3.100
E	2.900	-	3.100
D1	2.300	-	2.500
E1	1.550	-	1.750
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

NOTE: This drawing is subject to change without notice.

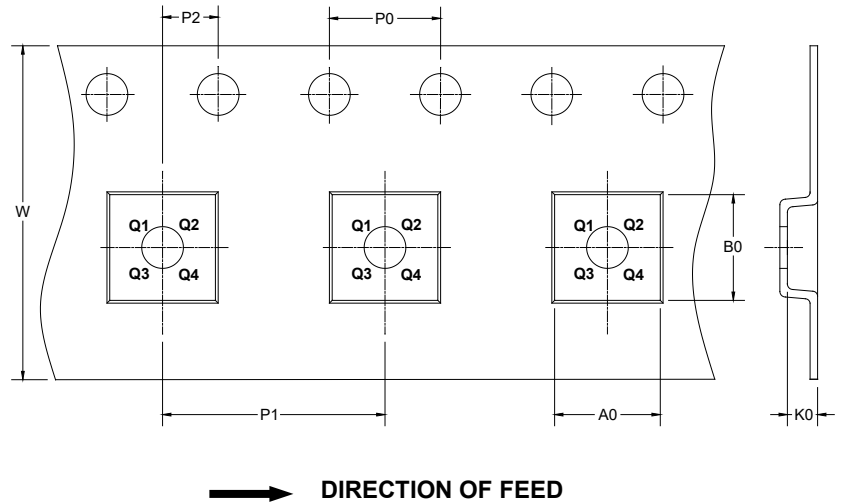
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

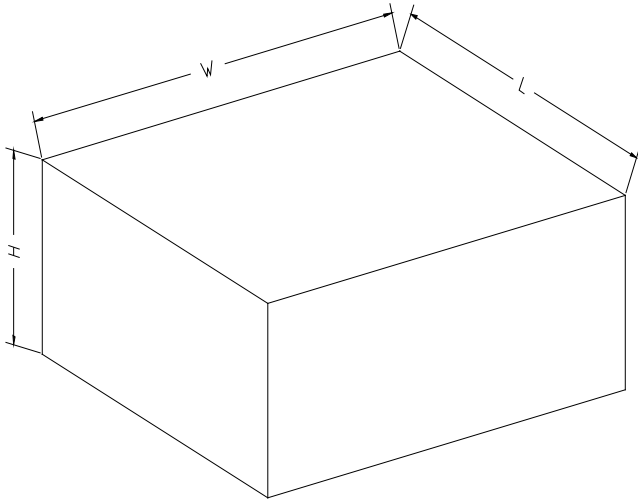
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10AL	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002