SGM623
Low Noise, Low Drift, High Precision, Instrumentation Amplifier

GENERAL DESCRIPTION

The SGM623 is a high accuracy, high voltage instrumentation amplifier, which is designed to set any gain from 1 to 1000 with one external resistor. The device works well in battery-powered applications due to the low power consumption of 1.7mA typical quiescent current. The SGM623 supports rail-to-rail output operation.

The SGM623 provides 180ppm (MAX) non-linearity and 70μV (MAX) low input offset voltage. The device also features low noise, low bias current and low power. The combination of these characteristics makes it a good choice for applications requiring excellent DC performance.

The SGM623 offers 20nV/$\sqrt{Hz}$ low input voltage noise, 1pA/$\sqrt{Hz}$ input current noise at 1kHz, and 13μV_{P-P} in the 0.1Hz to 10Hz band. It is suitable for pre-amplifier applications. The 10μs settling time to 0.1% makes SGM623 appropriate for multiplexed applications.

The SGM623 is available in Green SOIC-8 and MSOP-8 packages, which are much smaller than discrete classical-three-OPAs circuits. It is specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Single External Resistor Gain Set (Set Gain from 1 to 1000)**
- **Input Offset Voltage: 70μV (MAX)**
- **Input Offset Voltage Drift: 0.5μV/℃ (TYP)**
- **Input Bias Current: 10nA (TYP)**
- **CMRR DC: 88dB (MIN) (G = 1)**
- **Input Voltage Noise: 20nV/$\sqrt{Hz}$ (TYP) at 1kHz**
- **0.1Hz to 10Hz Voltage Noise: 13μV_{P-P} (G = 1)**
- **Bandwidth: 2600kHz (G = 1)**
- **Slew Rate: 2V/μs (TYP)**
- **Rail-to-Rail Output**
- **Allows Output RC Filter for Customized Noise Rejection**
- **Support Single or Dual Power Supplies: 4.6V to 36V or ±2.3V to ±18V**
- **Low Power Supply Current: 1.7mA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8 and MSOP-8 Packages**

APPLICATIONS

Industrial Equipment
Medical Equipment
Data Acquisition Systems
Telecom Equipment

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM623	SOIC-8	-40℃ to +125℃	SGM623XS8G/TR	SGM 623XS8 XXXXX	Tape and Reel, 4000
	MSOP-8	-40℃ to +125℃	SGM623XMS8G/TR	SGM623 XMS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Common Mode Voltage .... $\pm V_S$
Differential Input Voltage .... $\pm V_S$
Package Thermal Resistance
SOIC-8, θ_{JA} .... 96.4℃/W
SOIC-8, θ_{JB} .... 46.3℃/W
MSOP-8, θ_{JA} .... 131.1℃/W
MSOP-8, θ_{JB} .... 72.9℃/W
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility (1) (2)
HBM .... ±8000V
CDM (SOIC-8) .... ±500V
CDM (MSOP-8) .... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

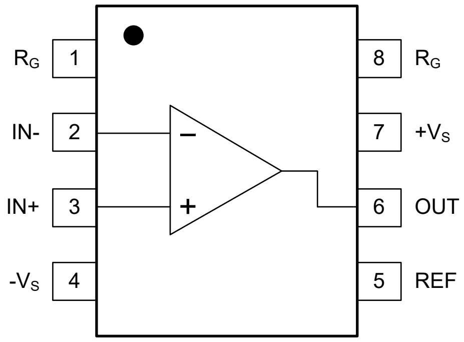
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8/MSOP-8

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 8	R_G	Gain Setting Pin. The gain can be set by placing the resistor across R_G. $G = 1 + (49.4k\Omega/R_G)$.
2	IN-	Inverting Input Pin.
3	IN+	Non-Inverting Input Pin.
4	$-V_S$	Negative Power Supply Pin.
5	REF	Voltage Reference Pin. A voltage source with low impedance can be placed to supply this terminal in order to shift the output level.
6	OUT	Output Pin.
7	$+V_S$	Positive Power Supply Pin.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, V_{REF} = 0V, R_L = 2kΩ, G = 1, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Voltage Offset (Total RTI Error = V_{OSI} + V_{OSO}/G)									
Input Offset Voltage		V_{OSI}			+25℃		20	70	μV
					Full			100	
Input Offset Voltage Drift		$\Delta V_{OSI}/\Delta T$			Full		0.5		μV/℃
Output Offset Voltage		V_{OSO}			+25℃		300	1500	μV
					Full			1600	
Output Offset Voltage Drift		$\Delta V_{OSO}/\Delta T$			Full		3		μV/℃
Offset RTI vs. Power Supply		PSRR	V_S = ±2.3V to ±18V	G = 1	+25℃	94	108		dB
				G = 10	+25℃	110	126		
				G = 100	+25℃	118	134		
				G = 1000	+25℃	120	134		
Input Current									
Input Bias Current		I_B			+25℃		10	20	nA
					Full			34	
Input Bias Current Drift		$\Delta I_B/\Delta T$			Full		100		pA/℃
Input Offset Current		I_{OS}			+25℃		2	5	nA
					Full			7	
Input Offset Current Drift		$\Delta I_{OS}/\Delta T$			Full		20		pA/℃
Input									
Input Impedance	Differential	Z_{DIFF}			+25℃		10 || 1		GΩ || pF
	Common Mode	Z_{CM}			+25℃		10 || 10		
Input Operating Voltage Range			V_S = ±2.3V to ±5V [1]		+25℃	$(-V_S)$ + 1.9		$(+V_S)$ - 1.2	V
					Full	$(-V_S)$ + 2.1		$(+V_S)$ - 1.3	
			V_S = ±5V to ±18V		+25℃	$(-V_S)$ + 1.9		$(+V_S)$ - 1.4	
					Full	$(-V_S)$ + 2.1		$(+V_S)$ - 1.4	
Common Mode Rejection Ratio									
Common Mode Rejection Ratio DC		CMRR	V_{CM} = -10V to +10V	G = 1	+25℃	88	108		dB
				G = 10	+25℃	108	128		
				G = 100	+25℃	124	138		
				G = 1000	+25℃	128	142		
Common Mode Rejection Ratio at 60Hz with 1kΩ Source Imbalance		CMRR	V_{CM} = -10V to +10V	G = 1	+25℃	86	102		dB
				G = 10	+25℃	94	105		
				G = 100	+25℃	94	105		
				G = 1000	+25℃	94	105		

NOTE:

1. One input terminal is connected to ground. G = 1.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, V_{REF} = 0V, R_L = 2kΩ, G = 1, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Reference Input								
Reference Input Resistance	R_{REF}			+25℃		20		kΩ
Reference Input Current	I_{REF}	V_{IN+} = V_{IN-} = 0V, V_{REF} = 0V		+25℃		0.1	0.6	μA
Voltage Range				+25℃	$-V_S$		$+V_S$	V
Gain to Output				+25℃		1 ± 0.00001		V/V
Output Characteristics								
Output Voltage Swing	V_{OH}	R_L = 10kΩ		+25℃		80	150	mV
				Full			200	
	V_{OL}	R_L = 10kΩ		+25℃		25	70	
				Full			100	
Short-Circuit Current	I_{SC}	R_L = 50Ω to V_S/2		+25℃		20		mA
Gain (G = 1 + (49.4kΩ/R_G))								
Gain Range					1		1000	V/V
Gain Error	GE	V_{OUT} = -10V to +10V	G = 1	+25℃		0.004	0.02	%
			G = 10	+25℃		0.1	0.3	
			G = 100	+25℃		0.1	0.3 (2)	
			G = 1000	+25℃		0.1	0.3 (2)	
Gain Non-Linearity		V_{OUT} = -10V to +10V	G = 1	+25℃		15	45	ppm
			G = 10	+25℃		15	50	
			G = 100	+25℃		20	60	
			G = 1000	+25℃		50	180	
Gain Temperature Coefficient			G = 1	Full		2		ppm/℃
			G > 1 (3)	Full		25		
Dynamic Response								
Small-Signal -3dB Bandwidth	BW		G = 1	+25℃		2600		kHz
			G = 10	+25℃		1000		
			G = 100	+25℃		300		
			G = 1000	+25℃		30		
Slew Rate	SR		G = 1	+25℃	1 (2)	2		V/μs
			G = 5 to 100	+25℃	1 (2)	2		
Settling Time to 0.1%	t_S	V_{OUT} = $10V_{P-P}$ step	G = 1 to 100	+25℃		10		μs
			G = 1000	+25℃		40		

NOTES:

2. Specified by design and characterization, not production tested.

3. Effects of external resistor R_G are not included.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, V_{REF} = 0V, R_L = 2kΩ, G = 1, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Noise (RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$)								
Input Voltage Noise Density	e_{ni}	f = 1kHz, V_{IN+} = V_{IN-} = 0V, V_{REF} = 0V		+25℃		20	25 (2)	nV/√Hz
Output Voltage Noise Density	e_{no}	f = 1kHz		+25℃		110	135 (2)	nV/√Hz
0.1Hz to 10Hz Voltage Noise, RTI		f = 0.1Hz to 10Hz	G = 1	+25℃		13		μV_{P-P}
			G = 10	+25℃		1.5		
			G = 100 to 1000	+25℃		0.5		
Input Current Noise Density	i_n	f = 1kHz		+25℃		1		pA/√Hz
0.1Hz to 10Hz Current Noise		f = 0.1Hz to 10Hz		+25℃		25		pA_{P-P}
Power Supply								
Operating Voltage Range	V_S	V_S = ±2.3V to ±18V		+25℃	±2.3		±18	V
Quiescent Current	I_Q	V_S = ±2.3V to ±18V, I_{OUT} = 0A		+25℃		1.7	2.1	mA
				Full			2.3	
Temperature Range								
Operating Temperature Range				+25℃	-40 to +125			℃

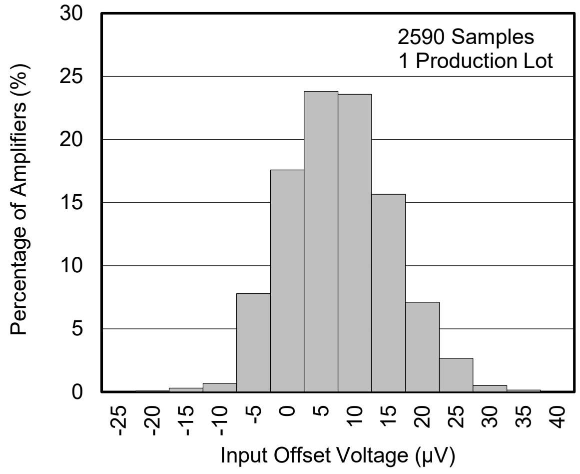
NOTE:

2. Specified by design and characterization, not production tested.

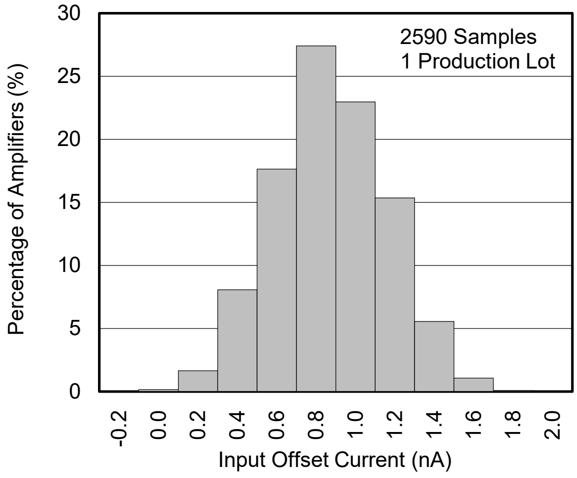
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±15V, R_L = 2kΩ, G = 1, unless otherwise noted.

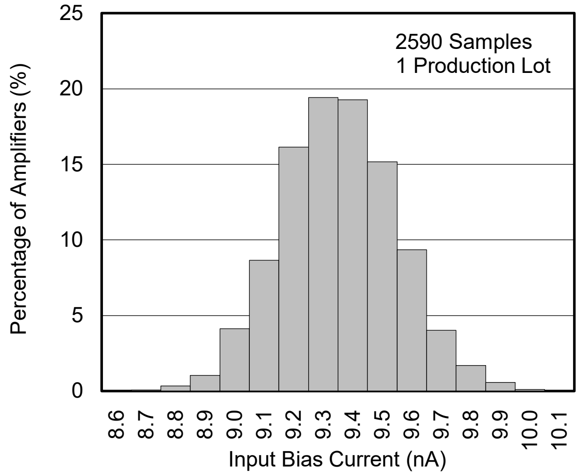
Input Offset Voltage Production Distribution



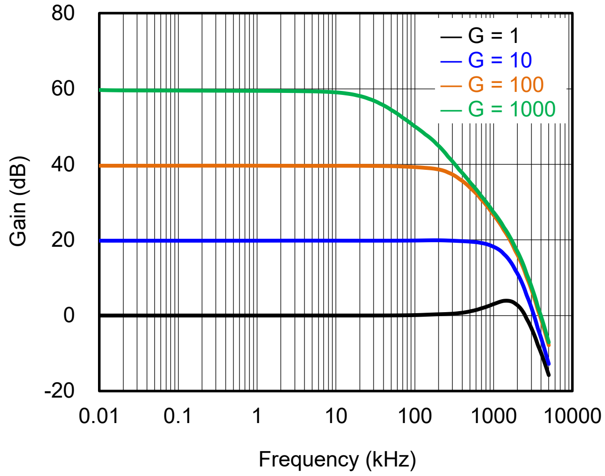
Input Offset Current Production Distribution



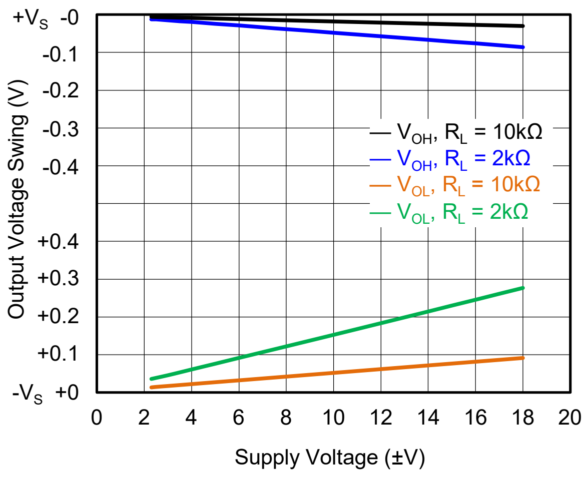
Input Bias Current Production Distribution



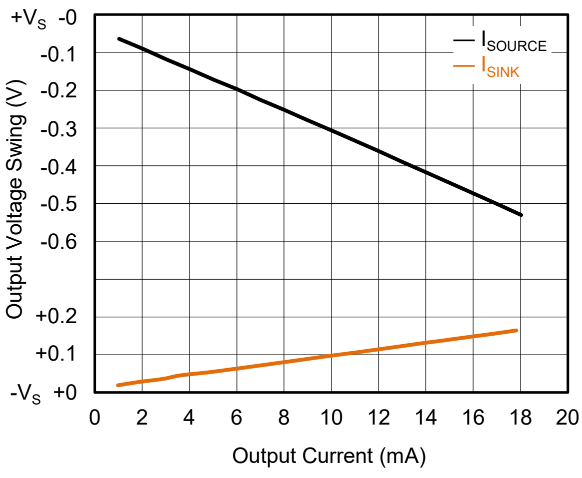
Gain vs. Frequency



Output Voltage Swing vs. Supply Voltage

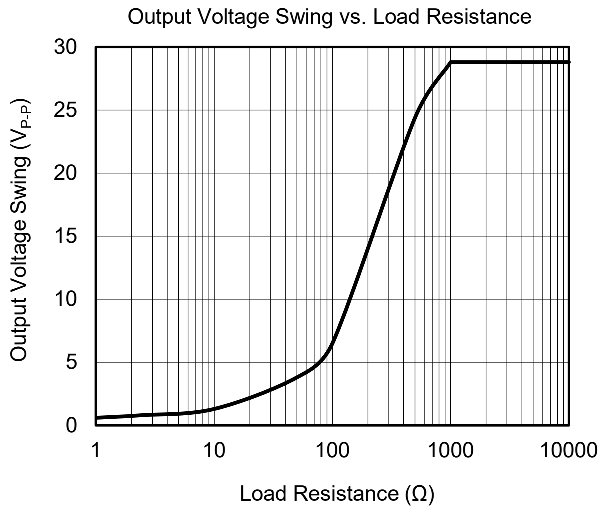


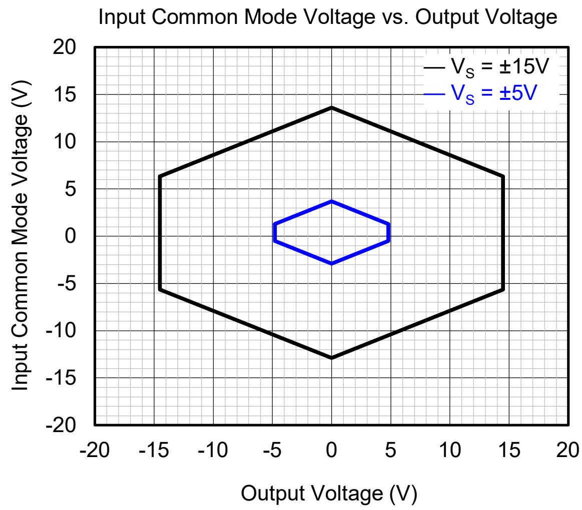
Output Voltage Swing vs. Output Current

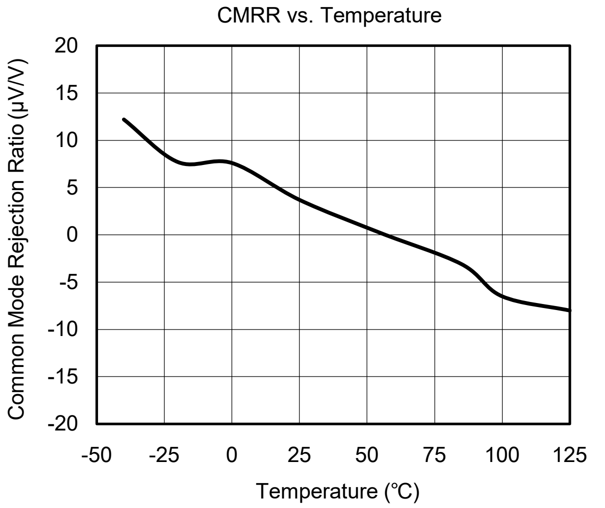


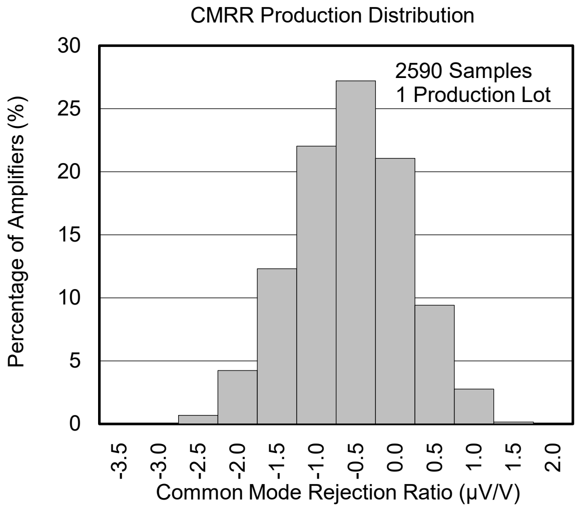
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

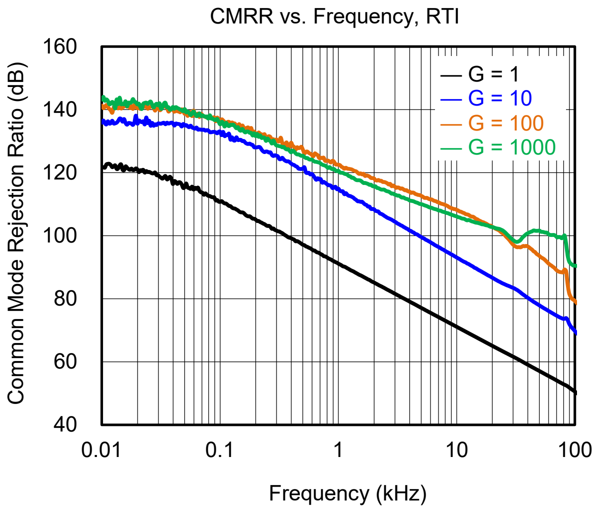
At T_A = +25℃, V_S = ±15V, R_L = 2kΩ, G = 1, unless otherwise noted.

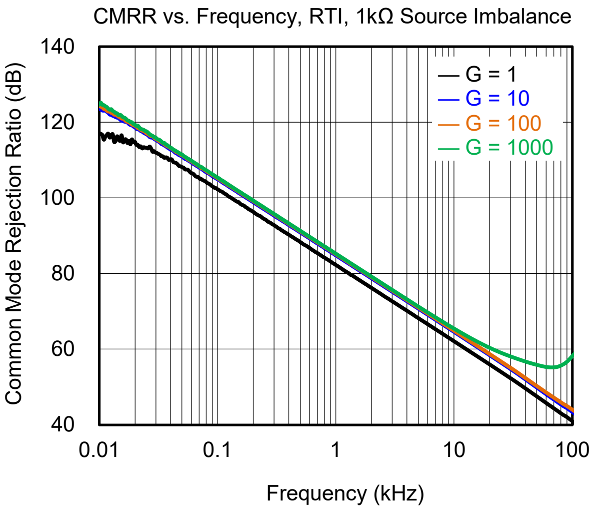






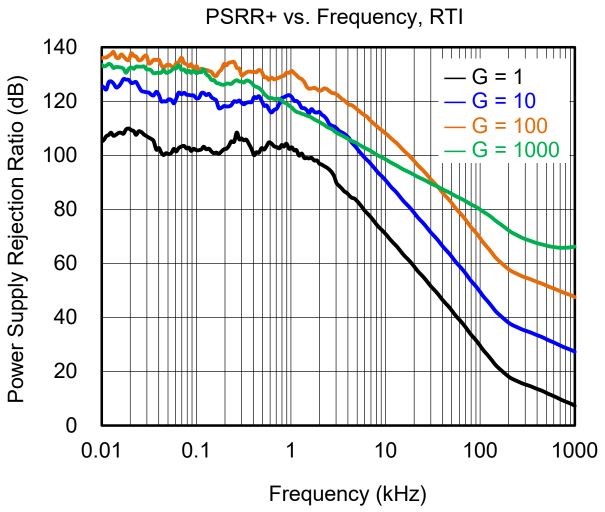


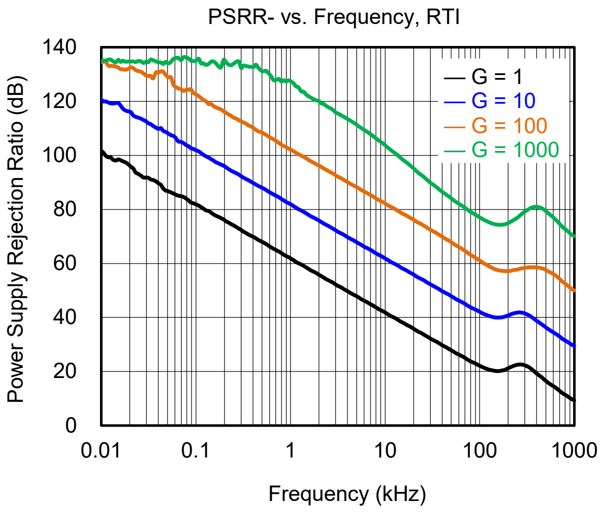


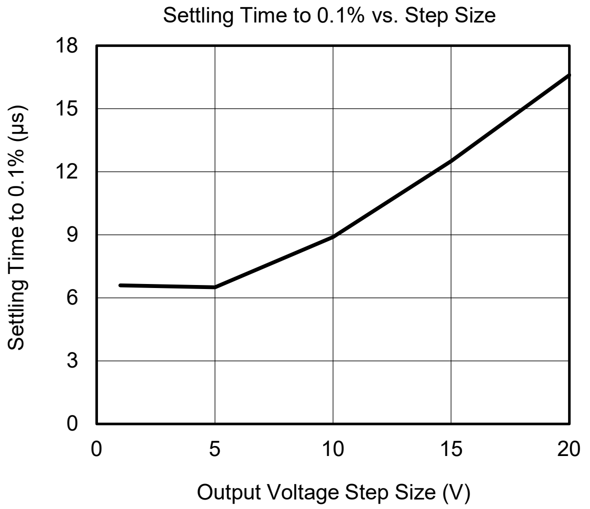


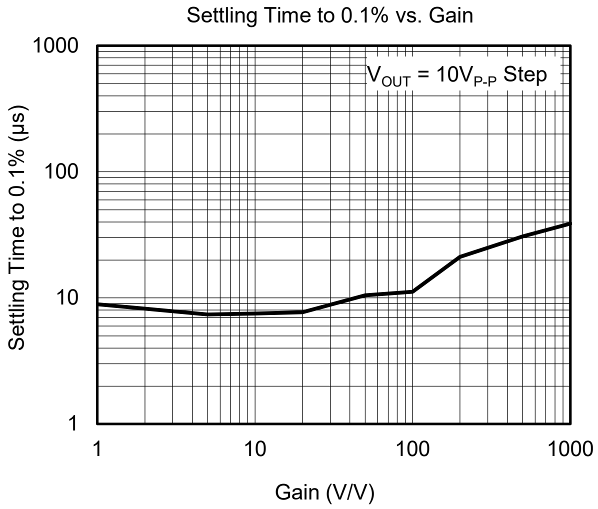
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

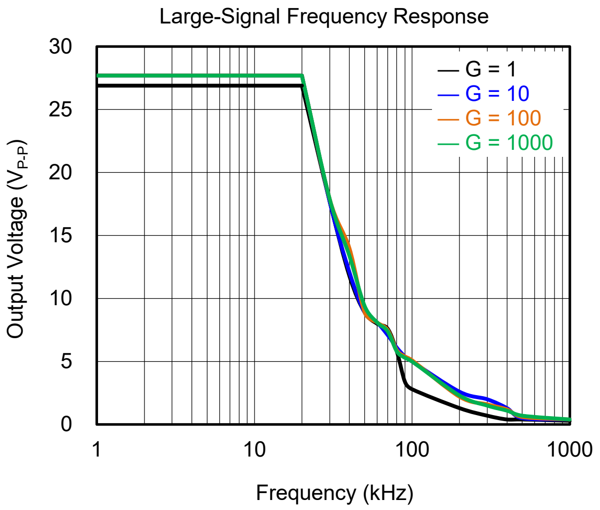
At T_A = +25℃, V_S = ±15V, R_L = 2kΩ, G = 1, unless otherwise noted.

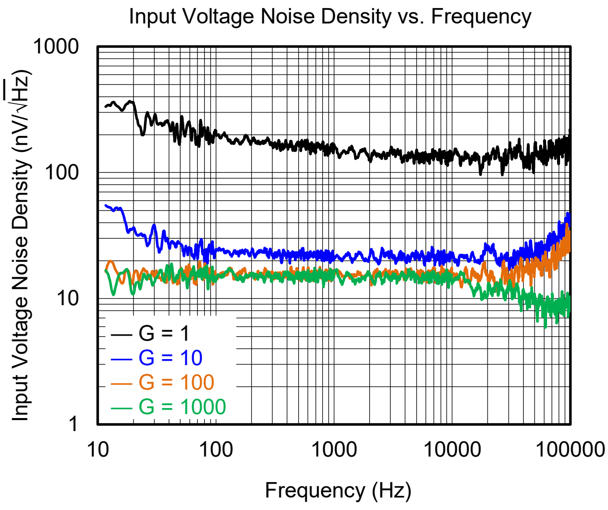








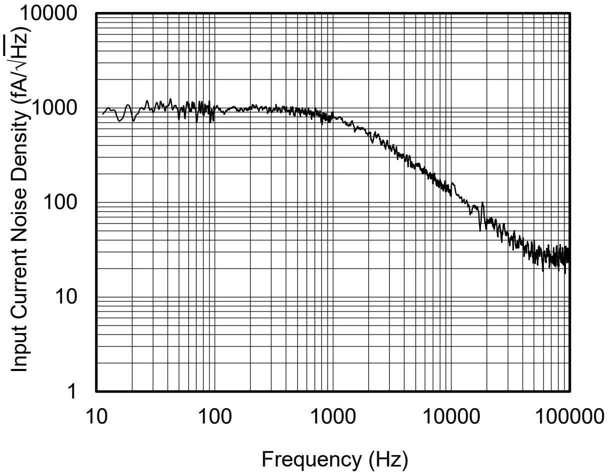




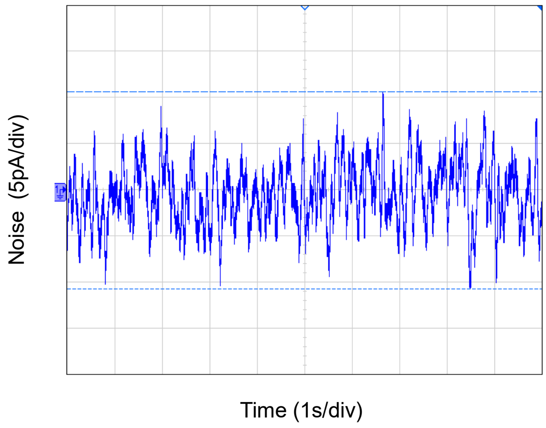
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, R_L = 2kΩ, G = 1, unless otherwise noted.

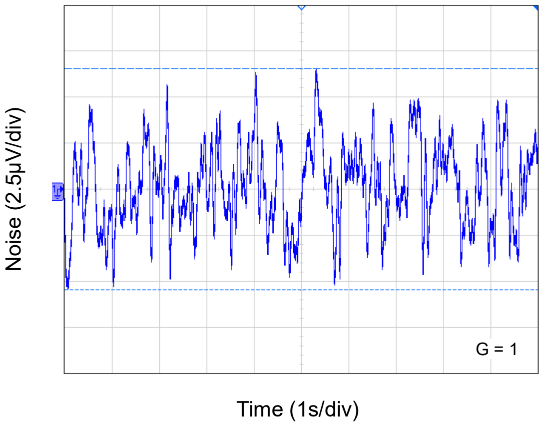
Input Current Noise Density vs. Frequency



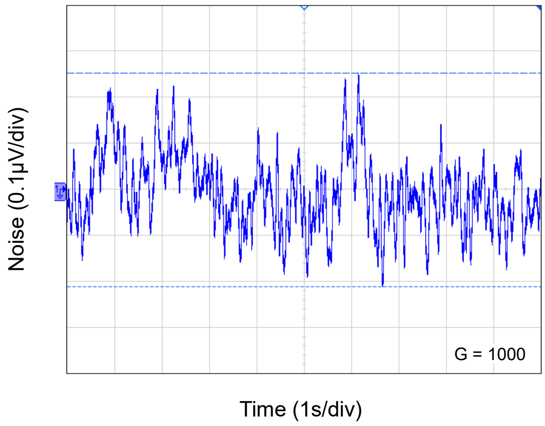
0.1Hz to 10Hz Input Current Noise



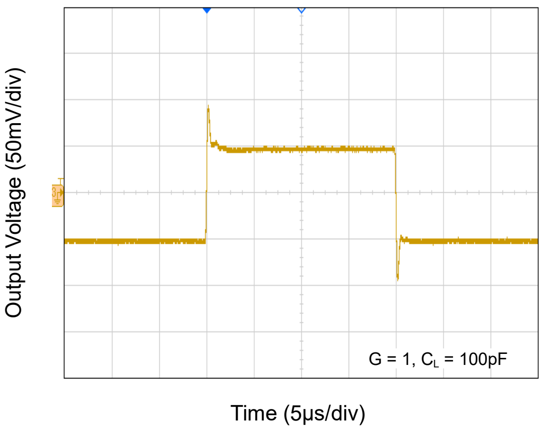
0.1Hz to 10Hz Input Voltage Noise, RTI



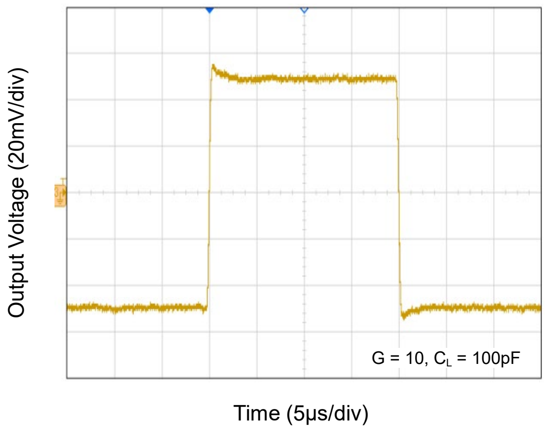
0.1Hz to 10Hz Input Voltage Noise, RTI



Small-Signal Step Response

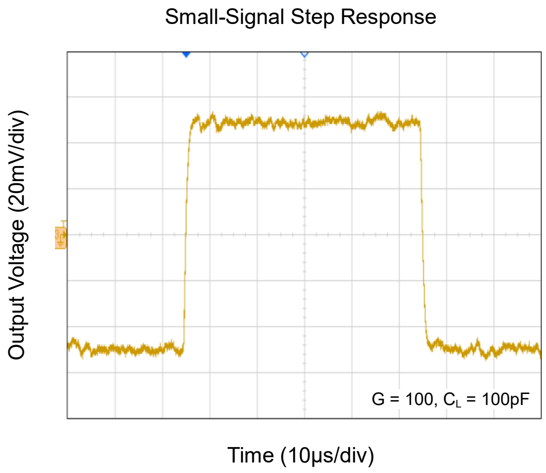


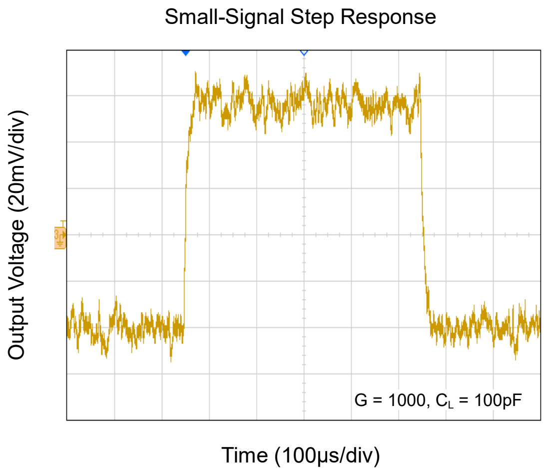
Small-Signal Step Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, G = 1, R_L = 2kΩ, unless otherwise noted.





OPERATION THEORY

The SGM623 is modified with the classic three-op-amp and it is a holistic instrumentation amplifier.

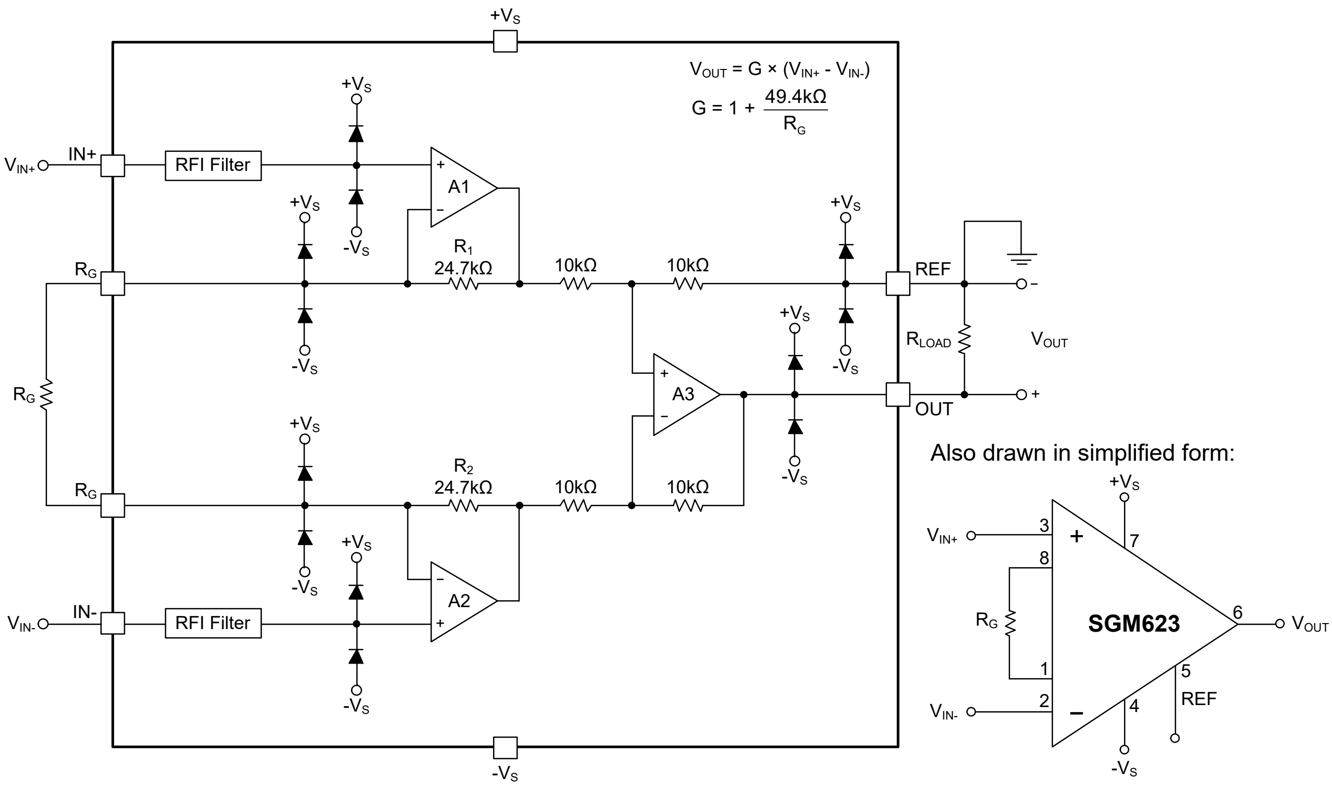


Figure 1. Simplified Schematic

The buffered differential input voltage across R_G leads to the flow of a signal current through both the R_G resistor and the two R_F resistors. The differential gain from A1/A2 outputs can be expressed by $G = 1 + (R_1 + R_2)/R_G$. The unity-gain subtractor (A3) can reject the common mode signal so that SGM623 produces a single-ended output with REF pin biased.

The transconductance of the pre-amplifier is determined by the resistance of R_G. The transconductance will increase gradually to that of the input transistors if the resistance of R_G is reduced for larger gains. The important benefits are shown below:

- Boosting the open-loop gain can also increase the programmed gain, so that the related error of gain is reduced.
- The gain-bandwidth product and the transconductance of the pre-amplifier can increase with programmed gain, so that the frequency response is enhanced.
- Maintain 88dB (MIN) common mode rejection throughout the input range.
- Reducing the input voltage noise to $20nV/\sqrt{Hz}$, and it is determined by the auto-calibration technique of the amplifiers. The integrated resistors (R_1 and R_2) inside the SGM623 are set to 24.7kΩ, so that the gain can be programmed with the external resistor R_G.

The equation of gain is shown as below:

$$G = \frac{49.4k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4k\Omega}{G - 1}$$

APPLICATION INFORMATION

Pressure Measurement

SGM623 is widely used in the application of bridge, such as measuring the pressure in weigh scales. It is also suitable for detecting the pressure sensor with higher resistance due to high input impedance.

Figure 2 shows the pressure transducer bridge of 5kΩ which is powered by a 5V single supply. For the circuit which is illustrated as below, the combination of the resistive bridge that is in front of the circuit, the buffered voltage divider and the SGM623 can consume approximately 3.2mA of the total supply current.

The advantage of small size for SGM623 is attractive for the transducers of pressure. Because of the low noise and drift, it can also be used in the application of diagnostic non-invasive blood pressure measurement.

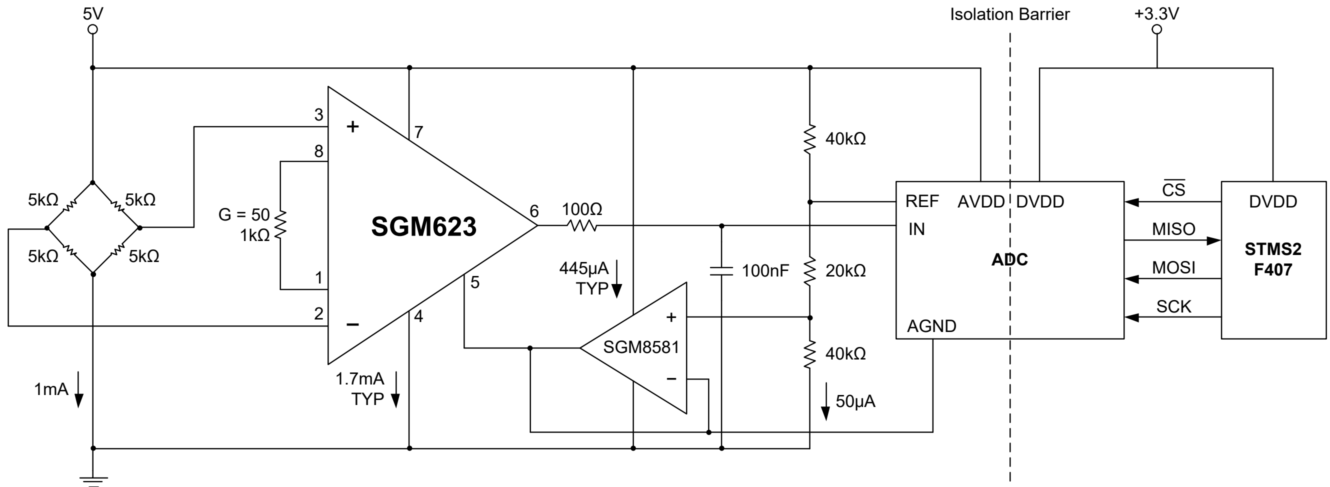


Figure 2. The Operation of the Pressure Monitor Circuit with 5V Single Supply

APPLICATION INFORMATION (continued)

Medical ECG Amplifier

Because of the advantage of low current noise, SGM623 can be used in ECG monitors (Figure 3) where the source resistances can reach 1MΩ or higher. It is the best choice to use SGM623 in the battery-powered data recorders as it can operate on the condition of low supply voltage, low power and space-saving packages.

Moreover, for better performance, combining with the advantages of low voltage noise, low current noise and low bias currents can enhance the dynamic range of SGM623.

The stability of the right leg drive loop can be maintained by the capacitor C_1. Moreover, for protecting the patient from the possible harm, the isolation safeguards should be added between the patient and the circuit part.

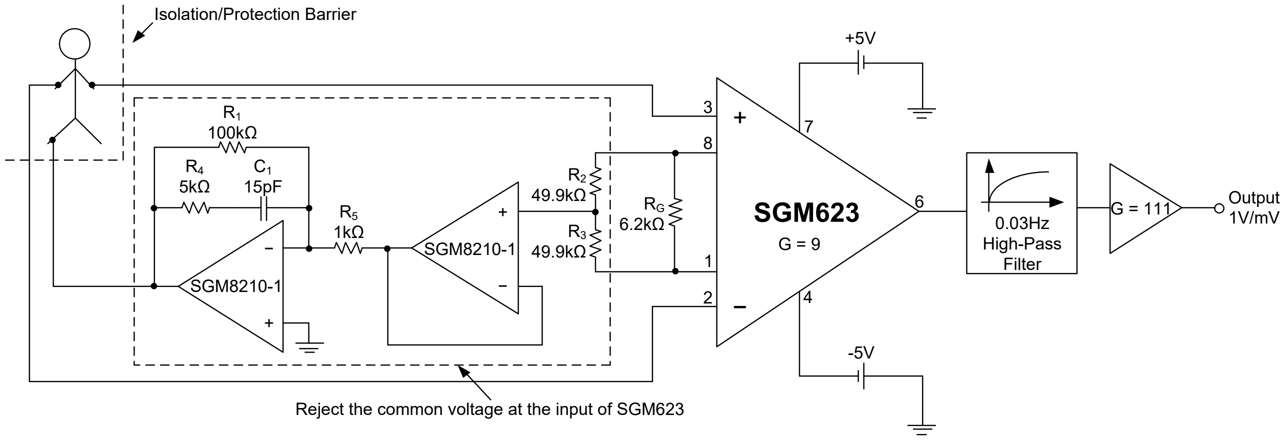


Figure 3. The Circuit of Medical ECG Monitor

It is worth noting that when an instrumentation amplifier is used in small-signal acquisition, high-precision acquisition systems, or scenarios requiring ultra-low noise on the output signal, it is best to add an RC filter at the output. This can effectively suppress high-frequency noise in the output signal, reduce glitches and fluctuations, make the output signal closer to the ideal state, and improve signal quality. The design of the RC cutoff frequency needs to be determined by the user based on the actual application requirements.

APPLICATION INFORMATION (continued)

Precision V-I Converter

It's easy to realize a precision current source (Figure 4) utilizing one SGM623, another operational amplifier and two resistors. To obtain a better CMRR of SGM623, a buffer should be placed between the REF pin and the OUT pin of the amplifier. The equation which is shown in Figure 4 illustrates the output current of the circuit.

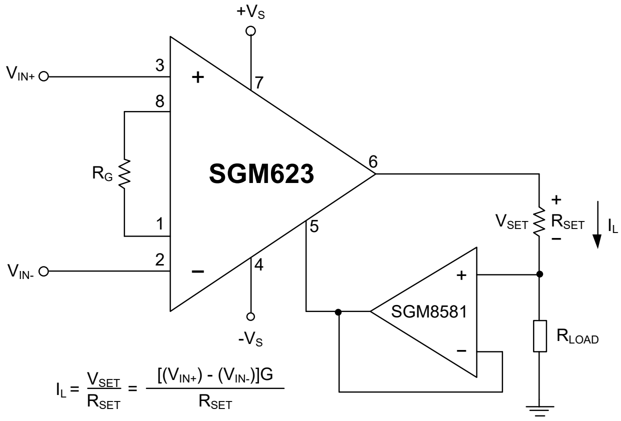


Figure 4. Precision Voltage-to-Current Converter

Input and Output Offset Voltage

Two main sources which are error of input and output result in the low errors of SGM623. When referred to the input, the output error should be divided by the gain of the instrumentation amplifier. From the equations which are shown as below, the input error takes a leading position at large gains while the output error takes a leading position at small gains.

Total Error Referred to Input (RTI) = Input Error + (Output Error/G)

Total Error Referred to Output (RTO) = (Input Error × G) + Output Error

Terminal of Reference

Potential of the reference terminal defines the zero output voltage. It becomes extremely useful while the load is not tied to the precise ground of the rest of the system. The reference terminal provides one way to bias a precise voltage to the output, and the reference voltage should be within the power supply range. On top of these, to keep better CMRR, the parasitic resistor at this pin should be low.

Selection of Gain

The gain of the instrumentation amplifier is determined by the external resistor R_G. The accuracy of the external resistor R_G is important as it may influence the error of gain. It is recommended that selecting the resistor with 1% or 0.1% precision is a good choice. The following table shows the gain effect with the selection of 1% or 0.1% precision resistor. Also, leaving the pin 1 and pin 8 (the place of R_G) open can make the gain of SGM623 equals to 1.

$$R_G = \frac{49.4k\Omega}{G - 1}$$

As mentioned before, the gain error can be minimized by equivalent parasitic resistor in series with R_G. Moreover, low TC of 2ppm/℃ is required for the selection of R_G to avoid the gain drift of SGM623.

Table 1. Different Values for Gain Resistor

1% STD Table Value of R_G (Ω)	Calculated Gain	0.1% STD Table Value of R_G (Ω)	Calculated Gain
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1003.0

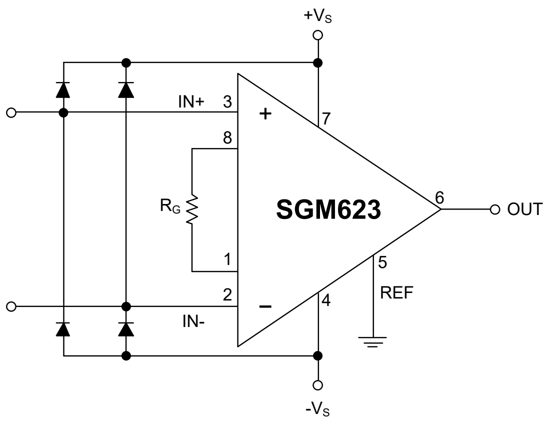


Figure 5. Diode for Protecting V_{IN} from Larger than V_S

APPLICATION INFORMATION (continued)

RF Interference

One of the characteristics of instrumentation amplifier is rectifying the small signal which is out of the band. This kind of disturbance can be described as the small biased voltage. All of the high frequency components can be filtered by the R-C network which is placed in the input position of the instrumentation amplifier, as shown in Figure 6. The following equation shows the equation of filtering frequency for the differential and common mode part of the input signal.

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

$C_D \geq 10C_C$ is required in the above equation.

The capacitor C_D influences the quality of the differential signal, while C_C influences the quality of the common mode signal. The common mode rejection ratio would be reduced if the R × C_C is mismatched. To reduce this negative influence and obtain a good CMRR, it is recommended that the capacitance of C_D should be 10 times larger than C_C. To conclude, the larger the ratio of C_D:C_C is, the less negative influence to the circuit.

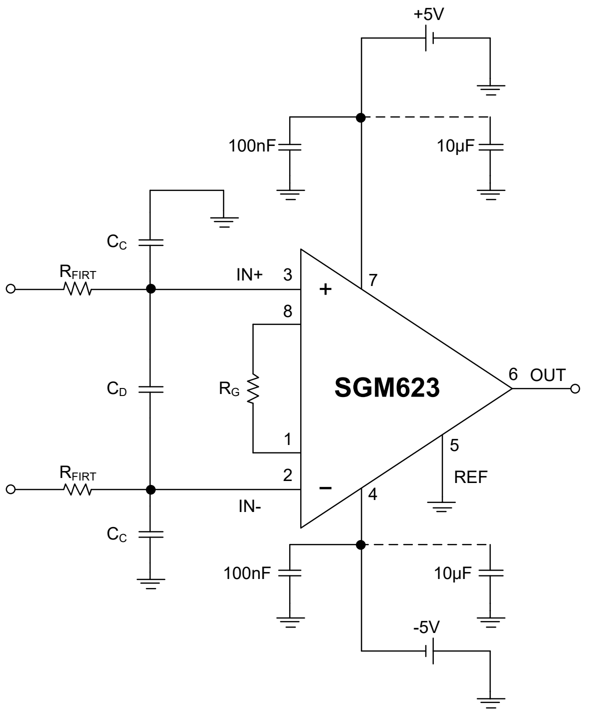


Figure 6. One Method to Reduce the Interference of RF

Common Mode Rejection

The common mode rejection ratio of the instrumentation amplifier is high as it can measure the differential signal between the two inputs when both IN+ and IN- increase or decrease equally. Also, this specification can be defined in the whole range of input voltage.

To obtain a best CMRR, it is recommended that the REF pin should be connected to a low impedance input and the difference of impedance between two inputs should be as small as possible. Also, using shielded cable can effectively reduce the noise of the circuit, and it should be driven properly for better value of CMRR. The following two figures (Figure 7 and Figure 8) illustrate the method to increase the CMRR for alternating circuit by bootstrapping the capacitance of the shielded cable, and this kind of method can also reduce the mismatching of capacitance at the inputs.

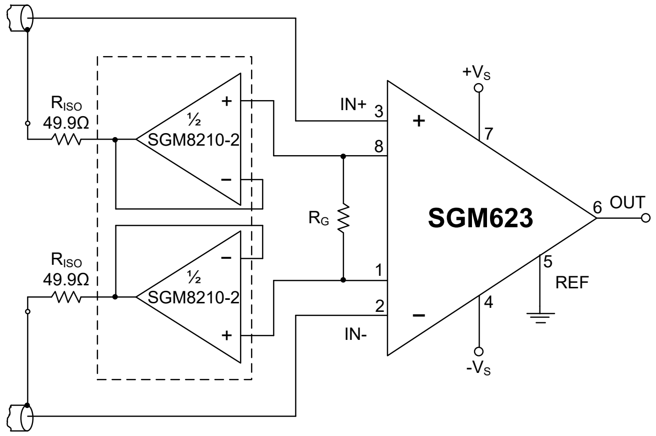


Figure 7. Differential Input Shield Driving

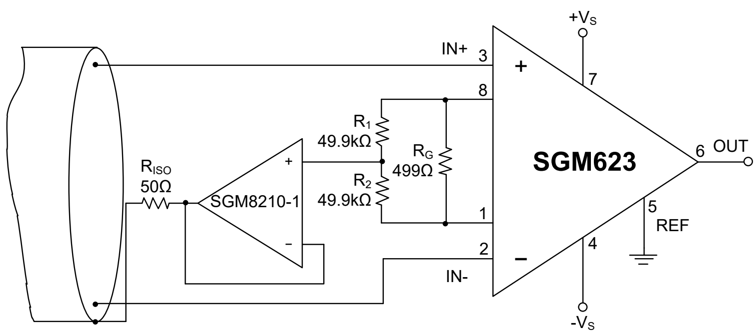


Figure 8. Common Mode Input Shield Driving

APPLICATION INFORMATION (continued)

Isolation of Grounding

For solving the problems of grounding, REF pin should be connected to the "local ground" as the output of the instrumentation amplifier is biased with V_{REF}.

Because of the noisy environment of the digital circuit, the component of data-acquisition such as Analog Digital Converter (ADC) has two pins which are AGND and DGND. Also, the isolation can be made by using a single line or 0Ω resistor. However, each returns of ground should be separated so that the current flow from the sensitive point could be minimized. Also, the ground returns between analog and digital should be tied together with one point, which is shown in ADC part of Figure 9.

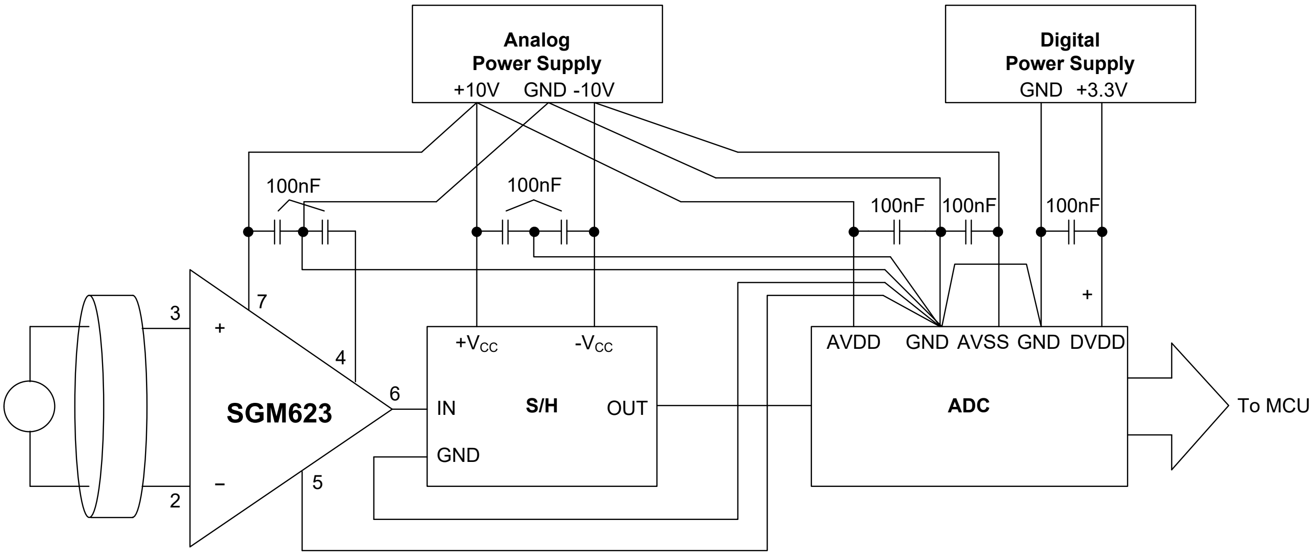


Figure 9. Isolation of Grounding

APPLICATION INFORMATION (continued)

Return of Grounding for I_B

The bias current (I_B) at the inputs is needed for operating and biasing the transistor at the input stage of the instrumentation amplifier, so it is also necessary to design a ground return path for the bias current. For example, for operating the floating inputs of the amplifier (see Figure 10 ~ 12), such as AC-coupled transformer, there should be an electrical line between the input and the ground for ground return of bias current.

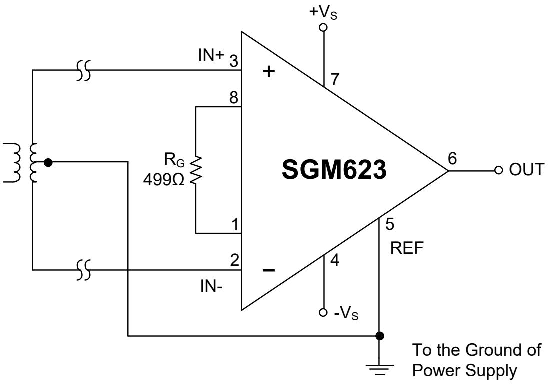


Figure 10. Return of Grounding for I_B with Transformer-Coupled Inputs

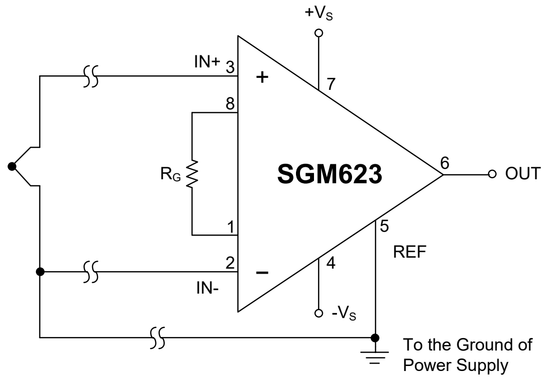


Figure 11. Return of Grounding for I_B with Thermocouple Inputs

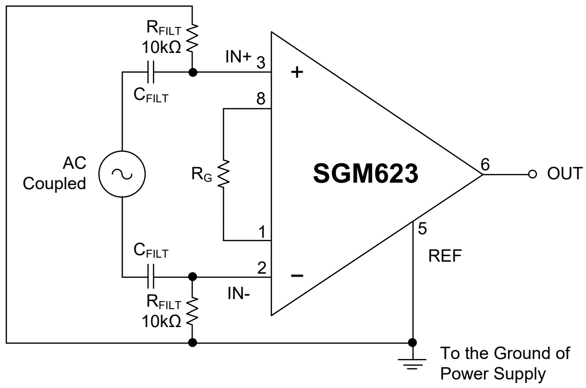


Figure 12. Return of Grounding for I_B with AC-Coupled Input

APPLICATION INFORMATION (continued)

Layout Requirements

A good layout is very important for signal processing circuits. Please refer to the following content for detailed requirements.

Power Supply

A clean and low noise power supply is very important in instrument amplifier circuit design. Besides of input signal noise, the power supply is one of important source of noise to the instrument amplifier through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. Usually, in applications, a 10μF and a 0.1μF decoupling capacitors are used, and the decoupling capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

Grounding

In applications, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high precision applications, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Input and REF Terminal

To prevent the input signal from being affected by unexpected interference and reduce parasitic coupling, the input end should be kept as far away from the interference source as possible. When laying out, it is necessary to ensure that the input signal traces are short and directly routed. In order to obtain a more accurate output voltage, the reference pin should be connected to a low noise and stable voltage source or to a clean ground plane based on the user's circuit design.

R_G Terminal

In order to prevent the impact of radio frequency interference (RFI) and achieve a higher CMRR, it is necessary to minimize parasitic capacitance and inductance on the R_G pin as much as possible. In addition, the PCB traces from the R_G configuration resistor to the R_G pin should be as short as possible, and the trace between the two R_G pins connecting the resistors at both ends should be as symmetrical as possible. For example, in applications where analog switches are used to switch R_G to configure circuit gain, it is important to ensure that the parasitic capacitance of the selected switch is as small as possible.

During the layout design, the external components related to instrumentation amplifier should be placed as close to the chip as possible. The Figure 13 is SGM623 PCB layout example for reference only.

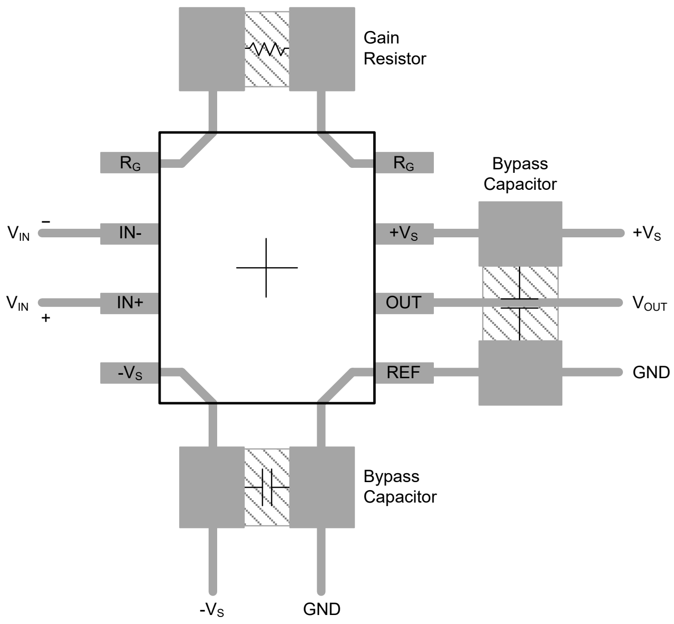


Figure 13. PCB Layout Example

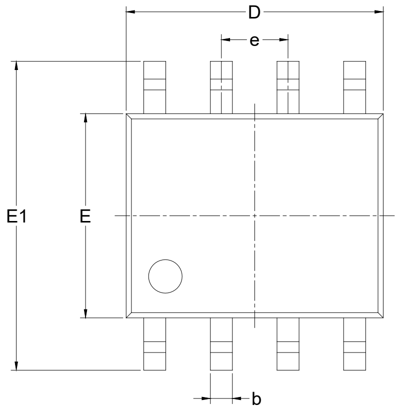
REVISION HISTORY

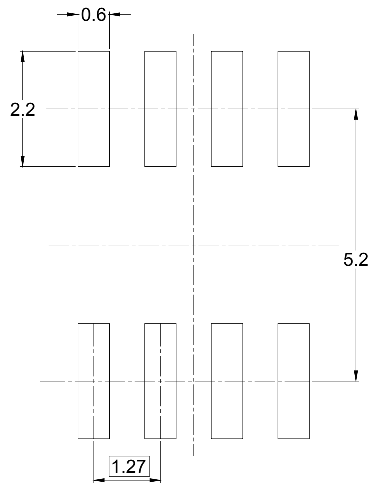
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data	All

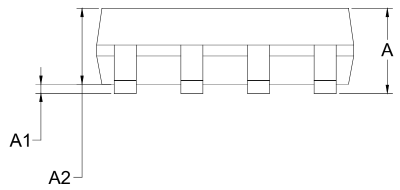
PACKAGE OUTLINE DIMENSIONS

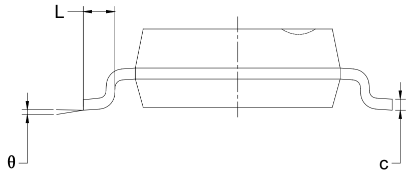
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



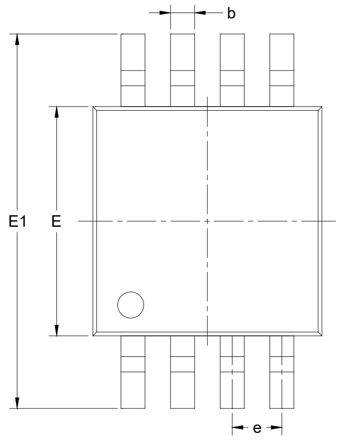


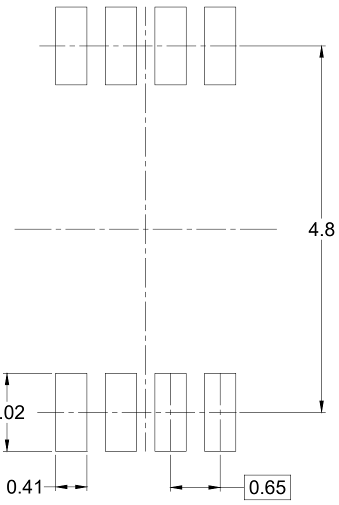
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

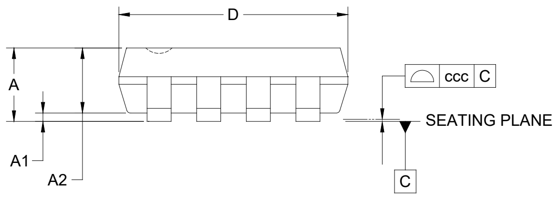
PACKAGE OUTLINE DIMENSIONS

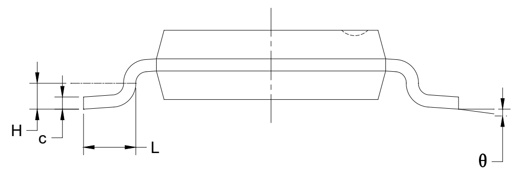
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



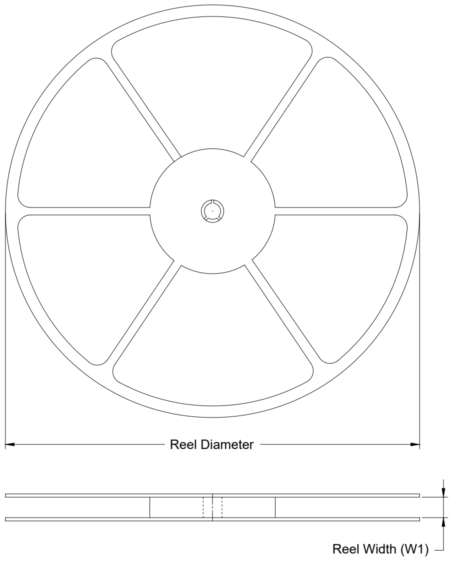


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.220	-	0.380
c	0.080	-	0.230
D	2.800	-	3.200
E	2.800	-	3.200
E1	4.650	-	5.150
e	0.650 BSC		
L	0.400	-	0.800
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

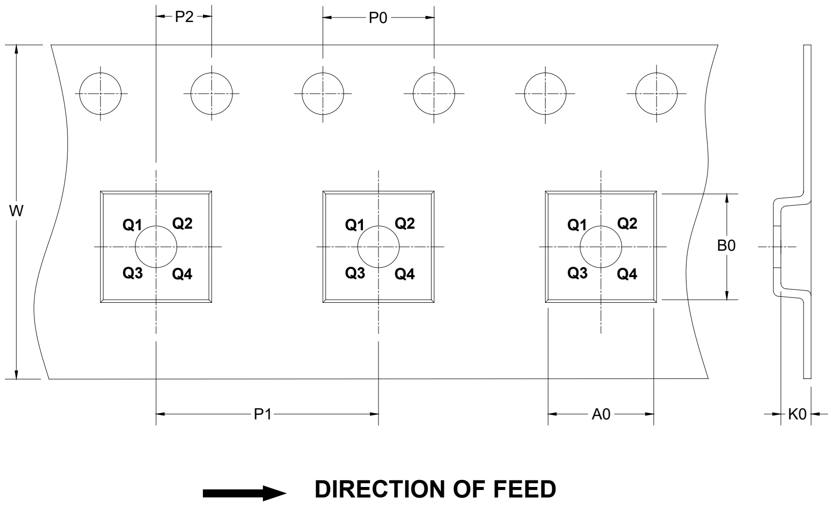
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



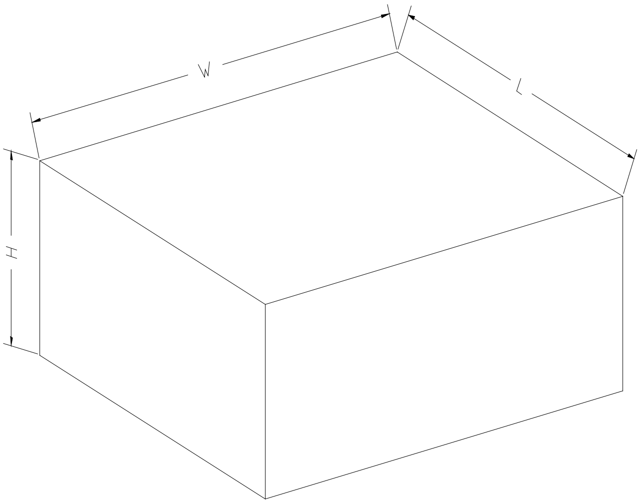
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002