

GENERAL DESCRIPTION

The SGM819S is an independent watchdog timer circuit. It can be used to guard against system failures due to hardware types like peripherals errors and bus occupancy or software types like infinite code execution in a loop.

This device has a WDI input and an nWDO output. In normal conditions, the WDI is toggled within the preset timeout period called t_{WD} in order to clear the watchdog timer. However, if an error event occurs and the watchdog timer is not reset within t_{WD} , the nWDO is asserted to send out the alarm signal.

The SGM819S has an enable pin (nEN) to control the device to turn on/off the watchdog function. To turn on the watchdog function, just connect nEN pin which has a built-in pull-down resistor to GND or leave it floating.

The SGM819S is available in Green UTDFN-1.45×1-6AL and SOT-23-5 packages. It operates over the junction temperature range of -40°C to +125°C.

DEVICE DESCRIPTION

Model: SGM819S-m/SGM819S-mn						
Watchdog Timeout Period Options						
Option Code: "m"	A	B	C	D	E	F
Watchdog Timeout Period	3.4ms	6.8ms	108.8ms	1.7s	7.0s	27.9s
Watchdog Active Time Options						
Option Code: "n"	A		B			
Watchdog Active Time	27.2ms		217.6ms			

FEATURES

- **Current Consumption:** 3.5μA (TYP)
- **Six Selectable Watchdog Timeout Periods:** 3.4ms, 6.8ms, 108.8ms, 1.7s, 7.0s and 27.9s
- **Two Selectable Watchdog Active Time:** 27.2ms and 217.6ms
- **Watchdog Timer Accuracy:** ±20%
- **Active-Low Enable Input**
- **Open-Drain nWDO Output**
- **Available in Green UTDFN-1.45×1-6AL and SOT-23-5 Packages**

APPLICATIONS

Industrial Equipment
Telecommunications
Safety Applications
Networking
Medical Equipment
UPS System

TYPICAL APPLICATION

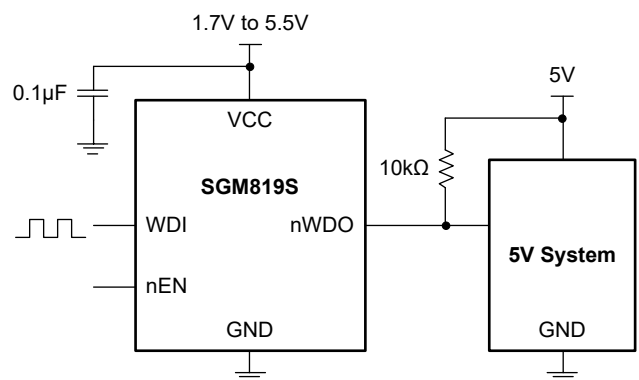


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM819S-A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-AXUDL6G/TR	1MX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-AXN5G/TR	1GV XXXXX	Tape and Reel, 3000
SGM819S-BA	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-BAXUDL6G/TR	1NX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-BAXN5G/TR	1GW XXXXX	Tape and Reel, 3000
SGM819S-BB	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-BBXUDL6G/TR	1OX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-BBXN5G/TR	1GX XXXXX	Tape and Reel, 3000
SGM819S-CA	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-CAXUDL6G/TR	1PX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-CAXN5G/TR	1GY XXXXX	Tape and Reel, 3000
SGM819S-CB	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-CBXUDL6G/TR	1FX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-CBXN5G/TR	15L XXXXX	Tape and Reel, 3000
SGM819S-DA	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-DAXUDL6G/TR	1QX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-DAXN5G/TR	1GZ XXXXX	Tape and Reel, 3000
SGM819S-DB	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-DBXUDL6G/TR	1RX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-DBXN5G/TR	15M XXXXX	Tape and Reel, 3000
SGM819S-EA	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-EAXUDL6G/TR	1SX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-EAXN5G/TR	1H0 XXXXX	Tape and Reel, 3000
SGM819S-EB	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-EBXUDL6G/TR	1TX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-EBXN5G/TR	1H1 XXXXX	Tape and Reel, 3000
SGM819S-FA	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-FAXUDL6G/TR	1UX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-FAXN5G/TR	1H2 XXXXX	Tape and Reel, 3000
SGM819S-FB	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM819S-FBXUDL6G/TR	1VX	Tape and Reel, 5000
	SOT-23-5	-40°C to +125°C	SGM819S-FBXN5G/TR	1H3 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: X = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

UTDFN-1.45×1-6AL

YY X

— Date Code - Quarter
— Serial Number

SOT-23-5

XXXXX

— Vendor Code
— Trace Code
— Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to 7V
Input or Output Voltage, V_{IN} , V_{OUT}	-0.3V to $V_{CC} + 0.3V$
Output Current.....	20mA
Package Thermal Resistance	
UTDFN-1.45×1-6AL, θ_{JA}	231.3°C/W
UTDFN-1.45×1-6AL, θ_{JB}	117.9°C/W
UTDFN-1.45×1-6AL, θ_{JC}	176.2°C/W
SOT-23-5, θ_{JA}	180.1°C/W
SOT-23-5, θ_{JB}	46°C/W
SOT-23-5, θ_{JC}	69.5°C/W
Junction Temperature.....	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM.....	±4000V
CDM	±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}	1.7V to 5.5V
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.2V to $0.8 \times V_{CC}$
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

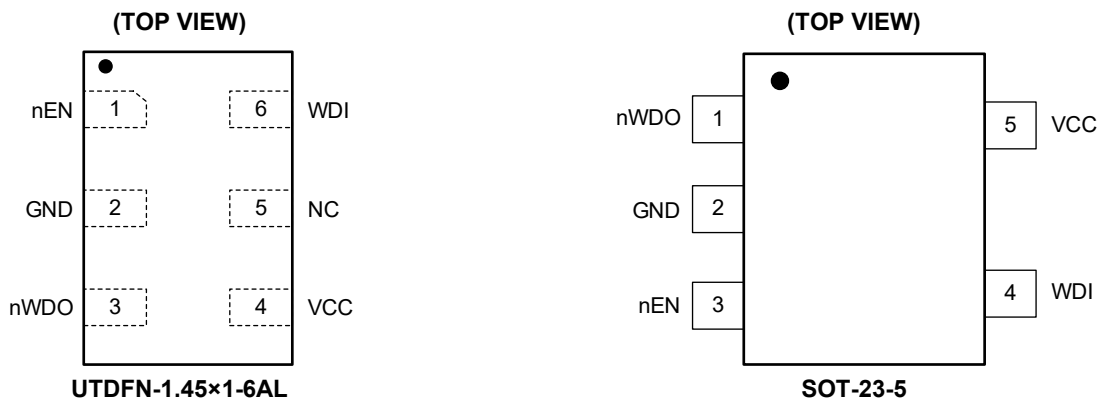
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

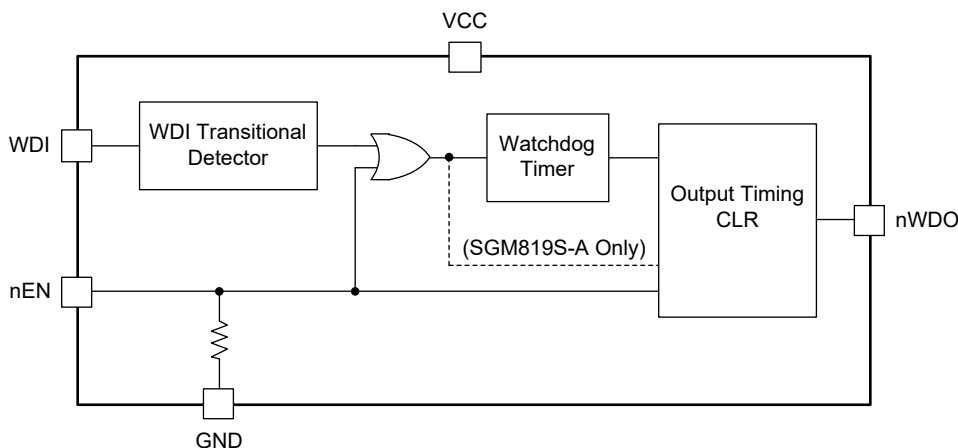
PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		NAME	FUNCTION
UTDFN-1.45×1-6AL	SOT-23-5		
1	3	nEN	Active-Low Enable Input Pin.
2	2	GND	Ground.
3	1	nWDO	Watchdog Output Pin.
4	5	VCC	Supply Voltage.
5	—	NC	No Connection.
6	4	WDI	Watchdog Input Pin. This pin cannot be left floating.

FUNCTIONAL BLOCK DIAGRAM



NOTE: If the positive pulse on the enable pin, nEN, is longer than 1μs, it resets the watchdog.

Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.7V to 5.5V, T_J = -40°C to +125°C, typical values are measured at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V _{CC}		1.7	3.3	5.5	V
VCC Supply Current	I _{CC}			3.5	10	μA
Open-Drain Output Leakage Current	I _{LO}	From output to the GND or VCC	-1		1	μA
WDI Input Leakage Current			-1		1	μA
WDI, nEN Input High Voltage	V _{IH}		0.7 × V _{CC}			V
WDI, nEN Input Low Voltage	V _{IL}				0.3 × V _{CC}	V
nWDO Output Voltage		I _{SINK} = 1.2mA			0.2	V
		I _{SINK} = 3.2mA			0.4	
Enable Pin (nEN)						
nEN Input Pulse Width			1			μs
nEN Glitch Rejection				100		ns
nEN to nWDO delay ⁽¹⁾				120		ns
nEN Pull-Down Resistance			40	70	100	kΩ
Watchdog Timer						
Timer Startup Voltage	V _{START}		1.26	1.41	1.58	V
Watchdog Timeout Period	t _{WD}	SGM819S-A	2.8	3.4	4.0	ms
		SGM819S-Bn (n = A, B)	5.5	6.8	8.1	
		SGM819S-Cn (n = A, B)	87.1	108.8	130.5	
		SGM819S-Dn (n = A, B)	1.4	1.7	2.08	s
		SGM819S-En (n = A, B)	5.6	7.0	8.3	
		SGM819S-Fn (n = A, B)	22.3	27.9	33.4	
Watchdog Active Time	t _{PW}	SGM819S-mA (m = B, C, D, E, F)	21.8	27.2	32.6	ms
		SGM819S-mB (m = B, C, D, E, F)	174.1	217.6	261.1	
WDI Pulse Width			1			μs
WDI Glitch Rejection				100		ns
WDI to nWDO Delay ⁽²⁾				100		ns

NOTES:

1. nWDO asserts for minimum of 20μs even if nEN transitions high.
2. nWDO asserts for minimum of 20μs regardless of transition on WDI (valid for SGM819S-A only).

DETAILED DESCRIPTION

The SGM819S is a watchdog timer circuit to monitor the operating state of the MCU. A watchdog reset signal must be issued before the watchdog timeout period ends. If not, the watchdog timeout function is activated and the watchdog output is asserted low. The watchdog function can also be turned on or off through nEN pin.

Watchdog Input (WDI)

The WDI pin is used to periodically reset the watchdog in a watchdog timeout period, t_{WD} . The WDI pin must be toggled in the period of t_{WD} or the watchdog output, nWDO, is asserted. The following conditions can reset the watchdog timer:

1. By a transition on nWDO (see Timeout without Re-Trigger section)
2. By a pulse on nEN (see nEN Triggering section)
3. By a transition on WDI (rising edge effective on all versions and falling edge effective on the all versions excluding SGM819S-A).

The WDI input detects the pulse width larger than $1\mu s$, and ignores pulse width less than 100ns.

If WDI maintains a stable logic state (high or low) and nEN is logic low, the nWDO of SGM819S-A flips every t_{WD} and the rest versions flip every t_{WD} and t_{PW} (see Timeout without Re-Trigger section).

Watchdog Output (nWDO)

During the power-on process, the watchdog timer begins to count after the VCC voltage is higher than the timer startup voltage, V_{START} . Once the timer is not reset within t_{WD} , the nWDO turns to logic low (see Power-On section).

For SGM819S-A, the nWDO is asserted low for a period between $20\mu s$ and t_{WD} when the watchdog timeout event occurs (see Timeout without Re-Trigger and Trigger after Timeout sections). For the rest versions, the nWDO is asserted low for t_{PW} without detecting the WDI transitions (see Trigger after Timeout section).

The nWDO pin is an open-drain structure. Connect this pin to a voltage rail no larger than 6V through an external pull-up resistor as shown in Figure 3. Users should carefully consider the factors such as capacitive loading, logic low output voltage (V_{OL}), and the leakage current through the nWDO pin (I_{LO}) to select appropriate resistance values. It ensures that the high and low output voltage values meet the requirements of subsequent applications. A 10k Ω pull-up resistor is recommended in most conditions.

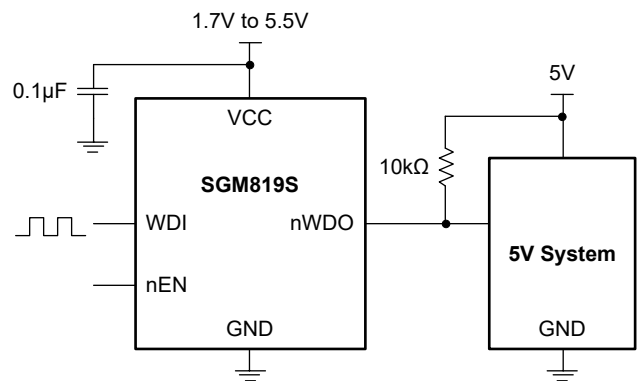


Figure 3. Open-Drain nWDO Output Connection

Chip Enable Input (nEN)

All those mentioned in Watchdog Input (WDI) and Watchdog Output (nWDO) are described in the precondition that nEN is logic low. The function logic of nEN is the same to all versions of SGM819S.

During the power-on process, if nEN goes high after VCC voltage is higher than V_{START} but before t_{WD} , the nWDO keeps high as long as nEN is high. Once nEN goes low, the nWDO is asserted after t_{WD} . If nEN goes high at any time of nWDO, the nWDO goes high immediately. Note that the minimum nWDO asserted time is $20\mu s$ (see nEN Triggering section).

The nEN input detects the pulse width larger than $1\mu s$, and ignores pulse width less than 100ns.

TIMING DIAGRAM

Power-On

In the power-on process, the watchdog timer starts running once V_{CC} rises above about V_{START} .

Transitions of WDI do not matter. WDI can be either logic high or low but not floating. For the SGM819S-A, low-to-high edge on WDI will clear the watchdog timer. For the other models, both low-to-high edge and high-to-low edge on WDI will clear the watchdog timer. WDI transition has nothing to do with starting the watchdog timing.

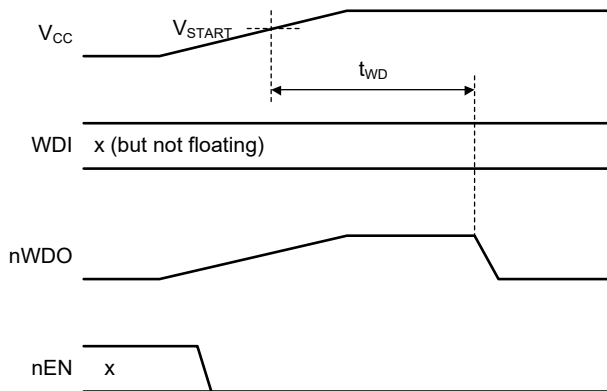


Figure 4. Power-On Timing Diagram of SGM819S

Normal Triggering

For the SGM819S-A, only rising edge of WDI is effective. Falling edge is invalid.

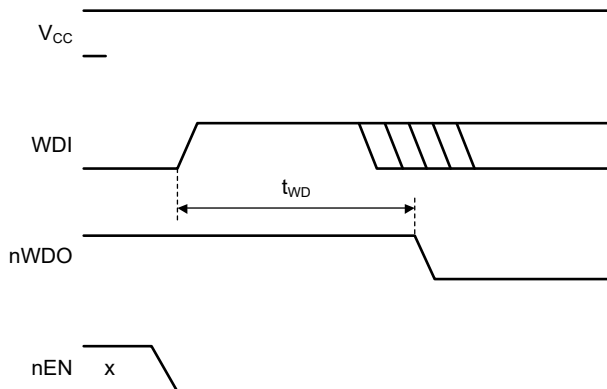


Figure 5. Normal Triggering Timing Diagram of SGM819S-A

For the other models, both rising edge and falling edge are effective.

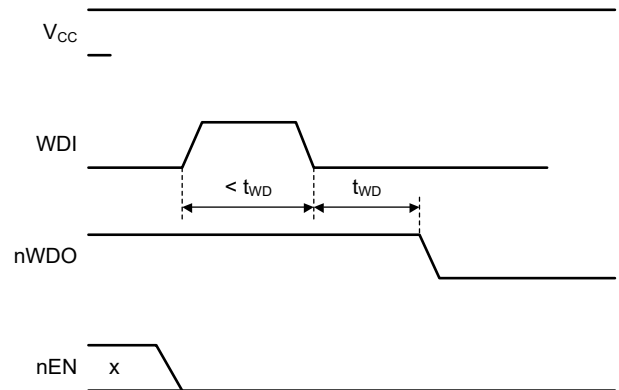


Figure 6. Normal Triggering Timing Diagram of All Models except SGM819S-A

Timeout without Re-Trigger

For the SGM819S-A, when a timeout event occurs, nWDO will be asserted low for t_{WD} and then goes high. Once no rising edge of WDI is detected within t_{WD} , nWDO will be asserted low for t_{WD} again. The nWDO keeps this way unless a rising edge of WDI is detected.

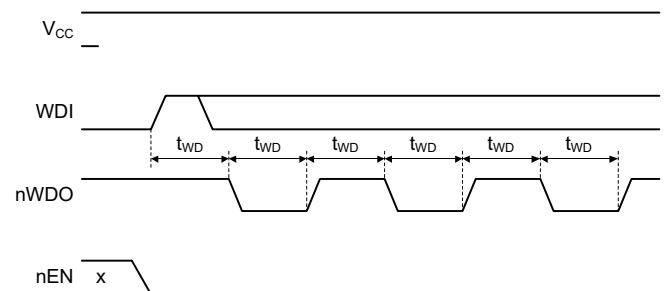


Figure 7. Timeout without Re-Trigger Timing Diagram of SGM819S-A

For the other models, when a timeout event occurs, nWDO will be asserted low for t_{PW} and then goes high. Once no rising/falling edge of WDI is detected within t_{WD} , nWDO will be asserted low for t_{PW} again. The nWDO keeps this way unless a rising or falling edge of WDI is detected.

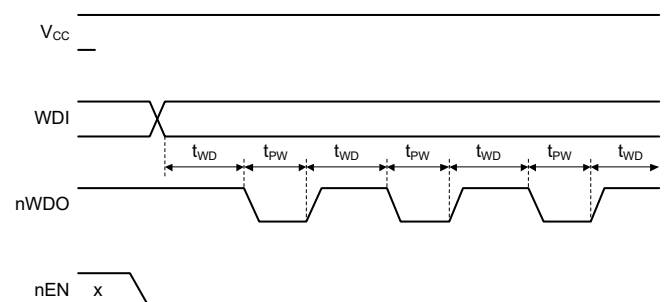


Figure 8. Timeout without Re-Trigger Timing Diagram of All Models except SGM819S-A

TIMING DIAGRAM (continued)

Trigger after Timeout

For the SGM819S-A, when the WDI goes high after the nWDO is asserted low, the nWDO will be asserted for minimum 20 μ s regardless of the WDI transitions.

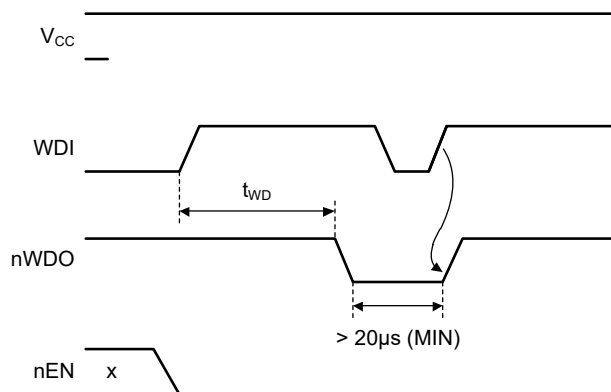


Figure 9. Trigger after Timeout Timing Diagram of SGM819S-A

For the other models, when the WDI goes high after the nWDO is asserted low, the trigger of WDI is invalid and the nWDO will be asserted for t_{PW} . Trigger of WDI is ignored when nWDO is low.

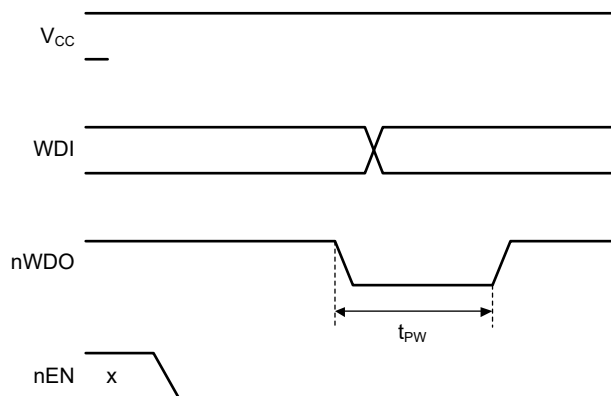


Figure 10. Trigger after Timeout Timing Diagram of All Models except SGM819S-A

nEN Triggering

For all versions of SGM819S, once nEN goes high, all timing is cleared and the watchdog is disabled. Timing counts again from 0 when nEN goes low. WDI can be either logic high or low but not floating.

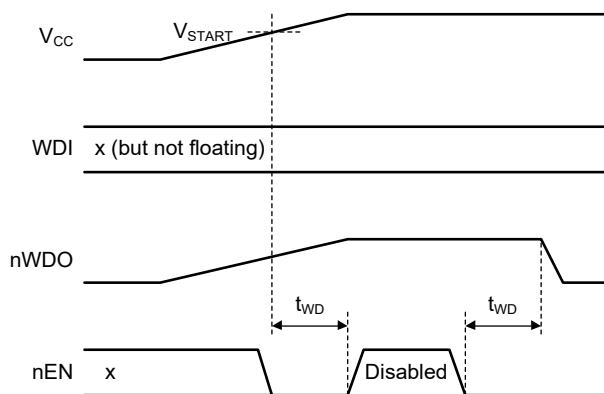


Figure 11. nEN Triggering Diagram 1

For all versions of SGM819S, when nEN goes high in the asserted state of nWDO, the nWDO will be asserted for minimum 20 μ s regardless of the nEN transitions. WDI can be either logic high or low but not floating.

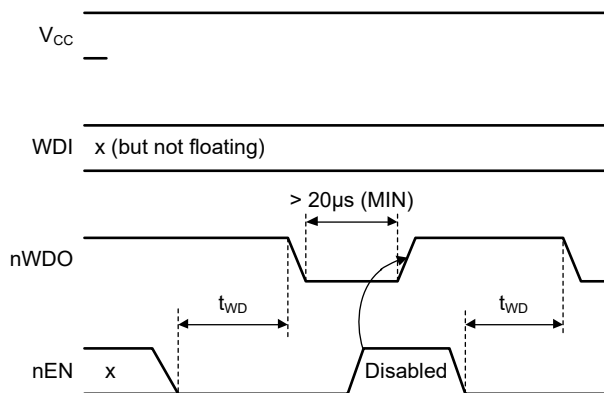


Figure 12. nEN Triggering Diagram 2

APPLICATION INFORMATION

Interfacing to μ P with Bidirectional Reset Pins

The reset pin of some μ P devices is bidirectional and can be connected with nWDO of SGM819S. Connecting the nWDO output of SGM819S to nRST output of μ P directly may cause race conditions and hazards. For example, if nWDO is logic high and the nRST is logic low, connecting them directly may result in indeterminate logic levels or even damage the nRST pin of μ P. Therefore, a 4.7k Ω resistor is recommended to be connected between nWDO and the μ P reset I/O as show in Figure 13. Besides, buffer the nWDO output to reset other system components.

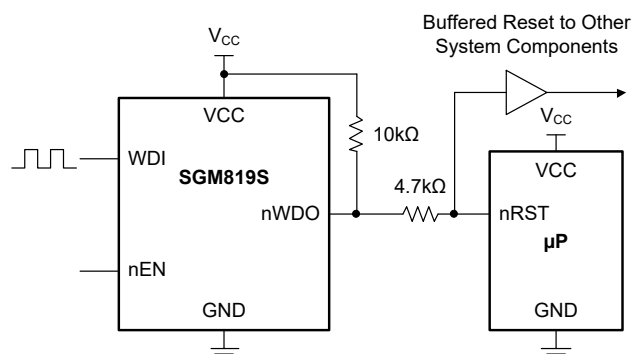


Figure 13. Interfacing to μ P with Bidirectional Reset I/O

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2025 – REV.A to REV.A.1

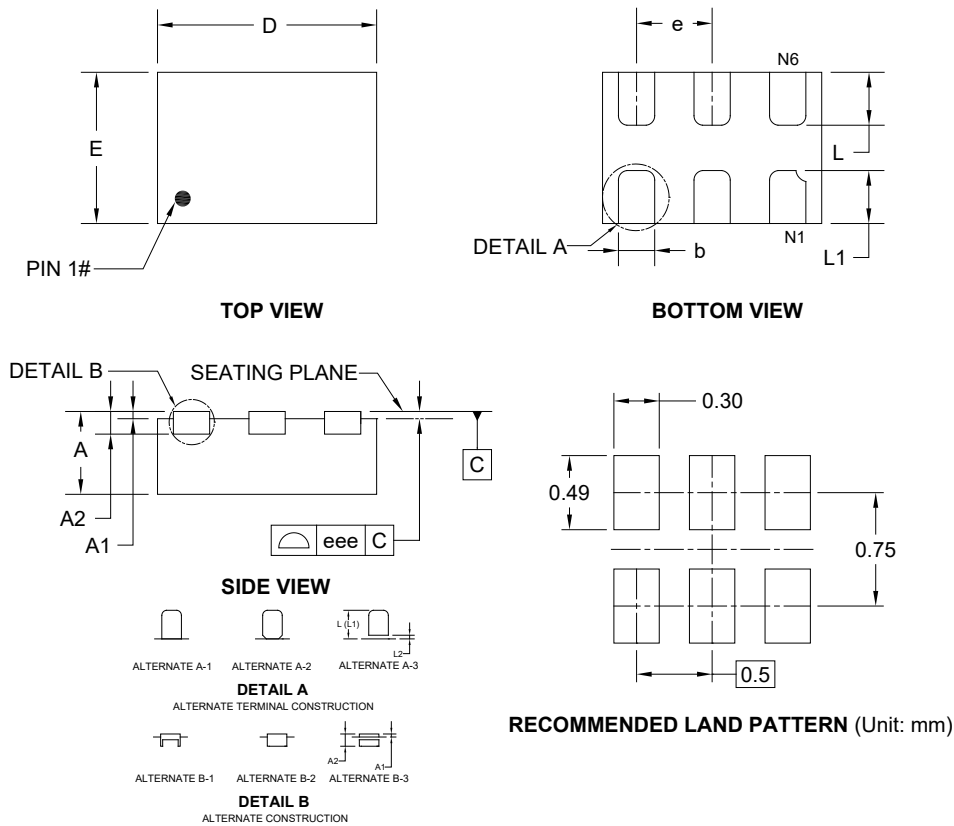
	Page
Added UTDFN-1.45×1-6AL package	2, 3, 4, 10

Changes from Original to REV.A (JULY 2024)

	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

UTDFN-1.45×1-6AL

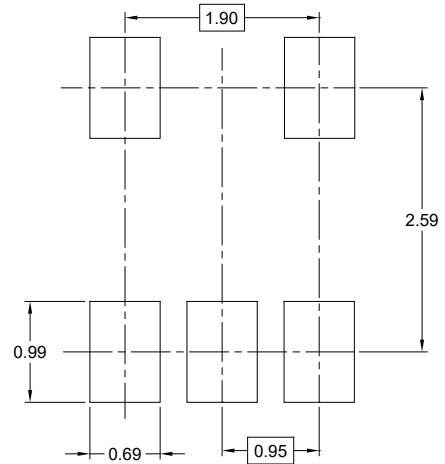
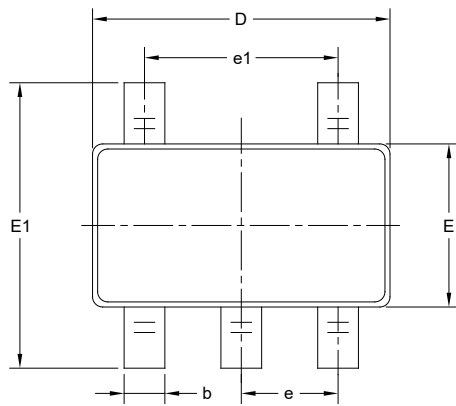


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.450	-	0.600
A1	-0.004	-	0.050
A2	0.150 REF		
b	0.150	-	0.300
D	1.374	-	1.526
E	0.924	-	1.076
e	0.500 BSC		
L	0.250	-	0.450
L1	0.250	-	0.500
L2	0.000	-	0.100
eee	0.050		

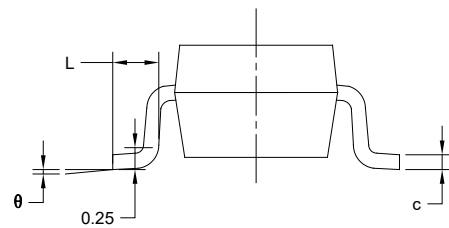
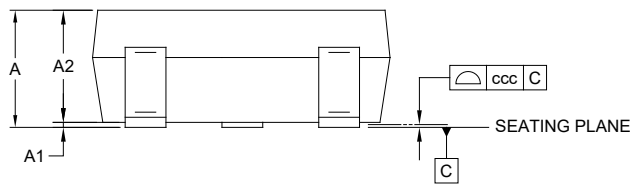
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

SOT-23-5



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

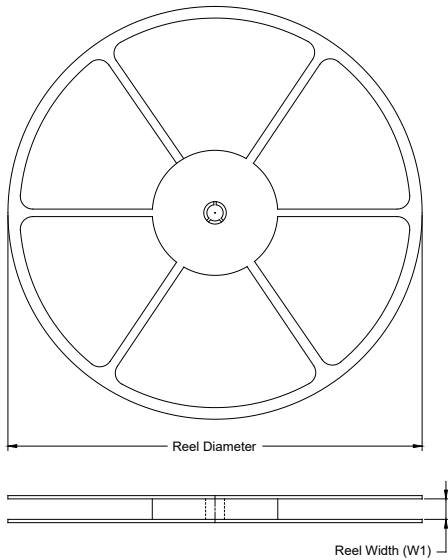
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

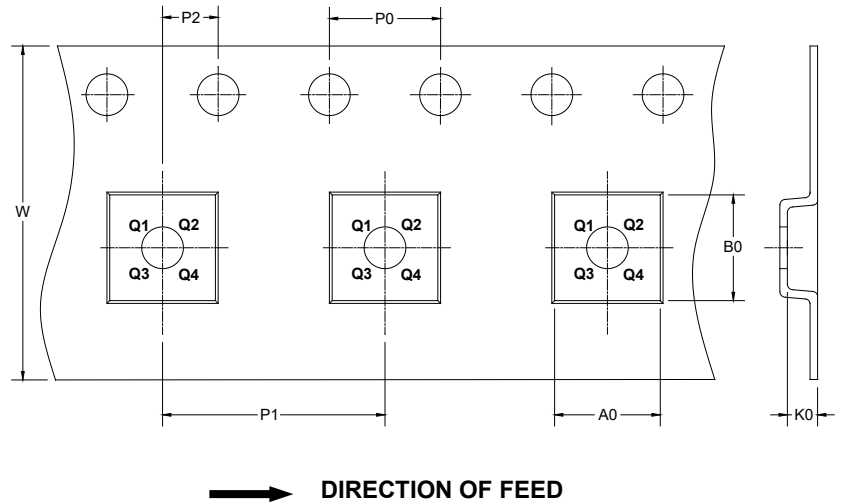
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

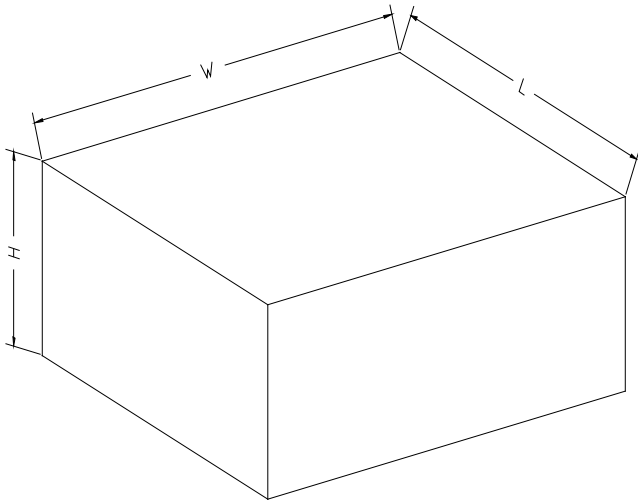
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.45×1-6AL	7"	9.5	1.15	1.60	0.75	4.0	4.0	2.0	8.0	Q1
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002