SGM31180
18-Channel LED Driver with Selectable PWM Frequency

GENERAL DESCRIPTION

SGM31180 consists of 18 constant current channels each with independent PWM control, designed for driving LEDs. PWM frequency can be programmed to the corresponding value according to 8/10/12/16-bit PWM resolution setting and oscillator frequency setting via I^2C interface. The output current of each channel can be set to 20mA via a 4kΩ external resistor and an internal register. SGM31180 has a current limit function to avoid over current, which is configured by register bit. The average LED current of each channel can be changed in maximum 65535 steps by changing the PWM duty cycle via an I^2C interface.

Pulling SDB low or using the software shutdown feature can turn off the SGM31180 to reduce power consumption.

SGM31180 is available in a Green TQFN-4×4-32AL package. It operates from 2.7V to 5.5V over the temperature range of -40℃ to +85℃.

APPLICATIONS

Mobile Phones and Other Hand-Held Devices for LED Display

LED in Home Appliances

FEATURES

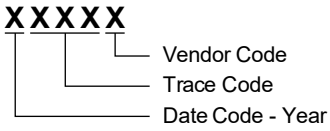
- **2.7V to 5.5V Supply**
- **I^2C Interface, Automatic Address Increment Function**
- **Four Selectable I^2C Addresses and a Broadcast Address**
- **SDB Reset I^2C Module and Internal Reset Register**
- **ECO Mode for Auto Power Saving**
- **High Precision Current Sinking**
  - **Device to Device Error: ±5%**
  - **Channel to Channel Error: ±5%**
- **Adjustable PWM Frequency:**
  - **125kHz; 62.5kHz; 31kHz; 488Hz; 244Hz; 122Hz @ 8-Bit PWM Resolution**
  - **31kHz; 15.6kHz; 7.8kHz; 122Hz @ 10-Bit PWM Resolution**
  - **7.8kHz, 3.9kHz, 2kHz @ 12-Bit PWM Resolution**
  - **488Hz, 244Hz, 122Hz @ 16-Bit PWM Resolution**
- **18-Channel RGB LED Driver**
  - **256-Level Global Current Configuration**
  - **256-Level Green/Red/Blue Light Current Setting**
  - **256-Level LED Module Current Setting**
  - **Max 65535-Level Individual PWM Modulation**
- **EMI and Audible Noise Reduction**
  - **Phase Shifting and Inverting Function**
  - **Spread Spectrum Function**
  - **PWM Scatter Method**
- **-40℃ to +85℃ Temperature Range**
- **Available in a Green TQFN-4×4-32AL Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM31180	TQFN-4×4-32AL	-40℃ to +85℃	SGM31180YTSE32G/TR	SGM31180 YTSE32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.3V to 6.0V
Voltage at SCL, SDA, SDB, OUT1 to OUT18
..... -0.3V to 6.0V
Package Thermal Resistance
TQFN-4×4-32AL, θ_{JA} ..... 32.4℃/W
TQFN-4×4-32AL, θ_{JB} ..... 11.6℃/W
TQFN-4×4-32AL, $\theta_{JC\ (TOP)}$ ..... 29℃/W
TQFN-4×4-32AL, $\theta_{JC\ (BOT)}$ ..... 4.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

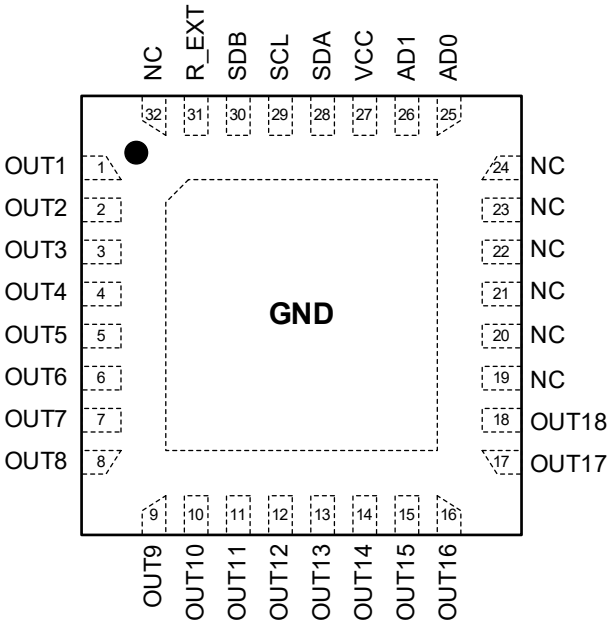
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM31180 (TOP VIEW)

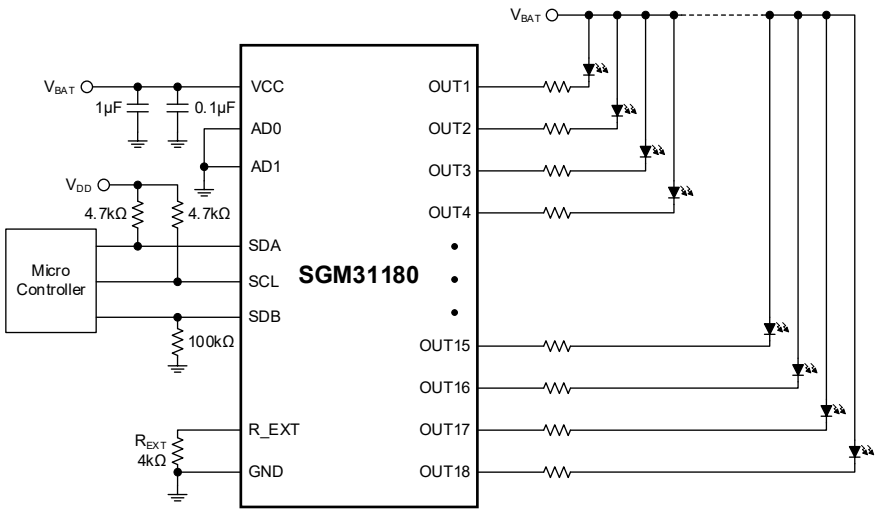


TQFN-4×4-32AL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1 ~ 18	OUT1 ~ OUT18	Output Channel 1 ~ 18 for LEDs.
19 ~ 24, 32	NC	No Connection.
25	AD0	I^2C Address Setting. Connect to GND, VCC to assign the I^2C address of the device. See Table 2 for details.
26	AD1	
27	VCC	Power Supply.
28	SDA	I^2C Serial Data Line.
29	SCL	I^2C Serial Clock Line.
30	SDB	Shutdown the chip when pulled low.
31	R_EXT	Input Terminal Used to Connect an External Resistor. This regulates the global output current.
Exposed Pad	GND	Ground.

TYPICAL APPLICATION



NOTE: 1. The maximum global output current is set to 20mA when R_{EXT} = 4kΩ. Please see Page 9 for setting LED current.

Figure 1. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.6V, R_{EXT} = 4kΩ, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7		5.5	V
VCC UVLO Rising Threshold	V_{UVLO_R}			2.5		V
VCC UVLO Falling Threshold	V_{UVLO_F}			2.35		V
Maximum Sink Current per Channel	I_{MAX}	V_{OUT} = 0.8V, at 100% PWM and full DC Current	19	20	21	mA
Sink Current Limit per Channel	I_{LIM_L}	V_{REXT} = 0V	40	60	80	mA
	I_{LIM_H}	V_{REXT} = 0V	65	90	120	mA
Headroom Voltage per Channel	V_{HR}	the voltage when the LED current drops 5%, at 100% PWM and full DC Current		180	320	mV
Quiescent Current of VCC	I_{CC}	V_{SDB} = V_{CC}, enable CHIP_EN, at 100% PWM and full DC Current		11	13	mA
		V_{SDB} = V_{CC}, enable CHIP_EN, at 100% PWM and no DC Current		4	6	mA
Standby Current of VCC	I_{STB}	V_{SDB} = V_{CC}, enable CHIP_EN and ECO mode, all output PWM registers = 0h > 32ms		1.5		μA
		V_{SDB} = V_{CC}, disable CHIP_EN		1.5	3	μA
Shutdown Current of VCC	I_{SD}	V_{SDB} = 0V		0.1	1	μA
PWM Frequency of Output	f_{OUT}	Set as 8-bit PWM, f_{OSC} = 32MHz		125		kHz
		Set as 8-bit PWM, f_{OSC} = 31.25kHz		122		Hz
Accuracy of PWM Frequency of Output	f_{OUT_ACC}	Set as 8-bit PWM, f_{OSC} = 32MHz	-5		5	%
		Set as 8-bit PWM, f_{OSC} = 31.25kHz	-5		5	%
Device to Device Current Error	I_{ERR_DD}	100% PWM and full DC Current	-5		5	%
Channel to Channel Current Error	I_{ERR_CC}	100% PWM and full DC Current	-5		5	%
Output Leakage Current	I_{OZ}	V_{OUT} = 5.5V, V_{SDB} = 0V		0.1	1	μA
Thermal Shutdown	T_{SD}			155		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		℃
Output Voltage of R_EXT Pin	V_{EXT}		0.38	0.4	0.42	V
Reference Current Ratio	K_{EXT}			200		
Logic Electrical Characteristics (SDA, SCL, SDB, AD0, AD1)						
SDA, SCL, SDB, AD0/1 Logic Low Voltage	V_{IL}	T_A = -20℃ to +85℃			0.4	V
SDA, SCL, SDB, AD0/1 Logic High Voltage	V_{IH}	T_A = -20℃ to +85℃	0.95			V
Logic “0” Input Current	I_{IL}	V_{INPUT} = 0V		5		nA
Logic “1” Input Current	I_{IH}	V_{INPUT} = V_{CC}		5		nA

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		400		1000	kHz
Bus-Free Time between STOP and START Condition	t_{BUF}	1.3		0.5		μs
START or Repeated START Hold Time	$t_{HD;STA}$	0.6		0.26		μs
Repeated START Setup Time	$t_{SU;STA}$	0.6		0.26		μs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		0.26		μs
Data Hold Time	$t_{HD,DAT}$	0		0		μs
Data Setup Time	$t_{SU;DAT}$	100		50		ns
SCL Low Period	t_{LOW}	1.3		0.5		μs
SCL High Period	t_{HIGH}	0.6		0.26		μs
SDA and SCL Rise Time	t_R		300		120	ns
SDA and SCL Fall Time	t_F	20 × (V_{DD}/5.5)	300	20 × (V_{DD}/5.5)	120	ns
Capacitive Load for Each Bus Line	C_B		400		550	pF
Data Valid Time	$t_{VD;DAT}$		0.9		0.45	μs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9		0.45	μs

NOTE:

1. Industry standard I²C timing characteristics are according to I²C-Bus Specification.

FUNCTIONAL BLOCK DIAGRAM

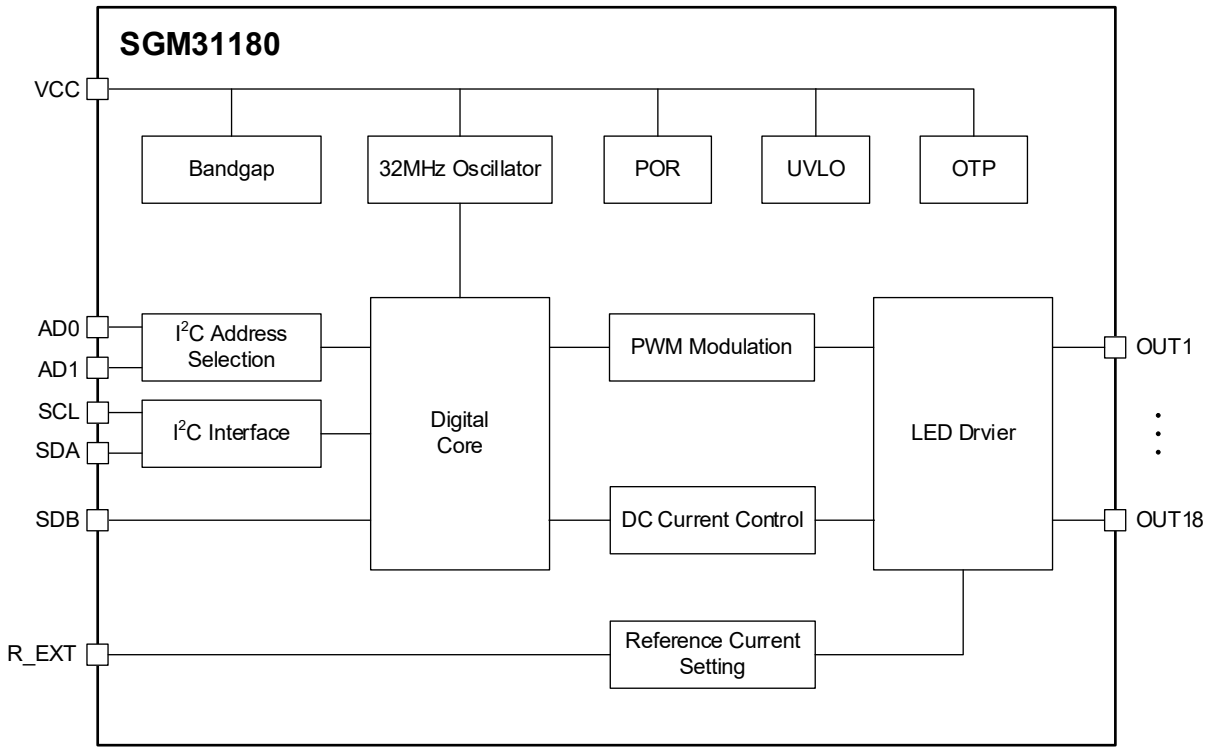


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Operation Description

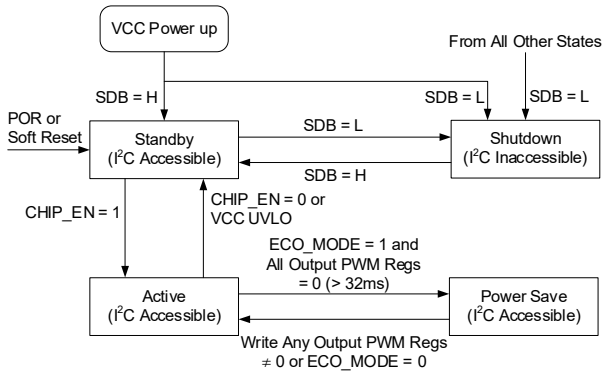


Figure 3. SGM31180 Operation State Diagram

Power-on Reset

Upon initial VCC power-up, SGM31180 is reset. All registers are reset to default values, and the LED driver is shut down. Once V_{CC} falls below the threshold voltage of POR (2V), SGM31180 will be reset again.

It is required to wait for at least 200μs before I^2C write or read operation when V_{CC} rises above the POR threshold and to wait for another 200μs before LED lighting effects are enabled.

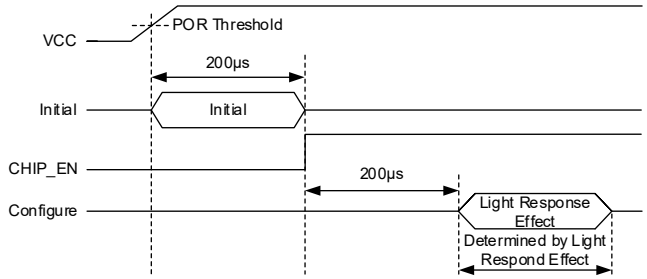


Figure 4. Power-up Timing

Register Reset

By writing 0x00 to REG0x5D reset register, the software reset is triggered. After software reset, all registers are reset to the default value and enter standby mode.

After the software reset command is acknowledged via I^2C bus, it is required to wait for at least 200μs before LED lighting effects are enabled.

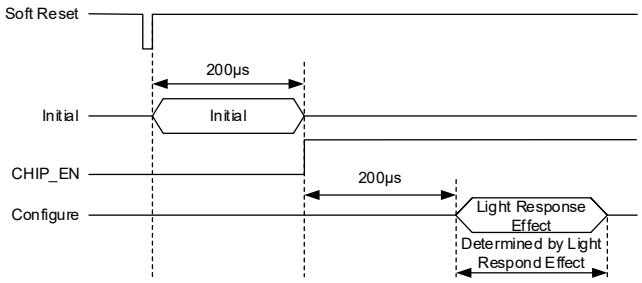


Figure 5. Software Reset Timing

Shutdown Mode

SGM31180 enters shutdown mode automatically when SDB is pulled to low level. In this situation, I^2C interface is not accessible, and all registers cannot be configured and will be reset.

Standby Mode

SGM31180 enters standby mode when SDB is pulled from low to high, or CHIP_EN bit is set from 1 to 0, or VCC under-voltage lockout occurs in active mode. CHIP_EN bit will be reset when VCC voltage is too low or over-temperature protection occurs. In standby mode, all analog blocks are powered down. However, I^2C interface is accessible, and all registers can be configured.

Active Mode

When SDB pin is high and CHIP_EN bit is set to 1, SGM31180 enters the active mode.

ECO Mode

When ECO_MODE is set to 1, the auto ECO mode is enabled. If ECO_MODE = 1 and the values of registers from REG0x01 to REG0x24 are 00H for longer than 32ms, the chip automatically enters ECO mode. Once writing a non-zero value into any register from REG0x01 to REG0x24, the device exits ECO mode and enters active mode immediately.

Over-Temperature Protection

Over-temperature protection is only enabled in active mode. The SGM31180 will shut down all output channels when the temperature rises above +155℃.

VCC Under-Voltage Lockdown Protection

UVLO protection operates in active mode. It prevents abnormal operation in case of VCC under voltage and will shut down the lighting effects. The UVLO falling threshold is 2.35V.

DETAILED DESCRIPTION (continued)

Current Configuration

The average output current of each green/red/blue LED can be expressed as:

$$I_{OUTn} = K \times \frac{V_{REXT}}{R_{EXT}} \times \frac{I_{GLB}}{255} \times \frac{I_{COLz}}{255} \times \frac{I_{LEDy}}{255} \times \frac{PWMx}{256\times256} \quad (1)$$

where

K is the voltage ratio of 200;

V_{REXT} is the reference voltage on R_{EXT} pin, 0.4V;

R_{EXT} is the hardware resistor on R_{EXT} pin;

I_{GLB} is the 8-bit global current register;

I_{COLz} is the 8-bit single color current register;

z is the number of the single color, from 1 to 3. For specific controlled output pins, please refer to the register description;

I_{LEDy} is 8-bit LED module current register;

y is the number of the LED modules, from 1 to 6. For specific controlled output pins, please refer to the register description;

PWMx is 16-bit PWM register of each LEDs, consisting of the PWMx_LSB and the PWMx_MSB;

x is the number of the output pins, from 1 to 18.

The maximum output current for one green/red/blue LED is decided by R_{EXT}, I_{GLB}, I_{COLz}, I_{LEDy}, and PWMx, which is 20mA at R_{EXT} = 4kΩ. The recommended minimum value of R_{EXT} is 2kΩ. The current limit is set by ILIM bit, even if R_{EXT} is shorted.

PWM Modulation

The PWM frequency is decided by three bits of oscillator frequency setting and two bits of PWM resolution setting. Table 1 shows the relationship of PWM frequency and related bits. To avoid the MLCC audible noise, it is recommended to use PWM frequency lower than 500Hz or higher than 20kHz.

If PWM is set to FFFFH, the output duty cycle is forced to full duty cycle (100%).

Table 1. PWM Frequency Setting

PWM Frequency						
OSC_FRQ[2:0] / PWM_RES[1:0]	000b	001b	010b/ 011b	100b	101b	110b/ 111b
00b: 8-Bit	125kHz	62.5kHz	31kHz	488Hz	244Hz	122Hz
01b: 10-Bit	31kHz	15.6kHz	7.8kHz	122Hz	—	—
10b: 12-Bit	7.8kHz	3.9kHz	2kHz	—	—	—
11b: 16-Bit	488Hz	244Hz	122Hz	—	—	—

Output PWM Scatter Method

The PWM scatter function is controlled by REG0x5B[7], which can scatter the positive pulse width to the entire PWM period (see Figure 6).

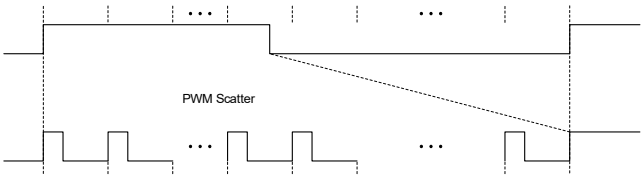


Figure 6. PWM Scatter Timing Diagram

The scatter function remains the internal digital oscillator frequency and high PWM resolution, but increases the refresh rate of the LED. For example, if the PWM resolution is configured to 16 bits, and the oscillator frequency is configured to the maximum 32MHz, the output PWM frequency without scatter function is:

$$f_{16bit\_32MHz} = 32 \times 10^6/2^{16} = 488Hz$$

The output PWM frequency with scatter method increases to:

$$f_{16bit\_32MHz\_scatter} = 32 \times 10^6/2^{16} \times 2^8 = 125kHz$$

In applications, low switching frequencies such as 488Hz give rise to electromagnetic emitting and audible noise leakage to the external environment. They also induce noticeable LED flicker in displays and degrade RGB color rendering performance. To balance high PWM resolution and refresh frequency, the scatter function can be implemented. The corresponding output spectral plot presented in Figure 7 fully demonstrates the advantages of this function. The PWM frequency is elevated from 488Hz to 125kHz, with the spectral energy in the low-frequency range significantly attenuated.

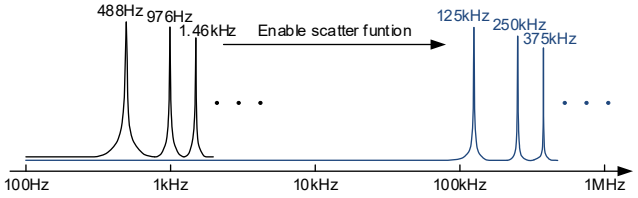


Figure 7. Output Frequency Spectrum

DETAILED DESCRIPTION (continued)

Output PWM Phase Delay Method

The PWM phase control is decided by REG0x5A register PHASE_DELAY_EN bit. The output is divided into three groups, OUT1 to OUT6, OUT7 to OUT12, and OUT13 to OUT18. Each group has its own phase and these phases are shifted in sequence, so that the total current sink powering on the V_{LED} line can be averaged to each phase (see Figure 8). However, this method cannot ease the current sink in one phase.

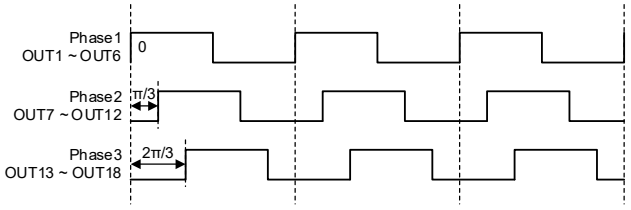


Figure 8. Phase Shift Scheme

Output PWM Inverting Method

The PWM inverting control is decided by REG0x5A[2:0] bits. The enable function also consists of three independent controls, followed by phase delay groups. By using PWM inverting method, the current ripple in one group can be reduced since each rising edge of the odd number PWM and the falling edge of the even number PWM are triggered simultaneously. (see Figure 9).

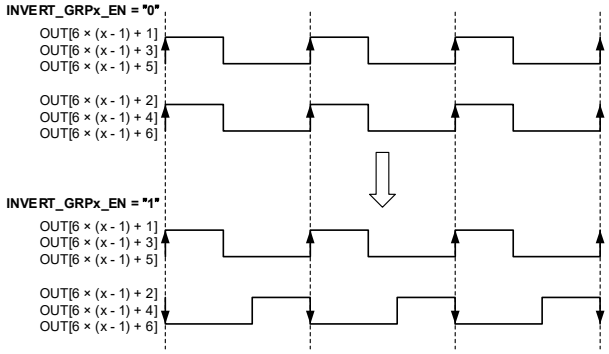


Figure 9. Phase Invert Scheme

Output PWM Spread Spectrum Function

PWM is a troublesome for some application which takes EMI into consideration. This chip has spread spectrum function to optimize the EMI performance. If SPREAD_EN bit (REG0x5B[4]) is set to “1”, spead spectrum function is enabled. By setting SPREAD_RANGE[1:0] bits (REG0x5B[3:2]), four spread spectrum range of 4%/8%/16%/32% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band which degrades the peak energy of EMI significantly. This function works on settings only when PWM frequency is larger than 7.8kHz.

I²C Serial Interface and Data Communication

Standard I^2C interface is used to program SGM31180 parameters and get status reports. I^2C is well known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM31180 supports write and read operations, and it has four I^2C address options that depend on the connection of AD1 and AD0 pins. See Table 2 for more detailed information.

Table 2. 7-Bit Slave Address

AD1	AD0	A[6:2]	A[1:0]	HEX	DEC
0	0	01000	00	20H	32D
0	1		01	21H	33D
1	0		10	22H	34D
1	1		11	23H	35D
Broadcast		0011100		1CH	28D

It has fifty two 8-bit registers, numbered from REG0x00 to REG0x5D.

DETAILED DESCRIPTION (continued)

Physical Layer

The standard I²C interface of SGM31180 supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s and the fast mode plus is up to 1Mbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 10. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

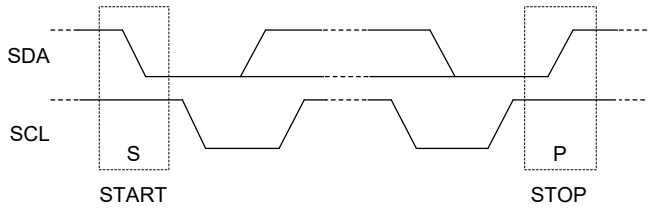


Figure 10. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 11.

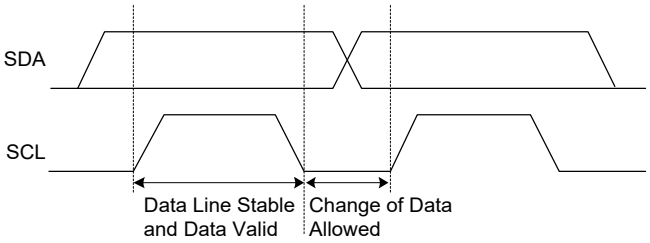


Figure 11. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 12 shows the byte transfer process with I²C interface.

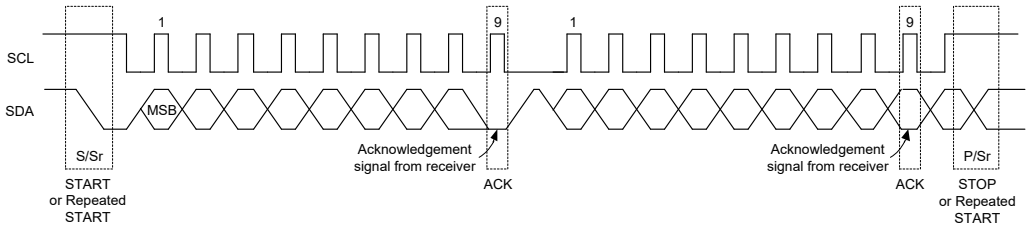


Figure 12. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 13.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 14 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 15), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

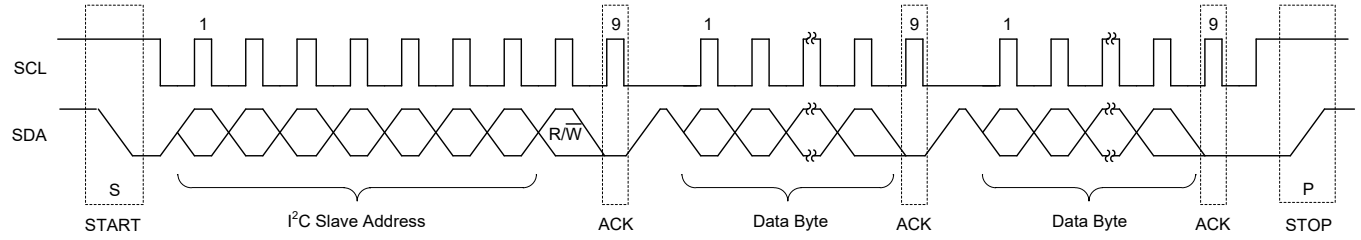


Figure 13. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

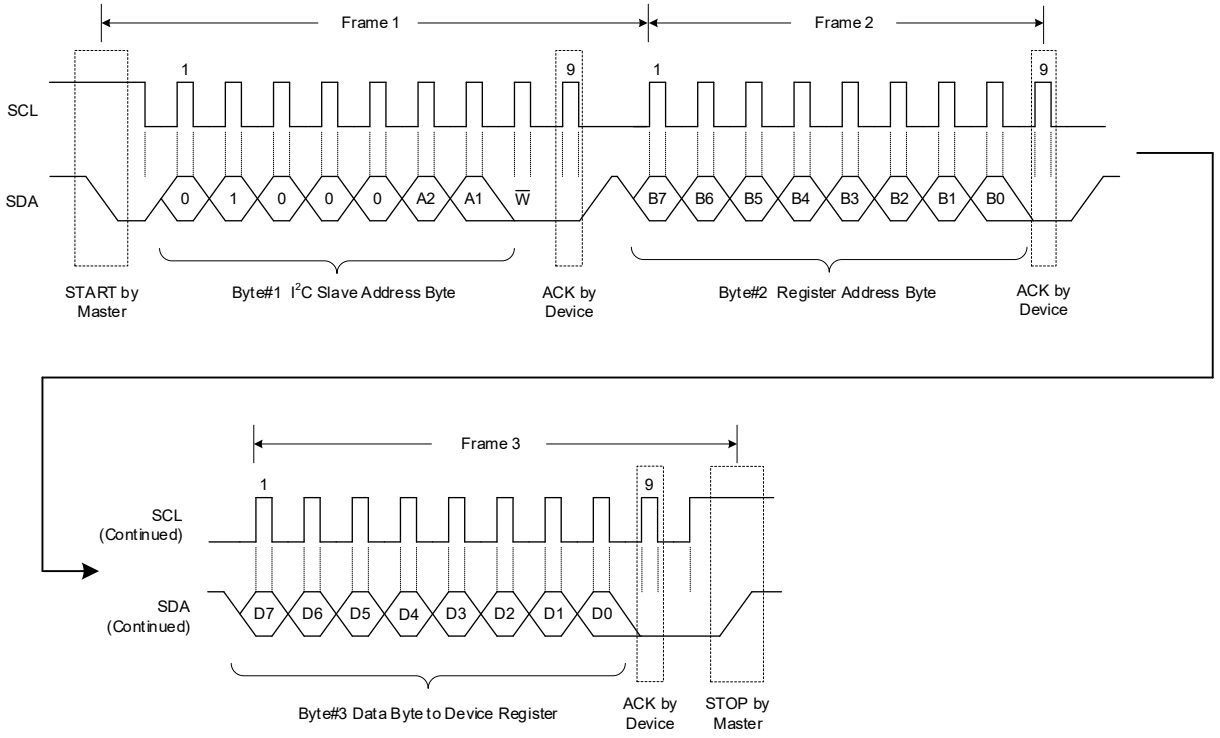


Figure 14. A Single Write Transaction

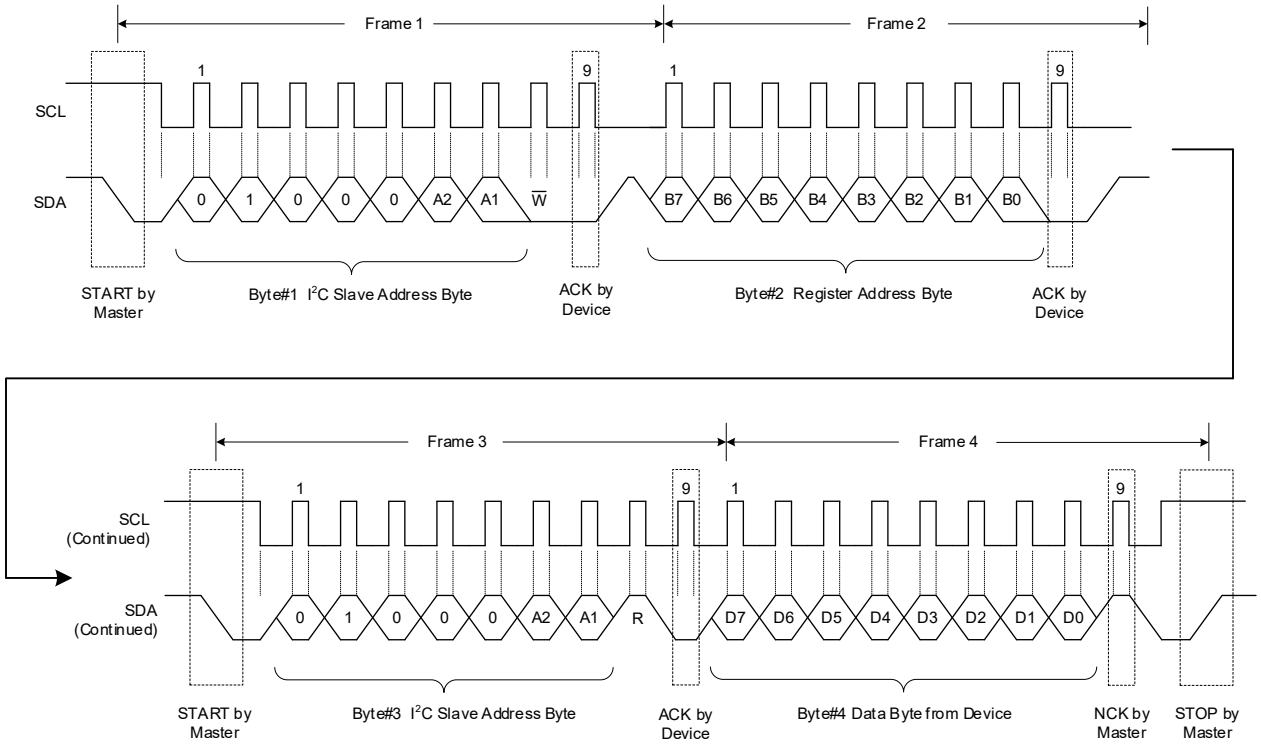


Figure 15. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-write is supported by SGM31180 for REG0x00 through REG0x5D registers, as explained in Figure 16 and Figure 17. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

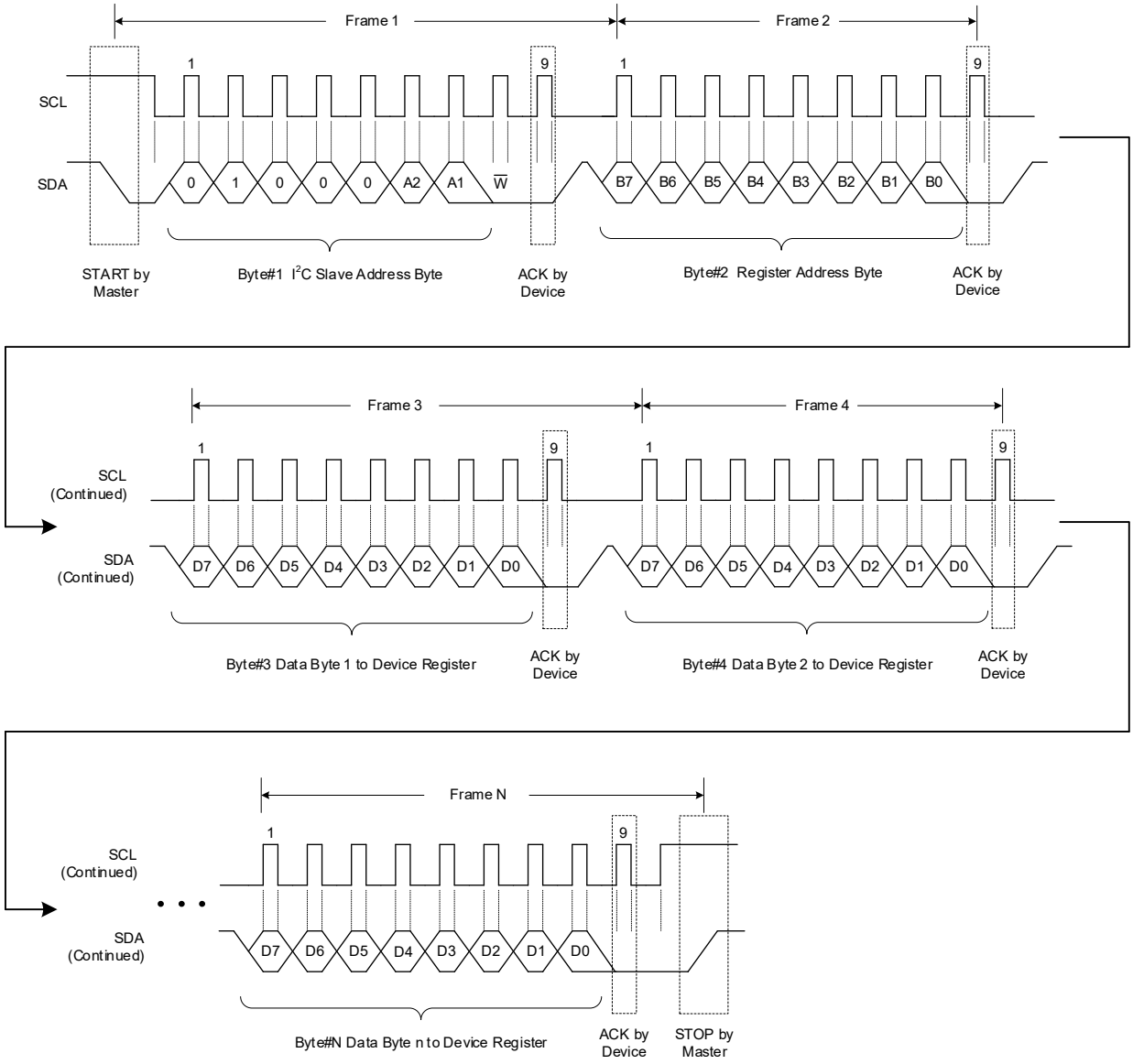


Figure 16. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

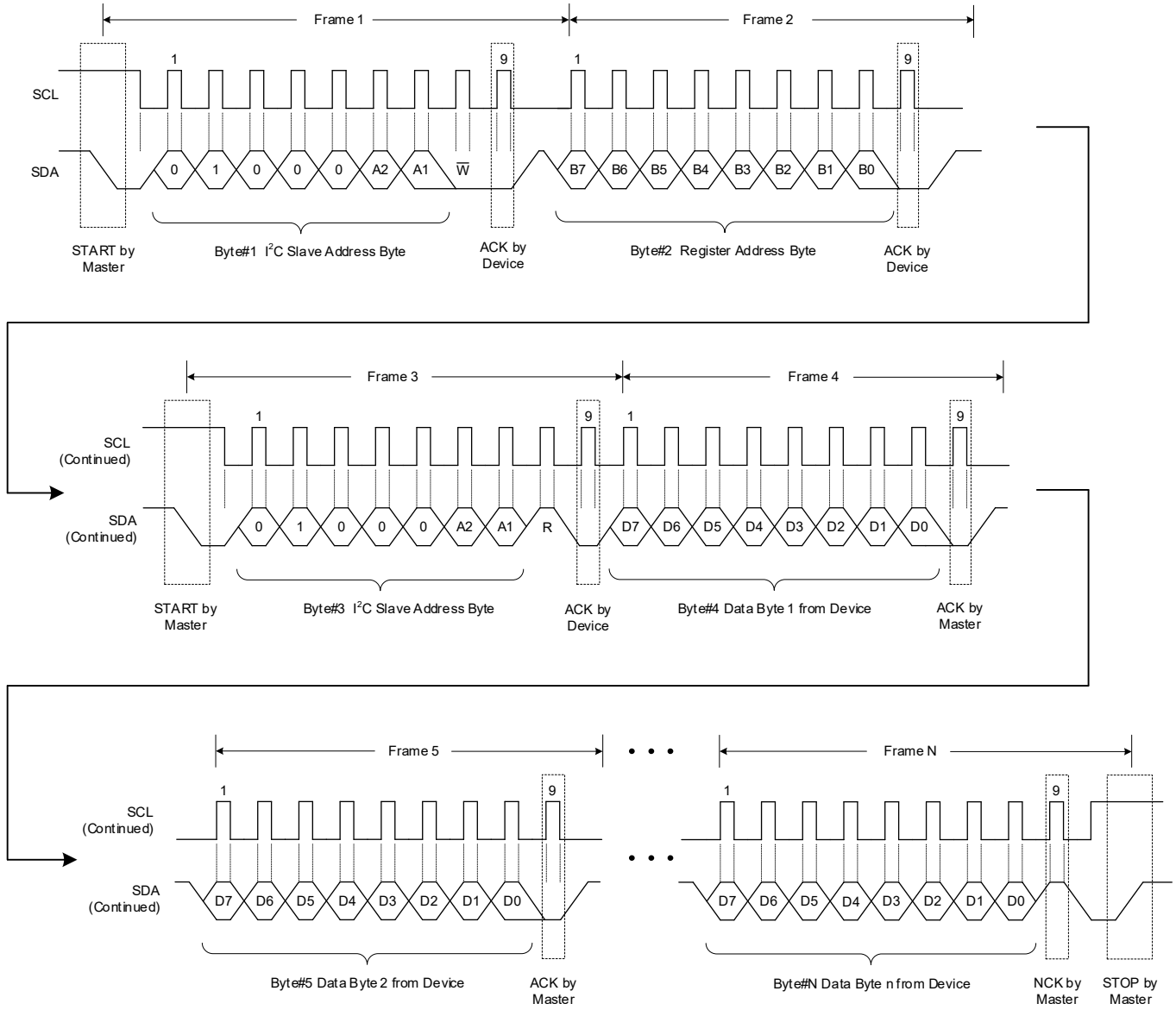


Figure 17. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB). The device I^{2}C address depends on the connection of AD0 and AD1 pins, as described in I^{2}C Serial Interface and Data Communication section.

I^{2}C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
DEVICE_ID		–	–	0x5C[7:0]	–	–
Soft Reset	–	–	–	–	0x5D[7:0]	–
CHIP Enable	–	–	–	–	0x00[0]	–
ECO Mode Enable	–	–	–	–	0x00[7]	–
PWM Resolution Setting	–	–	–	0x00[2:1]	–	–
Oscillator Frequency Setting	–	–	–	0x00[6:4]	–	–
Output Current Limit Setting	–	–	–	0x00[3]	–	–
Output Phase Shift	–	–	–	–	0x5A[7]	–
Output Inverting	–	–	–	–	0x5A[2:0]	–
Output Scatter	–	–	–	–	0x5B[7]	–
Output Frequency Spread in Spectrum	–	–	–	0x5B[3:2] & 0x5B[1:0]	0x5B[4]	–
PWM_x Output Setting (x = 1 to 18)	–	–	–	LSB: 0x01[7:0], MSB: 0x02[7:0] to LSB: 0x23[7:0], MSB: 0x24[7:0]	–	–
PWM Update	–	–	–	–	0x49[7:0]	–
LED Module_y Current Setting (y = 1 to 6)	–	–	–	0x4A[7:0] to 0x4F[7:0]	–	–
Color1 Current Setting	–	–	–	0x56[7:0]	–	–
Color2 Current Setting	–	–	–	0x57[7:0]	–	–
Color3 Current Setting	–	–	–	0x58[7:0]	–	–
Global Current Setting	–	–	–	0x59[7:0]	–	–

REGISTER MAPS (continued)

Bit Types:
R: Read only
R/W: Read/Write
WCLR: Write clears the bit

REG0x00: Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ECO_MODE	0	R/W	ECO Mode 0 = Disable ECO mode. The chip will always work in standby mode, even if no LED outputs. (default) 1 = Enable ECO mode. Then the chip enters ECO mode when all output PWM registers set to zero after 32ms.	SOFT_RESET
D[6:4]	OSC_FRQ[2:0]	000	R/W	Oscillator Frequency (f_{OSC}) Setting 000 = 32MHz (default) 001 = 16MHz 010/011 = 8MHz 100 = 125kHz 101 = 62.5kHz 110/111 = 31.25kHz	SOFT_RESET
D[3]	ILIM	0	R/W	Current Limit 0 = 60mA per channel (default) 1 = 90mA per channel	SOFT_RESET
D[2:1]	PWM_RES[1:0]	00	R/W	PWM Resolution 00 = 8-bit (default) 01 = 10-bit 10 = 12-bit 11 = 16-bit	SOFT_RESET
D[0]	CHIP_EN	0	R/W	Chip Enable 0 = Disable chip (default) 1 = Enable chip	SOFT_RESET

REG0x01 to REG0x24: Output1 ~ 18 PWM Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PWMx_LSB[7:0]	00000000	R/W	PWM LSB Value of OUT1-18 placed at REG0x01, REG0x03, REG0x05, ..., REG0x23.	SOFT_RESET
D[7:0]	PWMx_MSB[15:8]	00000000	R/W	PWM MSB Value of OUT1-18 placed at REG0x02, REG0x04, REG0x06, ..., REG0x24.	SOFT_RESET

NOTE: x = 1 to 18.

REG0x49: PWM Update Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PWM_UPDATE[7:0]	00000000	WCLR	Write 00H to this register to update REG0x01-REG0x24 PWM data to output.	SOFT_RESET

REGISTER MAPS (continued)

REG0x4A ~ REG0x4F: LED Module1 ~ 6 Current Ratio Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	I_LEDy[7:0]	00000000	R/W	DC Current Ratio Setting on Each RGB LED Modules. It will control the current of OUT1, OUT2 and OUT3 for y = 1; OUT4, OUT5 and OUT6 for y = 2; OUT7, OUT8 and OUT9 for y = 3; OUT10, OUT11 and OUT12 for y = 4; OUT13, OUT14 and OUT15 for y = 5; OUT16, OUT17 and OUT18 for y = 6.	SOFT_RESET

NOTE: y = 1 to 6.

REG0x56: Color1 DC Current Ratio Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	I_COL1[7:0]	00000000	R/W	DC Current Ratio Setting on One Single Color1. It will control the current of the OUT1, OUT4, OUT7, OUT10, OUT13, and OUT16 channels.	SOFT_RESET

REG0x57: Color2 DC Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	I_COL2[7:0]	00000000	R/W	DC Current Ratio Setting on One Single Color2. It will control the current of the OUT2, OUT5, OUT8, OUT11, OUT14, and OUT17 channels.	SOFT_RESET

REG0x58: Color3 DC Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	I_COL3[7:0]	00000000	R/W	DC Current Ratio Setting on One Single Color3. It will control the current of the OUT3, OUT6, OUT9, OUT12, OUT15, and OUT18 channels.	SOFT_RESET

REG0x59: Global Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	I_GLB[7:0]	00000000	R/W	DC Current Ratio Setting on All Channels	SOFT_RESET

REGISTER MAPS (continued)

REG0x5A: Inverting Group Enable Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PHASE_DELAY_EN	0	R/W	Phase Delay Function Enable 0 = Disable the phase delay function (default) 1 = Enable the phase delay function The phases of output channel groups from OUT1-6, OUT7-12, and OUT13-18 are shifted in sequence.	SOFT_RESET
D[6:3]	Reserved	0000	R	Reserved	N/A
D[2]	INVERT_GRP3_EN	0	R/W	Invert Group3 Function Enable 0 = Disable the Inverting function (default) 1 = Enable the Inverting function of OUT13 to OUT18	SOFT_RESET
D[1]	INVERT_GRP2_EN	0	R/W	Invert Group2 Function Enable 0 = Disable the Inverting function (default) 1 = Enable the Inverting function of OUT7 to OUT12	SOFT_RESET
D[0]	INVERT_GRP1_EN	0	R/W	Invert Group1 Function Enable 0 = Disable the Inverting function (default) 1 = Enable the Inverting function of OUT1 to OUT6	SOFT_RESET

REG0x5B: Spread Spectrum Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SCATTER_EN	0	R/W	PWM Scatter Function Enable 0 = Disable PWM Scatter Function (default) 1 = Enable PWM Scatter Function	SOFT_RESET
D[6:5]	Reserved	00	R	Reserved	N/A
D[4]	SPREAD_EN	0	R/W	Spread Spectrum Enable 0 = Disable (default) 1 = Enable	SOFT_RESET
D[3:2]	SPREAD_RANGE[1:0]	00	R/W	Spread Range Setting 00 = ±4% (default) 01 = ±8% 10 = ±16% 11 = ±32%	SOFT_RESET
D[1:0]	SPREAD_CYCLE[1:0]	00	R/W	Spread Cycle Setting 00 = 2048μs (default) 01 = 1024μs 10 = 512μs 11 = 256μs	SOFT_RESET

REG0x5C: DEVICE_ID Register [Reset = 0x33]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DEVICE_ID[7:0]	00110011	R	Device ID 00110011 = SGM31180	N/A

REG0x5D: Reset Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	SOFT_RESET[7:0]	00000000	WCLR	Write 00H to reset all register.	SOFT_RESET

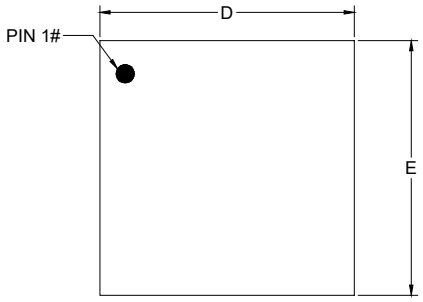
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

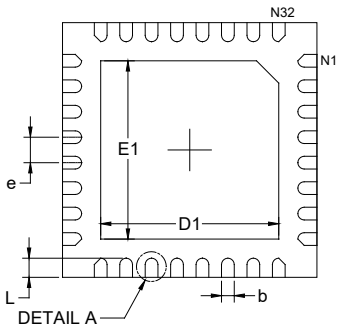
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

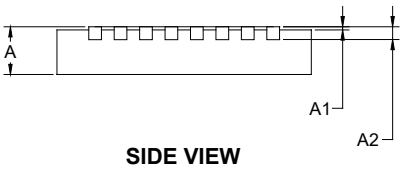
TQFN-4×4-32AL



TOP VIEW



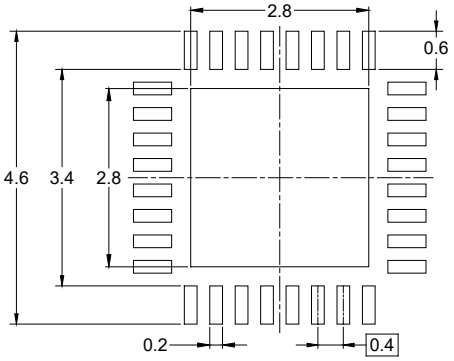
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



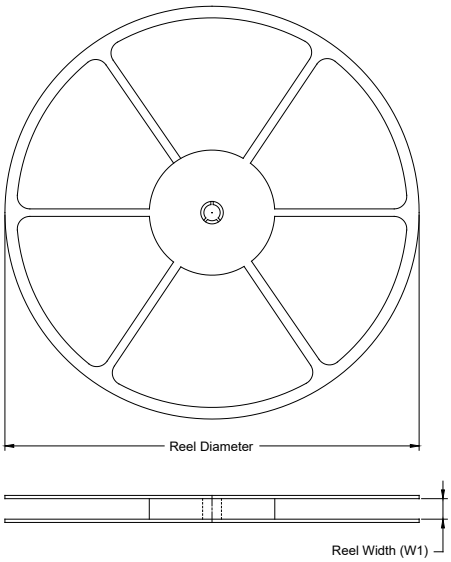
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
D	3.900	4.000	4.100
E	3.900	4.000	4.100
D1	2.700	2.800	2.900
E1	2.700	2.800	2.900
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.250	0.300	0.350

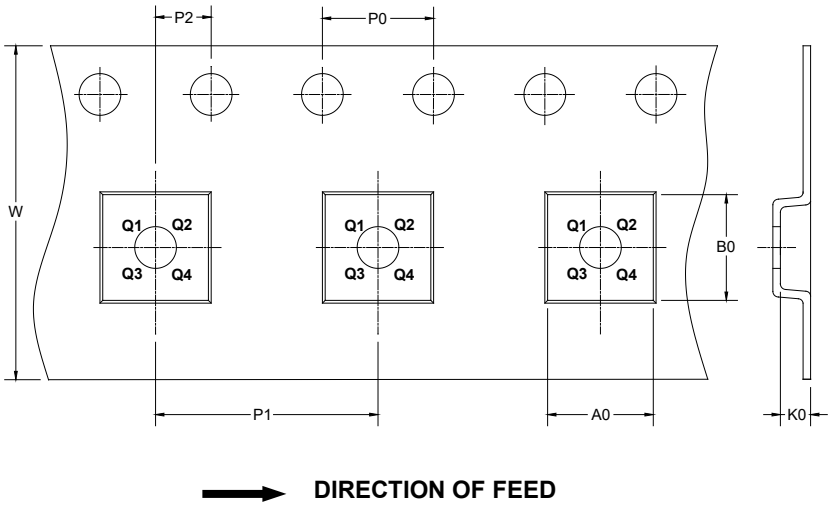
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



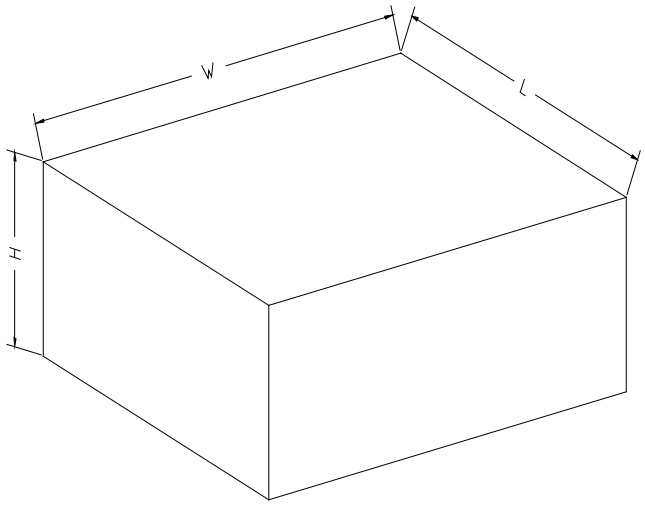
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-32AL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002