SGM257301Q
Reverse Polarity Protection Controller

GENERAL DESCRIPTION

The SGM257301Q is a reverse polarity protection controller with an external NMOS and offers low-loss reverse polarity protection. Its 3.2V to 65V wide supply input range facilitates control over various DC bus voltages commonly found in automotive battery systems like 12V, 24V, and 48V. The device supports input voltage down to 3.2V, making it well-suited for automotive systems with stringent cold crank conditions. It also protects connected loads against reverse supply voltages as low as -65V.

This controller incorporates a charge pump gate driver for an external NMOS. Its high voltage rating simplifies system designs for automotive EMC transient interference standard ISO7637. When the enable pin is held low, the controller remains disabled and consumes only about 1.1μA of supply current.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM257301Q is available in a Green TSOT-23-8 package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Functional Safety-Capable**
- **Documentation Available for Assisting in Functional Safety System Design**
- **Input Voltage: 3.2V to 65V (3.9V Start-Up)**
- **-65V Reverse Voltage Rating**
- **Charge Pump for External NMOS**
- **Enable Pin (EN)**
- **Supply Shutdown Current: 1.1μA (TYP)**
- **Supply Quiescent Current: 107μA (TYP)**
- **Compliance with Automotive ISO7637 Transient Requirements with Appropriate TVS Diode**
- **Available in a Green TSOT-23-8 Package**

APPLICATIONS

Automotive Infotainment Systems: Digital Cluster and Head Unit
Automotive ADAS Systems: Camera Integration
Enterprise Power Supplies
Industrial Factory Automation: PLC Integration

SIMPLIFIED SCHEMATIC

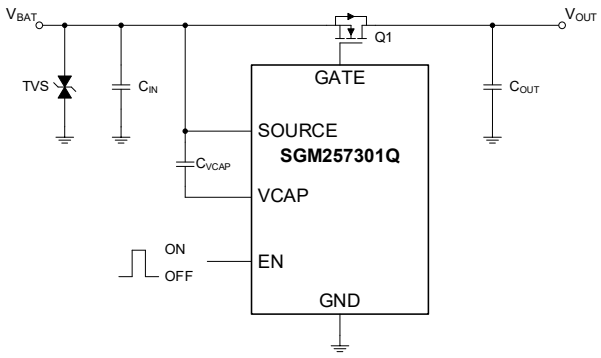


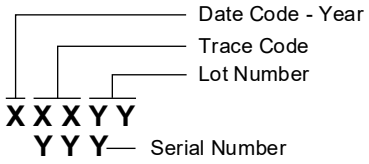
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM257301Q	TSOT-23-8	-40℃ to +125℃	SGM257301QTN8G/TR	XXXYY 2XV	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code. YY = Lot Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Pins
- SOURCE to GND ..... -65V to 65V
- EN to GND, (V_{SOURCE} > 0V) ..... -0.3V to 65V
- EN to GND, (V_{SOURCE} ≤ 0V) ..... V_{SOURCE} to 65V + V_{SOURCE}

Output Pins
- GATE to SOURCE ..... -0.3V to 15V
- VCAP to SOURCE ..... -0.3V to 15V

Package Thermal Resistance
- TSOT-23-8, θ_{JA} ..... 125.3℃/W
- TSOT-23-8, θ_{JB} ..... 50.6℃/W
- TSOT-23-8, θ_{JC} ..... 81.3℃/W

Package Thermal Characterization Parameter
- TSOT-23-8, ψ_{JT} ..... 6.1℃/W
- TSOT-23-8, ψ_{JB} ..... 49.7℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM (Connect EN Pin to SOURCE Pin) ..... ±2000V
HBM (All Pins except EN) (3) ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

3. The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. 2kV rating for all pins except EN which is rated for 1.5kV.

RECOMMENDED OPERATING CONDITIONS

Input Pins
- SOURCE to GND ..... -60V to 60V
- EN to GND ..... -60V to 60V

External Capacitance
- SOURCE ..... ≥ 22nF
- VCAP to SOURCE ..... ≥ 0.1μF

External MOSFET Max V_{GS} Rating
- GATE to SOURCE ..... ≥ 15V

Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

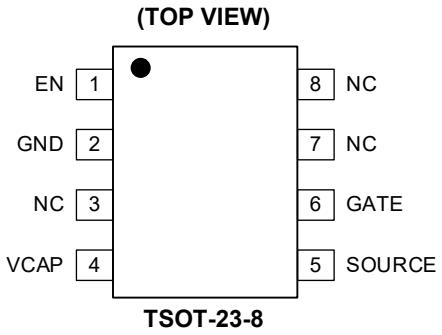
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	EN	I	Enable. This pin is connected to SOURCE during always on operation.
2	GND	G	Ground.
3, 7, 8	NC	—	No Connection.
4	VCAP	O	Charge Pump Output. This pin is connected to external charge pump capacitor.
5	SOURCE	I	Controller Input Supply Pin. Route to the source of the external N-channel MOSFET.
6	GATE	O	Gate Drive Output. This pin is connected to the gate of the external MOSFET.

NOTE: 1. I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, all typical values are measured at T_A = +25℃, V_{SOURCE} = 12V, C_{VCAP} = 0.1μF and V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SOURCE} Supply Voltage						
Operating Input Voltage	V_{SOURCE}		4		60	V
V_{SOURCE} POR	V_{SOURCE_POR}	Rising threshold			3.9	V
		Falling threshold	2.46	2.78	3.08	V
V_{SOURCE} POR Hysteresis	$V_{SOURCE\_POR\_HYS}$		0.73		1.03	V
Supply Shutdown Current	I_{SD}	V_{EN} = 0V		1.1	3	μA
Supply Quiescent Current	I_Q			107	150	μA
Enable Input (EN)						
Enable Input Low Threshold	V_{EN_IL}		0.9	1.26	1.52	V
Enable Input High Threshold	V_{EN_IH}		1.79	2.10	2.45	V
Enable Hysteresis	V_{EN_HYS}		0.53	0.85	1.15	V
Enable Sink Current	I_{EN}	V_{EN} = 12V		1.7	4	μA
Gate Drive (GATE)						
Peak Source Current	I_{GATE}	V_{GATE} - V_{SOURCE} = 5V	6	10.1		mA
Peak Sink Current		EN from high to low, V_{GATE} - V_{SOURCE} = 5V		1670		mA
Discharge Switch R_{DSON}	R_{DSON}	EN from high to low, V_{GATE} - V_{SOURCE} = 100mV	0.3		2.3	Ω
Charge Pump						
Charge Pump Source Current	I_{VCAP}	Charge pump on, V_{CAP} - V_{SOURCE} = 7V	200	300	400	μA
Charge Pump Sink Current		Charge pump off, V_{CAP} - V_{SOURCE} = 13V		7	13	μA
Charge Pump Voltage at V_{SOURCE} = 3.2V	V_{CAP} - V_{SOURCE}	I_{VCAP} ≤ 10μA	7.5			V
Charge Pump Turn-On Voltage			9.1	10.5	12	V
Charge Pump Turn-Off Voltage			10	11.6	13	V
Charge Pump Enable Comparator Hysteresis			0.6	1.03	1.4	V
V_{CAP} - V_{SOURCE} UV Release	V_{CAP_UVLO}	Rising edge	5.4	6.3	7.2	V
V_{CAP} - V_{SOURCE} UV Threshold		Falling edge	4.5	5.4	6.2	V

NOTE:

1. Parameter assured by design and characterization.

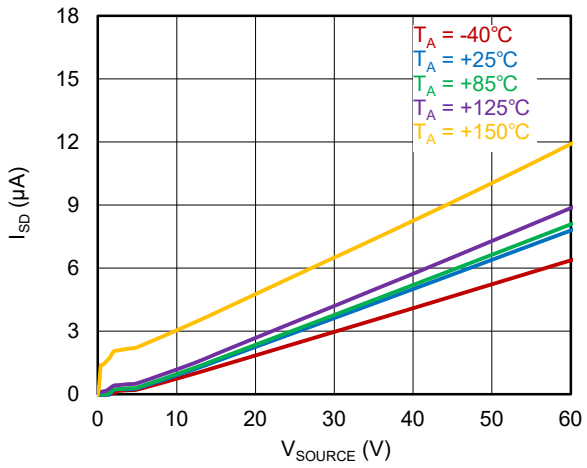
SWITCHING CHARACTERISTICS

(T_A = -40℃ to +125℃, all typical values are measured at T_A = +25℃, V_{SOURCE} = 12V, C_{VCAP} = 0.1μF and V_{EN} = 3.3V, unless otherwise noted.)

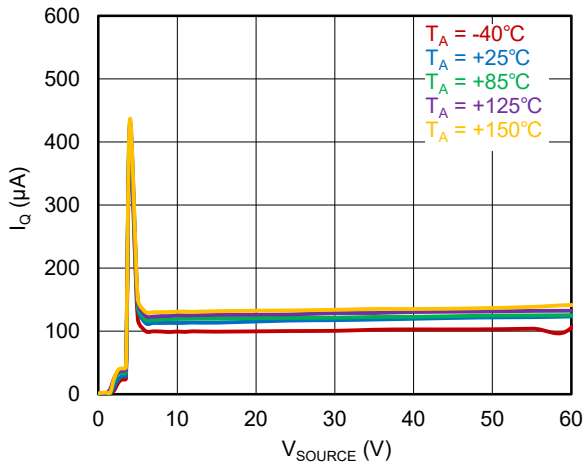
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable (Low to High) to Gate Turn-On Delay	t_{EN_TDLY}	V_{CAP} > $V_{CAP\_UVLO\_R}$		90	135	μs

TYPICAL PERFORMANCE CHARACTERISTICS

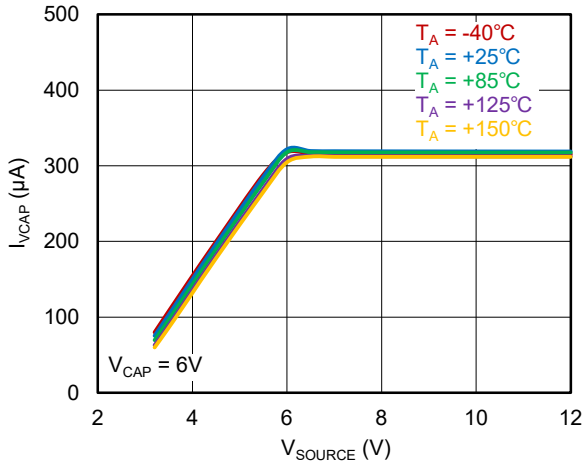
I_{SD} vs. V_{SOURCE}



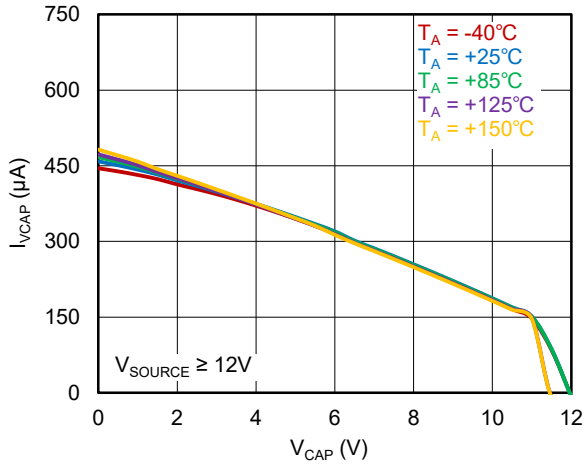
I_Q vs. V_{SOURCE}



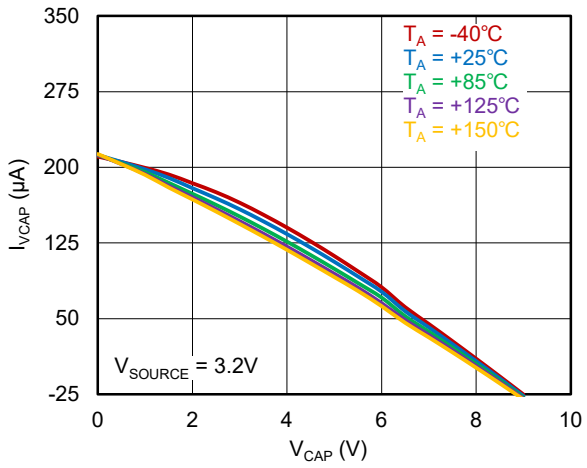
I_{VCAP} vs. V_{SOURCE}



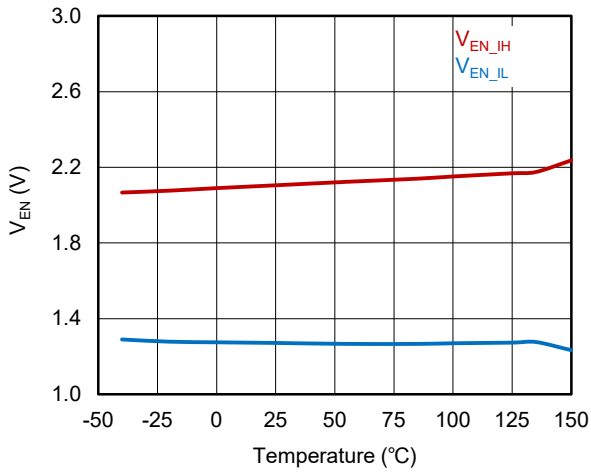
I_{VCAP} vs. V_{CAP}



I_{VCAP} vs. V_{CAP}

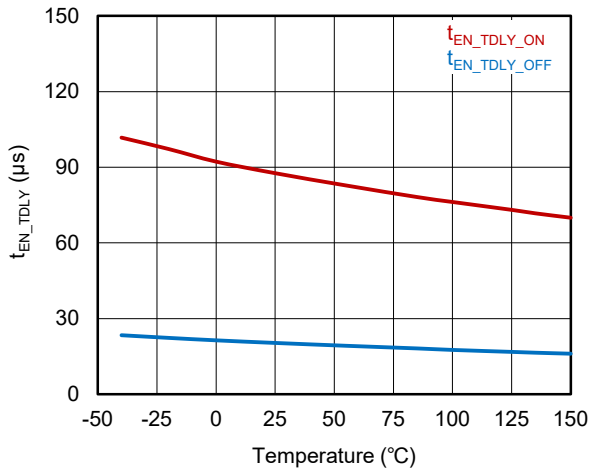


V_{EN} vs. Temperature

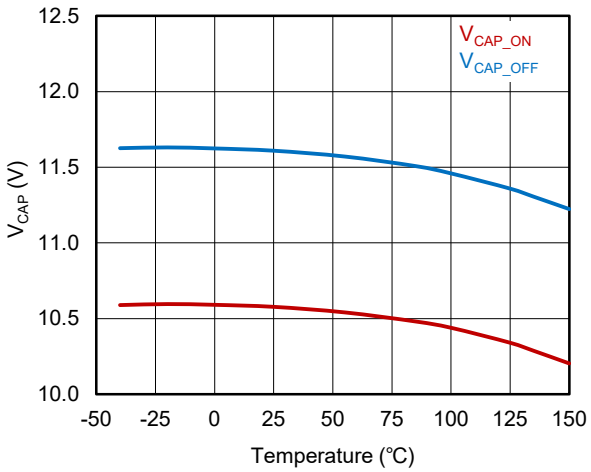


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

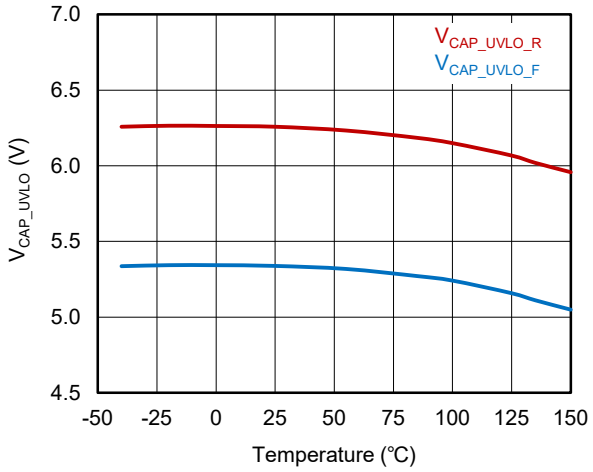
t_{EN_TDLY} vs. Temperature



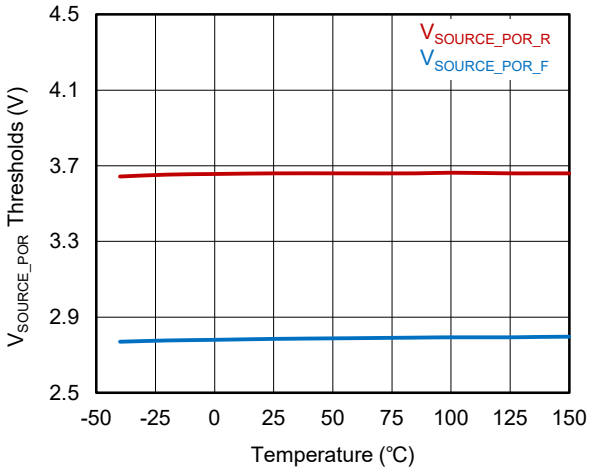
V_{CAP} vs. Temperature



V_{CAP_UVLO} vs. Temperature

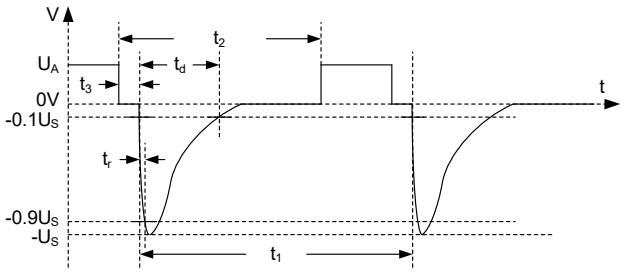


V_{SOURCE_POR} Thresholds vs. Temperature

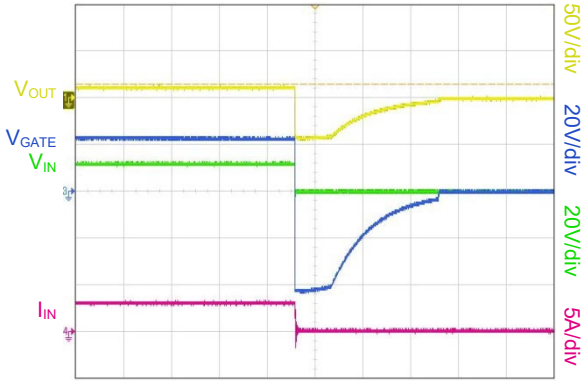


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

ISO 7637-2 Pulse 1

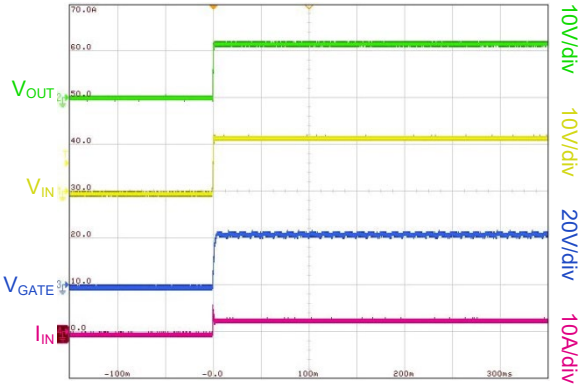


Response to ISO 7637-2 Pulse 1



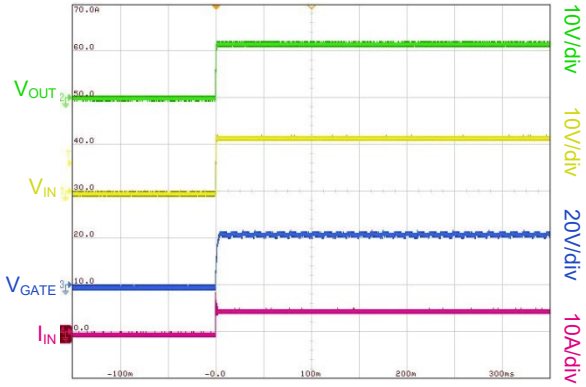
Time (1ms/div)

Startup with 3A Load



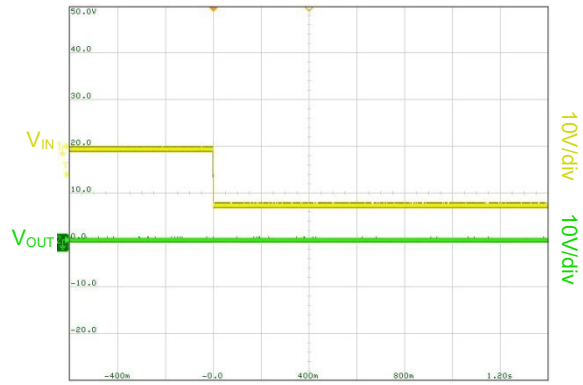
Time (50ms/div)

Startup with 5A Load



Time (50ms/div)

Startup with Input Reverse Voltage (-12V)



Time (200ms/div)

FUNCTIONAL BLOCK DIAGRAM

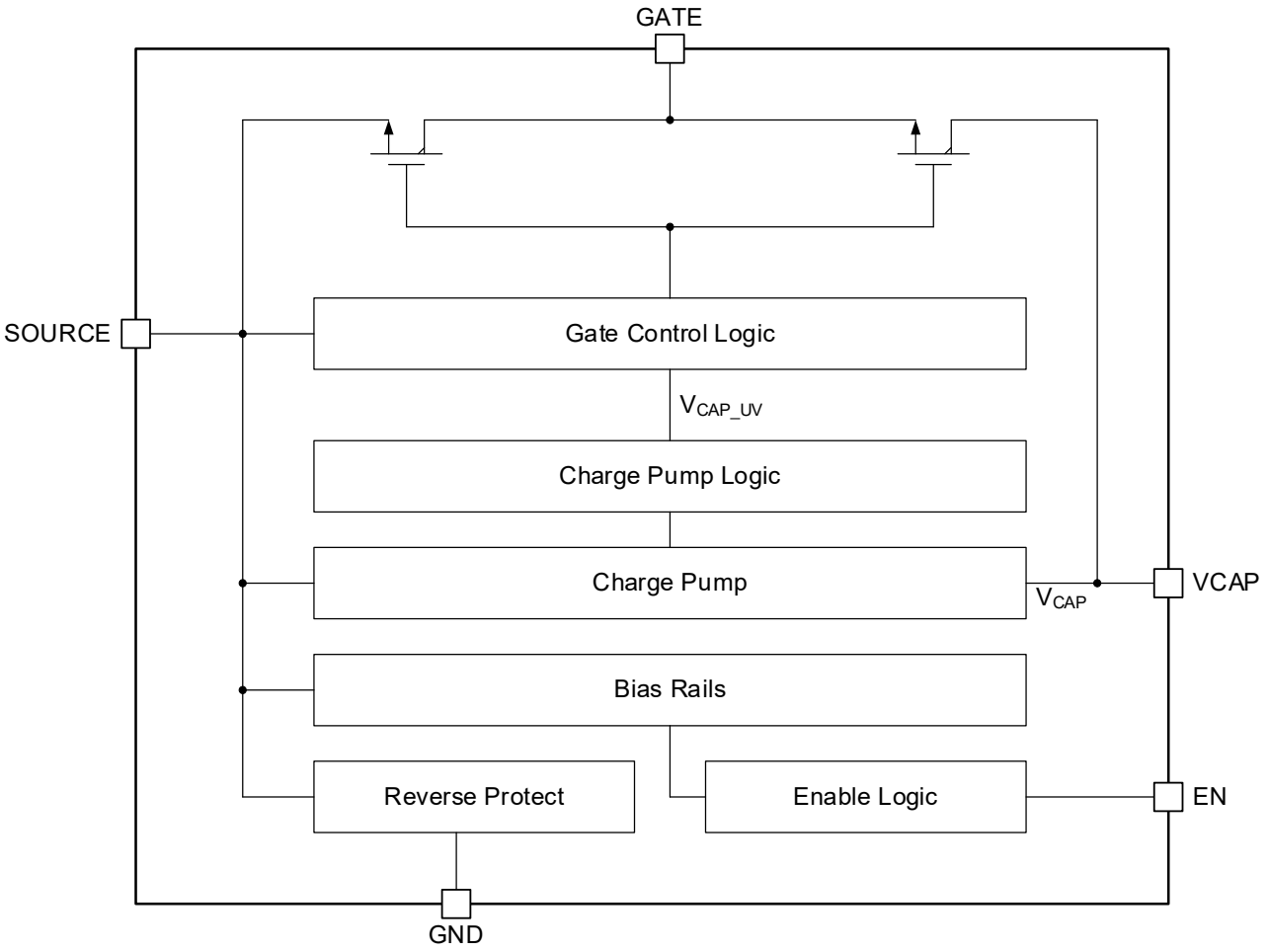


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM257301Q integrates all necessary features to enable a fast, efficient reverse polarity protection solution. Designed for simplicity, it controls an external N-channel MOSFET, which serves as a high-efficiency replacement for traditional P-channel MOSFET-based schemes. An internal charge pump boosts the gate drive to approximately 15V, ensuring full enhancement of the N-channel MOSFET. The device also includes an enable pin (EN) that, when asserted, forces the controller into shutdown, disabling the MOSFET and minimizing quiescent current consumption.

Input Voltage

The SOURCE pin supplies power to the internal circuitry of the SGM257301Q. Generally, it consumes 107μA when it is enabled and 1.1μA when disabled. When the voltage of the SOURCE pin exceeds the POR rising threshold, the SGM257301Q will operate either in shutdown mode or conduction mode, depending on the voltage of the EN pin. The designed voltage range from the SOURCE to GND is from 65V to -65V. This enables the SGM257301Q to endure negative voltage transients.

Charge Pump

The external NMOS is driven by the voltage produced by the charge pump. An external charge-pump capacitor is positioned between the VCAP and SOURCE pins. This capacitor supplies the energy required to activate the external MOSFET. The charge pump will only supply power to the external capacitor when the voltage on the EN pin exceeds the specified input high-level threshold V_{EN_IH}. Once enabled, it typically provides a charging current of 300μA. When the EN pin is set to a low level, the charge pump remains inoperative. In order to guarantee the external MOSFET can be driven to a voltage higher than its specified threshold, the voltage between VCAP pin and SOURCE pin must exceed the under-voltage lockout threshold, which is typically 6.3V. This condition must be met before enabling the internal gate driver. Calculate the initial gate driver enable delay using Equation 1. Here, C_{VCAP} represents the charge-pump capacitance connected between the SOURCE pin and VCAP pin, and $V_{CAP\_UVLO\_R}$ = 6.3V (TYP).

$$t_{DRV\_EN} = 90\mu s + C_{VCAP} \times \frac{V_{CAP\_UVLO\_R}}{300\mu A} \quad (1)$$

To eliminate gate drive chatter, approximately 900mV of hysteresis is applied to the VCAP under-voltage lockout threshold. The charge pump continues operating until the VCAP-to-SOURCE voltage rises to 11.6V (TYP). Once this voltage level is reached, the charge pump is switched off. This action results in a reduction of the current consumption on the SOURCE pin. The charge pump remains in the disabled state until the voltage from VCAP to SOURCE drops below 10.5V typically. Once this voltage condition is met, the charge pump is activated. As illustrated in Figure 3, the voltage between VCAP and SOURCE cycles through charging and discharging processes within the range of 10.5V to 11.6V. This on-off operation of the charge pump serves to reduce the quiescent operating current of the SGM257301Q. When disabled, the charge pump typically sinks a current of 7μA.

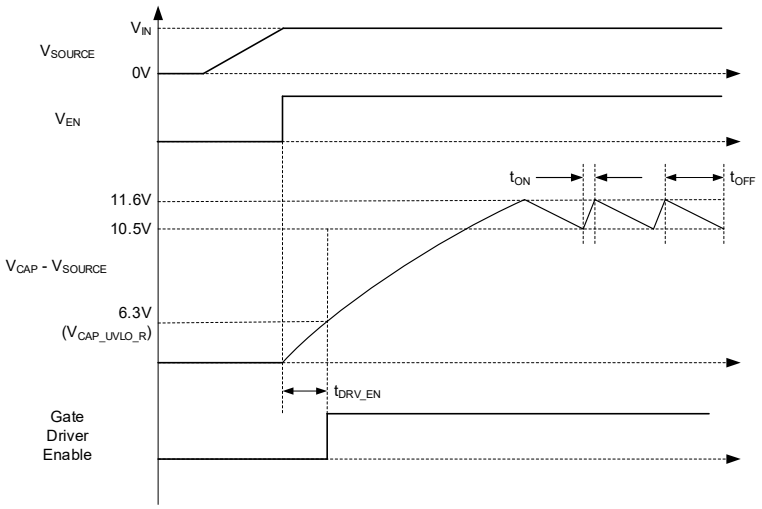


Figure 3. Charge Pump Operation

DETAILED DESCRIPTION (continued)

Gate Driver

The gate driver controls the external N-channel MOSFET by generating the required voltage between its gate and source terminals.

The gate driver will not enable unless all three of the following conditions are met:

- The voltage at the EN pin must exceed the enable input high threshold.
- The voltage between VCAP and SOURCE must remain above the under-voltage lockout (UVLO) threshold.
- The SOURCE voltage must stay above the V_{SOURCE} power-on-reset (POR) rising threshold.

If the required conditions are not met, an internal connection will be established between the GATE pin and the SOURCE pin. This ensures that the external MOSFET is turned off. Once the conditions are met, the gate controller will operate.

Enable

The SGM257301Q is equipped with an enable (EN) pin. An external signal uses this pin to enable or disable the gate driver. When $V_{EN} > V_{EN\_IH}$, the gate driver and charge pump function as outlined in the sections above. When $V_{EN} < V_{EN\_IL}$, the charge pump and gate driver are disabled, causing the SGM257301Q to enter a shutdown state. The EN pin has a specified voltage tolerance ranging from -65V to 65V. When the enable function is unnecessary, it can be directly connected to the SOURCE pin. When the EN pin floats, a 1.7μA internal sink current pulls it to a low level, thus disabling the device.

Shutdown Mode

When $V_{EN} < V_{EN\_IL}$, the charge pump and gate driver are disabled, causing the SGM257301Q to enter the shutdown mode. During the shutdown mode, the SGM257301Q operates in a low quiescent current (low-I_Q) state. Specifically, the SOURCE pin only consumes a current of 1.1μA. In shutdown mode, the SGM257301Q does not block forward current in the external MOSFET; instead, the current flows through the MOSFET's intrinsic body diode.

Conduction Mode

The SGM257301Q operates in conduction mode solely when the gate driver is active (refer to the Gate Driver section). In this state, the GATE pin is internally tied to VCAP, causing the external MOSFET's gate-to-source voltage to closely follow the voltage between VCAP and SOURCE. This connection minimizes the MOSFET's on-resistance RDSON, thereby reducing conduction losses-especially under high forward current conditions.

APPLICATION INFORMATION

Reverse Battery Protection for Automotive Body Control Module Applications

Reverse battery protection activates when the battery is connected with reversed polarity such as during jump-starts, vehicle maintenance, or servicing, as incorrect connections can damage ECU components that are not designed to withstand reverse voltage. N-channel MOSFET (N-FET) reverse polarity protection solutions are now widely preferred over traditional discrete approaches like Schottky diodes and P-channel FETs (P-FETs), owing to their lower conduction losses, improved thermal performance, and reduced PCB footprint. Depending on application requirements, reverse polarity protection schemes fall into two main categories:

- Applications needing integrated reverse polarity input protection and reverse-current prevention.
- Applications requiring input reverse polarity protection only, without reverse-current blocking.

Figure 4 illustrates the two primary categories of reverse polarity protection solutions. In applications where the output supplies DC/DC converters, voltage regulators, and downstream logic (e.g., MCUs or processors), input reverse polarity protection and reverse current blocking are both necessary. For such logic-path implementations, an ideal diode controller such as the SGM25733Q is well suited.

When it comes to load-driving scenarios in body control modules (BCM), ensuring input reverse polarity protection is imperative, although reverse-current blocking is not a requirement. For such use cases, a controller like the SGM257301Q offers an effective reverse polarity protection solution.

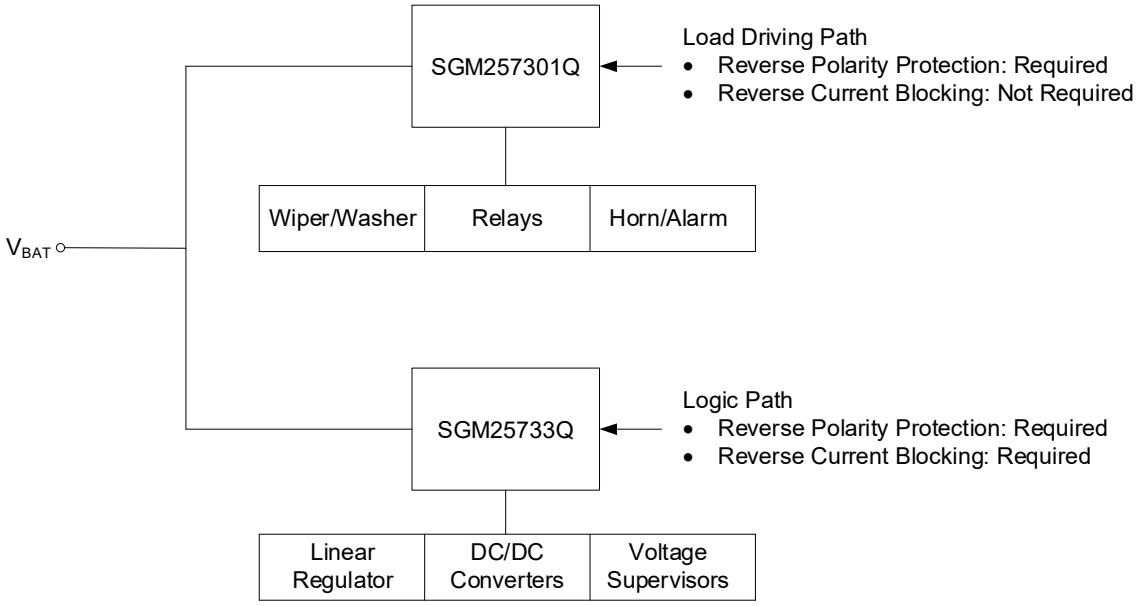


Figure 4. Representative Block Diagram of Reverse Battery Protection in the BCM Load-Driver Path

APPLICATION INFORMATION (continued)

In certain body control module (BCM) load-driving applications, such as wiper motors and door actuators, the output loads are inductive. For these use cases, the reverse polarity protection solution must safeguard against incorrect battery polarity without blocking reverse current flow from the load back to the supply.

Blocking such current can lead to destructive voltage overshoots during inductive load turn-off, caused by flyback energy or motor regenerative effects. Notably, in wiper motor systems, a rapid speed transition (e.g., from high to low) can induce significant voltage spikes due to back-EMF coupling.

The SGM257301Q is specifically designed for these scenarios, providing robust input reverse polarity protection while allowing reverse current conduction. A typical implementation for BCM load-driving paths is shown in Figure 5.

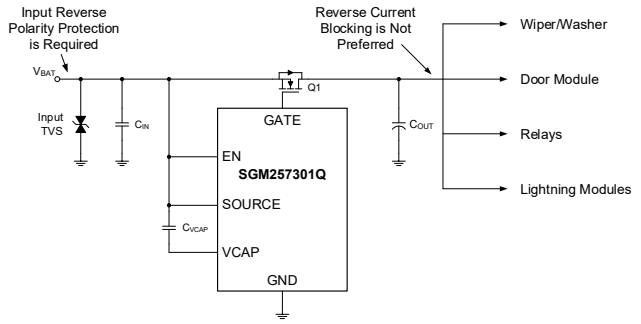


Figure 5. Standard Block Diagram for Reverse Battery Protection in Body Control Module Load Driving Circuits

Reverse Polarity Protection

P-channel MOSFET (P-FET)-based reverse polarity protection is widely used in industrial and automotive systems due to its simplicity and low insertion loss. However, an N-FET-based approach using the SGM257301Q with an external N-channel MOSFET offers a superior alternative delivering lower conduction loss, reduced solution size, and enhanced performance under cold-crank conditions.

As illustrated in Figure 6, at equivalent power levels, the SGM257301Q + (N-FET) solution occupies approximately one-third the PCB area of a comparable P-FET implementation.

The limitation of P-FET solutions stems from their gate-drive mechanism: the gate is typically pulled low relative to the source, resulting in a gate-to-source voltage (V_{GS}) that scales with input voltage. During severe cold-crank events, battery voltage drops below 4V the effective V_{GS} diminishes, causing the P-FET's on-resistance R_{DSON} to rise sharply. This leads to excessive voltage drop and, in some cases, unintended turn-off due to insufficient V_{GS} relative to the device's threshold voltage (V_{TH}), potentially triggering system resets.

In contrast, the SGM257301Q actively drives the external N-FET and maintains full enhancement down to an input voltage of 3.2V, ensuring stable operation even under extreme cold-crank conditions.

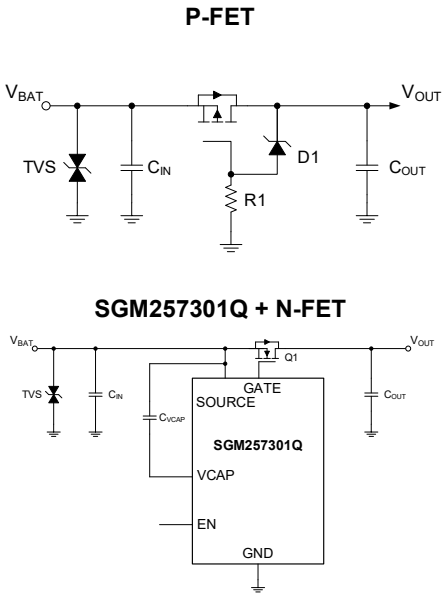


Figure 6. Typical Application Diagram

APPLICATION INFORMATION (continued)

The SGM257301Q is a reverse polarity protection controller that drives an external N-channel MOSFET in series with the battery; a typical 12V battery protection schematic is shown in Figure 7. Although a TVS diode is not required for the SGM257301Q to function, TVS devices may be employed to clamp positive and negative input voltage surges. An output capacitor (C_{OUT}) is recommended to mitigate output voltage droop resulting from line transients or abrupt load changes.

Typical Application

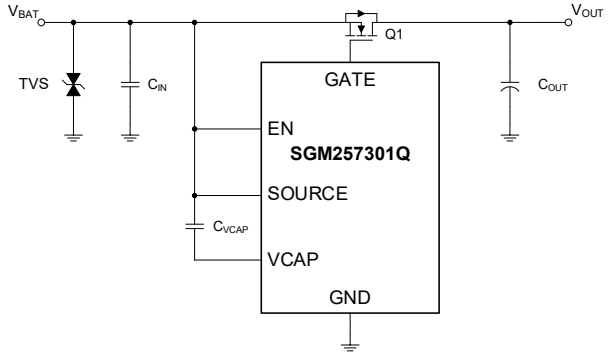


Figure 7. Typical Application Circuit

Design Requirements

A design example is illustrated, with key system parameters outlined in Table 1.

Table 1. Design Parameters

Design Parameter	Example Value
Input Voltage Range	12V battery, 12V TYP with 3.2V cold crank and 35V load dump.
Output Voltage	3.2V during cold crank to 35V load dump.
Output Current Range	3A TYP, 5A MAX.
Output Capacitance	220μF typical output capacitance.
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2.

Detailed Design Procedure

Design Considerations

- Input voltage range covering cold-crank and load-dump scenarios.
- Typical and peak load current requirements.

MOSFET Selection

Critical MOSFET electrical parameters encompass the highest continuous drain current (I_D) and the maximum voltage rating from drain to source V_{DS_MAX}, peak body diode forward current, and on-resistance R_{DSON}.

To ensure proper operation, the MOSFET's maximum allowable drain current (I_D) must be higher than the greatest expected continuous load current, and its V_{DS_MAX} rating should be capable of withstanding the maximum voltage differential in the system, including foreseeable fault conditions. For use with the SGM257301Q, MOSFETs with a V_{DS} rating up to 60V are recommended, as the device's SOURCE pin is rated for a maximum of 65V.

The SGM257301Q can drive a gate-source voltage V_{GS} up to 13V; therefore, it is recommended to use a MOSFET rated for at least 15V $V_{GS,}$ otherwise, a Zener diode should be added to restrict V_{GS} to a safe level.

At power-up, inrush current passes through the body diode to charge the output bulk hold-up capacitors; the body diode's maximum forward (source) current rating must exceed the peak inrush current anticipated in the application.

To reduce conduction losses in the MOSFET, a suitably low R_{DSON} is preferred.

Based on the design specifications, the suggested MOSFET ratings are:

- 60V V_{DS_MAX} and ±20V V_{GS_MAX}

The DMT6007LFG MOSFET from Diodes Incorporated is chosen to satisfy the 12V reverse-battery protection design criteria, featuring the following specifications:

- 60V V_{DS_MAX} and ±20V V_{GS_MAX}
- Typical R_{DSON} of 6.5mΩ and maximum of 8.5mΩ at V_{GS} = 4.5V, ensuring low conduction losses in the FET.

The MOSFET's thermal resistance should be assessed relative to its anticipated peak power dissipation to ensure effective control of the junction temperature (T_A).

Charge Pump VCAP, Input and Output Capacitance

The minimum required capacitance values for the charge pump are as follows:

- C_{VCAP}: A minimum of 0.1μF is required, with a recommended value of C_{VCAP} (μF) ≥ 10 × C_{ISS_MOSFET} (μF).
- A minimum of 0.1μF for input capacitance.
- C_{OUT}: Standard output capacitance of 220μF.

APPLICATION INFORMATION (continued)

TVS Diode and MOSFET Selection Guidelines for 12V Battery Protection Applications

In automotive electrical systems, transient voltage suppression devices play a critical role in safeguarding circuits. For the 12V battery protection application circuit presented in Figure 8, a bi-directional TVS diode is used. It defends against transient voltage spikes in both the positive and negative polarities that happen when the car is running normally. The levels and pulses of these transient voltages are defined by the ISO7637-2 and ISO16750-2 standards.

Two critical parameters of a TVS (Transient Voltage Suppressor) are its breakdown voltage and clamping voltage. The breakdown voltage is the specific voltage at which the TVS diode begins to conduct via an avalanche effect, effectively protecting the circuit from over-voltage conditions, similar to that of a Zener diode. It is specified under a low current condition, usually 1mA. The breakdown voltage must surpass the steady-state voltages encountered in the system under the worst case scenarios. The breakdown voltage of TVS+ is required to be greater than the 24V jump start voltage as well as the 35V suppressed load dump voltage, and it should be lower than the 65V maximum ratings of SGM257301Q. To safeguard against damage due to extended reverse-battery exposure, the breakdown voltage of TVS- should be lower than the maximum reverse battery voltage of -16V.

The clamping voltage refers to the stabilized potential a TVS maintains during high-energy surge events, significantly exceeding its nominal breakdown threshold. TVS diodes are designed to suppress transient pulses without affecting the normal steady state operation of the circuit. Under the conditions of ISO7637-2 pulse 1, the input voltage can reach -150V, with the generator having an impedance of 10Ω. As a result, a current of 15A passes through the TVS-, and the voltage across the TVS will be approximately equal to its clamping voltage.

The design must ensure that the SGM257301Q's absolute minimum source voltage rating (-65V) and the MOSFET's maximum V_{DS} rating are not exceeded; accordingly, a 60V rated MOSFET is used in this example

MBJ-series TVS diodes, with a peak pulse power rating of up to 600W, offer sufficient robustness for ISO 7637-2 transients and suppressed load-dump conditions as defined in ISO 16750-2 Pulse B.

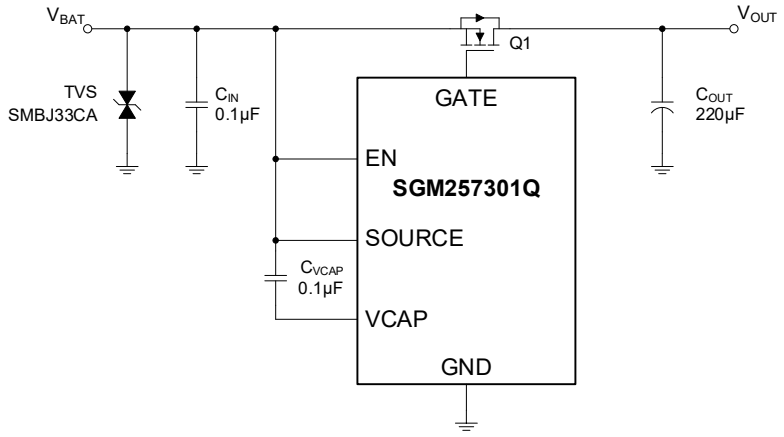


Figure 8. 12V Battery Protection Solution Using A Single Bidirectional TVS

APPLICATION INFORMATION (continued)

TVS Diode and MOSFET Selection Guidelines for 24V Battery Protection Applications

Figure 9 illustrates a typical 24V battery protection circuit employing two unidirectional TVS diodes to safeguard against both positive and negative voltage transients.

In a standard 24V battery protection circuit, as depicted in Figure 9, two uni-directional TVS diodes are employed to safeguard against both positive and negative transient voltage spikes. For the TVS+ diode, its breakdown voltage must exceed the 48V jump start voltage. Simultaneously, it should not exceed the absolute maximum ratings of the source and enable pin of the SGM257301Q, which is 65V. Additionally, it needs to endure the 65V suppressed load dump. Regarding the TVS diode, its breakdown voltage should be set below 32V (in magnitude) relative to the maximum specified reverse battery voltage to ensure the TVS remains undamaged during prolonged reverse-battery conditions.

During the ISO7637-2 Pulse 1 event, the input voltage reaches to -600V with a 50Ω generator impedance, causing 12A to flow through the TVS-. The clamping voltage of the TVS- in this scenario differs from that of the 12V battery protection setup. Since during the ISO7637-2 pulse, the SOURCE -to-CATHODE voltage observed is equal to the sum of the negative TVS clamping voltage and the output capacitor voltage. In a 24V battery application, where the maximum battery voltage amounts to 32V, the clamping voltage of the TVS- must not be more than 75V - 32V, equating to 43V.

A single bi-directional TVS diode is unsuitable for 24V battery protection due to the conflicting requirements for the breakdown voltage and clamping voltage. Specifically, the TVS+ requires a breakdown voltage of at least 65V, while the maximum clamping voltage must not exceed 43V, which is impossible since the clamping voltage cannot be lower than the breakdown voltage. Therefore, with a current of 15A flowing through the TVS, the voltage drop across the TVS will be close to its clamping voltage. For the positive side TVS+, the SMBJ58A is suggested, featuring a minimum breakdown voltage of 64.4V and a typical value of 67.8V. For the negative side TVS-, the SMBJ26A is recommended, as it offers a breakdown voltage near 32V (to tolerate the maximum reverse battery voltage of -32V) and a maximum clamping voltage of 42.1V. In the case of 24V battery protection, it is suggested to employ a MOSFET with a 75V rating. Additionally, at the input, the SMBJ26A and SMBJ58A, connected back-to-back, are to be utilized.

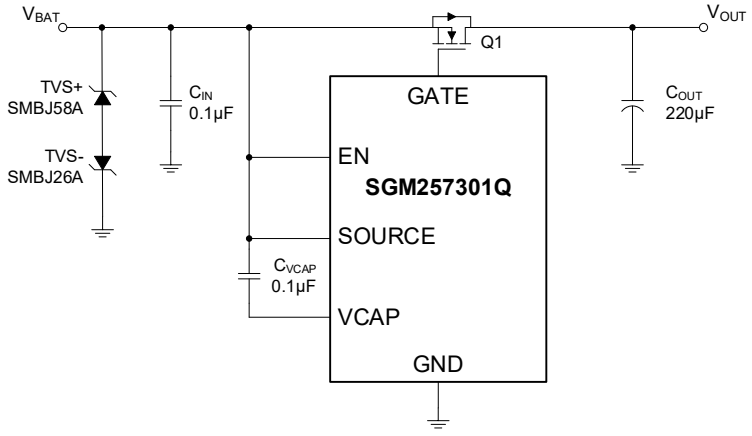


Figure 9. 24V Battery Protection Solution Using Two Unidirectional TVS

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM257301Q ideal diode controller is designed to operate within a supply voltage range of 3.2V to 65V. When the input supply is situated several inches or more away from the device, it's best to employ an input ceramic bypass capacitor with a capacitance greater than 22nF. To avoid damage to the SGM257301Q and its surrounding components in the event of a direct output short circuit, a power supply offering overload and short circuit protection is essential.

Layout Guidelines

- Connect the SOURCE, GATE, pins of SGM257301Q near the corresponding SOURCE, GATE, pins of the MOSFET.
- Position the charge pump capacitor (between VCAP and SOURCE) away from the MOSFET to minimize capacitance drift due to heat.
- Use a short and robust trace to connect the SGM257301Q's GATE pin to the MOSFET gate, avoiding thin or lengthy traces.
- The GATE pin of the SGM257301Q should be connected to the MOSFET gate using a short, low-impedance trace; avoid long or narrow routing to minimize gate drive loop inductance and resistance.
- Place the GATE pin as close as possible to the MOSFET to reduce turn-off delays resulting from trace resistance.
- Acceptable results can be obtained with different layout designs, but the layout in Figure 10 is a recommended approach for achieving good performance.

Layout Example

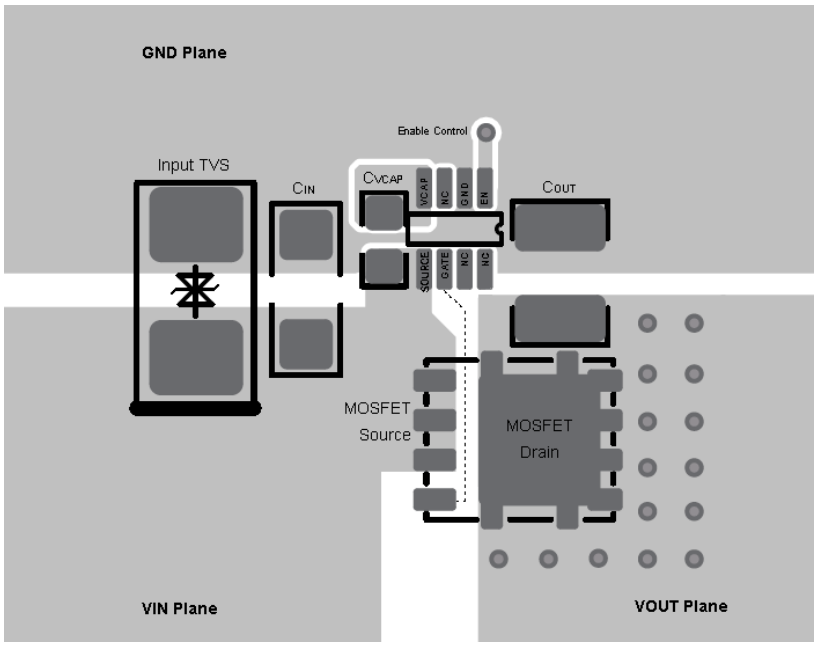


Figure 10. TSOT-23-8 Layout Example

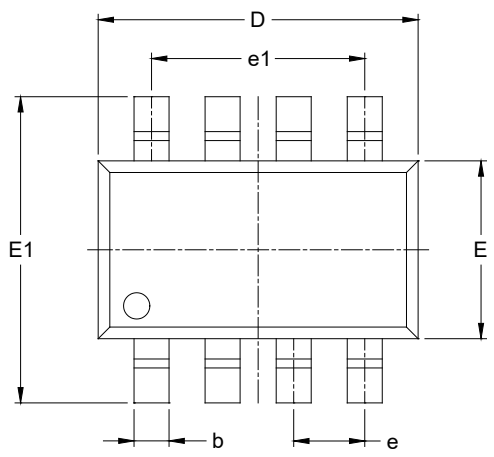
REVISION HISTORY

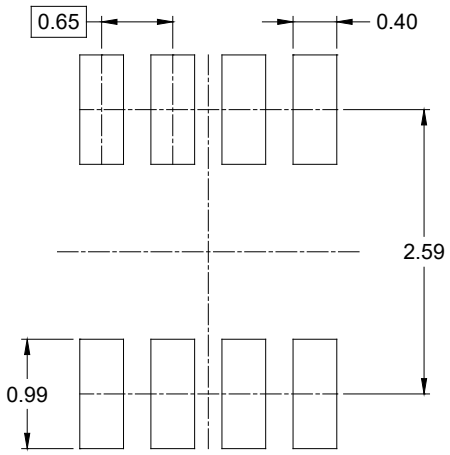
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JULY 2026)	Page
Changed from product preview to production data	All

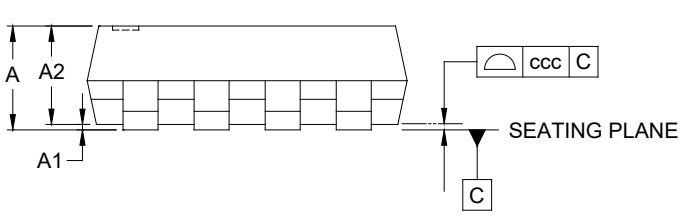
PACKAGE OUTLINE DIMENSIONS

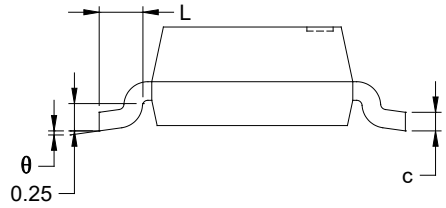
TSOT-23-8





RECOMMENDED LAND PATTERN (Unit: mm)



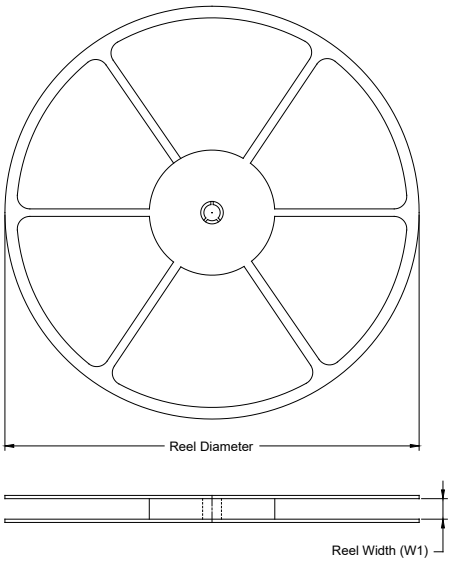


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.220	-	0.380
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.550	-	3.050
e	0.650 BSC		
e1	1.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

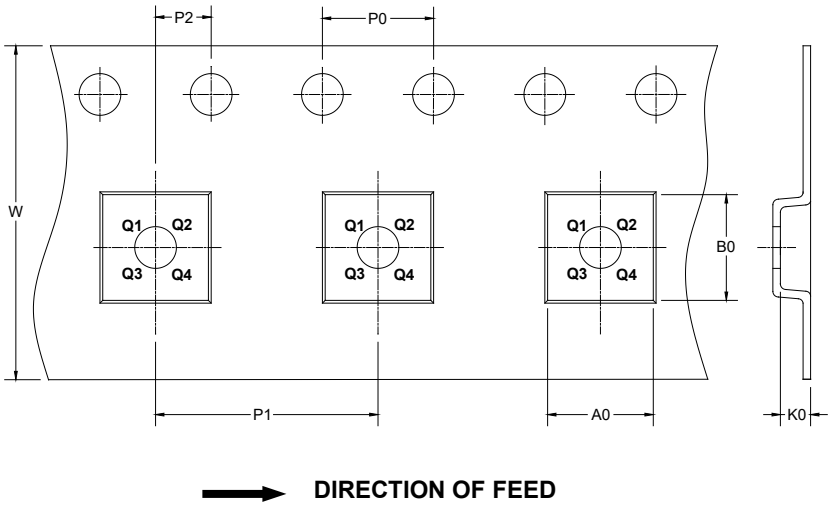
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



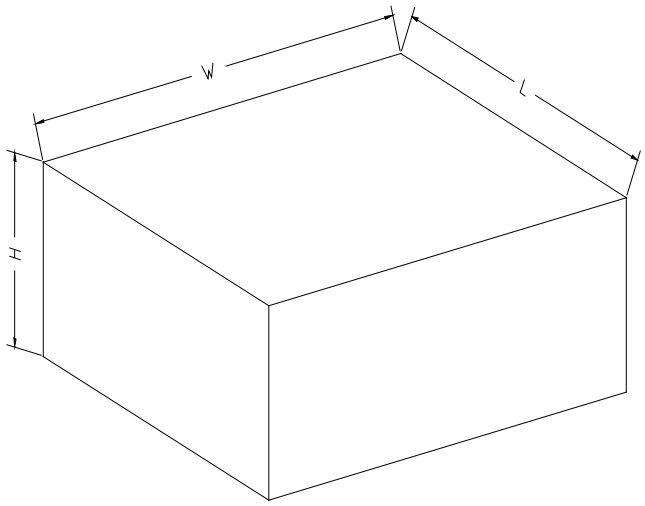
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-8	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002