# SGM61169
# 4V to 18V Input, 6A Synchronous Buck Converter

## GENERAL DESCRIPTION

The SGM61169 is an efficient 6A synchronous Buck converter with a wide 4V to 18V input voltage range and an internally compensated innovative emulated current mode (IECM) control with fixed frequency. The device has 5 fixed selectable switching frequencies, from 500kHz to 2.2MHz, which can be used to provide high efficiency and external clock synchronization with the SYNC/FSEL pin. It also has the features like selectable soft-start times, selectable current limits, monotonic startup and power good output monitor.

The SGM61169 also provides full protections, including over-voltage protection (OVP), under-voltage protection (UVP), over-current protection (OCP), and thermal shutdown.

The SGM61169 is available in a Green TQFN-3×2.5-14L package.

## SIMPLIFIED SCHEMATIC

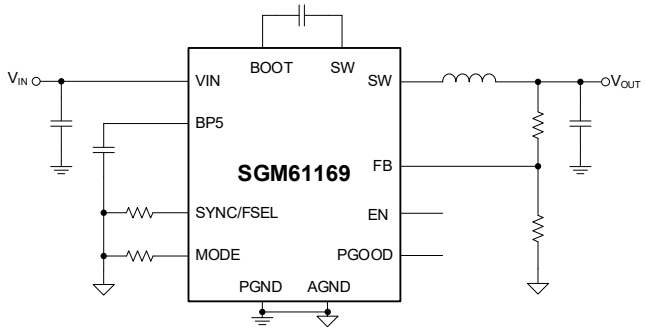



**Figure 1. Simplified Schematic**

## FEATURES

- **4V to 18V Input Voltage Range**
- **0.5V to 7V Output Voltage Range**
- **Internally Compensated Innovative Emulated Current Mode (IECM) Control with Fixed Frequency**
- **0.5V Internal Reference Voltage**
- **±0.5% Reference Voltage Accuracy**
- **25mΩ/6.2mΩ Low Integrated MOSFETs**
- **500kHz, 750kHz, 1MHz, 1.5MHz and 2.2MHz Selectable Switching Frequencies**
- **External Clock Synchronization**
- **Three Selectable PWM Ramp Options for Optimized Control Loop Performance**
- **0.5ms, 1ms, 2ms and 4ms Selectable Soft-Start Times**
- **Selectable Current Limits to Support 6A and 3A Operation**
- **Monotonic Startup with Pre-Biased Outputs**
- **Power Good Output Monitor**
- **Input Under-Voltage Lockout (UVLO)**
- **Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), and Thermal Shutdown**
- **Available in a Green TQFN-3×2.5-14L Package**

## APPLICATIONS

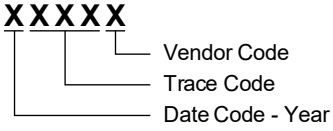
Test and Measurement Instruments
Medical Imaging Equipment
Business Exchange and Server
Wireless Infrastructure
Telecommunications Infrastructure

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM61169 | TQFN-3×2.5-14L | -40℃ to +150℃ | SGM61169TTWS14G/TR | 61169<br>XXXXX | Tape and Reel, 5000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

VIN ..... -0.3V to 20V
BOOT ..... -0.3V to 26V
BOOT to SW ..... -0.3V to 6V
EN, PGOOD, MODE, SYNC/FSEL, FB, BP5 ..... -0.3V to 6V
SW, DC ..... -0.3V to 20V
SW, Transient 10ns ..... -3V to 28V
Package Thermal Resistance
TQFN-3×2.5-14L, $\theta_{JA}$ ..... 53.2℃/W
TQFN-3×2.5-14L, $\theta_{JB}$ ..... 3.2℃/W
TQFN-3×2.5-14L, $\theta_{JC}$ ..... 49.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

## RECOMMENDED OPERATING CONDITIONS

Input Voltage, $V_{IN}$ (3) ..... 4V to 18V
Output Voltage, $V_{OUT}$ ..... 0.5V to 7V
Output Current, $I_{OUT}$ ..... 6A (MAX)
External Clock Frequency, $f_{SYNC}$ ..... 400kHz to 2600kHz
Operating Junction Temperature, $T_J$ ..... -40℃ to +150℃

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

3. The UVLO rising voltage is 4.2V (MAX), while its falling voltage is below 4V. Therefore, the input voltage must be higher than 4.2V (maximum UVLO rising threshold) for startup, and the SGM61169 can work down to 4V input voltage after startup.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

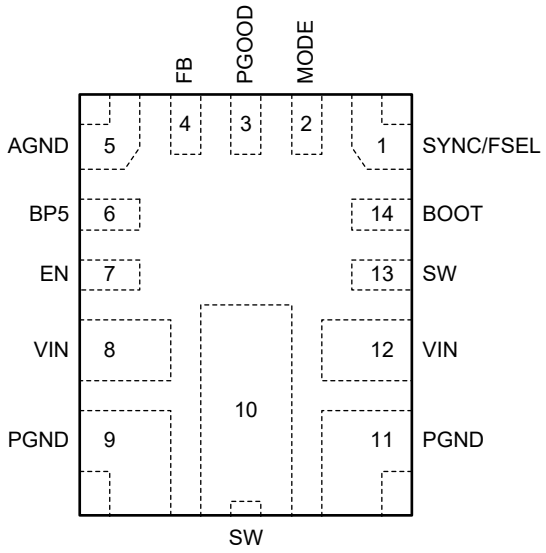
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TQFN-3×2.5-14L

## PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | SYNC/FSEL | AI | External Clock Synchronization and Frequency Selection Pin. This pin can be used to synchronize the switching frequency by an external clock. The switching frequency is programmed by the resistor connected to ground. If any case, a resistor needs to be connected between this pin and the ground. |
| 2 | MODE | AI | A resistor connected to ground selects the current limit, soft-start time, and PWM ramp amplitude. |
| 3 | PGOOD | DO | Power Good Open-Drain Output Pin. Connect this pin to the pull-up power supply through a resistor |
| 4 | FB | AI | Feedback Input. The output voltage can be programmed by connecting this pin to the midpoint of a resistor divider. |
| 5 | AGND | P | Analog Ground. |
| 6 | BP5 | AO | Internal 4.5V Regulator Output. Bypass this pin to AGND with a 2.2μF capacitor. |
| 7 | EN | AI | Enable Input Pin. The EN pin can be used to adjust the input UVLO and hysteresis by a resistor divider. |
| 8, 12 | VIN | P | Power Input. The two VIN pins are connected to input capacitiors with a low-impedance connection. A capacitor of 10nF to 100nF is suggested to put from each VIN to PGND near the IC. |
| 9, 11 | PGND | P | Ground Return for Low-side Power MOSFET. |
| 10 | SW | P | Switching Node Output of the Converter. Connect it to one terminal of the output inductor. |
| 13 | SW | P | Return Path for the Bootstrap Capacitor of Internal High-side MOSFET Gate Driver. External bootstrap capacitor must be connected between this SW pin and BOOT pin. The SW pins are connected internally. |
| 14 | BOOT | P | Bootstrap Input to Supply the High-side Gate Driver. Connect a capacitor between this pin and SW pin. |

NOTE: AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power.

# ELECTRICAL CHARACTERISTICS

($T_J$ = -40℃ to +150℃, $V_{IN}$ = 4V to 18V, typical values are measured at $V_{IN}$ = 12V and $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| VIN Operating Non-Switching Supply Current | $I_{Q\_VIN}$ | $V_{EN}$ = 1.3V, $V_{FB}$ = 550mV, 1MHz | | 1720 | 2500 | μA |
| VIN Shutdown Supply Current | $I_{SD\_VIN}$ | $V_{EN}$ = 0V | | 5.2 | 16 | μA |
| VIN UVLO Rising Threshold | $V_{UVLO}$ | VIN rising | 3.8 | 4 | 4.2 | V |
| VIN UVLO Hysteresis | | | | 150 | | mV |
| **ENABLE and UVLO** | | | | | | |
| EN Voltage Rising Threshold | $V_{EN\_RISE}$ | EN rising, enable switching | | 1.2 | 1.25 | V |
| EN Voltage Falling Threshold | $V_{EN\_FALL}$ | EN falling, disable switching | 1 | 1.1 | | V |
| EN Voltage Hysteresis | $V_{EN\_HYS}$ | | | 100 | | mV |
| EN Pin Sourcing Current | | $V_{EN}$ = 1V | 0.9 | 1.5 | | μA |
| | | $V_{EN}$ = 1.3V | | 12 | | |
| **Internal LDO BP5** | | | | | | |
| Internal LDO BP5 Output Voltage | $V_{BP5}$ | $V_{IN}$ = 12V | | 4.5 | | V |
| BP5 Dropout Voltage | | $V_{IN}$ - $V_{BP5}$, $V_{IN}$ = 3.8V, $I_{OUT}$ = 10mA | | | 300 | mV |
| BP5 Short-Circuit Current Limit | | $V_{IN}$ = 12V, $V_{BP5}$ = 3.5V | | 75 | | mA |
| **Reference Voltage** | | | | | | |
| Internal Reference Voltage | $V_{REF}$ | $T_J$ = +25℃ | 497.5 | 500 | 502.5 | mV |
| | | $T_J$ = -40℃ to +150℃ | 495 | | 505 | |
| Input Leakage Current into FB Pin | $I_{FB\_LKG}$ | $V_{FB}$ = 0.5V, non-switching, $V_{IN}$ = 12V, $V_{EN}$ = 0V | | 1 | | nA |
| **Switching Frequency and Oscillator** | | | | | | |
| Switching Frequency | $f_{SW}$ | $R_{FSEL}$ ≥ 24.3kΩ | 450 | 500 | 550 | kHz |
| | | $R_{FSEL}$ = 17.4kΩ | 675 | 750 | 825 | |
| | | $R_{FSEL}$ = 11.8kΩ | 900 | 1000 | 1100 | |
| | | $R_{FSEL}$ = 8.06kΩ | 1350 | 1500 | 1650 | |
| | | $R_{FSEL}$ ≤ 4.99kΩ | 1980 | 2200 | 2420 | |
| **Synchronization** | | | | | | |
| High-Level Input Voltage | $V_{IH\_SYNC}$ | $V_{IN}$ = 12V | 1.8 | | | V |
| Low-Level Input Voltage | $V_{IL\_SYNC}$ | $V_{IN}$ = 12V | | | 0.8 | V |
| **Soft-Start** | | | | | | |
| Soft-Start Time | $t_{SS1}$ | $R_{MODE}$ = 1.78kΩ | | 0.5 | | ms |
| | $t_{SS2}$ | $R_{MODE}$ = 2.21kΩ | | 1 | | |
| | $t_{SS3}$ | $R_{MODE}$ = 2.74kΩ | | 2 | | |
| | $t_{SS4}$ | $R_{MODE}$ = 3.32kΩ | | 4 | | |
| **Power Stage** | | | | | | |
| High-side MOSFET On-Resistance | $R_{DSON\_HS}$ | $T_J$ = +25℃, $V_{IN}$ = 12V, $V_{BOOT-SW}$ = 4.5V | | 25 | 46 | mΩ |
| Low-side MOSFET On-Resistance: High Current Limit Selected | $R_{DSON\_LS1}$ | $T_J$ = +25℃, $V_{BP5}$ = 4.5V, $R_{MODE}$ = 1.78kΩ | | 6.2 | 12 | mΩ |
| Low-side MOSFET On-Resistance: Low Current Limit Selected | $R_{DSON\_LS2}$ | $T_J$ = +25℃, $V_{BP5}$ = 4.5V, $R_{MODE}$ = 22.1kΩ | | 11.6 | 22 | mΩ |
| BOOT-SW UVLO Rising Threshold | $V_{BOOT-SW\_UVR}$ | $V_{BOOT-SW}$ rising | | 2.7 | | V |
| BOOT-SW UVLO Falling Threshold | $V_{BOOT-SW\_UVF}$ | $V_{BOOT-SW}$ falling | | 2.5 | | V |
| Minimum On-Pulse Width (1) | $t_{ON\_MIN}$ | $I_{OUT}$ > 1/2$I_{L_PK-PK}$ | | 30 | 38 | ns |
| Minimum Off-Pulse Width (1) | $t_{OFF\_MIN}$ | $V_{IN}$ = 4V,$V_{OUT\_SET}$ = 3.3V, $I_{OUT}$ = 0A, $f_{SW}$ = 2.2MHz | | 110 | 140 | ns |

## ELECTRICAL CHARACTERISTICS (continued)

($T_J$ = -40℃ to +150℃, $V_{IN}$ = 4V to 18V, typical values are measured at $V_{IN}$ = 12V and $T_J$ = +25℃, unless otherwise noted.)

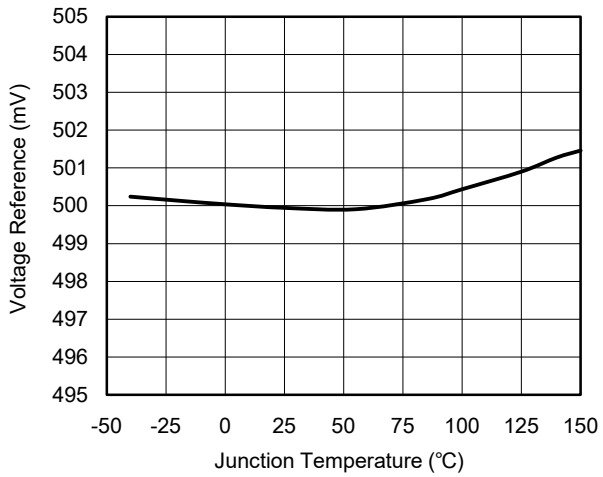
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Current Sense and Over-Current Protection** | | | | | | |
| High-side Peak Current Limit | $I_{OC\_HS\_pk1}$ | $R_{MODE}$ = 1.78kΩ | 8.2 | 9 | 9.8 | A |
| | $I_{OC\_HS\_pk2}$ | $R_{MODE}$ = 22.1kΩ | 3.9 | 4.5 | 5.1 | |
| Low-side Sourcing Current Limit | $I_{OC\_LS\_src1}$ | $R_{MODE}$ = 1.78kΩ | 6.5 | 7.3 | 8 | A |
| | $I_{OC\_LS\_src2}$ | $R_{MODE}$ = 22.1kΩ | 3.4 | 3.9 | 4.4 | |
| Low-side Sinking Current Limit | $I_{OC\_LS\_snk}$ | Current into SW pin, $R_{MODE}$ = 1.78kΩ | 2 | | | A |
| | | Current into SW pin, $R_{MODE}$ = 22.1kΩ | 2.2 | | | |
| **Output Over-Voltage and Under-Voltage Protections** | | | | | | |
| Over-Voltage Protection (OVP) Threshold Voltage | $V_{OVP}$ | $V_{FB}$ rising | | 120 | | $\%V_{REF}$ |
| Under-Voltage Protection (UVP) Threshold Voltage | $V_{UVP}$ | $V_{FB}$ falling | | 80 | | |
| **Power Good** | | | | | | |
| PGOOD Threshold | $V_{PG\_OV}$ | $V_{FB}$ rising (fault) | 113 | 116 | 119 | $\%V_{REF}$ |
| | | $V_{FB}$ falling (good) | 105 | 108 | 111 | |
| | $V_{PG\_UV}$ | $V_{FB}$ rising (good) | 89 | 92 | 95 | |
| | | $V_{FB}$ falling (fault) | 81 | 84 | 87 | |
| Leakage Current into PGOOD Pin When Open-Drain Output is High | $I_{PGOOD\_LKG}$ | $V_{PGOOD}$ = 4.7V | | | 1 | μA |
| PGOOD Low-Level Output Voltage | $V_{PG\_LOW}$ | $I_{PGOOD}$ = 2mA, $V_{IN}$ = 12V | | | 0.5 | V |
| Min VIN for Valid PGOOD Output | | $V_{PG}$ < 0.5V at 100μA | | 0.95 | 1.2 | V |
| **Hiccup** | | | | | | |
| Hiccup Time before Restart | | | | 7 × $t_{SS}$ | | ms |
| **Output Discharge** | | | | | | |
| Output Discharge Resistance | $R_{Dischg}$ | $V_{IN}$ = 12V, $V_{SW}$ = 0.5V, power conversion disabled | | 66 | | Ω |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold (1) | $T_{SD}$ | Temperature rising | | 165 | | ℃ |
| Thermal Shutdown Hysteresis (1) | $T_{HYS}$ | | | 12 | | ℃ |

NOTE:

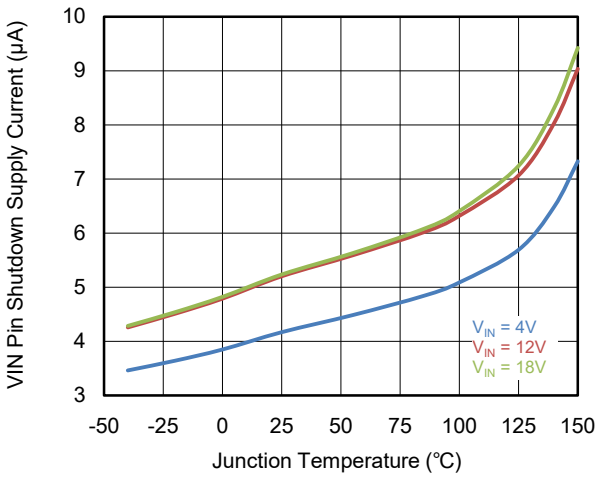
1. Specified by design. Not production tested.

## TYPICAL PERFORMANCE CHARACTERISTICS

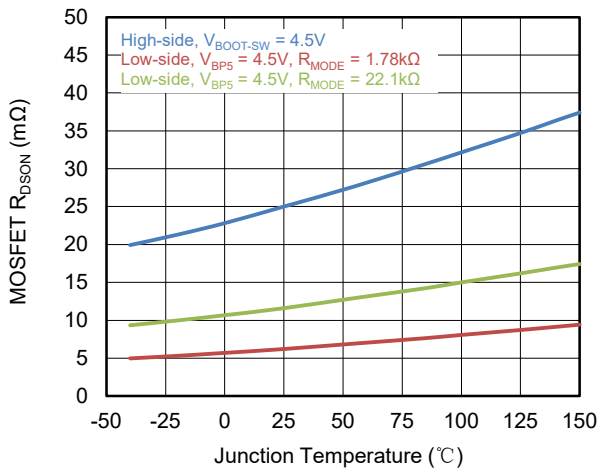
Voltage Reference vs. Junction Temperature



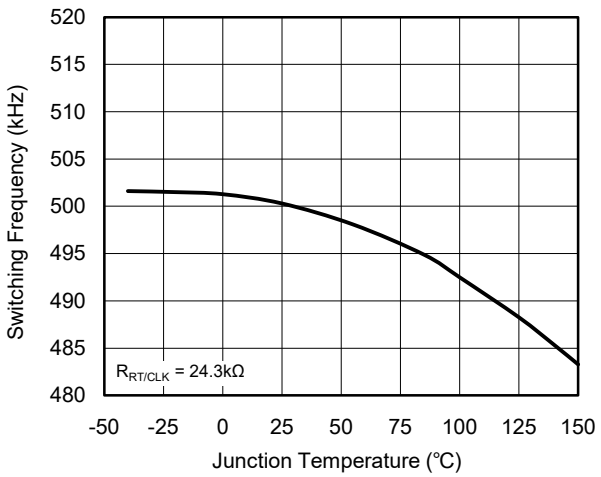

VIN Pin Shutdown Current vs. Junction Temperature



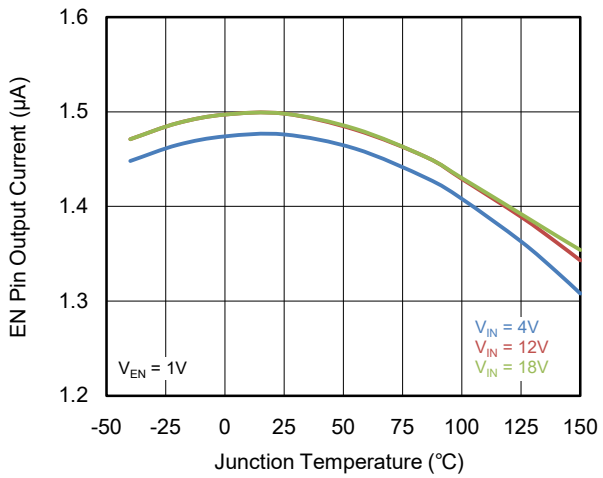

MOSFET $R_{DSON}$ vs. Junction Temperature



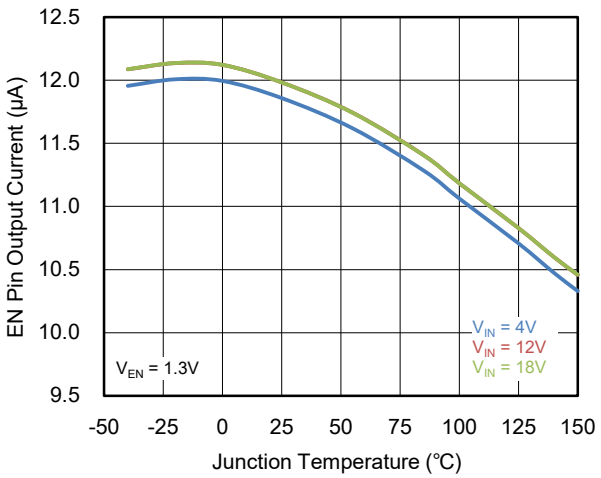

Switching Frequency vs. Junction Temperature (500kHz)




EN Pin Output Current vs. Junction Temperature

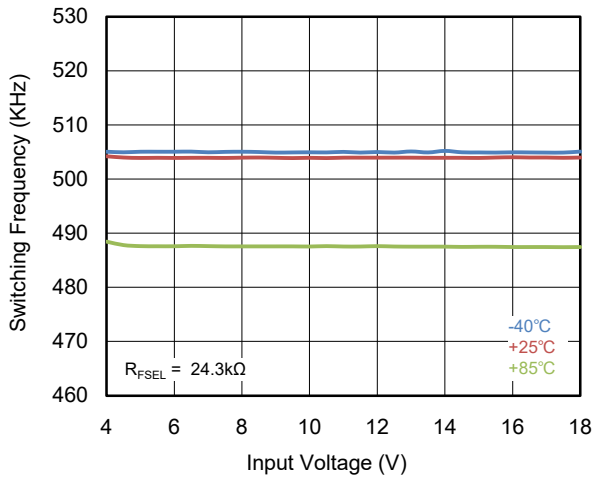



EN Pin Output Current vs. Junction Temperature

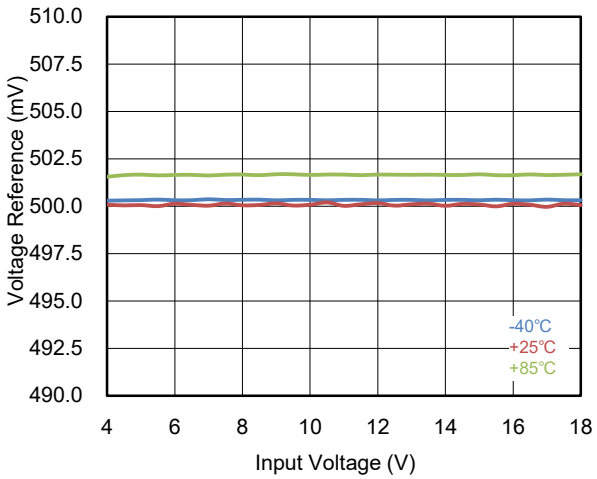


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

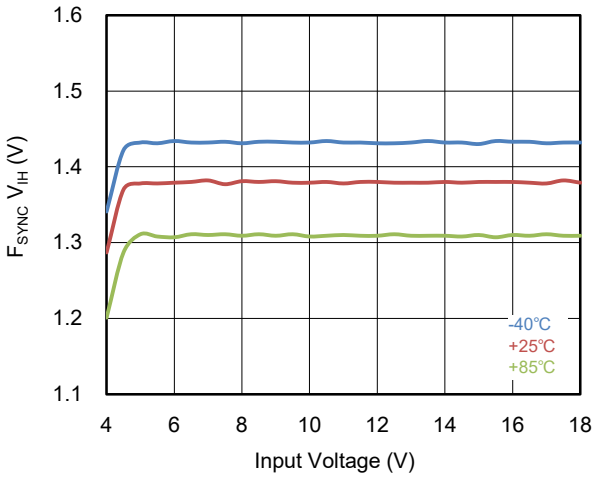
Switching Frequency vs. Input Voltage



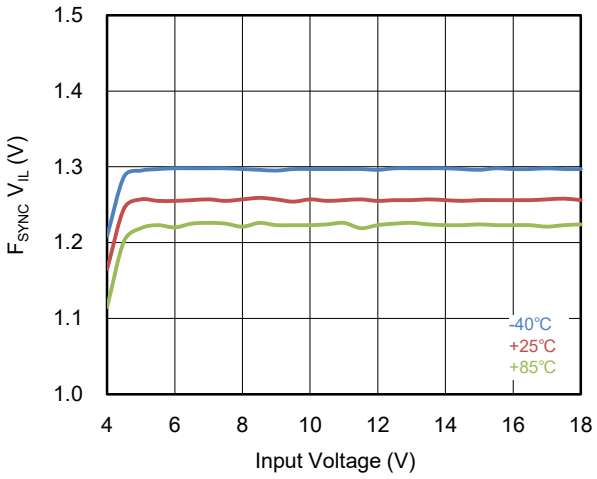

Voltage Reference vs. Input Voltage




$F_{SYNC}$ $V_{IH}$ vs. Input Voltage



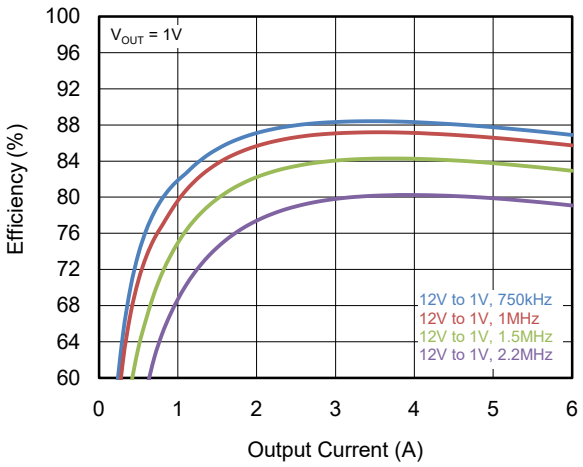

$F_{SYNC}$ $V_{IL}$ vs. Input Voltage



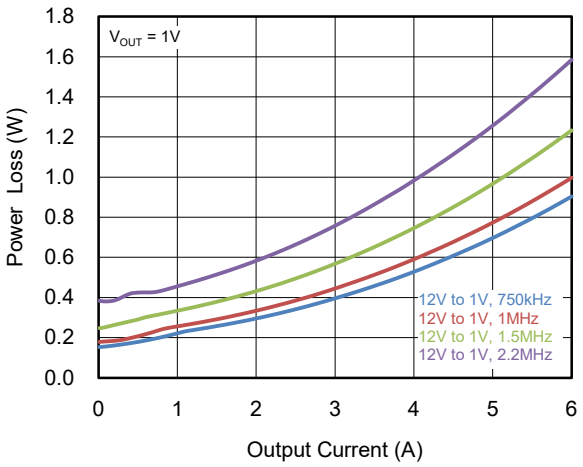
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 1V, L = 0.6μH, DCR = 4mΩ, $f_{SW}$ = 1MHz, unless otherwise noted.

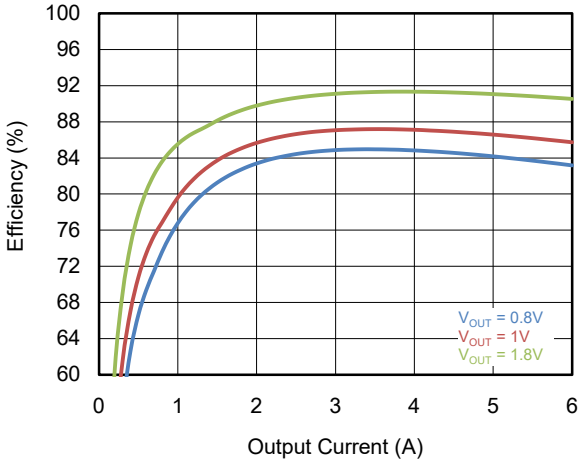
Efficiency vs. Output Current



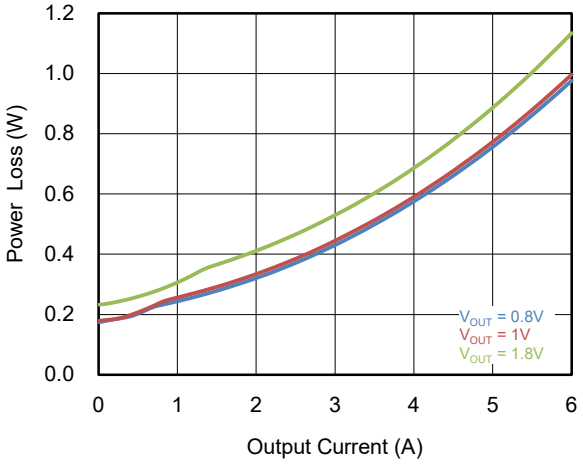

Power Loss vs. Output Current



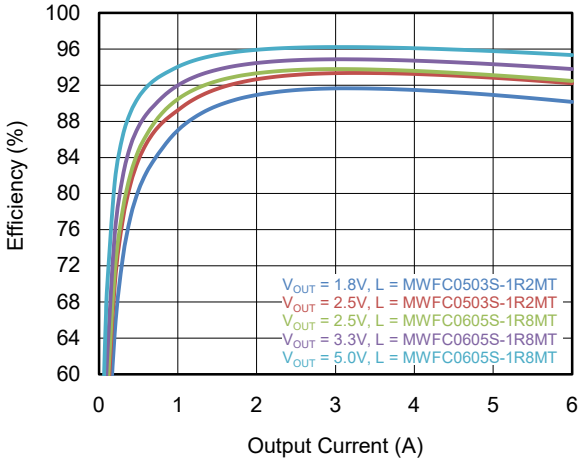

Efficiency vs. Output Current



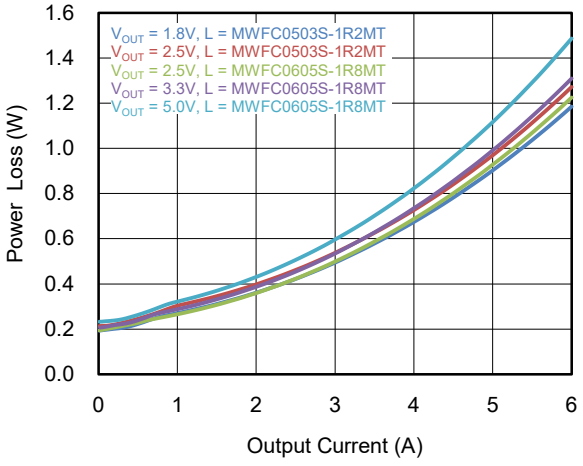

Power Loss vs. Output Current




Efficiency vs. Output Current



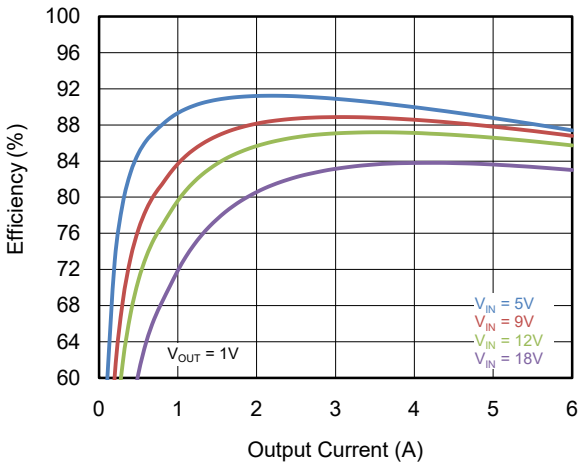

Power Loss vs. Output Current



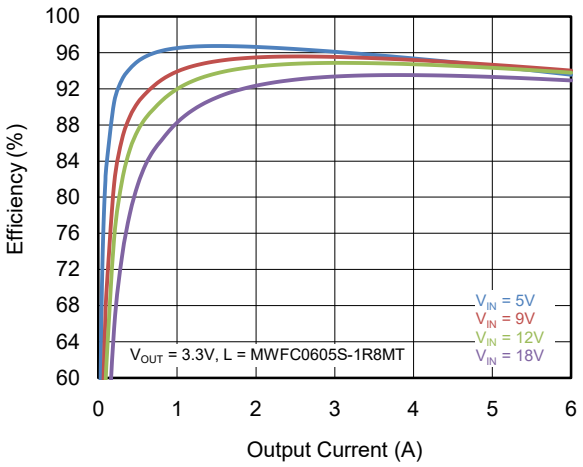
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 1V, L = 0.6μH, DCR = 4mΩ, $f_{SW}$ = 1MHz, unless otherwise noted.

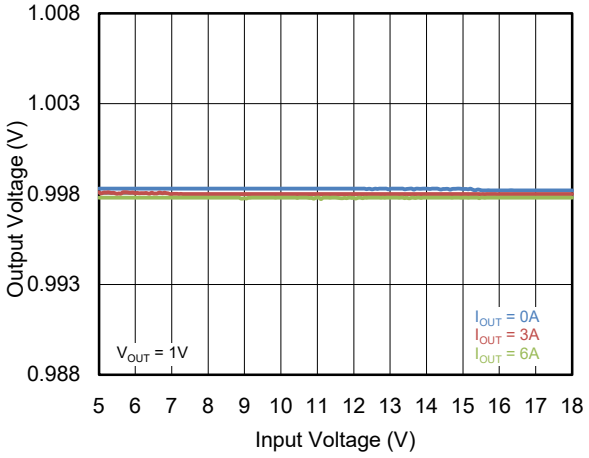
Efficiency vs. Output Current




Efficiency vs. Output Current




Line Regulation

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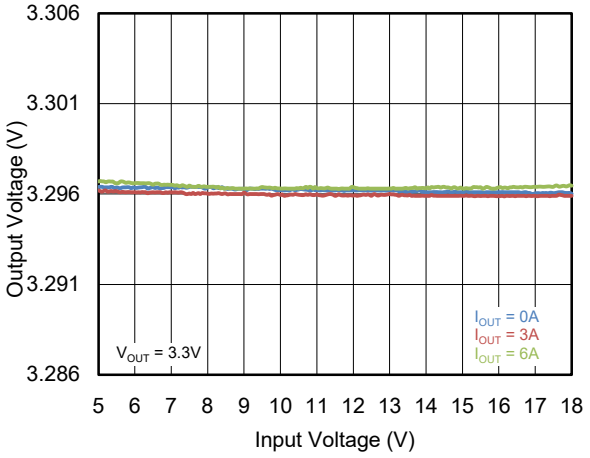
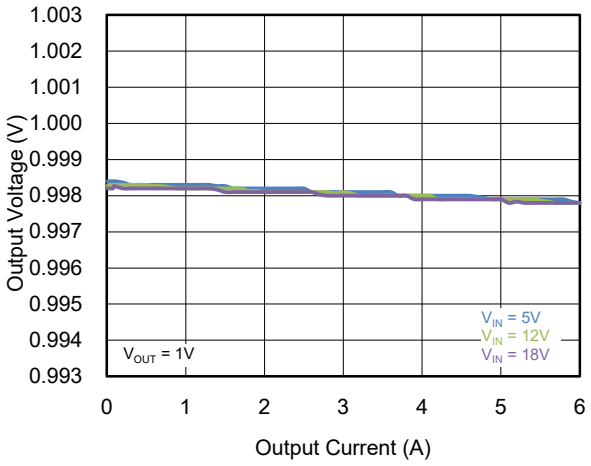
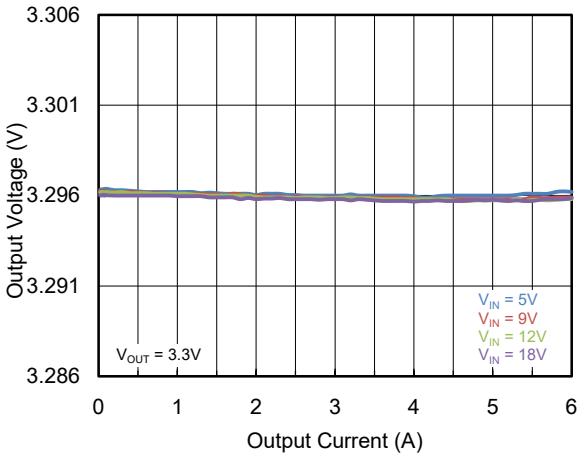



Load Regulation



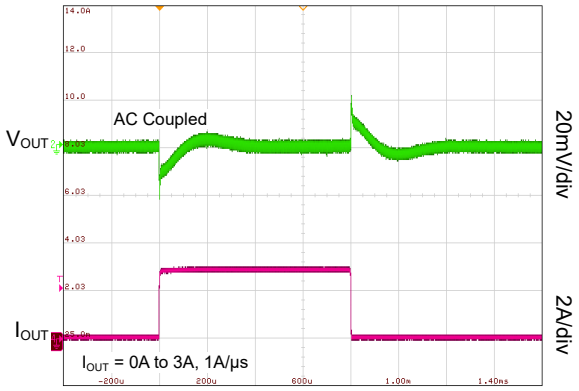

Load Regulation



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

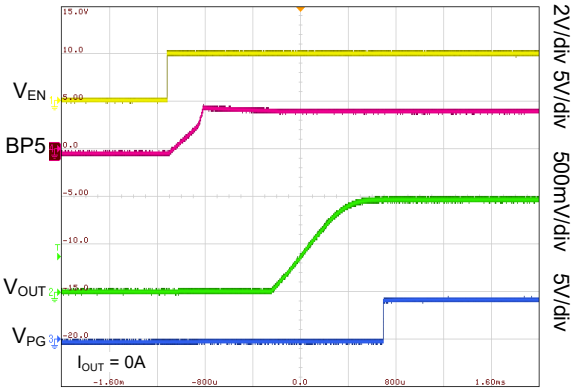
$T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 1V, L = 0.6μH, DCR = 4mΩ, $f_{SW}$ = 1MHz, unless otherwise noted.

Load Transient



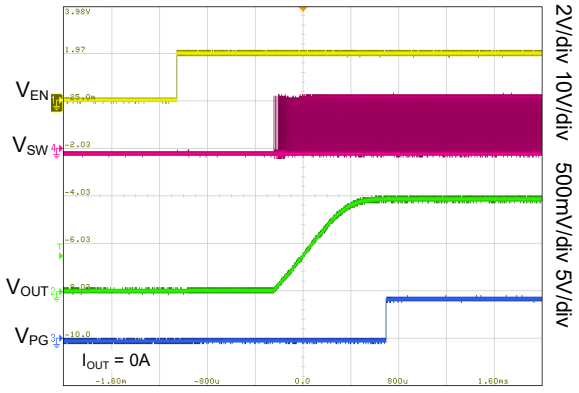

Time (200μs/div)

EN Startup Measuring BP5



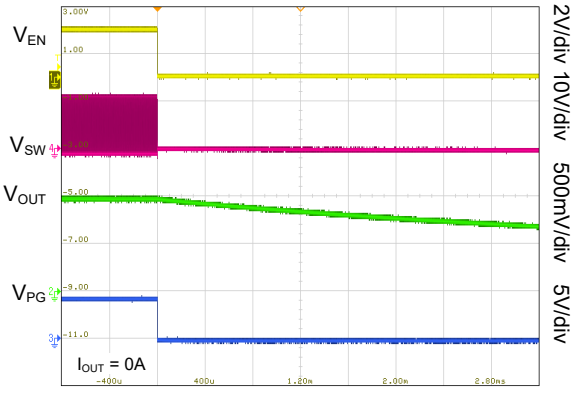

Time (400μs/div)

EN Startup Measuring SW



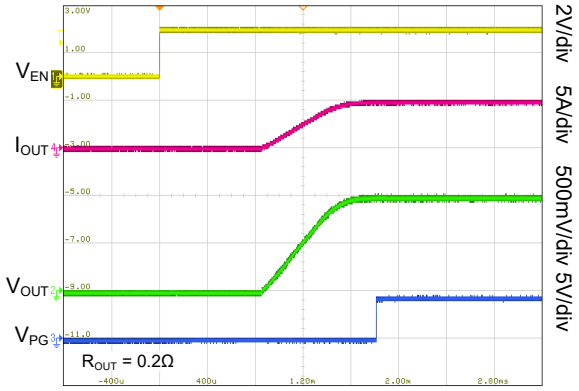

Time (400μs/div)

EN Shutdown



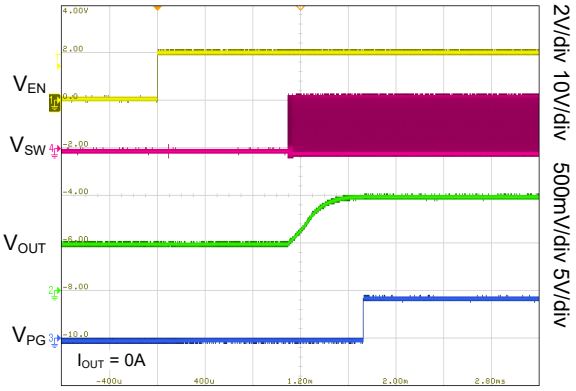

Time (400μs/div)

EN Startup with Load




Time (400μs/div)

EN Startup 0.5V Prebias

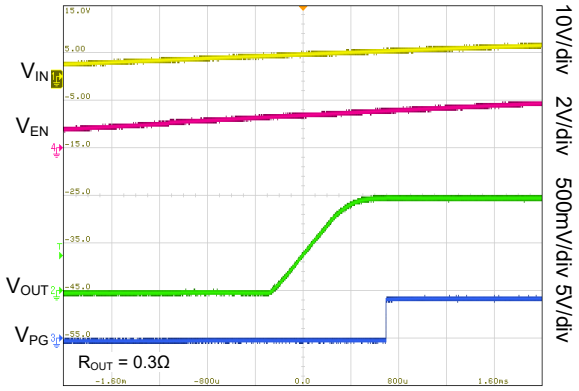



Time (400μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

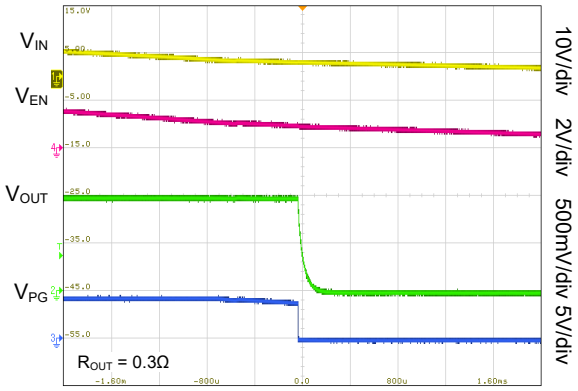
$T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 1V, L = 0.6μH, DCR = 4mΩ, $f_{SW}$ = 1MHz, unless otherwise noted.

VIN Startup



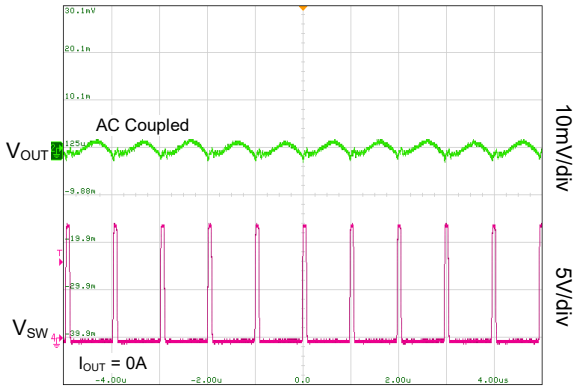

Time (400μs/div)

VIN Shutdown



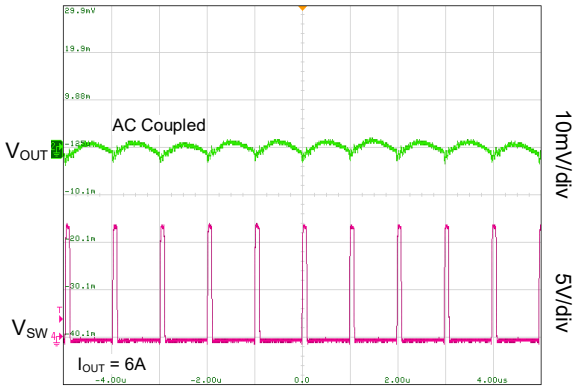

Time (400μs/div)

Output Ripple No Load



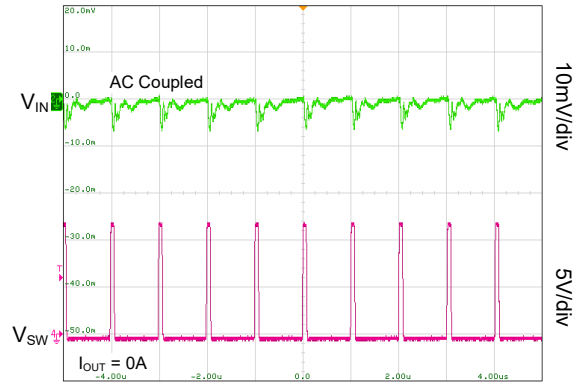

Time (1μs/div)

Output Ripple 6A Load



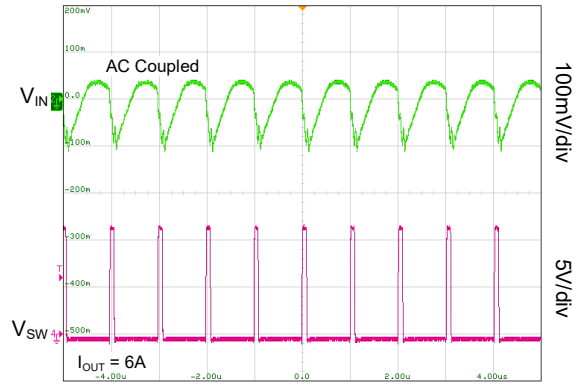

Time (1μs/div)

Input Ripple No Load




Time (1μs/div)

Input Ripple 6A Load

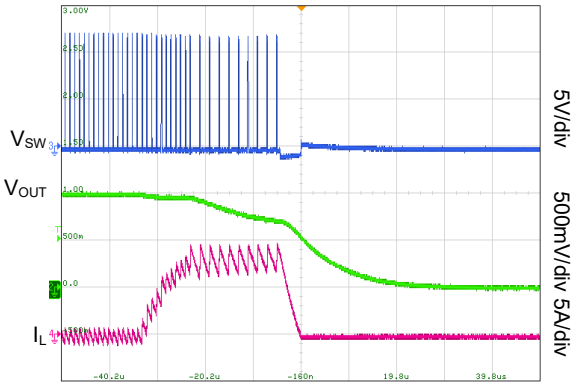



Time (1μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

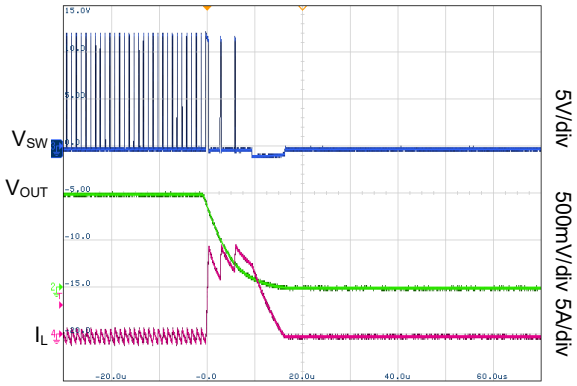
$T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 1V, L = 0.6μH, DCR = 4mΩ, $f_{SW}$ = 1MHz, unless otherwise noted.

Over-Current Protection Overload



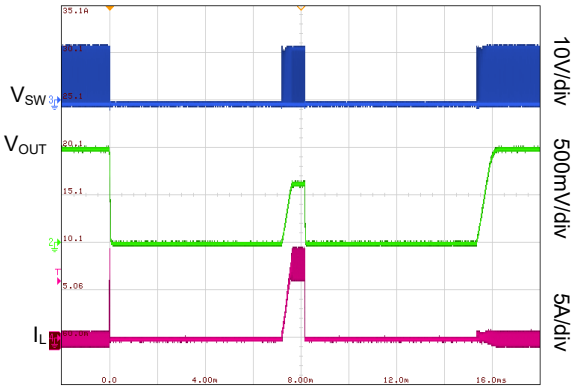

Time (10μs/div)

Over-Current Protection Short



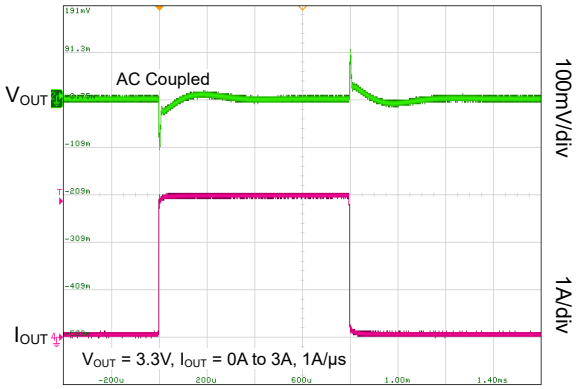

Time (10μs/div)

Over-Current Protection Hiccup and Recover



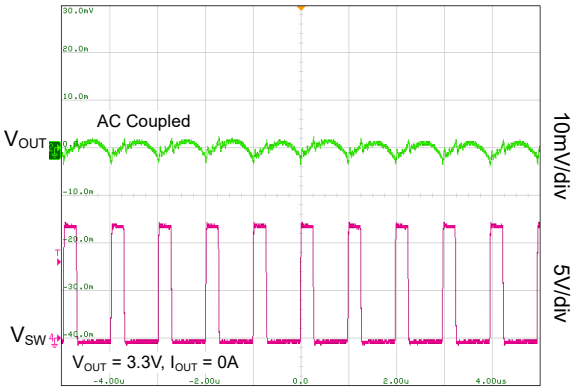

Time (2ms/div)

Load Transient



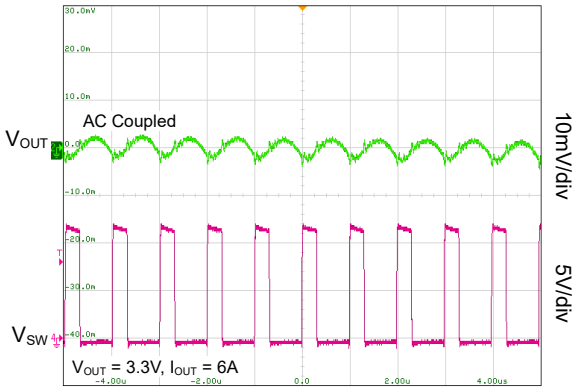

Time (200μs/div)

Output Ripple- No Load




Time (1μs/div)

Output Ripple- 6A Load




Time (1μs/div)

# FUNCTIONAL BLOCK DIAGRAM

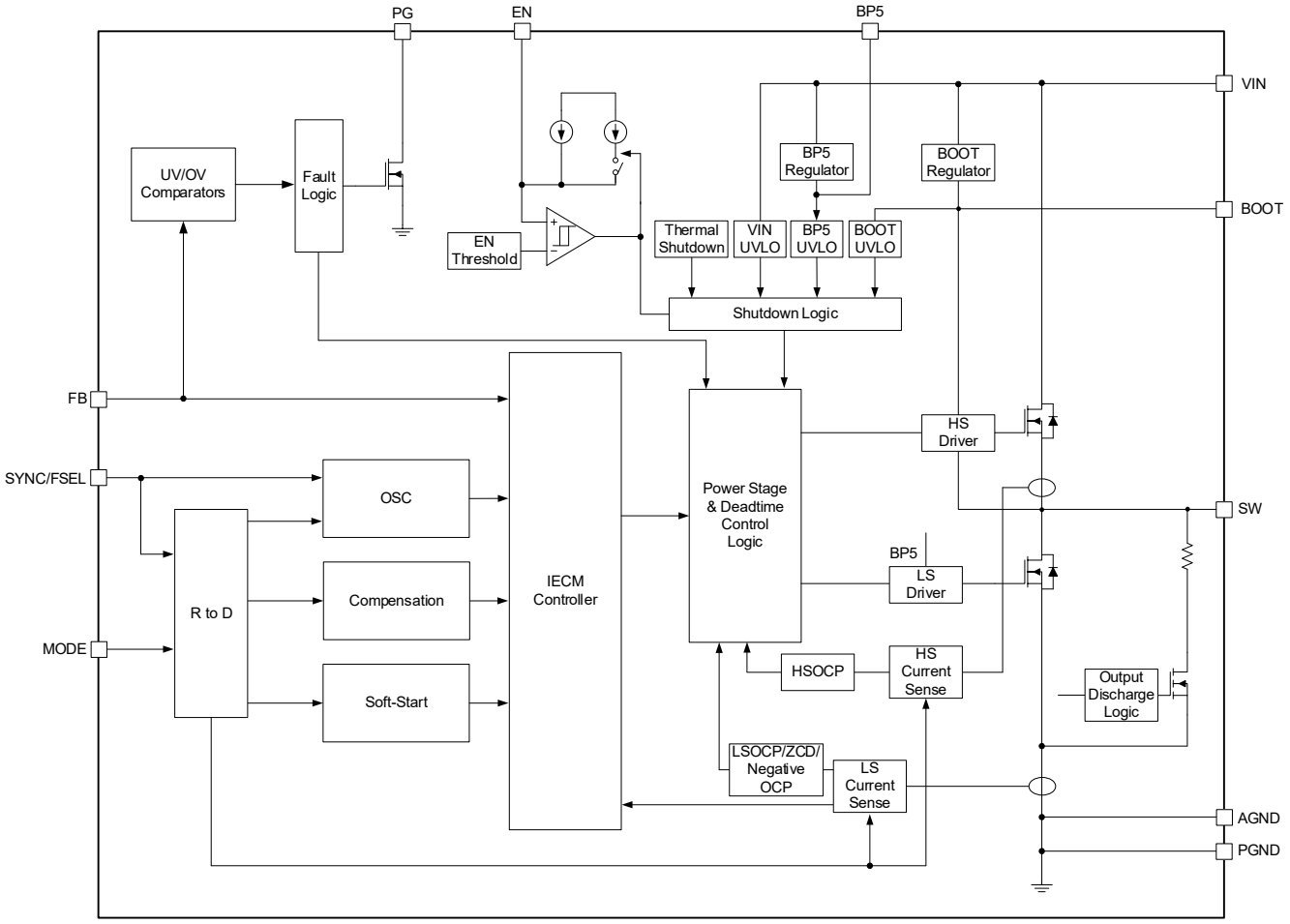



**Figure 2. Functional Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM61169 adopts innovative emulated current mode (IECM) control, fixed switching frequency and internal compensation, and is an efficient 18V, 6A synchronous Buck converter with integrated high-side and low-side MOSFET. The converter supports junction temperatures up to 150℃, enabling reliable operation in thermally demanding environments like wireless base stations. It accepts input voltages from 4V to 18V and generates adjustable outputs between 0.5V and 7V. The wide switching frequency is adjustable from 500kHz to 2.2MHz to allow optimizing of the efficiency and size of the converter. For adjusting the internal switching frequency, an external resistor $R_{FSEL}$ is connected between the SYNC/FSEL pin and GND. The device also accepts an external clock source on this pin to synchronize the oscillator.

Innovative emulated current mode (IECM) is an emulated peak current control topology. SGM61169 ensures reliable performance under both steady-state and dynamic load conditions while eliminating the need for intricate external compensation circuitry. Its control scheme integrates an internal slope compensation mechanism that emulates inductor current information, satisfying the application requirements of low-ESR capacitors such as multilayer ceramic types (MLCC). The integrated ramp compensation circuit enhances immunity to electrical disturbances by maintaining a high SNR (signal-to-noise ratio) in control signals. The device offers three configurable ramp to fine-tune the feedback loop for diverse inductor and capacitor configurations, requiring only a single grounding resistor for adjustment. Designed for simplicity, the regulator minimizes external component requirements while delivering rapid response to load transients. Its fixed-frequency architecture simplifys EMI filter design, ensuring predictable noise suppression and system stability.

## Input Under-Voltage Lockout (UVLO)

An internal UVLO circuit is implemented on the VIN pin to disable the device and prevent malfunction when the input voltage is too low. The internal VIN_UVLO rising threshold is 4V (TYP) with 150mV hysteresis.

## EN Pin and UVLO Programming

The EN pin is used to turn the device on and off. The device starts operation when the EN voltage rises above the enable rising threshold. Pulling the EN voltage below the enable falling threshold stops switching and reduces the device current to the very low quiescent shutdown level. Floating the EN pin will enable the device due to its internal pull-up current source. This current source is used for programming the UVLO threshold. An open-drain or open-collector output connected to the EN pin can be used to control the device.

When the EN pin voltage exceeds its enable threshold and the VIN pin voltage rises above the VIN UVLO threshold, the device initiates its startup sequence: the internal BP5 low-dropout regulator (LDO) is first activated to charge the external BP5 capacitor. Once the BP5 pin voltage exceeds its own UVLO threshold, the device enters a power-on delay phase, during which the resistor configuration parameters on the MODE pin and SYNC/FSEL pin are locked, and the control loop initialization is completed. Following the power-on delay, the output voltage gradually ramps up via the soft-start mechanism to prevent inrush current and ensure stable system startup.

To program a higher UVLO threshold for the VIN, the EN pin can be configured to one of the configurations shown in Figure 3. Without external components, the internal pull-up current ($I_P$) sets the EN pin default state to enable. When the device is enabled, the second current source ($I_H$) is activated. $I_P$ and $I_H$ are used to set the UVLO.

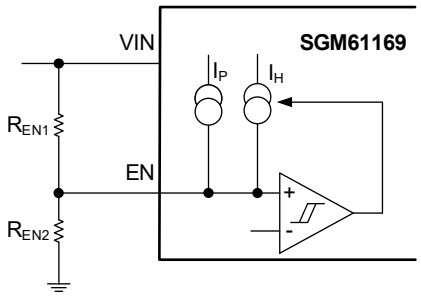



**Figure 3. VIN UVLO Setting with a Resistor Divider**

# DETAILED DESCRIPTION (continued)

The resistor divider can be calculated by Equations 1 and 2 based on the desired UVLO start and stop thresholds.

$$R_{EN1} = \frac{V_{START} \times \left( \frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_P \times \left( 1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_H} \quad (1)$$

$$R_{EN2} = \frac{R_{EN1} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{EN1} \times (I_P + I_H)} \quad (2)$$

where:

$I_H$ = 10.5μA.

$I_P$ = 1.5μA.

$V_{ENRISING}$ = 1.2V

$V_{ENFALLING}$ = 1.1V.

## Output Discharge

The device has built-in discharge circuit. When the device is shut down by EN, VIN UVLO, thermal shutdown or enters hiccup mode, the output capacitor will be discharged through the internal discharge resistor which is typically 66Ω. It should be noted that: When the $V_{IN}$ is less than 2V (TYP) or the $V_{EN}$ is less than 0.8V (TYP), the device does not have discharge capability.

## Soft-Start and Pre-Biased Output

During the startup sequence, the device gradually ramps the reference voltage to minimize inrush current. Four configurable soft-start time are available (0.5ms, 1ms, 2ms, or 4ms), representing the time required for the reference voltage to reach 0.5V of its target value. These soft-start time are set by connecting resistors of specific values between the MODE pin and analog ground. When operating in pre-biased output conditions during startup, the device actively blocks discharging current to prevent energy dissipation from the output. For the initial 16 cycles, it operates in DCM to guarantee a smooth, monotonic voltage rise.

## Power Good (PG)

The PG is an open-drain output. It is released if there is no fault and the FB pin voltage is in regulation. The PG is high impedance state if the FB voltage is between 92% and 108% of the reference voltage. Following soft-start completion, the PG signal transitions to a floating state after a 256μs (TYP) deglitch delay. A 10kΩ to 100kΩ pull-up resistor connected to a voltage rail less than 5.5V is recommended for PG. An option is using the output voltage for PG pull-up. The state of PG is uncertain until $V_{IN}$ > 1.2V. The PG is pulled low if the FB voltage is lower than 84% or above 116% of the reference voltage after a 12μs (TYP) deglitch time. For the SGM61169, the PG pin is driven to a low level during shutdown, VIN UVLO, EN pin is in a low and Thermal Shutdown states .

**Table 1. PG Output State in Different Conditions**

| Device Information | | PG State | |
|---|---|---|---|
| | | High-Z | Low |
| Enable (EN = High) | $V_{FB} \geq V_{PG\_OV}$ | | √ |
| | $V_{FB} \leq V_{PG\_OV}$ | √ | |
| | $V_{FB} \geq V_{PG\_UV}$ | √ | |
| | $V_{FB} \leq V_{PG\_UV}$ | | √ |
| Shutdown by EN | EN = Low | | √ |
| Thermal Shutdown | $T_J > T_{SD}$ | | √ |
| UVLO | $1.2V < V_{IN} < V_{UVLO}$ | | √ |
| Power Supply Removal | $V_{IN} < 1.2V$ | Uncertain | |

## Switching Frequency Setting

The device's switching frequency is programmable by connecting a resistor ($R_{FSEL}$) between the SYNC/FSEL pin and analog ground (AGND). Available frequency options and their corresponding resistor values are specified in Table 2. A resistor with 1% tolerance or better must be used to ensure accurate frequency setting.

**Table 2. Switching Frequency Setting**

| Resistance Range, $R_{FSEL}$ (1%) (kΩ) | Switching Frequency, $f_{SW}$ (kHz) |
|---|---|
| ≥ 24.0 | 500 |
| 17.4 ~ 18.0 | 750 |
| 11.8 ~ 12.1 | 1000 |
| 8.06 ~ 8.25 | 1500 |
| ≤ 5.11 | 2200 |

## Switching Frequency Synchronization to an External Clock

The device supports synchronization to an external clock by applying a 20% to 80% duty square wave signal to the SYNC/FSEL pin, either before startup or during normal operation. In any case, a resistor needs to be connected between this pin and the ground. When synchronizing to an external clock after device startup, the initial synchronization action occurs at only after detecting four sequential switching cycles with valid clock pulses on the SYNC/FSEL pin. And the range of the external clock frequency can not exceed ±20% of the frequency set by the SYNC/FSEL resistor.

## DETAILED DESCRIPTION (continued)

This fault-tolerant validation mechanism ensures stable frequency locking while rejecting transient noise, as shown in Figure 4.

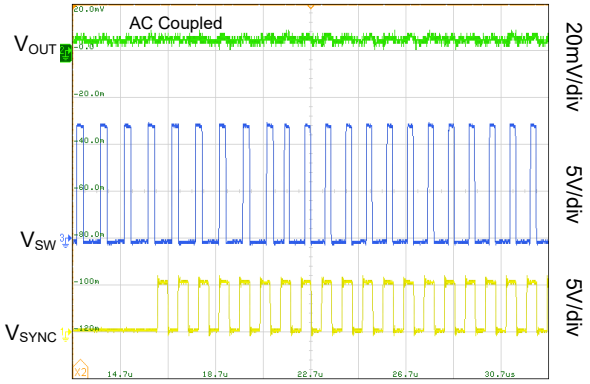



**Figure 4. External Clock Entry**

### Internal PWM Oscillator Frequency

The device synchronizes its switching frequency to an external clock when external clock signal is detected; otherwise, it defaults to the internal PWM oscillator frequency. If starting without an external clock, the internal frequency is set by the $R_{FSEL}$ resistor in Table 2, until external synchronization is applied.

When an external clock is applied before startup, the $R_{FSEL}$ resistor becomes redundant. The internal frequency is auto-configured by decoding the external clock frequency, with mapping relationships provided in Table 3.

**Table 3. Default Frequency Identification**

| External Clock Frequency (kHz) | Default Switching Frequency (kHz) |
|---|---|
| 450 - 550 | 500 |
| 675 - 825 | 750 |
| 900 - 1100 | 1000 |
| 1350 - 1650 | 1500 |
| 1980 - 2420 | 2200 |

### Loss of Synchronization

Once the external synchronization signal is lost during operation, the device reverts to its default PWM oscillator frequency and operates at 70% (TYP) of the internal frequency for four consecutive switching cycles. If no valid external clock pulses are detected within these cycles, the device resumes default frequency operation. The typical waveform is shown in Figure 5.

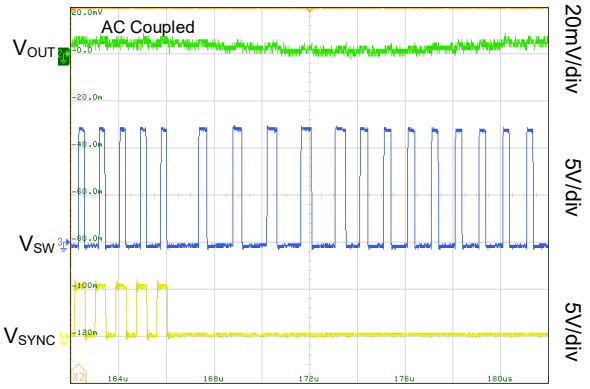



**Figure 5. External Clock Exit**

### Interfacing the SYNC/FSEL Pin

If an external synchronous clock is applied after the device has been powered on, a high-impedance buffer must be used to ensure accurate resistor value detection. The recommended application refers to Figure 6. The buffer leakage current at its output must remain below 5μA to prevent the resistance value of $R_{FSEL}$ from being wrongly identified its power supply should be sourced from the BP5 pin to guarantee stable VCC availability and high-impedance output before $R_{FSEL}$ is sampled. To maintain BP5 LDO stability, the total external load on BP5 (including buffer current) must not exceed 2mA. This configuration isolates external interference during startup, ensuring precise frequency configuration for subsequent clock synchronization.

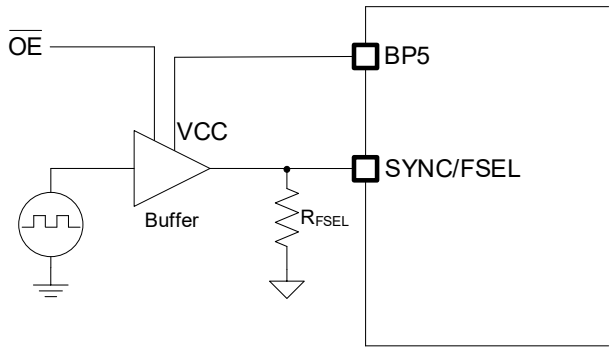



**Figure 6. Buffer Application**

# DETAILED DESCRIPTION (continued)

## Ramp Amplitude Selection

The SGM61169 generates an internal ramp compensation signal by combining VIN, duty cycle, and low-side MOSFET current information. The amplitude of this ramp signal is set by an integrated ramp capacitor ($C_{RAMP}$), which can be configured to three values (1pF, 2pF, or 4pF) by a resistor connected from the MODE pin to AGND. Increasing the ramp capacitor value reduces the ramp signal amplitude, thereby expanding the control loop bandwidth, as shown in Figure 7 and Figure 8.

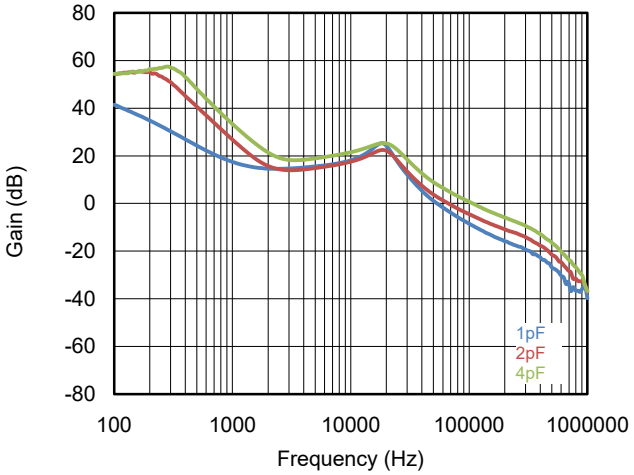



**Figure 7. Loop Gain vs. $C_{RAMP}$ (Application in Figure 9)**

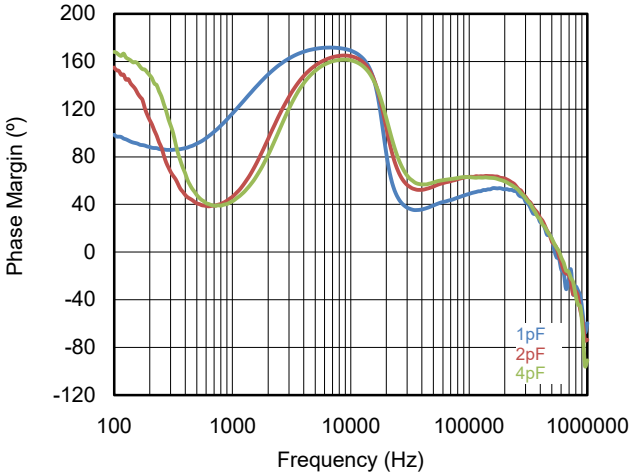



**Figure 8. Loop Phase vs. $C_{RAMP}$ (Application in Figure 9)**

## Mode Pin

The ramp compensation capacitor, soft-start time, and current limit thresholds are programmed by a single resistor ($R_{MODE}$) connected between the MODE pin and analog ground (AGND). Resistor values for available configurations are listed in Table 4, requiring a 1% tolerance resistor or better. For the "High" and "Low" mode current limit thresholds, refer to Over-Current Protection.

**Table 4. MODE Pin Selection**

| $R_{MODE}$ (kΩ) | Current Limits | $C_{RAMP}$ (pF) | Soft-Start Time (ms) |
|---|---|---|---|
| 1.78 | High | 1 | 0.5 |
| 2.21 | High | 1 | 1 |
| 2.74 | High | 1 | 2 |
| 3.32 | High | 1 | 4 |
| 4.02 | High | 2 | 0.5 |
| 4.87 | High | 2 | 1 |
| 5.9 | High | 2 | 2 |
| 7.32 | High | 2 | 4 |
| 9.09 | High | 4 | 0.5 |
| 11.3 | High | 4 | 1 |
| 14.3 | High | 4 | 2 |
| 18.2 | High | 4 | 4 |
| 22.1 | Low | 1 | 0.5 |
| 26.7 | Low | 1 | 1 |
| 33.2 | Low | 1 | 2 |
| 40.2 | Low | 1 | 4 |
| 49.9 | Low | 2 | 0.5 |
| 60.4 | Low | 2 | 1 |
| 76.8 | Low | 2 | 2 |
| 102 | Low | 2 | 4 |
| 137 | Low | 4 | 0.5 |
| 174 | Low | 4 | 1 |
| 243 | Low | 4 | 2 |
| 412 | Low | 4 | 4 |

## Over-Current Protection

Both high-side and low-side switches are protected from over-current with cycle-by-cycle current limiting as explained in the next two sections.

## High-side Switch Over-Current Protection

When the high-side (HS) MOSFET is turned on, a blanking time is applied to suppress noise interference. Then if the HS over-current threshold is exceeded, the HS MOSFET is immediately turned off, and the low-side (LS) MOSFET is turned on. The HS MOSFET remains off until the current drops below the LS MOSFET's over-current threshold, effectively limiting peak current during short-circuit conditions. If an HS over-current event is detected for 15 consecutive cycles, the device enters hiccup mode.

# DETAILED DESCRIPTION (continued)

## Low-side MOSFET Over-Current Protection

When the low-side (LS) MOSFET is turned on, a blanking time is applied to suppress noise interference too. After that, if the inductor current remains above the low-side over-current threshold, the LS MOSFET is kept on. Even the inductor current falls below the low-side over-current threshold, the LS MOSFET is kept on until the next PWM signal arrives, then the HS MOSFET will be turned on.

The positive over-current thresholds for both the high-side (HS) and low-side (LS) MOSFETs are programmable by the MODE pin, offering two selectable levels (“high” and “low”) as described in Table 5. These thresholds are calibrated by using open-loop DC current measurements. In practical operation, however, the inductor current slew rate is governed by the voltage across the inductor and its inductance value. This slew rate, combined with propagation delays in the current-sense circuitry, may cause slight deviations between actual triggering currents and the specified thresholds. In light of above factors, the HS over-current limit is slightly higher than the DC value, while the LS limit slightly lower than its DC value.

**Table 5. Current Limit Value (DC)**

| Mode Pin Current Limit Setting | High-Side Over-Current Typical Value (A) | Low-Side Over-Current Typical Value (A) |
|---|---|---|
| High | 9.0 | 7.3 |
| Low | 4.5 | 3.9 |

## Negative Inductor Current Protection

The device also has negative inductor current protection. Whenever the negative over-current threshold of the LS MOSFET is exceeded, the LS MOSFET is immediately turned off. The current will flow through the body diode of HS MOSFET. Similar to the positive inductor current protection, the actual negative inductor current limit may be slightly more negative than the DC threshold.

## Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The SGM61169 integrates output over-voltage protection (OVP) and under-voltage protection (UVP).

During an OVP event, the device rapidly reduces the output voltage to a safe level by turning on the low-side MOSFET until the negative current threshold is reached, then the current flow through the body diode of HS MOSFET. The switching frequency becomes half of the default frequency, and LS is turned on again at next clock. This process repeats cyclically until the $V_{FB}$ falls below 108% (TYP) of $V_{REF}$. Once this condition is met, the device restarts immediately and executes a soft-start cycle.

When an under-voltage condition is detected, the device enters hiccup mode immediately, then it waits for seven soft-start cycles before attempting a restart. The OVP and UVP protection is enabled only after the soft-start sequence completes.

## Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds $T_{SD}$, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 12℃ below the $T_{SD}$.

# APPLICATION INFORMATION

In this section, power supply design with the SGM61169 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

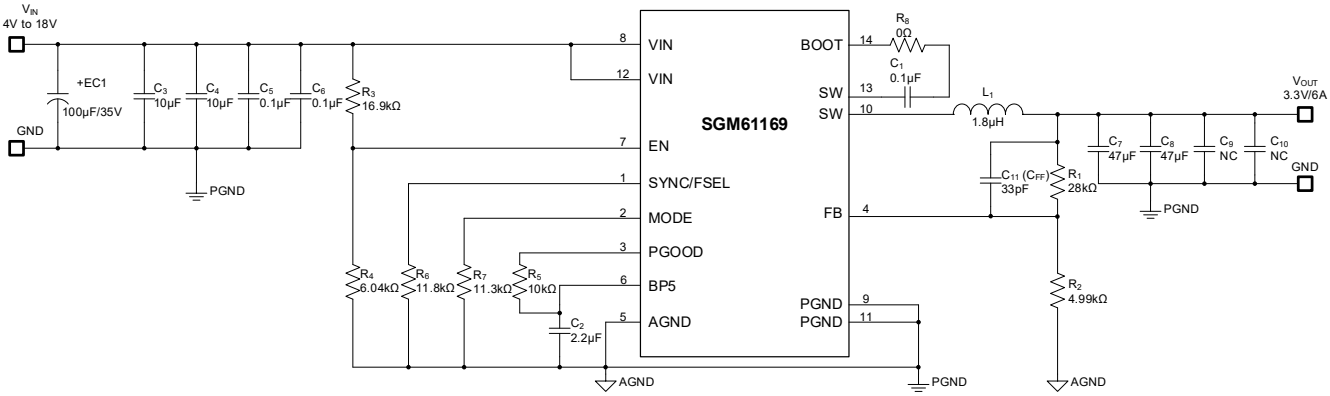



**Figure 9. 3.3V Output Voltage Application**

## Design Requirements

Table 6 summarizes the requirements for this example as shown in Figure 9. The selected components are given in Table 7.

**Table 6. Design Parameters for the Application Example**

| Design Parameter | Example Value |
|---|---|
| Input Voltage | 4V to 18V |
| Output Voltage | 3.3V |
| Output Current | ≤ 6A |
| Switching Frequency | 1000kHz |
| Steady State Output Ripple Voltage | 10mV |

**Table 7. Selected Components for the Design Example**

| Ref | Description | Manufacturer |
|---|---|---|
| $C_1$, $C_5$, $C_6$ | 0.1μF, 50V, X7R, 0402 | muRata |
| $C_2$ | 2.2μF, 10V, X7R, 0603 | muRata |
| $C_3$, $C_4$ | 10μF, 25V, X7S, 0805 | muRata |
| $C_7$, $C_8$ | 47μF, 10V, X5R, 0805 | muRata |
| $C_{11}$ | 33pF, 50V, C0G, 0402 | muRata |
| $L_1$ | 1.8μH Wire Wound, $DCR_{MAX}$ = 7.1mΩ, $I_{SAT(30\%)}$ = 13.5A, $I_{RMS(40℃)}$ = 12A, 6.4mm × 6.6mm × 4.8mm, P/N: MWFC0605S-1R8MT | Sunlord |
| $R_1$ | 28kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_2$ | 4.99kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_3$ | 16.9kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_4$ | 6.04kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_5$ | 10kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_6$ | 11.8kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_7$ | 11.3kΩ, Chip Resistor, 1%, 0402 | Standard |
| $R_8$ | 0Ω, Chip Resistor, 1%, 0402 | Standard |

NOTE: If the long input power cable is used, or the input voltage is on/off by air-break switch, EC1 should be installed.

## Switching Frequency Selection

The switching frequency of the regulator is configurable within a range (500 kHz to 2.2 MHz) and typically set via an external resistor connected to a dedicated frequency-select (SYNC/FSEL) pin. Higher switching frequency can minimize solution size by using smaller inductor and output capacitors. Meanwhile, a higher switching frequency is adapted to a higher loop bandwidth and a faster dynamic response. However, higher frequencies will increase switching losses and reduce efficiency.

In low output voltage applications, the maximum achievable frequency is limited by the regulator's minimum controllable on-time, which can be calculated by Equation 3.

$$f_{SW\_MAX} = \frac{1}{t_{ON\_MIN}} \times \frac{V_{OUT}}{V_{IN\_MAX}} \quad (3)$$

where:

$f_{SW\_MAX}$ is maximum switching frequency (MHz) limited by min-on time of HS.

$t_{ON\_MIN}$ is the minimum min-on time (μs) of HS.

$V_{IN\_MAX}$ is the maximum input DC voltage.

The relationship between the maximum input voltage and output voltage at different switching frequencies is shown in Figure 10.

## APPLICATION INFORMATION (continued)

When the load is light, the dead time between LS MOSFET turning off and HS MOSFET turning on can extend $t_{ON\_MIN}$. Thus in Figure 10, the value of $t_{ON\_MIN}$ is set to 45ns, and the 10% fluctuation range of the switching frequency is also taken into account. In practical applications, when choosing the switching frequency, it is also necessary to reserve some margin for closed-loop regulation.

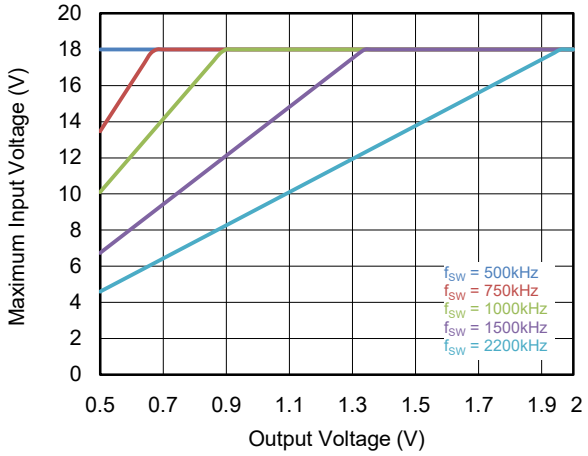



**Figure 10. Maximum Input Voltage Limit by $t_{ON\_MIN}$**

In high output voltage applications, the maximum achievable frequency is limited by the regulator's minimum controllable off-time. If exceeded, the duty cycle saturates, causing the output voltage to track input voltage drops. In this case, the maximum switching frequency needs to be calculated according to Equation 4. Based on the calculation results, sufficient margin must be reserved as the tolerance of the switching frequency.

$$f_{SW\_MAX} = \frac{V_{IN\_MIN} - V_{OUT} - I_{OUT\_MAX} \times (R_{DCR} + R_{DSON\_HS})}{t_{OFF\_MIN} \times \left(V_{IN\_MIN} - I_{OUT\_MAX} \times (R_{DSON\_HS} - R_{DSON\_LS})\right)} \quad (4)$$

where:

$f_{SW\_MAX}$ is maximum switching frequency (MHz) limited by min-off time of HS.

$V_{IN\_MIN}$ is the minimum input DC voltage.

$I_{OUT\_MAX}$ is the maximum output DC current.

$R_{DCR}$ is the DC resistance value (Ω) of the inductor.

$R_{DSON\_HS}$ is the high-side MOSFET on-resistance (Ω)

$R_{DSON\_LS}$ is the low-side MOSFET on-resistance (Ω)

$t_{OFF\_MIN}$ is the minimum min-off time (μs) of HS.

### Input Capacitor Selection

Use ceramic capacitors (X5R, X7R, or equivalent) for decoupling between the VIN and PGND pins. These capacitors must be placed as close as possible to the IC. Applications with long input traces or transient load demands may need additional bulk capacitance. For high-frequency noise suppression, 0.01μF to 0.1μF capacitors must be positioned directly adjacent to critical VIN pins (pins 8 and 12) on the same board layer as the IC. The capacitor's voltage rating must exceed the maximum input voltage. The ripple current rating of capacitors must exceed the calculated maximum input RMS capacitor current, derived from the regulator's operating parameters, which can be calculated by Equation 5. In most cases, two 10μF, 25V, X7S (0805 package) and two 0.1μF, 50V, X7R (0402 package) capacitors in parallel provide effective decoupling. A larger value reduces input voltage ripple and improve system stability. Ceramic capacitance decreases under DC bias. For example, 10μF capacitors decay to 5.4μF at 12V input. The input ripple voltage depends on the input capacitance, switching frequency, and duty cycle. Worst-case ripple occurs near 50% duty cycle. It can be calculated by Equation 6.

$$I_{C\_RMS} = I_{OUT\_MAX} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \quad (5)$$

where:

$I_{C\_RMS}$ is the maximum RMS current of capacitor.

$I_{OUT\_MAX}$ is the maximum output DC current.

$V_{IN\_MIN}$ is minimum input voltage.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}}{C_{IN} \times f_{SW}} \quad (6)$$

where:

$\Delta V_{IN}$ is the input ripple voltage (peak-to-peak).

$I_{OUT\_MAX}$ is the maximum output DC current.

$C_{IN}$ is the effective input capacitance value (μF)

$f_{SW}$ is switching frequency (MHz).

# APPLICATION INFORMATION (continued)

## Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. $I_{SAT}$ should be higher than $I_{L\_MAX}$, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 7 can be used to choose the inductance value based on $\Delta I_{L.}$. Please pay attention to avoid triggering the negative current limit protection when the device is operating at no load.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (7)$$

where:

$I_{OUT\_MAX}$ is the maximum output DC current.

$\Delta I_L$ is the inductor current ripple (peak-to-peak).

$f_{SW}$ is switching frequency (MHz).

L is the inductance value (μH).

## Output Capacitor Selection

The selection of output capacitors must address two primary criteria: output voltage ripple and load transient response performance. The final capacitance value should meet these two requirements.

During load current transients (rapid step-up/ step-down), the control loop cannot adjust the power stage instantaneously. The output capacitor temporarily acts as a charge buffer to stabilize the output voltage. System response speed is limited by the loop bandwidth (typically 1/10 of the switching frequency). The output voltage deviation under load transients can be estimated using:

$$C_{OUT\_MIN} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{SW}}{10}} \quad (8)$$

where:

$C_{OUT\_MIN}$ is the minimum effective output capacitance value (μF) that meets the requirements of output voltage change.

$\Delta I_{OUT}$ is the load step current.

$\Delta V_{OUT}$ is the output voltage change while load transient.

$f_{SW}$ is switching frequency (MHz).

When ceramic capacitors are used at the output, the voltage drop across their ESR is small enough to be considered negligible.

When the device operates in a low duty cycle condition, the time it takes for the inductor current to decrease after the load drops will affect the overshoot of the output voltage.

Equation 9 can be used to estimate the minimum value of the output capacitor to limit the output voltage overshoot after a step-down load.

$$C_{OUT\_MIN} > \frac{L \times \Delta I_{OUT}^{\ 2}}{2 \times \Delta V_{OUT} \times V_{OUT}} \quad (9)$$

where:

$C_{OUT\_MIN}$ is the minimum effective output capacitance value (μF) that meets the requirements of output voltage change.

$\Delta I_{OUT}$ is the load step current.

$\Delta V_{OUT}$ is the output voltage change while load transient.

L is the inductance value (μH).

Steady-state output ripple voltage depends on inductor current ripple and capacitor impedance. For ceramic capacitors with low ESR, the minimum capacitance requirement is:

$$C_{OUT\_MIN} \geq \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT}} \quad (10)$$

where:

$C_{OUT\_MIN}$ is the minimum effective output capacitance value (μF) that meets the requirements of output voltage ripple.

$\Delta I_L$ is the inductor current ripple (peak-to-peak).

$f_{SW}$ is switching frequency (MHz).

$\Delta V_{OUT}$ is the output ripple voltage (peak-to-peak).

The inductor (L) and the output capacitor ($C_{OUT}$) form a low-pass filter. Note that variations as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the $C_{OUT}$, due to tolerances, temperature and bias voltage derating the effective capacitance can vary by +20% to -50%, which must be taken into account for application.

Even if there are no strict requirements for load transient response or output voltage ripple in the application. A minimum capacitance is mandatory for loop stability:

# APPLICATION INFORMATION (continued)

$$C_{OUT\_MIN} > \left(\frac{Ratio}{2\pi \times f_{SW}}\right)^2 \times \frac{1}{L} \quad (11)$$

where:
$C_{OUT\_MIN}$ is the minimum effective output capacitance value (μF) that meets the requirements of loop stability.
Ratio is the minimum ratio of the switching frequency to the LC frequency. Refer to Figure 11.
$f_{SW}$ is switching frequency (MHz).
L is the inductance value (μH).

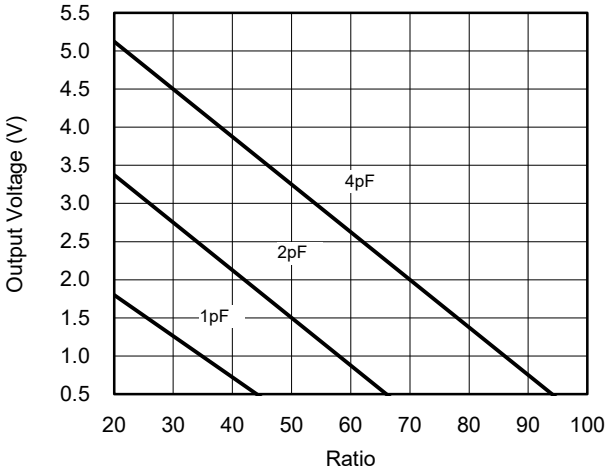



**Figure 11. $C_{RAMP}$ Applicable Range**

## Output Voltage Adjustment

Use Equation 12 for selecting the feedback resistors ($R_1$ and $R_2$) in Figure 9 to set the desired output voltage ($V_{OUT}$):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.5V \times \left(1 + \frac{R_1}{R_2}\right) \quad (12)$$

First choose $R_2$ value below 4.99kΩ to avoid high noise sensitivity on the FB pin. The smaller the $R_2$ resistance value is, the stronger the anti-noise ability will be, but at the same time, the loss on the voltage divider will also be greater.

## Ramp Configuration and Loop Compensation Design

The ramp setting is adjustable via a dedicated mode pin, typically offering three configurations (1pF, 2pF, 4pF). Optimal selection depends on output voltage, switching frequency, inductor (L) and output capacitor values. The ratio is:

$$Ratio = f_{SW} \times 2\pi\sqrt{L \times C_{OUT}} \quad (13)$$

where:
Ratio is the minimum ratio of the switching frequency to the LC frequency.
$f_{SW}$ is switching frequency (MHz).
L is the inductance value (μH).
$C_{OUT}$ is the effective output capacitance value (μF).

Take 1V output as an example.

Low Ratio (35-58): Use smaller ramp capacitance (1pF).
Mid Ratio (58-86): Use medium ramp capacitance (2pF).
High Ratio (>86): Use larger ramp capacitance (4pF).

When the Ratio is maintained, the larger the ramp capacitor is, the faster the transient response will be. However, it is necessary to ensure the stability margin of the system.

A feedforward capacitor ($C_{FF}$) introduces a zero and a pole in the control loop to enhance phase margin. The pole frequency is higher than the zero frequency and the ratio of them is fixed. Calculate $f_{ZERO}$:

$$f_{ZERO} = \frac{1}{2\pi R_1 C_{FF}} \quad (14)$$

When the value of R1 remains unchanged, increasing $C_{FF}$ can optimize the transient response. But excessively large $C_{FF}$ injects output noise into the feedback (FB) pin, increasing switching jitter.

## Bootstrap Capacitor

To maintain stable switching behavior, implement a 100nF ceramic capacitor across the BOOT-SW pins, the rated voltage of the capacitor is not less than 10V. The switching speed of the HS MOSFET can be reduced by inserting a current-limiting resistor in the bootstrap path. Although this application can reduce the overshoot of the SW node when the HS MOSFET is turning on, it introduces measurable efficiency degradation due to increased conduction losses. It is recommended to retain a 0Ω resistor during the design process, so that the resistance value can be changed later for adjusting the switching speed.

# APPLICATION INFORMATION (continued)

## Current Limit Setting

The MODE pin configures operational thresholds for current limit. When determining appropriate protection levels, the baseline threshold should exceed peak operating currents by ≥10% under worst-case conditions. It is necessary to reserve design margins not only for tolerance of inductor, but also for load transient conditions.

## Soft-Start Time Setting

The MODE pin can configure soft-start time through a programmable startup time. Extending the startup time can alleviate the inrush current demand during the capacitor charging stage, prevent the input rail voltage from dropping and avoid startup failure caused by large output capacitors.

## Additional Output Voltage Application

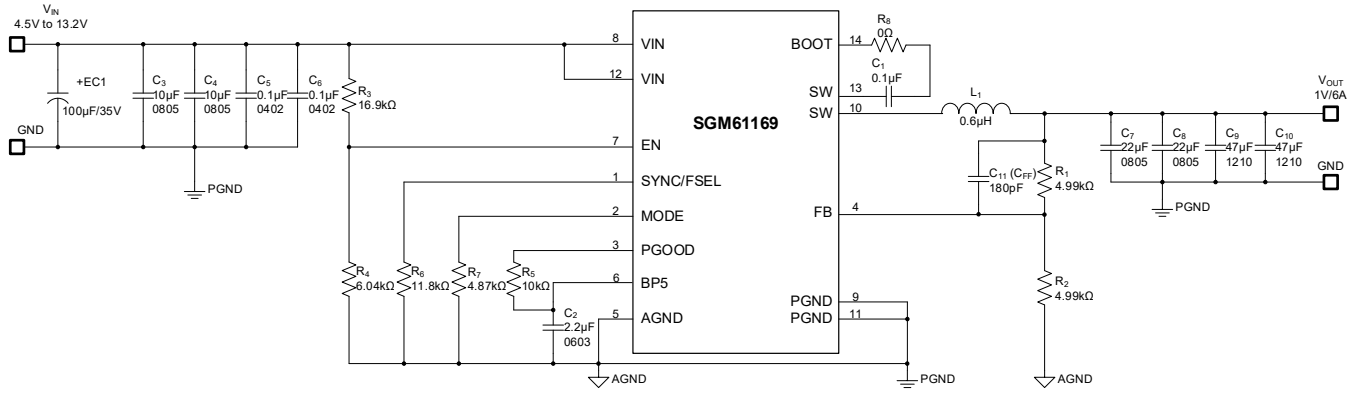



**Figure 12. 1V Output Voltage Application**

## Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61169.

- Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- To achieve the best power integrity, place the 10nF ~ 100nF low ESR decoupling capacitor as close as possible to the VIN-PGND pin on each side. Place the remaining input capacitors closer to them. It is not recommended to place the remaining input capacitors on another layer of PCB. If such a situation occurs, it is suggested to use sufficient vias near them to reduce the impedance between them and the IC.
- Connect to the VIN network of other layers through vias near the VIN pins on both sides to reduce impedance.
- Place the inductor as close as possible to pin 10 to reduce the length of the SW node route and thereby improve EMI performance.
- Connect the ground returns of the input and output capacitors close to the PGND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.
- Keep the output voltage sense trace, SYNC/FSEL pin and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node or the high-frequency signal line from another system to avoid magnetic and electric noise coupling.
- Use multiple vias near the PGND pin to connect the PGND copper-clad networks of each layer directly beneath the chip together to facilitate noise reduction and heat dissipation.
- The AGND pin must be connected to the PGND network only through a few relatively concentrated vias. These vias cannot be too far from the AGND pin.
- Place the BOOT-SW capacitor as close as possible to the BOOT (pin 14) and SW (pin 13), and the same applies to BP5 and AGND pins.
- The lower resistor of FB, the FSEL resistor, and the MODE resistor need to be connected with AGND island.

## APPLICATION INFORMATION (continued)

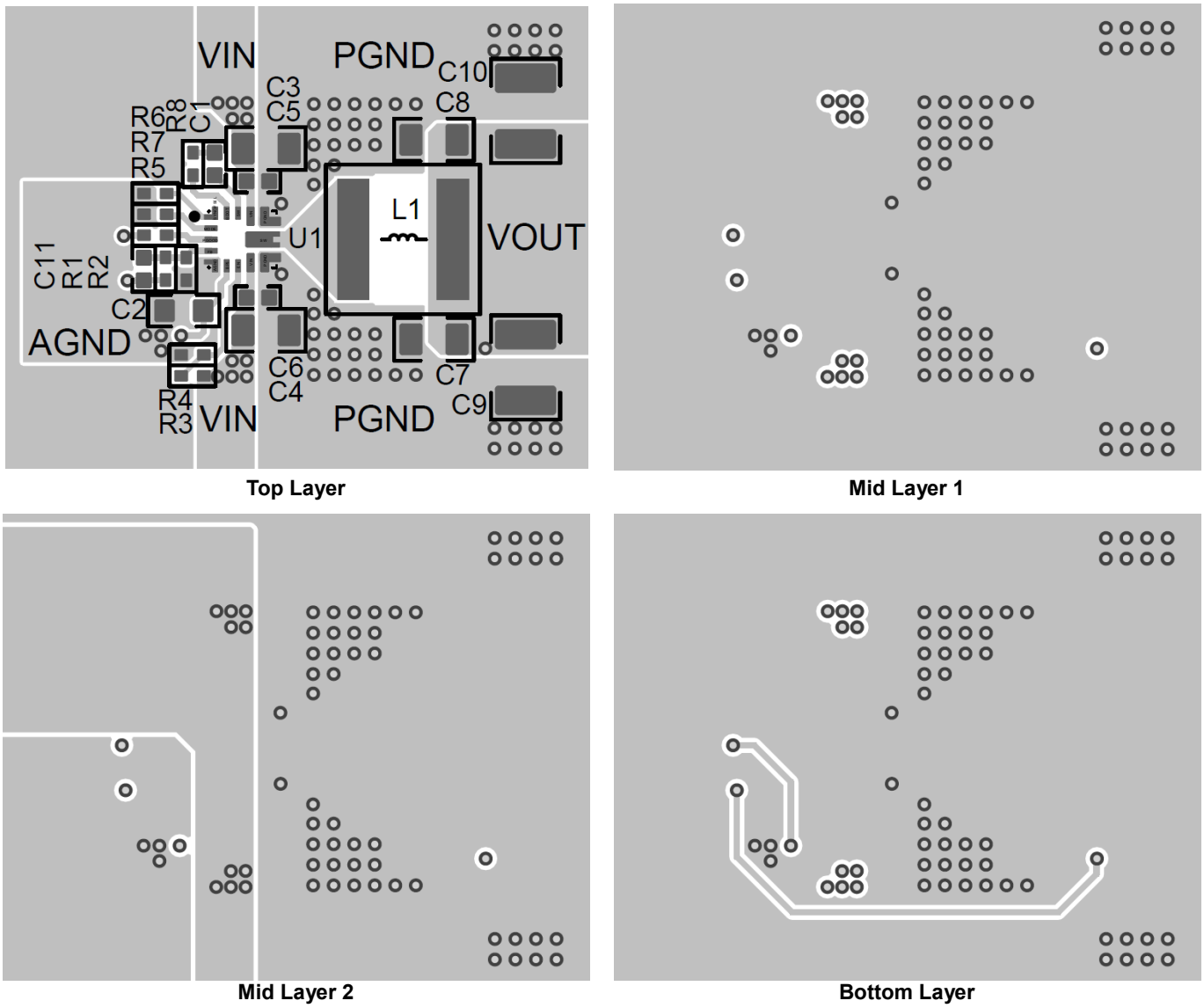



**Figure 13. PCB Layout**

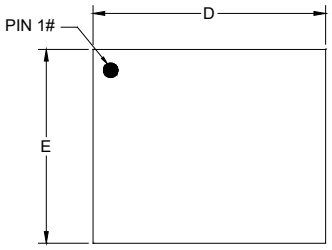
## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

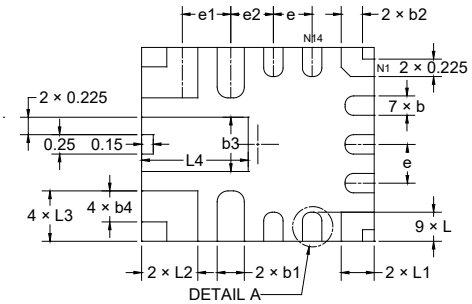
| Changes from Original to REV.A (DECEMBER 2025) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

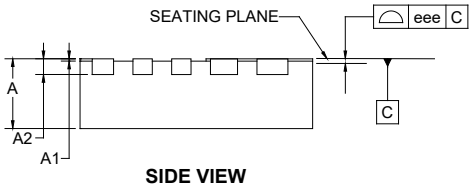
## TQFN-3×2.5-14L




TOP VIEW

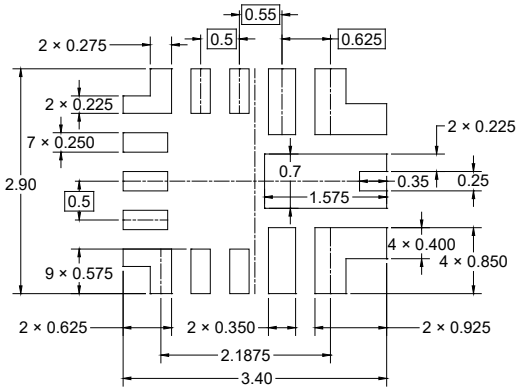



BOTTOM VIEW




SIDE VIEW


**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTION



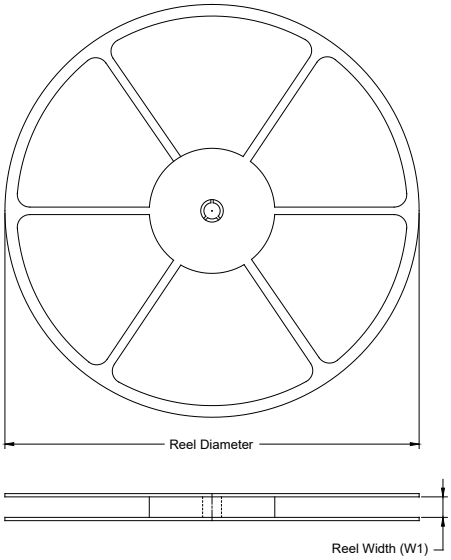

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.800 | - | 1.000 |
| A1 | 0.000 | - | 0.050 |
| A2 | | 0.203 REF | |
| b | 0.200 | - | 0.300 |
| b1 | 0.300 | - | 0.400 |
| b2 | 0.225 | - | 0.325 |
| b3 | 0.650 | - | 0.750 |
| b4 | 0.350 | - | 0.450 |
| D | 2.900 | - | 3.100 |
| E | 2.400 | - | 2.600 |
| e | | 0.500 BSC | |
| e1 | | 0.625 BSC | |
| e2 | | 0.550 BSC | |
| L | 0.275 | - | 0.475 |
| L1 | 0.325 | - | 0.525 |
| L2 | 0.625 | - | 0.825 |
| L3 | 0.550 | - | 0.750 |
| L4 | 1.275 | - | 1.475 |
| eee | | 0.080 | |

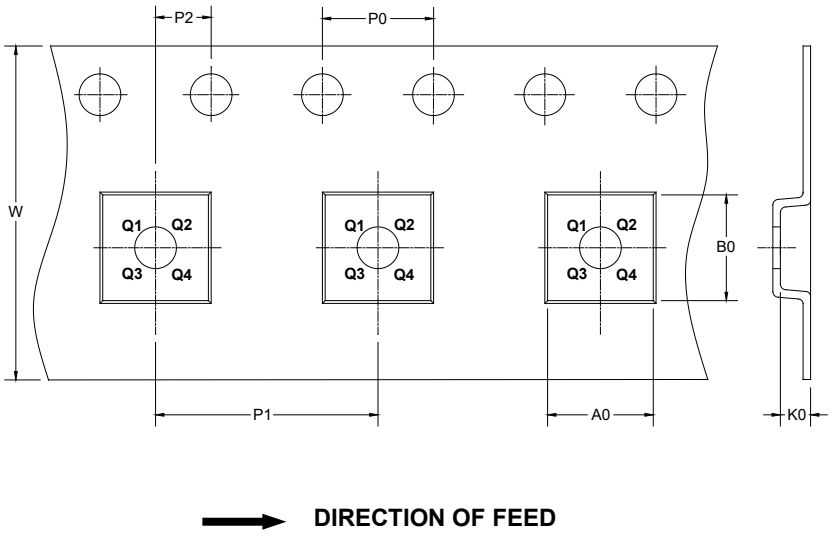
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




DIRECTION OF FEED

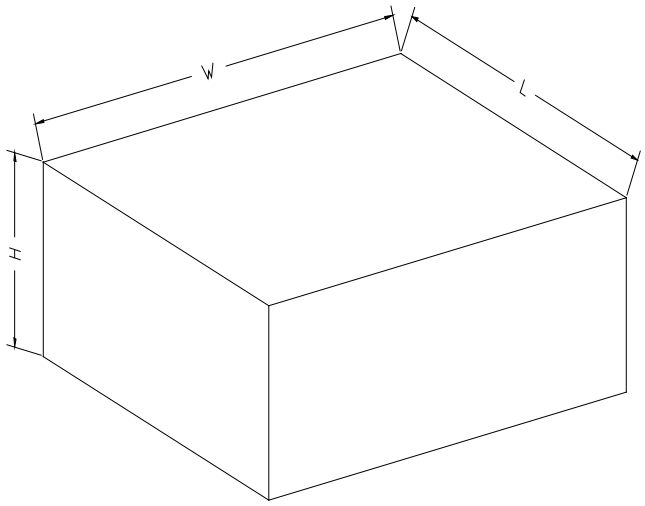
NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TQFN-3×2.5-14L | 13" | 12.4 | 2.80 | 3.30 | 1.20 | 4.0 | 8.0 | 2.0 | 12.0 | Q2 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002