

# **SGM2537 4A, 35mΩ eFuse with Selectable Over-Voltage Clamping Function**

## **GENERAL DESCRIPTION**

The SGM2537 family is a compact electronic fuse (eFuse) with circuit protection functions, which can be used as a solution to power management. The FET hot-swap device is also highly integrated in a small package. With very few external components, the SGM2537 can provide multiple protection modes. To encounter overloads, voltage surges, short-circuits and high inrush current, the device is suitable as a robust defense.

A single external resistor can be used to set the output current limit, and after detecting the voltage drop across the resistor, it is possible to monitor the load current accurately. Also, a single external capacitor is enough to set the output slew rate for applications with particular inrush current requirements. Using internal clamping circuits alone can quickly limit over-voltage events to a fixed maximum value within a safe range. The SGM2537-PRN variant provides an option to set a user-defined over-voltage cutoff threshold.

The SGM2537 is available in a Green TDFN-2×2-8AL package.

# **FEATURES**

- **Input Voltage: 2.7V to 18V, Surge up to 20V**
- **Low On-Resistance: 35mΩ (TYP)**
- **Output Clamp Response Time: 5μs (TYP)**
- **Programmable Current Limit: 0.5A to 4A**
- **±7.5% Current Limit Accuracy**
- **Load Current Monitor Output**
- **Quick Output Discharge (SGM2537-xRD)**
- **Programmable Soft-Start Time (SS)**
- **Over-Temperature Protection (OTP)**
- **Fault Flag (nFAULT Pin)**
- **UL Recognized Component (File No. E532373\*)**
- **Available in a Green TDFN-2×2-8AL Package**

## **APPLICATIONS**

Hot-Swap and Hot-Plug Adapter Power Devices SSD and HDD Drives Set-Top Boxes Printers White Goods Digital TVs



## <span id="page-0-0"></span>**SELECTABLE MODEL**



## **PACKAGE/ORDERING INFORMATION**



### **MARKING INFORMATION**

NOTE: XXXX = Date Code, Trace Code and Vendor Code.

- Trace Code Vendor Code - Date Code - Year **X X X X Y Y Y** Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.



#### **ABSOLUTE MAXIMUM RATINGS**

Pin Voltage Range



#### **RECOMMENDED OPERATING CONDITIONS**



#### NOTES:

1. It is recommended to limit the nominal input voltage according to the output clamp voltage.

2. When supply voltages are below 6V, the EN/UVLO and IN pins can be connected directly. When supply voltages exceed 6V, a suitable resistor divider should be used from IN, EN/UVLO to GND pin. This resistor is used to guarantee that the EN/UVLO pin voltage is within the set limits.

3. Guaranteed by design, not by tests at production.

#### **OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

#### **ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

#### **DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.



## **PIN CONFIGURATIONS**



## **PIN DESCRIPTION**





# **ELECTRICAL CHARACTERISTICS**

(T」= -40℃ to +125℃, V<sub>IN</sub> = 12V for SGM2537-13.7x/Ux/PRN, V<sub>IN</sub> = 5V for SGM2537-5.7x/5.7RD/5.7RN, V<sub>IN</sub> = 3.3V for SGM2537-3.8x/3.8RD, V $_{\rm EN}$  = 5V (0V for SGM2537-xRN only), R $_{\rm ILIM}$  = 1000Ω, C $_{\rm SS}$  = Open, OUT = Open, typical values are at T $_{\rm J}$  = +25℃, unless otherwise noted.)





## **ELECTRICAL CHARACTERISTICS (continued)**

(T $_{\rm J}$  = -40℃ to +125℃, V<sub>IN</sub> = 12V for SGM2537-13.7x/SGM2537-Ux, V<sub>IN</sub> = 5V for SGM2537-5.7x/5.7RD/5.7RN, V<sub>IN</sub> = 3.3V for SGM2537-3.8x/3.8RD, V<sub>EN</sub> = 5V, R<sub>ILIM</sub> = 1000Ω, C<sub>SS</sub> = Open, OUT = Open, typical values are at T」 = +25℃, unless otherwise noted.)



NOTES:

1. Takes the values based on 4σ.

2. Guaranteed by design, not by tests at production.



## **SWITCHING CHARACTERISTICS**

(R<sub>OUT</sub> = 100Ω, C<sub>OUT</sub> = 1μF, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)





# **TYPICAL PERFORMANCE CHARACTERISTICS**



# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



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# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



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# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, R<sub>ILIM</sub> = 487Ω, unless otherwise noted.















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# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, R<sub>ILIM</sub> = 487Ω, C<sub>OUT</sub> = 1µF, unless otherwise noted.



# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

T<sub>A</sub> = +25°C, R<sub>ILIM</sub> = 487Ω, C<sub>OUT</sub> = 1μF, nFAULT= 3.3V through 10kΩ, unless otherwise noted.













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# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

T<sub>A</sub> = +25°C, R<sub>ILIM</sub> = 487Ω, C<sub>OUT</sub> = 1μF, nFAULT= 3.3V through 10kΩ, unless otherwise noted.





## **FUNCTIONAL BLOCK DIAGRAM**



NOTES:

- 1. SGM2537-Ux/PRN does not include this block.
- 2. For SGM2537-xRD, this pin is QOD.
- 3. For SGM2537-xRN, this pin is nEN/OVLO.
- 4. For SGM2537-xRN, this voltage is OVLO.

#### **Figure 1. Block Diagram**



## **DETAILED DESCRIPTION**

#### **Overview**

SGM2537 is an integrated eFuse, which ensures the safety of the power delivery system due to its rich features. The device has many user- or factory-adjustable settings to suit the needs of different application scenarios. The device can be used to protect downstream equipment from input voltage fluctuations and over-current events, while a thermal shutdown mechanism is integrated to protect the device itself during fault conditions.

### **Under-Voltage Protection (UVP) and Under-Voltage Lockout (UVLO)**

SGM2537 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage  $(V_{UVP})$  is provided inside the device for under-voltage protection. During start-up, if the  $V_{IN}$ voltage exceeds  $V_{UVP(R)}$ , the device turns on the FET. During the on-process, if the VIN voltage is lower than  $V_{UVP(F)}$ , the device shuts down the FET. There is a hysteresis between the rising threshold and falling threshold of UVP.

For the SGM2537, the UVLO comparator on the EN/UVLO pin can be used to set the user-adjustable under-voltage lockout threshold through the external resistance voltage divider. [Figure 2](#page-17-0) shows how to set the specific value of under-voltage lockout threshold using an external resistance voltage divider. There is a hysteresis between the rising threshold and falling threshold of UVLO.



**Figure 2. Under-Voltage Lockout**

#### <span id="page-17-0"></span>**Over-Voltage Protection**

The SGM2537 devices provide two ways to implement input over-voltage protection.

#### **Over-Voltage Lockout (OVLO)**

The SGM2537-xRN can implement user-programmable input over-voltage threshold through an external resistor divider. When the power supply voltage exceeds a certain level, the device turns off the supply to the load. The resistance divider feeds the divided voltage of the power supply to the nEN/OVLO pin. When the voltage at the nEN/OVLO pin exceeds the threshold  $V_{\text{OVLO}}$ , the FET is disabled. When the voltage at the nEN/OVLO pin falls below the threshold, the FET is turned ON.

The user needs to determine the appropriate resistance divider in order to correctly map the over-voltage threshold of the input voltage to the internal threshold V<sub>OVLO</sub>.



**Figure 3. Over-Voltage Lockout**

#### **Over-Voltage Clamp (OVC)**

The SGM2537-3.8x/3.8RD, SGM2537-5.7x/5.7RD/5.7RN and SGM2537-13.7x devices provide the over-voltage clamp (OVC) function which continuously monitors the input voltage and ensures the output clamp voltage to  $V_{CLAMP}$  level within a very short time  $t_{OVC}$  once the input voltage exceeds the over-voltage clamp threshold V<sub>OVC</sub>.

When the input voltage falls below the over-voltage clamp threshold  $V_{\text{OVC}}$ , the clamp will release the output voltage, which can protect the safety of output device, and continuous output clamping condition usually results in thermal shutdown as shown in [Figure 4.](#page-18-0) Once the junction temperature exceeds +156℃, the power MOSFET will be turned off by the thermal shutdown circuitry. For SGM2537-xL, if the power supply or EN/UVLO is reset (pulled low and then pulled up), the device tries to turn on the power MOSFET again. For SGM2537-xR/xRD/xRN, the device is designed with an auto-retry cycle after device temperature drops by  $T_{HYS}$ and an additional delay of  $t_{TSD-RST}$ . Unless the fault is removed, the auto-retry cycle will be continued.



## **DETAILED DESCRIPTION (continued)** VIMO EN



<span id="page-18-0"></span>**Figure 4. SGM2537-xR/xRD/5.7RN Over-Voltage Clamp Response (Auto-Retry)**

As is shown in [SELECTABLE MODEL,](#page-0-0) multiple device options apply to different clamping voltage thresholds.

#### **Inrush Current, Over-Current and Short-Circuit Protections**

SGM2537 adopts three levels of forward over-current protection function:

1. Adjustable slew rate (SS) for inrush current protection.

2. Adjust threshold (ILIM) for over-current in steady state or start-up.

3. Adjust threshold  $(I_{SC})$  for severe over-current such as hard short-circuits in steady state or start-up.

#### **Slew Rate and Inrush Current Control (SS)**

When hot plugging or system charging large capacitive load occurs, the equipment power path will generate a large inrush current. The inrush current is proportional to the load capacitance and the output voltage slew rate. For a given load capacitance  $C_{\text{OUT}}$ , the relationship between the slew rate  $(SR_{ON})$  and inrush current ( $I_{INRUSH}$ ) is shown in Equation 2.

$$
SR_{ON}(V/ms) = \frac{I_{INRUSH}(mA)}{C_{OUT}(\mu F)}
$$
 (2)

The slew rate can be controlled by connecting a capacitor at the SS pin to lower inrush current. For a given slew rate, the corresponding  $C_{SS}$  can be calculated by Equation 3.

$$
C_{SS}(pF) = \frac{33000}{SR_{ON}(V/ms)}
$$
 (3)

#### **Active Current Limit**

The device will actively monitor the load current in both start-up and normal mode. When the load current rises to the over-current threshold  $I_{LIMIT}$  set by  $R_{LIM}$ , the device adjusts the FET to restrict the load current to  $I_{LIMIT}$  in the time of  $t_{LIM}$ . When the load current falls below the current limit, the device exits the current limit. Given a desired current limit  $I_{LIMIT}$ , the value of  $R_{ILM}$  can be calculated from Equation 4.

$$
R_{ILIM} = \frac{1998}{(l_{LIMIT} - 0.03)}
$$
 (4)

During the active current limit, there is more power dissipation on the device because the output voltage drops. If the internal temperature  $(T_1)$  of the device exceeds the thermal shutdown threshold  $(T_{SD})$ , the FET will be turned off, and the device will either be latched off (SGM2537-xL) or restarted automatically after a certain time interval (SGM2537-xR/xRD/xRN) as shown in the OTP section.



**Figure 5. SGM2537-xR/xRD/xRN Over-Current Response (Auto-Retry)**



## **DETAILED DESCRIPTION (continued)**



#### **Short-Circuit Protection**

When a serious over-current event similar to a short-circuit event occurs, the SGM2537 triggers a fast-trip response and limits the current to  $I_{LIMIT}$  in order to prevent the system from being damaged by excessive current flowing through the device. When the current falls below the current limit  $I<sub>LIMIT</sub>$ , the device exits the current limit. If the fault persists, the device continues to operate in the current limit mode, causing the internal temperature of the device to rise until the thermal shutdown. Thereafter, the device will either be latched off (SGM2537-xL) or restarted automatically after a certain time interval (SGM2537-xR/xRD/xRN) as shown in the OTP section.



**Figure 7. SGM2537 Short-Circuit Response**

#### **Over-Temperature Protection (OTP)**

The SGM2537 always monitors the temperature  $(T_1)$  of the internal die. Once the internal temperature exceeds the thermal shutdown threshold  $(T_{SD})$ , the device shuts down immediately. When SGM2537-xL triggers the thermal shutdown, it still remains in the shutdown state unless the equipment is power cycled or re-enabled. When SGM2537-xR/xRD/xRN triggers the thermal shutdown, it remains in the shutdown state until the internal temperature of the equipment drops by  $T_{HYS}$ . After that, it will retry to turn on automatically after a  $t_{RST}$ delay time if it is still enabled. See [Table 1.](#page-19-0)

<span id="page-19-0"></span>**Table 1. SGM2537 Thermal Shutdown**

<b>Device</b>	Enter $T_{SD}$	$Ext T_{SD}$
SGM2537-xL (Latch-Off)	$T_{\rm d} \geq T_{\rm SD}$	$T_{\rm J}$ < $T_{\rm SD}$ , device power cycled or re-enabled (with EN/UVLO pin)
SGM2537-xR/xRD/xRN (Auto-Retry)	$T_1 \geq T_{SD}$	$T_J < T_{SD}$ - $T_{HYS}$ , $t_{TSD-RST}$ timer expired

#### **nFault Indication (nFAULT)**

[Table 2](#page-20-0) shows the protection response of equipment under different fault conditions. The SGM2537 provides an active-low external fault indication pin.



# **DETAILED DESCRIPTION (continued)**

#### <span id="page-20-0"></span>**Table 2. SGM2537 Fault Summary**



A latched fault can be cleared by power cycling (pulling  $V_{IN}$  to 0V) or re-enable.

### **Quick Output Discharge (QOD)**

Some applications require the output capacitor to be discharged quickly when the eFuse is turned off, so that downstream devices will not take unexpected actions due to slow discharge of the output capacitor. SGM2537-xRD internally integrates the Quick Output Discharge function, which can be enabled by connecting the OUT pin to the QOD pin. The QOD pin has an internal FET to provide a fast discharge path. Initially the FET operates in the saturation region and causes a constant current discharge in the output capacitor. The FET then operates in the linear region, where the output capacitor discharges through an equivalent resistance.

The QOD function of the chip can be equivalent to an RC discharge circuit to simplify the analysis. Among them, the discharge time of the output capacitor is the same as the charging time of the output capacitor under the same conditions. The discharge resistor RQOD is the equivalent resistance of the FET when it is used for discharge. It takes 5 times the time constant (τ  $=$  R×C) to discharge the capacitor voltage to 0.7% of the initial value. For example, when the equivalent QOD resistance is 15Ω, the time required to discharge a 100μF output capacitor from 5V to 35mV can be calculated by Equation 5.

$$
t_{\text{Discharge}} = 5 \times 15 \Omega \times 100 \mu F = 7.5 ms \hspace{1cm} (5)
$$

#### **Device Functional Modes**

The specific characteristics of the device depend on the operation mode.

### **EN/UVLO and nFAULT Pins Functional Mode 1: Single Device**

#### *Self-Controlled*

In this operation mode, there is no external host. The input power supply enables this device. The nFAULT pin pulls up to an external power supply and can optionally be monitored by an external host. See [Figure](#page-20-1)  [8.](#page-20-1)



**Figure 8. Single Device, Self-Controlled**

#### <span id="page-20-1"></span>*Host-Controlled*

In this operation mode, an external host can enable the device via a GPIO driving the EN/UVLO pin. The nFAULT pin pulls up to an external power supply and can optionally be monitored by an external host. See [Figure 9.](#page-20-2)



<span id="page-20-2"></span>**Figure 9. Single Device, Host-Controlled**



# **DETAILED DESCRIPTION (continued)**

### **EN/UVLO and nFAULT Pins Functional Mode 2: Multiple Devices**

#### *Self-Controlled*

In this operation mode, there is no host, so the devices are all self-controlling. EN/UVLO, nFAULT pins of no more than three devices are connected as shown in [Figure 10,](#page-21-0) so that one device can automatically disable other devices when a fault event is detected.



**Figure 10. Multiple Devices, Self-Controlled**

<span id="page-21-0"></span>It should be noted that this connection method is only suitable for the active high SGM2537-xR variants.

[Figure 11](#page-21-1) and [Figure 12](#page-21-2) are tested under the conditions of [Figure 9.](#page-21-0)



<span id="page-21-1"></span>**Figure 11. SGM2537-13.7R Self-Controlled Mode Response with Overload Fault on OUT1 Followed by** 



<span id="page-21-2"></span>**Figure 12. SGM2537-13.7R Self-Controlled Mode Response with Overload on OUT1 Followed by Recovery with Fault Removed**

## **APPLICATION INFORMATION**

### **Typical Application**



NOTE: 1.  $C_{\text{IN}}$  is optional. A 10µF capacitor is recommended for transient suppression from the inductance of PCB routing or input wiring.

#### **Figure 13. Typical Application Schematic: Simple eFuse for Set-Top Boxes**

#### **Design Requirements**

[Table 3](#page-22-0) shows the design requirements for the SGM2537-13.7x.

<span id="page-22-0"></span>

**Programming the Current Limit Threshold: R<sub>ILIM</sub> Selection** The over-current threshold can be set by the resistor  $R_{ILIM}$  connected to the ILIM pin, and its value can be calculated by Equation 6:

$$
R_{ILM} = \frac{1998}{(I_{LIMIT} - 0.03)}
$$
 (6)

For  $I_{LIMIT}$  = 3.7A, according to Equation 5, R<sub>ILIM</sub> = 544 $\Omega$ . Using the closest standard 1% resistor values,  $R_{\text{IUM}}$  = 549Ω is chosen.

#### **Under-Voltage Lockout Set Point**

The supply under-voltage lockout (UVLO) threshold is set by a resistor divider connected to the EN/UVLO pin. This threshold can be calculated from Equation 7:

$$
V_{UV} = \frac{R_1 + R_2}{R_2} \times V_{UVLO_R}
$$
 (7)

Where  $V_{UVLO,R}$  is the rising threshold (1.2V) of the EN/UVLO pin.  $R_1$  and  $R_2$  are the resistors of the resistor divider. Since  $R_1$  and  $R_2$  cause additional leakage current to flow out of the input voltage, their values need to be taken into account for the acceptable leakage current of the system. The leakage current flowing through  $R_1$  and  $R_2$  from the supply is  $I_{R12}$  =  $V_{1N}/(R_1 + R_2)$ . Considering that an external active device connected to a resistor divider causes additional leakage current, this increases the calculation error of the supply under-voltage threshold. Therefore, the leakage current flowing through  $R_1$  and  $R_2$  ( $I_{R12}$ ) should be greater than 20 times the leakage current expected by the EN/UVLO pin.

According to the application scenario requirements, V<sub>UVR</sub> = 4.3V. Given R<sub>1</sub> = 1MΩ, R<sub>2</sub> = 387kΩ can be obtained according to the above equation.



# **APPLICATION INFORMATION (continued)**

#### **Setting Output Voltage Ramp Time (tss)**

During the design process, it must be ensured that the junction temperature of the device does not meet the thermal shutdown threshold under either start-up or steady-state conditions. Given that the power stress to which the device is subjected at start-up is typically an order of magnitude greater than under steady-state conditions, the determination of start-up time and inrush current limit is particularly important to avoid thermal shutdown at start-up. There are two possible cases to discuss during start-up:

#### *Case 1: Start-Up without Load. Output Capacitance Draws Current*

During start-up, the voltage stress of the FET decreases as the output capacitor voltage increases. Use Equation 8 to calculate the average power dissipated on the device.

$$
P_{D(\text{INRUSH})} = 0.5 \times V_{\text{IN}} \times I_{\text{INRUSH}} \tag{8}
$$

Given the output voltage rise time, the inrush current can be calculated from Equation 9.

$$
I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}}
$$
 (9)

The prerequisite for Equation 8 is that no load current is generated until the output voltage rises to  $V_{\text{IN}}$ .

#### *Case 2: Start-Up with Load. Output Capacitance and Load Draw Current*

If the load keeps drawing current from the power supply during start-up, the power dissipated on the device will be greater. Assuming that the system has a resistive load, Equations 10 to 13 give the power dissipated by the resistive load during the start-up of the device.

$$
P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{1N}^{2}}{R_{L(SU)}} \tag{10}
$$

The total power dissipated during the start-up phase can be calculated by Equation 11.

$$
P_{D(\text{STARTUP})} = P_{D(\text{INRUSH})} + P_{D(\text{LOAD})} \tag{11}
$$

The total current during the start-up phase can be calculated by Equation 12.

$$
I_{\text{STARTUP}} = I_{\text{INRUSH}} + I_{L}(t) \tag{12}
$$

If the total current during start-up exceeds  $I_{LIMIT}$ , the current is limited to  $I_{LIMIT}$ . Use Equation 13 to calculate the current-limited charging time.

$$
t_{\text{SS(Current-Limited)}} = C_{\text{OUT}} \times R_{\text{L(SU)}} \times \left[ \frac{I_{\text{LIMIT}}}{I_{\text{INRUSH}}} - 1 + \ln \left( \frac{I_{\text{INRUSH}}}{I_{\text{LIMIT}} - \frac{V_{\text{IN}}}{R_{\text{L(SU)}}}} \right) \right]
$$
\n(13)

For  $C_{SS}$  = Open, the slew rate is 85mV/ $\mu$ s, and the rising time  $t_{SS}$  for 12V input is 112 $\mu$ s.

Use Equation 14 to calculate the current drawn by the output capacitor during ramp-up.

$$
I_{INRUSH} = \frac{1\mu F \times 85mV}{1\mu s} = 85mA \tag{14}
$$

The dissipated power can be calculated by Equation 15.

$$
P_{D(\text{INRUSH})} = 0.5 \times 12 \times 85 \text{mW} = 510 \text{mW} \tag{15}
$$

Thermal Shutdown Time vs. Power Dissipation shows that for 510mW,  $T_A = +85^{\circ}C$ , the device thermal shutdown time is infinite, which is much larger than the output rise time  $t_{SS}$  = 112µs. Therefore, setting the output rise time to 5ms has no negative impact on device security. Therefore, it is safe to use 112µs as the startup time without any load on the output.

The additional power dissipated during start-up due to a 4Ω resistive load can be calculated from Equation 10.

$$
P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6W
$$
 (16)

The total power dissipated during start-up can be calculated by Equation 17.

$$
P_{D(STARTUP)} = 6W + 510mW = 6.51W
$$
 (17)

Thermal Shutdown Time vs. Power Dissipation shows that for 6.51W,  $T_A$  = +85 °C, the device thermal shutdown time is more than 20ms, which is within the acceptable limits to avoid using an external capacitor  $C_{SS}$  with a 4Ω load. If the output capacitor  $C_{OUT}$  is large, it is recommended to increase the capacitance of  $C_{SS}$ to reduce the power dissipation.



# **APPLICATION INFORMATION (continued)**

#### **Support Component Selection: CIN**

A ceramic capacitor in the range from 0.1μF to 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.



#### **Quick Output Discharge Using SGM2537-xRD**

When the SGM2537-xRD is disabled, the internal FET is turned off and the OUT pin is left floating, where the OUT voltage drop process is determined by the external load. In some applications, this can cause downstream equipment to be in an unpredictable state because the OUT voltage is in an undesired state. Connect the QOD pin to the OUT pin to realize the Fast Output Discharge function of the SGM2537-xRD, as shown in [Figure 16.](#page-24-0) When the SGM2537-xRD is disabled via EN, the QOD pin is pulled low and provides a fast discharge path for the output capacitor. The output voltage discharge rate is determined by the output capacitance, the total resistance of the discharge path (internal plus external), and the external load.



<span id="page-24-0"></span>**Figure 16. Circuit Implementation with Quick Output Discharge Function Using SGM2537-xRD**

# **APPLICATION INFORMATION (continued)**



#### **Over-Voltage Lockout Using SGM2537-PRN**

The SGM2537-PRN implements the input over-voltage protection via a resistor divider circuit, which is connected from the supply to the nEN/OVLO pin to GND (as shown in [Figure 19\)](#page-25-0) to achieve a programmable over-voltage threshold. When the divided voltage on the nEN/OVLO exceeds  $V_{\text{OVLO}}$ , the device turns off the internal FET and protects the downstream load.



<span id="page-25-0"></span>





# **APPLICATION INFORMATION (continued)**

### **Power Supply Recommendations**

The SGM2537 devices are suitable for a supply voltage from 2.7V to 18V. If the input supply is more than a few inches away from the device, it is recommended to place an input bypass ceramic capacitor greater than 0.1μF. The rated current of the power supply must be greater than the over-current threshold set by the device, otherwise the supply voltage will drop in the event of an over-current or short-circuit.

#### **Transient Protection**

In the case of a short-circuit or over-current limit, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input and output, and a negative voltage spike will occur at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the output pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

Use Equation 18 to calculate the input capacitance value.

$$
V_{\text{SPIKE}}\text{(Absolute)} = V_{\text{IN}} + I_{\text{LOAD}} \times \sqrt{\frac{L_{\text{IN}}}{C_{\text{IN}}}}\tag{18}
$$

Where  $V_{IN}$  is the rating of the input voltage,  $I_{LOAD}$  is the load current,  $L_{IN}$  is the effective inductance seen looking into the source, and  $C_{\text{IN}}$  is the capacitance of the input.

[Figure 21](#page-26-0) shows a circuit implementation with optional protection components.



<span id="page-26-0"></span>NOTE: 1. C<sub>IN</sub> is optional. A 10μF capacitor is recommended for transient suppression from the inductance of PCB routing or input wiring.

#### **Figure 21. Circuit Implementation with Optional Protection Components**

# **APPLICATION INFORMATION (continued)**

### **Output Short-Circuit Measurements**

The output short-circuit waveform may be affected by factors such as input leads, power supply bypass, layout, device selection, circuit location, and output short-circuit method. It is difficult to obtain repeatable and similar output short-circuit test results. Therefore, the short-circuit results in this datasheet are for informational purposes only. Different short-circuit test results may be achieved because of different test conditions.

### **Layout Guidelines**

- In any application, it is recommended to connect a 0.1μF or greater decoupling capacitor between IN and GND. This decoupling capacitor should be as close as possible to the IN and GND pins to minimize the area of the IN-decoupling capacitor-GND loop.
- The power path should be as wide and short as possible, with a current-carrying capacity of more than twice the device's current limit.
- The GND pin of the device must be connected to PCB ground which is a copper plane or island as short as possible.
- In order to achieve the accuracy of the eFuse function, it is recommended to provide the eFuse with a ground plane that does not flow through large currents. The ground plane of the device is connected to the ground plane of the system via a star connection.
- External components of the device as follows should be placed as close to the corresponding pins as possible:
	- 1.  $R_{IIIM}$
	- $2. C<sub>SS</sub>$
	- 3. Resistor dividers of EN/UVLO
- The other end of these components is connected to ground via the shortest possible path. The ILIM pin should have a parasitic capacitance of less than 50pF, and the connection path of this pin should be away from the switching signal.
- Protection components such as TVS, snubbers, capacitors or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.



## **REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.





# **PACKAGE OUTLINE DIMENSIONS TDFN-2×2-8AL**





NOTE: This drawing is subject to change without notice.

# **TAPE AND REEL INFORMATION**

#### **REEL DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

### **KEY PARAMETER LIST OF TAPE AND REEL**



### **CARTON BOX DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

### **KEY PARAMETER LIST OF CARTON BOX**



