SGM48550

Single-Channel High-side and Low-side Gate Driver with High CMR Truly Differential Input

GENERAL DESCRIPTION

The SGM48550 is single-channel non-isolated truly differential input (TDI) MOSFETs and GaN HEMTs driver for both the high-side and low-side.

The TDI stage concept enables the driver to have high common mode robustness (CMR) and no false triggering even if a common mode voltage exists on the input differential pair. The peak common mode voltage between ground reference (GND) and driver inputs (IN-, IN+) can reach up to ±200V DC and ±400V AC.

The SGM48550 is available in a Green SOT-23-6 package.

APPLICATIONS

Half-Bridge, Full-Bridge, Push-Pull, Synchronous Buck and Forward Converters

Synchronous Rectifiers

Motor Control

FEATURES

- **High Common Mode Robustness**
- **Static CMR Range up to ±200V, Dynamic CMR Range up to ±400V**
- **4A Peak Source and 8A Peak Sink Currents**
- **47ns Typical Propagation Delay**
- **UVLO Options**
  - **SGM48550A: 4.2V**
  - **SGM48550B: 7.95V**
- **Topologies**
  - **Driving Kelvin-Source MOSFETs (4-Pin Packages)**
  - **Applications in Low-side Drive with Significant Parasitic PCB-Inductance**
  - **Applications in High-side Drive**
  - **Applications in Half and Full-Bridge Configurations**
  - **Driving SJ and SiC MOSFETs, GaN HEMTs**
  - **Switches Requiring Negative Voltage Shutdown**
- **Fully Qualified According to JEDEC for Industrial Grade Applications**
- **Available in a Green SOT-23-6 Package**

TYPICAL APPLICATION

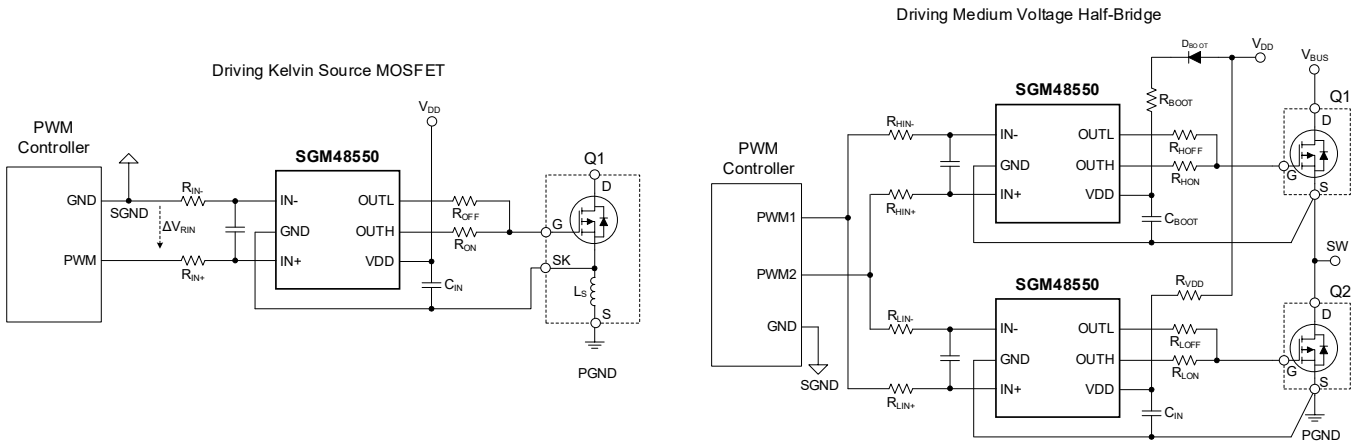


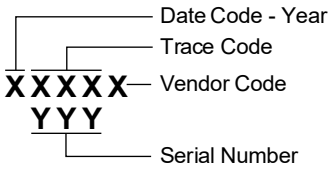
Figure 1. SGM48550 Typical Application Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48550A	SOT-23-6	-40℃ to +150℃	SGM48550AXN6G/TR	XXXXX 1V0	Tape and Reel, 3000
SGM48550B	SOT-23-6	-40℃ to +150℃	SGM48550BXN6G/TR	XXXXX 1V1	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.3V to 28V
IN+, IN- Voltage Range..... -10V to 10V
OUTH Voltage Range
DC.....-0.3V to V_{DD} + 0.3V
Repetitive Pulse < 200ns .....-2V to V_{DD} + 2V
OUTL Voltage Range
DC.....-0.3V to V_{DD} + 0.3V
Repetitive Pulse < 200ns .....-2V to V_{DD} + 2V
Pulsed Reverse Sink and Source (0.5μs), I_{OUT_PULSED} (1).....
..... -5A/5A
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 139.7℃/W
SOT-23-6, θ_{JB} ..... 27.9℃/W
SOT-23-6, θ_{JC} ..... 71.9℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (2) (3)
HBM.....±3000V
CDM .....±1000V

NOTE:

1. Verified by characterization on bench.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD}
SGM48550A .....4.5V to 26V
SGM48550B .....8.6V to 26V
IN+, IN- Voltage Range..... -7V to 6V
Operating Junction Temperature Range.....-40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

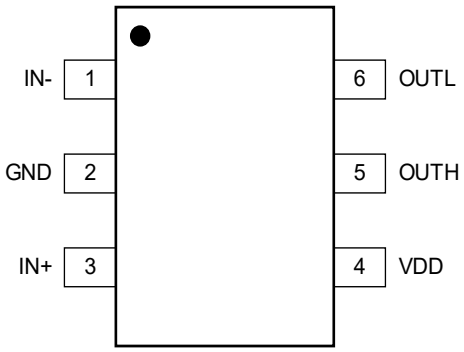
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOT-23-6

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IN-	I	Negative Logic-Level Input. An input resistor is connected between IN- and controller PWM or ground.
2	GND	G	Ground. Reference pin for all signals.
3	IN+	I	Positive Logic-Level Input. An input resistor is connected between IN+ and controller PWM or ground.
4	VDD	I	Input Voltage Supply.
5	OUTH	O	Driver Source Current Output.
6	OUTL	O	Driver Sink Current Output.

NOTE: I: input, O: output, G: ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
VDD Supply Voltage	V_{DD}	SGM48550A	4.5		26	V
		SGM48550B	8.6		26	
VDD Quiescent Current	I_{VDDH}	OUT = high, V_{DD} = 12V		1.3		mA
		OUT = high, V_{DD} = V_{DD_MIN} to 26V			2	
	I_{VDDL}	OUT = low, V_{DD} = 12V		1.13		mA
		OUT = low, V_{DD} = V_{DD_MIN} to 26V			1.8	
Under-Voltage Lockout (UVLO)						
Under-Voltage Lockout Turn-On Threshold	V_{UVLO_ON}	SGM48550A	3.9	4.2	4.5	V
		SGM48550B	7.4	7.95	8.5	
Under-Voltage Lockout Turn-Off Threshold	V_{UVLO_OFF}	SGM48550A	3.6	3.9	4.1	V
		SGM48550B	6.4	6.95	7.5	
UVLO Threshold Hysteresis	V_{UVLO_HYS}	SGM48550A		0.3		V
		SGM48550B		1		
Inputs IN+, IN-						
Differential Input Voltage Turn-On Threshold (at Input Resistor) (1)	ΔV_{RINH}	Independent of V_{DD}, R_{IN+} = R_{IN-} = 33kΩ		1.72	2.4	V
Differential Input Voltage Turn-Off Threshold (at Input Resistor) (1)	ΔV_{RINL}	Independent of V_{DD}, R_{IN+} = R_{IN-} = 33kΩ	0.7	1.3		V
Total Input Resistance on Each Leg (1)	R_{IN+}, R_{IN-}	R_{IN+} = R_{IN-} = 33kΩ	35.5	36	36.5	kΩ
Static Output Characteristics						
Output Pull-Up Resistance (2)	R_{OH}	I_{OUT} = 50mA		5.5	12	Ω
Peak Source Current	I_{PK_SOURCE}	V_{DD} = 12V		4.6		A
		V_{DD} = 18V		5.3		
Output Pull-Down Resistance	R_{OL}	I_{OUT} = 50mA		0.35	0.9	Ω
Peak Sink Current	I_{PK_SINK}	V_{DD} = 12V		-8.7		A
		V_{DD} = 18V		-9.4		

NOTES:

1. Refer to Figure 1.

2. R_{OH} represents constant pull-up resistance only. Pull-up resistance R_{OH_PULSE} operates in pulse mode during the output rising stage, R_{OH_PULSE} = 880mΩ (TYP).

SWITCHING CHARACTERISTICS

(V_{DD} = 12V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time (1)	t_R	C_{OUT} = 1.8nF		6.5	13	ns
		C_{OUT} = 200pF		2.5	6.5	
Fall Time (1)	t_F	C_{OUT} = 1.8nF		6.5	13	ns
		C_{OUT} = 200pF		2.5	6.5	
Minimum Input Pulse Width that Changes Output State	t_{PW}	C_{OUT} = 1.8nF		25		ns
(IN+ - IN-) to Output Propagation Delay (1)	t_{DON}	C_{OUT} = 200pF	29	43	62	ns
	t_{DOFF}	C_{OUT} = 200pF	34	47	69	ns

NOTE:

1. Refer to Figure 3.

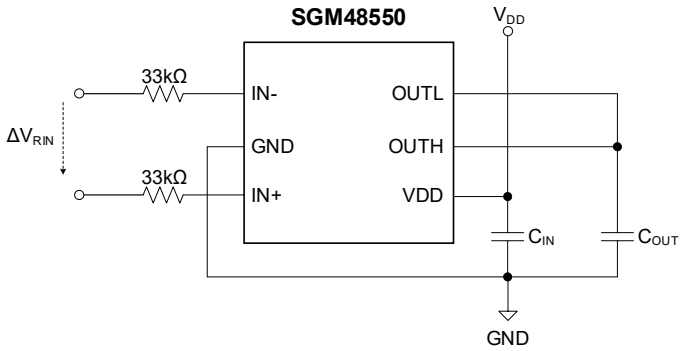


Figure 2. Test Circuit

TIMING DIAGRAMS

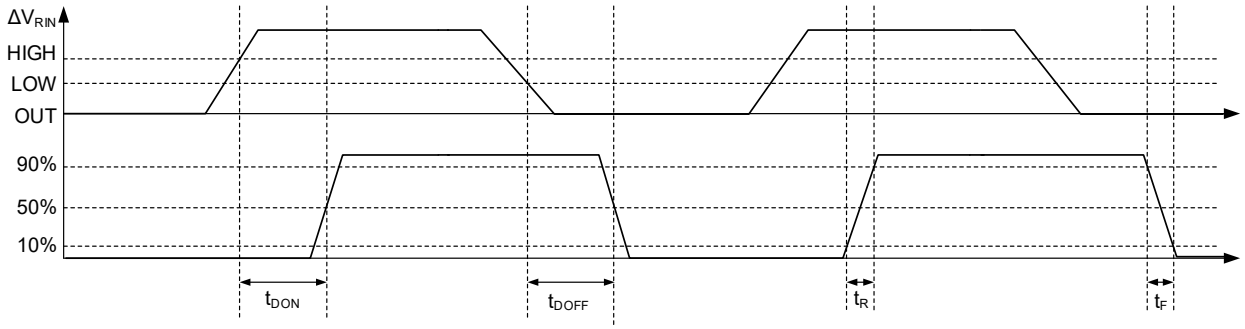


Figure 3. Timing Diagram

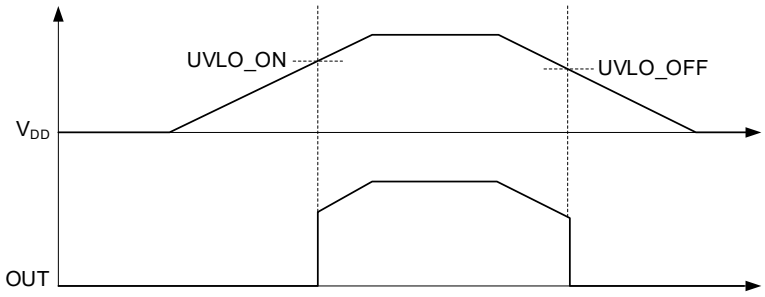
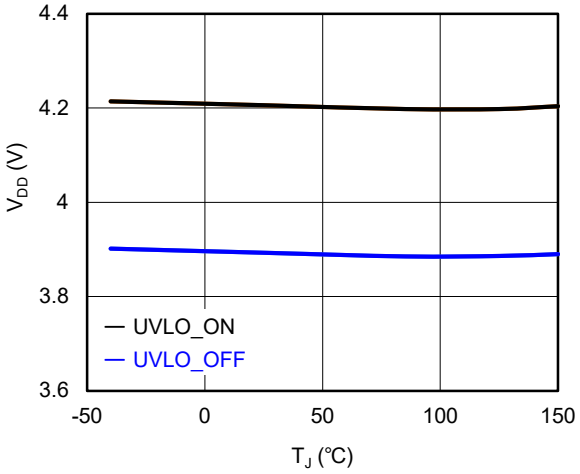


Figure 4. UVLO Behavior (Output State High)

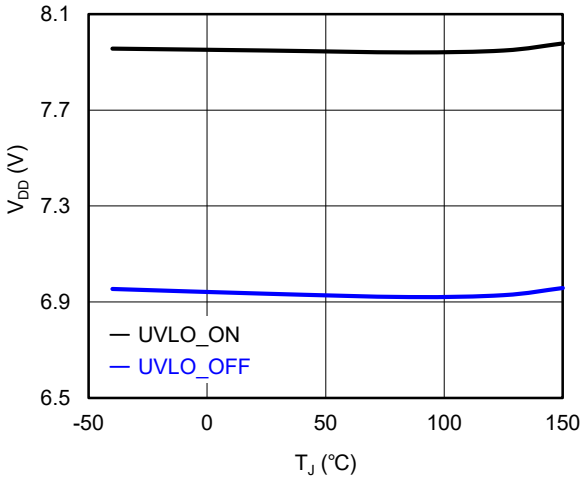
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = -40℃ to +150℃, unless otherwise noted.

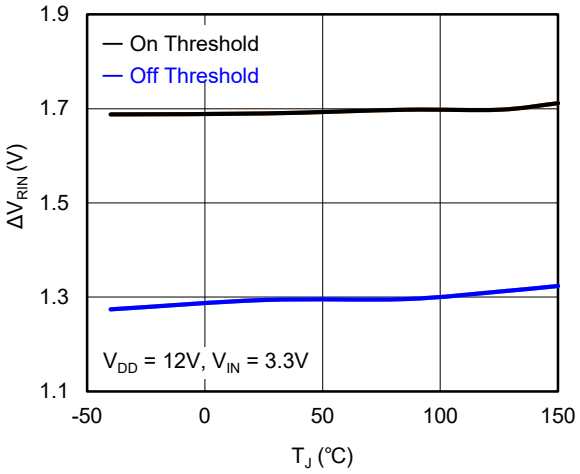
Under-Voltage Lockout Threshold vs. Temperature (SGM48550A)



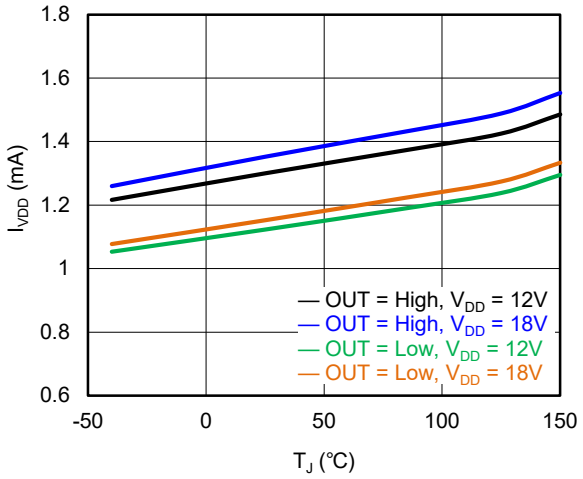
Under-Voltage Lockout Threshold vs. Temperature (SGM48550B)



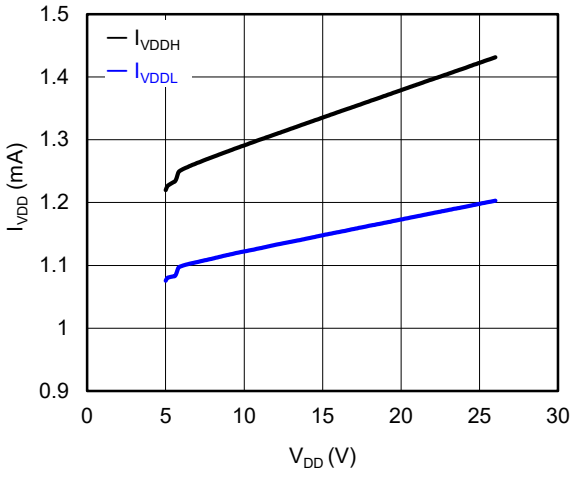
Differential Voltage Threshold vs. Temperature



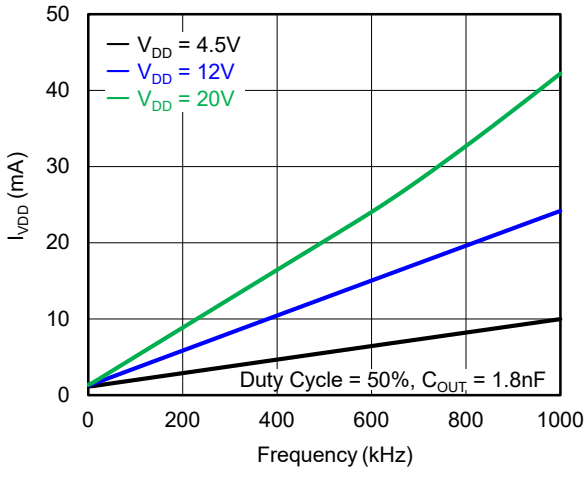
Typical Quiescent Current vs. Temperature



Typical Quiescent Current vs. Supply Voltage



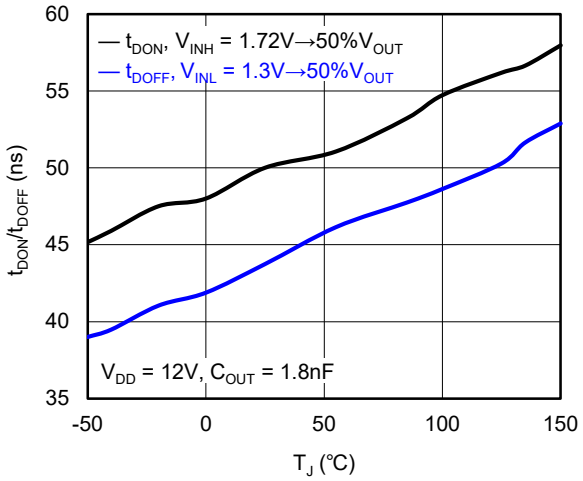
Total Operating Current Consumption with Capacitive Load vs. Frequency



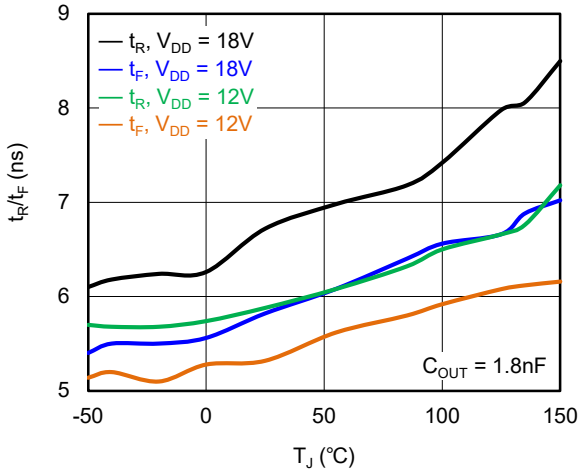
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +150℃, unless otherwise noted.

Typical Propagation Delay vs. Temperature



Typical Rise and Fall Time vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

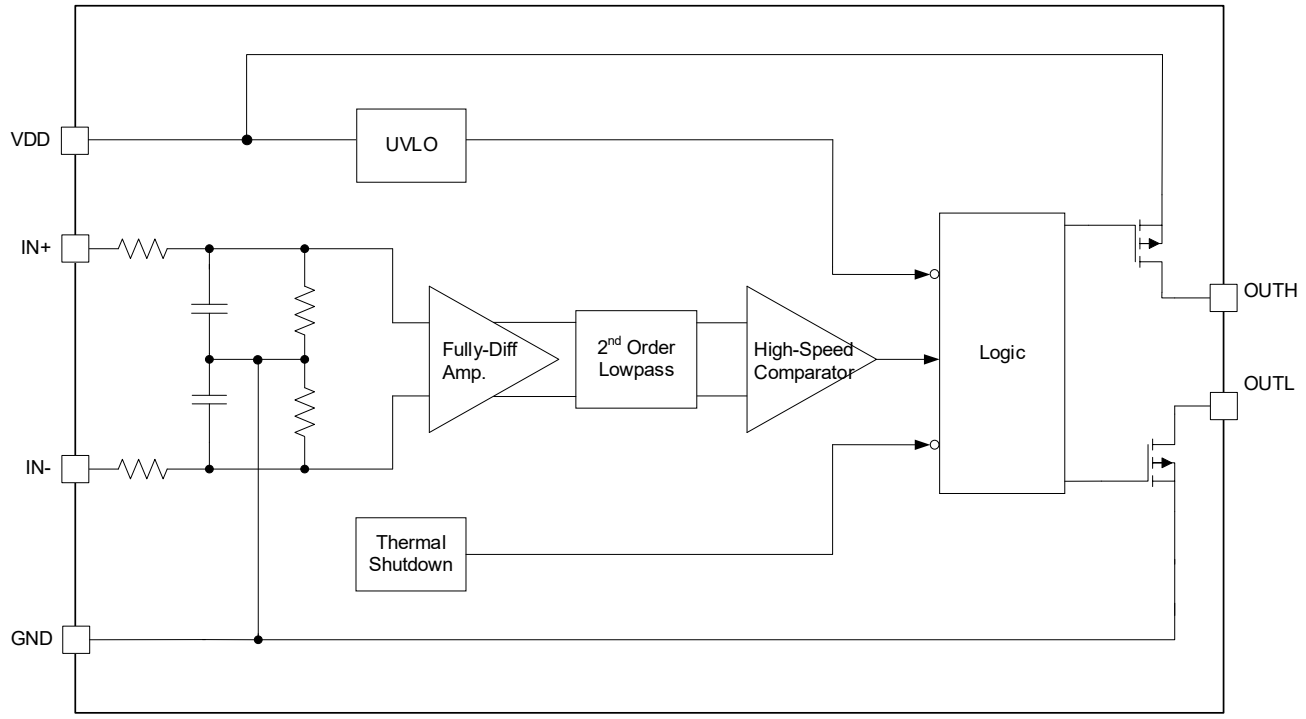


Figure 5. Functional Block Diagram

DETAILED DESCRIPTION

The SGM48550 is a high-side and low-side single-channel non-isolated truly differential input (TDI) gate driver. Since it supports true differential inputs, the SGM48550 can replace traditional isolated and level-shift drivers, resulting in significant cost reduction. The TDI has high common mode robustness (CMR), and it will not trigger incorrectly even if there is a common mode voltage on the input differential pair. The peak common mode voltage between ground reference (GND) and driver inputs (IN-, IN+) can reach up to ±200V DC and ±400V AC.

Therefore, the SGM48550 can be used in any application where the ground shift robustness between driver and controller within the static common mode range (±200V MAX) and dynamic common mode range (±400V MAX), such as half-bridge driving and switches with bipolar gate drive.

Truly Differential Input (TDI)

Figure 6 depicts the operating principle of the SGM48550's truly differential inputs (TDI).

The SGM48550 cannot connect IN- directly to GND and IN+ directly to PWM used as a standard low-side driver. The output signal of the controller should be connected to IN+ and IN- of the SGM48550 through a resistor, respectively, as shown in Figure 6. The input resistors R_{IN+}, R_{IN-}, and the 2kΩ and 1kΩ resistors inside driver together form a differential amplifier with high common mode rejection ratio (CMRR), which decouples the controller outputs from the driver's ground.

The selection of input resistors R_{IN+} and R_{IN-} depends on the ground shift robustness between the driver and controller and the maximum ΔVR_{IN}, as shown in Table 2.

For example, when the maximum ΔVR_{IN} = 3.3V, R_{IN+} and R_{IN-} should be equal to 33kΩ. And according to the following equation, the voltage ratio of the controller's output PWM signal to the input signal of the driver is k = 12:

$$k = (R_{IN}\ [k\Omega] + 3)/3 \quad (1)$$

For ΔVR_{IN} other than 3.3V, R_{IN+} and R_{IN-} should meet the following equation:

$$R_{IN+} = R_{IN-} = (10.9 \times V_S - 3)\ [k\Omega] \quad (2)$$

where V_S is the high voltage level of the controller's output PWM signal.

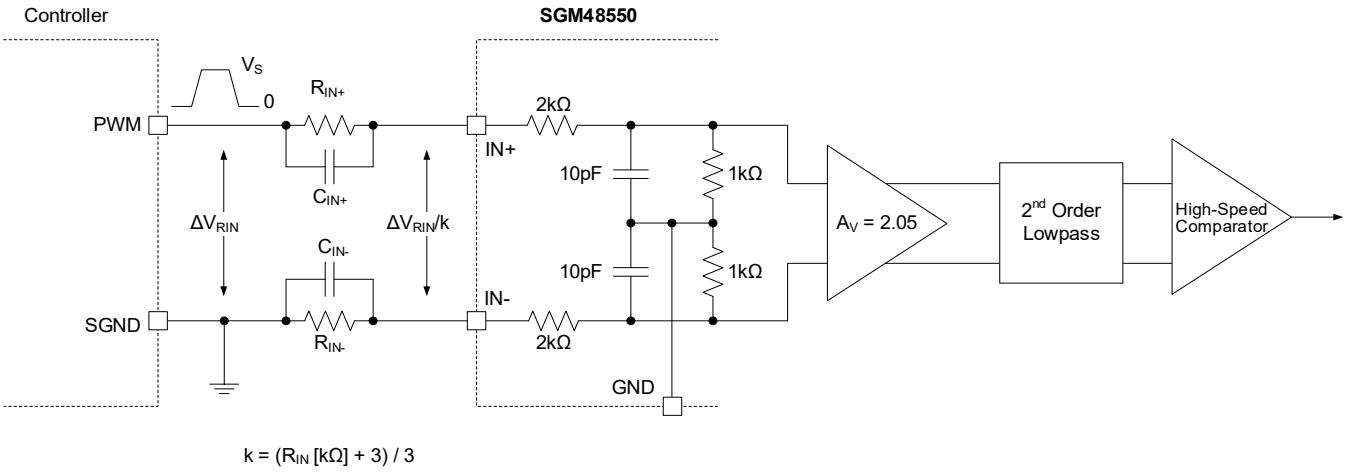


Figure 6. Operating Principle of the SGM48550 with Truly Differential Inputs (TDI)

DETAILED DESCRIPTION (continued)

Then, the input signal is first filtered by a passive differential RC filter, amplified by a high CMRR amplifier by a factor of 2.05, and filtered by a 23MHz 2nd low-pass filter. Then the filtered output signal is fed into high-speed comparator. The entire input signal undergoes 3rd filtering, which can effectively suppress noise at frequencies of 100MHz and above, while also maintaining robustness of the driver in the case of a mismatch between C_{IN+} and C_{IN-} (50fF to 100fF range). The minimum input pulse width of the pulse expander is 25ns, which greatly improves the noise immunity of the driver. The overall propagation delay from input to output is 47ns.

Common Mode Input Range

The common mode robustness (CMR) means the maximum ground shift allowed between the controller and the driver. The passive low-pass filtering at the input side can suppress some high-frequency noise. So according to the common mode voltage frequency content, the CMR can be divided into CMR static which represents the ability of the driver to withstand DC voltages and CMR dynamic which represents the ability of the driver to withstand AC voltages.

In order to increase the CMR of the SGM48550, the selection of input resistors R_{IN+} and R_{IN-} is particularly important. When selecting the value and accuracy of the input resistors, the maximum device voltage ratings of the driver IN+/IN- pins must be considered. When selecting the form factor of the input resistors, it is necessary to consider the power dissipation and creepage requirements.

Meanwhile, the CMR is limited by the voltage of input pins IN+/IN-. The operating voltage range of input pins IN+/IN- of SGM48550 is from -7V to +6V, which affects CMR static. The absolute maximum ratings range of input pins IN+/IN- is from -10V to +10V, which affects CMR dynamic. For example, when the controller PWM output voltage is 3.3V and the input resistor is configured with 33kΩ, 0.1% tolerance, and 0603 form factor, the static CMR range of SGM48550 is -72V/+84V, and the dynamic CMR range is ±150V.

Similarly, when the controller PWM output voltage is 12V and the input resistor is configured with 127kΩ, 0.1% tolerance, and 1206 form factor, the static CMR range of SGM48550 is ±200V, and the dynamic CMR range is ±400V.

The specific input resistor configuration can be obtained by consulting Table 2.

It should be noted that in order to achieve the ideal CMR in Table 2, the input signal path must be completely symmetrical. If there is parasitic asymmetry in the input signal path, the common mode signal will be converted into a differential signal, thereby reducing CMR performance.

Driver Outputs

The output stages of driver are connected to the gate of the power MOSFET in the power train. The high slew rate, low resistance, and high peak current capability of the output driver allow for efficient switching of the power MOSFETs. SGM48550 provides 4A peak source and 8A peak sink currents, and the outputs are separated to allow custom pull-up and pull-down drive strength to suit the application. In order to achieve 4A peak source current capability, the output stage pull-up structure uses a PMOS and one additional NMOS in parallel. When the output changes from low to high, the NMOS in parallel can be turned on briefly to increase the peak source current. The sinking MOSFET of the SGM48550 output stage is an NMOS with 0.35Ω R_{OL}.

When the input is floating, the driver out will be pulled down to GND.

Supply Voltage and Under-Voltage Lockout (UVLO)

The SGM48550 provides under-voltage lockout (UVLO) function to protect the driver in the event of a fault condition. VDD is monitored. When VDD is below the specified threshold, the VDD UVLO disables driver. Table 1 lists the output states for different pin combinations.

Table 1. Logic Table

ΔV_{RIN}	UVLO	OUTH	OUTL
x	Active (1)	Z (5)	L
L (2)	Inactive (3)	Z (5)	L
H (4)	Inactive (3)	H	Z (5)

NOTES:

1. V_{DD} < UVLO_OFF.
2. ΔV_{RIN} < ΔV_{RINL}.
3. V_{DD} > UVLO_ON.
4. ΔV_{RIN} > ΔV_{RINH}.
5. Z = High Impedance.

APPLICATION INFORMATION

Input Resistor Configuration

Table 2 shows how to select the input resistors R_{IN+} and R_{IN-}, which depends on the static and dynamic common mode voltage between driver ground and controller ground and the controller PWM output voltage. When R_{IN+}, R_{IN-} and the controller PWM output voltage are known, look up Table 2 to get the maximum allowed CMR.

Table 2. Input Resistor Configuration Lookup Table

Controller PWM Output Voltage	Input Resistor Configuration			Ground Shift Robustness	
	Value	Tolerance	Form Factor (1)	CMR Static (2)	CMR Dynamic
2.5V	24kΩ	1%	≥0402	-30V/+30V	±110V
		0.1%	≥0603	-54V/+63V	±120V
3.3V	33kΩ	1%	≥0402	-40V/+40V	±120V
		0.1%	≥0603	-72V/+84V	±150V
5V	51kΩ	1%	≥0603	-60V/+60V	±120V
		0.1%	≥0805	-108V/+126V	±150V
12V	127kΩ	1%	≥0805	-140V/+140V	±200V (3)
		1%	≥1206	-140V/+140V	±400V (3)
		0.1%	≥1206	-200V/+200V	±400V (3)
15V	160kΩ	1%	≥0805	-150V/+150V	±200V (3)
		1%	≥1206	-175V/+175V	±400V (3)
		0.1%	≥1206	-200V/+200V	±400V (3)

NOTES:

1. It is related to the PWM signal duty cycle and the power rating of the resistor.
2. Driver ground to system ground.
3. Guaranteed by design.

Supply Voltage VDD

SGM48550A/B supports a maximum power supply voltage of 26V and is suitable for applications such as Si MOSFET, IGBT, SiC MOSFET, etc. The bias supply voltage on the VDD pin should never exceed the values listed in the Absolute Maximum Ratings section. The UVLO protection is integrated on the VDD power circuit block. If this function is not available, the gate of the external power device may be driven at low voltage, resulting in high channel impedance of the power device. This may lead to very high conduction losses within the power device and result in power device failure. It is recommended to place a low-ESL MLCC of 4.7μF or larger in parallel with a low-ESL 100nF high-frequency decoupling MLCC near the VDD and GND pins. High frequency noise on the power supply may cause internal circuit failures. To avoid any potential issues, the maximum ripple on the power supply should be less than ±1V, and the VDD slew rate should be limited to below 1V/μs to prevent rapid voltage spikes from introducing transient surge currents.

When the VDD voltage is greater than 20V and the equivalent capacitance of the MOS connected to the OUT pin is greater than 10nF, it is required that the gate turn-on resistance be no less than 6.5Ω and the gate turn-off resistance be no less than 5.8Ω.

Applications in Half-Bridge Configurations

The design of SGM48550 supporting true differential inputs (TDI) enables it to drive high-side MOSFETs as shown in Figure 7, replacing traditional isolated and level-shift drivers in half-bridge or full-bridge configurations.

In Figure 7, when the high-side switch is on, the voltage of the ground of the high-side driver is V_{BUS}, and a DC offset ΔV_{BUS} is generated between the high-side driver's ground and the controller ground. Using the TDI of the SGM48550, select appropriate input resistors R_{IN+} and R_{IN}- to obtain high common mode robustness (CMR). For example, for 3.3V controller PWM output voltage and input resistors configured with 33kΩ, 0.1% tolerance, and 0603 form, the maximum static CMR can reach up to +84V.

APPLICATION INFORMATION (continued)

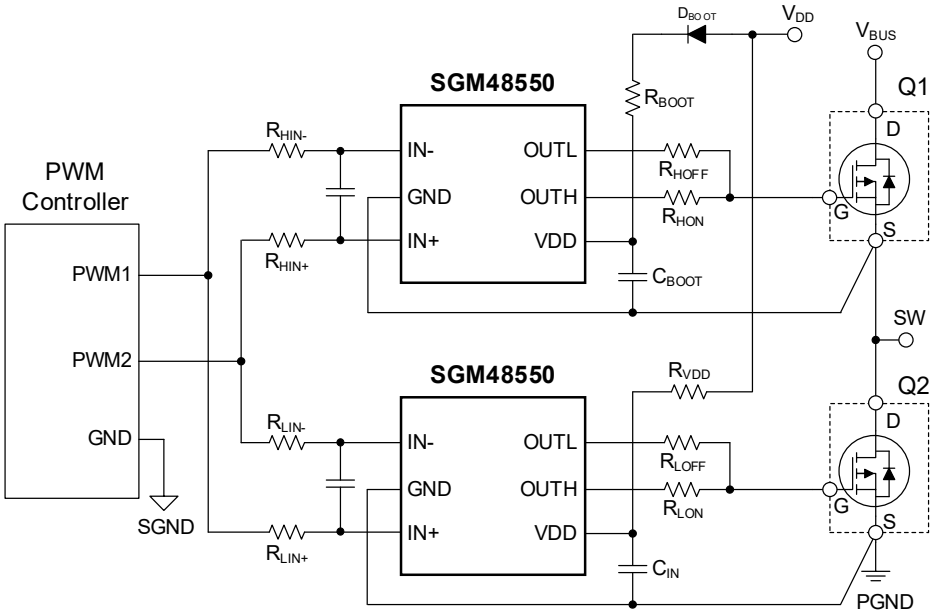


Figure 7. SGM48550 Applications in Half-Bridge Configurations

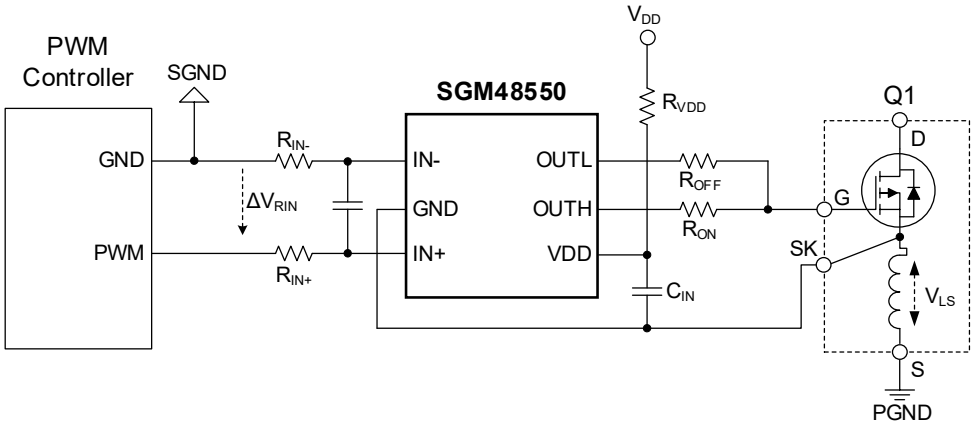


Figure 8. SGM48550 Driving a Kelvin-Source MOSFET (4-Pin Packages)

Driving Kelvin-Source MOSFETs (4-Pin Packages)

Figure 8 shows the SGM48550 driving a Kelvin-source 4-pin MOSFET. The Kelvin-source connection effectively decouples the gate drive circuit and power circuit, so that the changes in the power-side current do not affect the gate drive circuit, and can effectively improve the switching speed and reduce losses. However, there is still an inductive voltage drop, V_{LS} between the gate driver's ground and SGND, which can be up to 100V and above in fast-switching high-current applications. The SGM48550, which supports truly differential input and has high common mode robustness, can solve this problem.

Also, due to the presence of V_{LS}, the SGND-related V_{DD} cannot directly supply power to the driver, otherwise the supply will be unstable. Generally, the frequency of V_{LS} is greater than 100MHz, so V_{DD} can be connected to the driver through a filter consisting of impedance R_{VDD} and bypass capacitor C_{IN}.

APPLICATION INFORMATION (continued)

Applications with High PCB Parasitic Inductance

PCB parasitic inductance is unavoidable. The inductive voltage drop generated by the parasitic inductance can cause interference to the system, especially in fast-switching high-current systems. To solve this problem, in addition to optimizing the PCB layout to reduce parasitic parameters as much as possible, it is also possible to use the SGM48550 with high ground shift robustness instead of the traditional low-side gate driver.

Figure 9 shows the SGM48550 in applications with significant parasitic PCB inductances.

Switches Requiring Negative Voltage Shutdown

Power switches in practice usually generate high dV/dt voltage spike and di/dt current spike, and these noises can easily lead to gate voltage rising, causing power switches such as MOSFETs, SiC, and GaN to be mistakenly turned on. Therefore, in order to ensure the correct operation of the power switch, negative voltage shutdown is usually used.

Figure 10 shows the application of the SGM48550 in driving power switches that require negative voltage shutdown. A biased Zener diode is utilized to generate a positive V_{GS} driving voltage for V_B, and a negative V_{GS} driving voltage for V_B - V_{DD}.

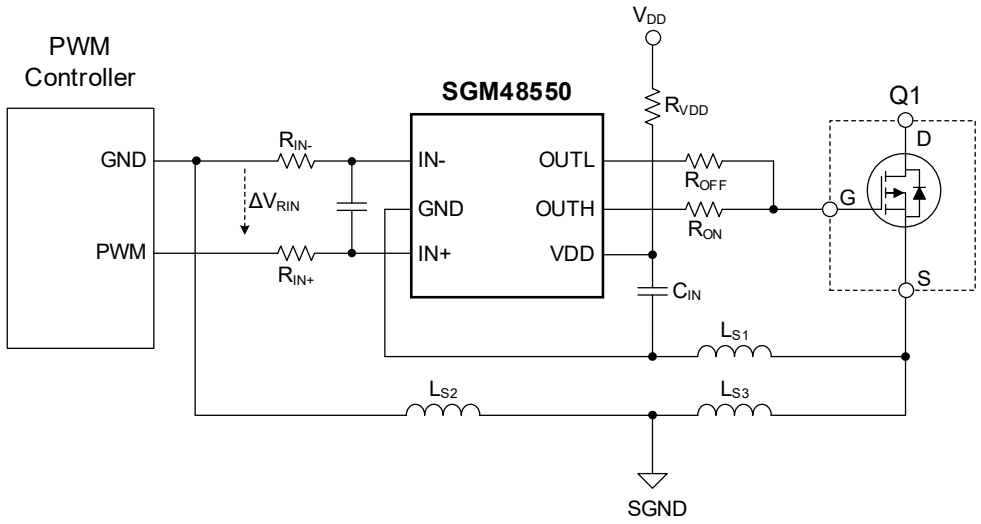


Figure 9. SGM48550 in Applications with High PCB Parasitic Inductances

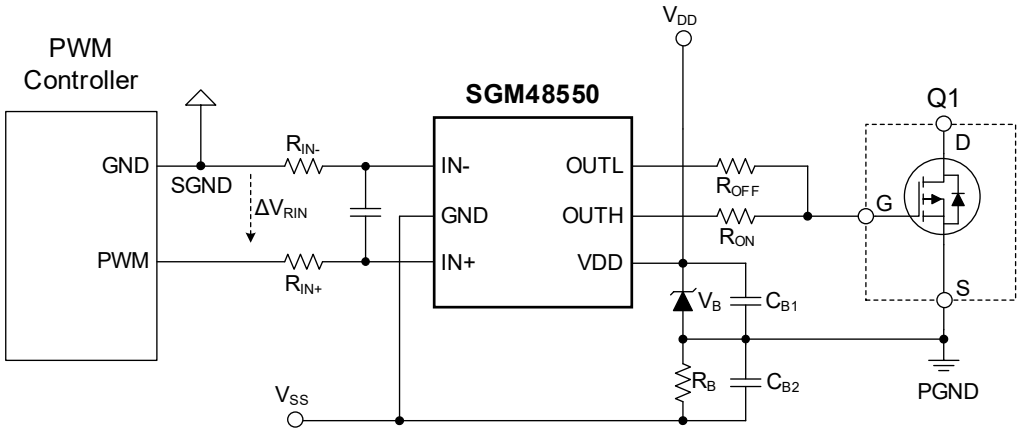


Figure 10. SGM48550 Driving a MOSFET Requiring Negative Voltage Shutdown

APPLICATION INFORMATION (continued)

Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. In order to achieve the maximum performance and CMR capabilities of SGM48550, in addition to selecting the appropriate input resistor, the following layout rules also need to be noted:

• The input resistor R_{IN} should be placed as close as possible to the IN+ and IN- pins of the driver, and the layout of the input signal path should be as symmetrical as possible.

• The V_{DD} power supply uses decoupling capacitors with low ESR, which should be located as close as possible to the driver pins.

• To reduce ringing and increase switching speed, the parasitic inductance of the gate drive circuit should be minimized as much as possible, such as minimizing the loop area and keeping compact components close.

Figure 11 shows the layout example of the SGM48550.

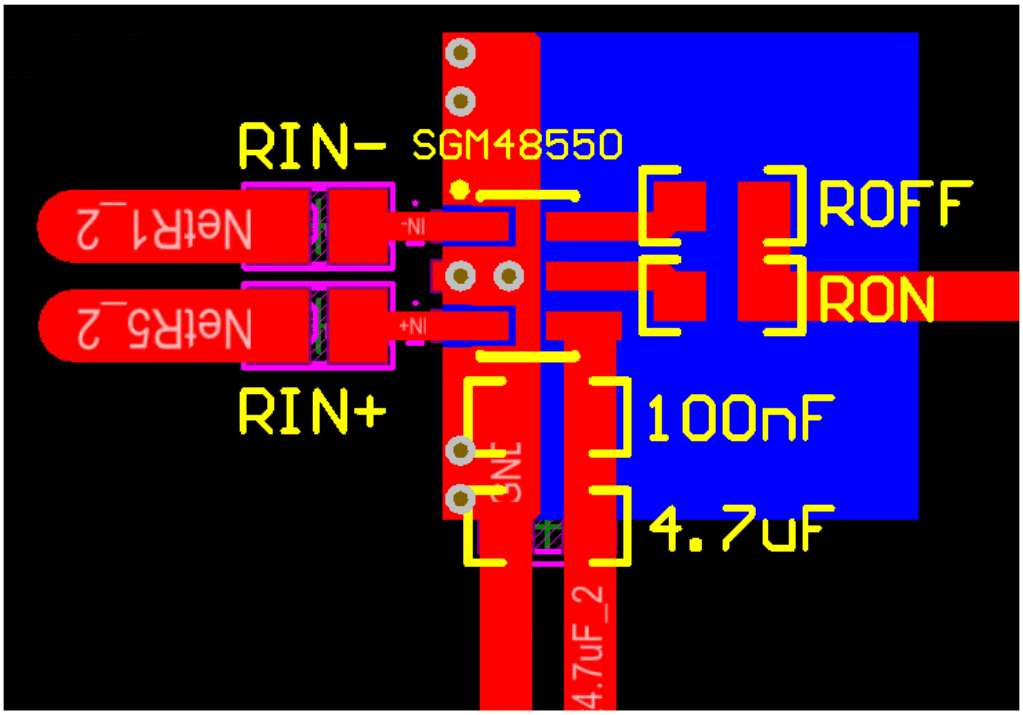


Figure 11. Layout Example

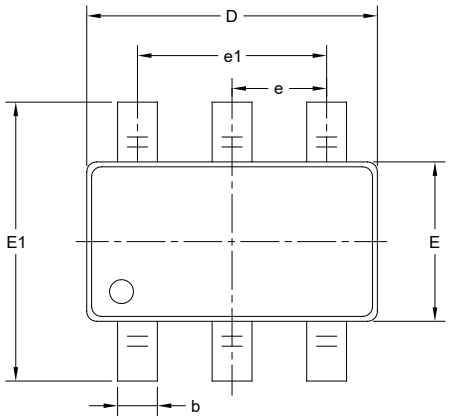
REVISION HISTORY

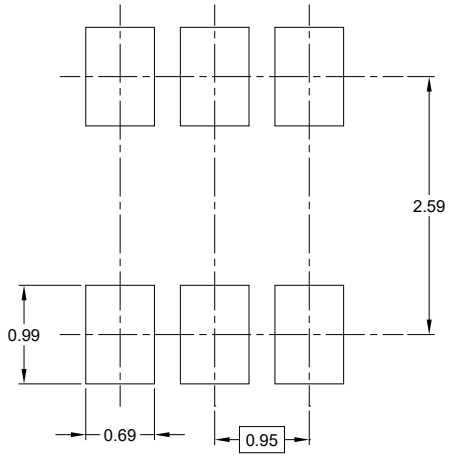
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

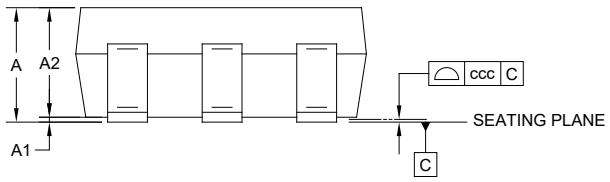
PACKAGE OUTLINE DIMENSIONS

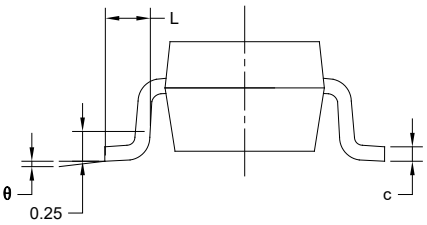
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



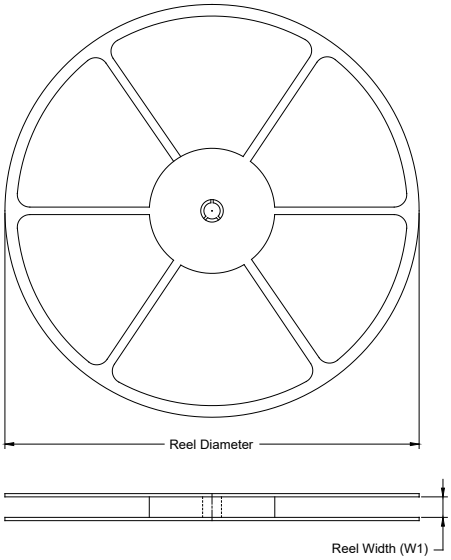


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

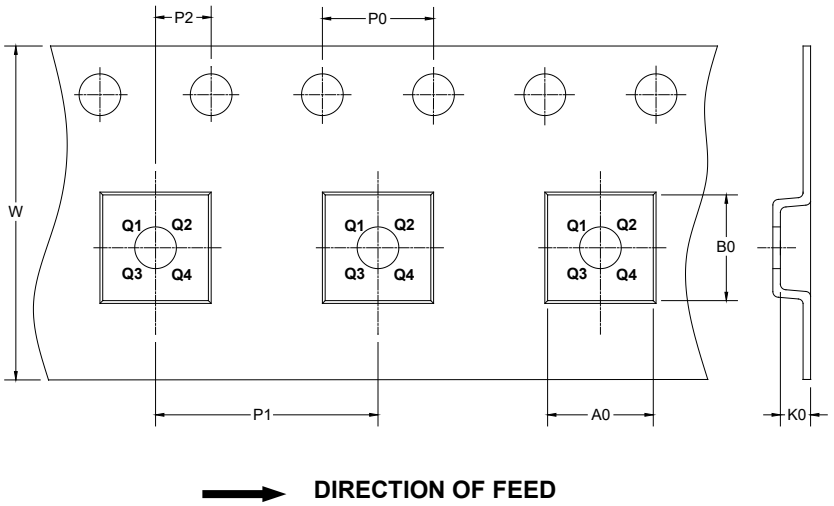
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



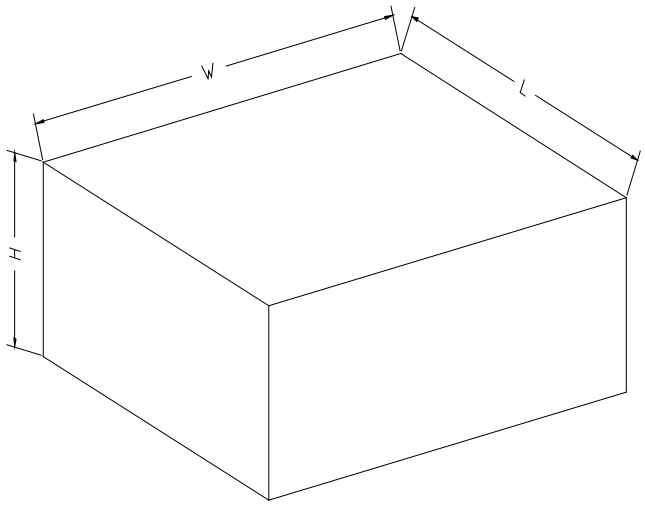
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002