SGM25720
System Power Management and Protection IC with PMBus

GENERAL DESCRIPTION

The SGM25720 is an advanced hot-swap controller designed for compute blades and storage systems, featuring an SMBus/I²C dual-compatible interface compliant with PMBus standards. This device provides precise electrical parameter monitoring, system-level protection, and dynamic control for compute and storage blades connected to high-density backplane power buses, ensuring reliability in demanding environments.

The control block of the SGM25720 incorporates a distinctive hot-swap architecture. This architecture delivers current and power limiting capabilities, which safeguard sensitive circuitry when boards are inserted into a live system backplane or any other active power source. Additionally, a rapid-response circuit breaker prevents damage if a short circuit occurs at the output. Key parameters such as input under-voltage and over-voltage levels, hysteresis, insertion delay time, and fault detection time are all configurable. The SGM25720 also features a temperature monitoring module that interfaces with a low-cost external diode. This diode is used to monitor the temperature of external MOSFETs or other thermally sensitive components. The power good (PGD) output serves as a quick indicator whenever input or output voltages deviate from their programmed ranges.

The monitoring module of the SGM25720 calculates two types of values for subsystem operating parameters (V_{IN}, I_{IN}, P_{IN}, V_{OUT}): real-time values and average values. It also computes the peak power of the subsystem. Accurate power averaging is achieved by calculating the average of the product derived from input voltage and input current. Furthermore, the device includes a black box function (referred to as Telemetry/Fault Snapshot). This function triggers the capture and storage of telemetry data and device status whenever a warning or fault condition arises.

The SGM25720 is available in a Green TQFN-4×5-24AL package.

FEATURES

- **Input Voltage Range: 2.9V to 18V**
- **I²C/SMBus Interface and PMBus Compliant Command Structure**
- **Programmable 24.5mV or 45mV Current Limit Threshold**
- **Configurable Circuit Breaker Protection for Hard Shorts**
- **Configurable Under-Voltage and Over-Voltage Lockouts with Hysteresis**
- **Remote Temperature Sensing with Programmable Warning and Shutdown Thresholds**
- **Detection and Notification of MOSFET Health**
- **Real-Time 12-Bit ADC for V_{IN}, V_{OUT}, I_{IN}, P_{IN}, V_{AUX} and 1kHz Sampling Rate**
- **Current Measurement Accuracy: ±1.8% Over-Temperature**
- **Power Measurement Accuracy: ±2.2% Over-Temperature**
- **Accurate Dynamic Power Reading Averaging Achieved Through Simultaneous V_{IN} and I_{IN} Sampling**
- **Programmable Interval-Based Averaging of V_{IN}, I_{IN}, P_{IN}, and V_{OUT}, with Interval Ranges from 1ms to 4s**
- **Configurable WARN and FAULT Thresholds, Equipped with nSMBA Notification**
- **Black Box Recording of Telemetry Data and Device Status, Activated by Warn or Fault Events**
- **Available in a Green TQFN-4×5-24AL Package**

APPLICATIONS

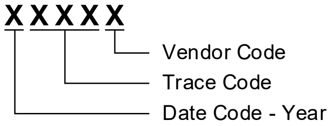
Server Backplane Systems
Basestation Power Distribution Systems
Solid-State Circuit Breaker

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25720	TQFN-4×5-24AL	-40℃ to +125℃	SGM25720XTQY24G/TR	SGM25720 XTQY24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input voltage
VIN, SENSE to GND (1) .... -0.3V to 24V
GATE, FB, UVLO/EN, OVLO, PGD to GND (1) .... -0.3V to 20V
OUT to GND .... -1V to 20V
SCL, SDA, nSMBA, CL, CB, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, nRETRY to GND....................... -0.3V to 6V
VIN to SENSE... -0.3V to 0.3V
Package Thermal Resistance
TQFN-4×5-24AL, θ_{JA}.. 31.1℃/W
TQFN-4×5-24AL, θ_{JB}.. 9.4℃/W
TQFN-4×5-24AL, $\theta_{JC\ (TOP)}$ .... 20.7℃/W
TQFN-4×5-24AL, $\theta_{JC\ (BOT)}$ .... 1.4℃/W
Package Thermal Characterization Parameter
TQFN-4×5-24AL, ψ_{JT} .... 0.2℃/W
TQFN-4×5-24AL, ψ_{JB} .... 8.9℃/W
Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility (2) (3)
HBM...±2000V
CDM ....±1000V

NOTES:

1. The GATE pin voltage is typically 7.5V above VIN when the SGM25720 is enabled. Therefore, the Absolute Maximum Rating of 24V for VIN and SENSE apply only when the SGM25720 is disabled or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is 20V.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VIN, SENSE, OUT Voltage.................................2.9V to 18V
VDD...2.9V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SIMPLIFIED SCHEMATIC

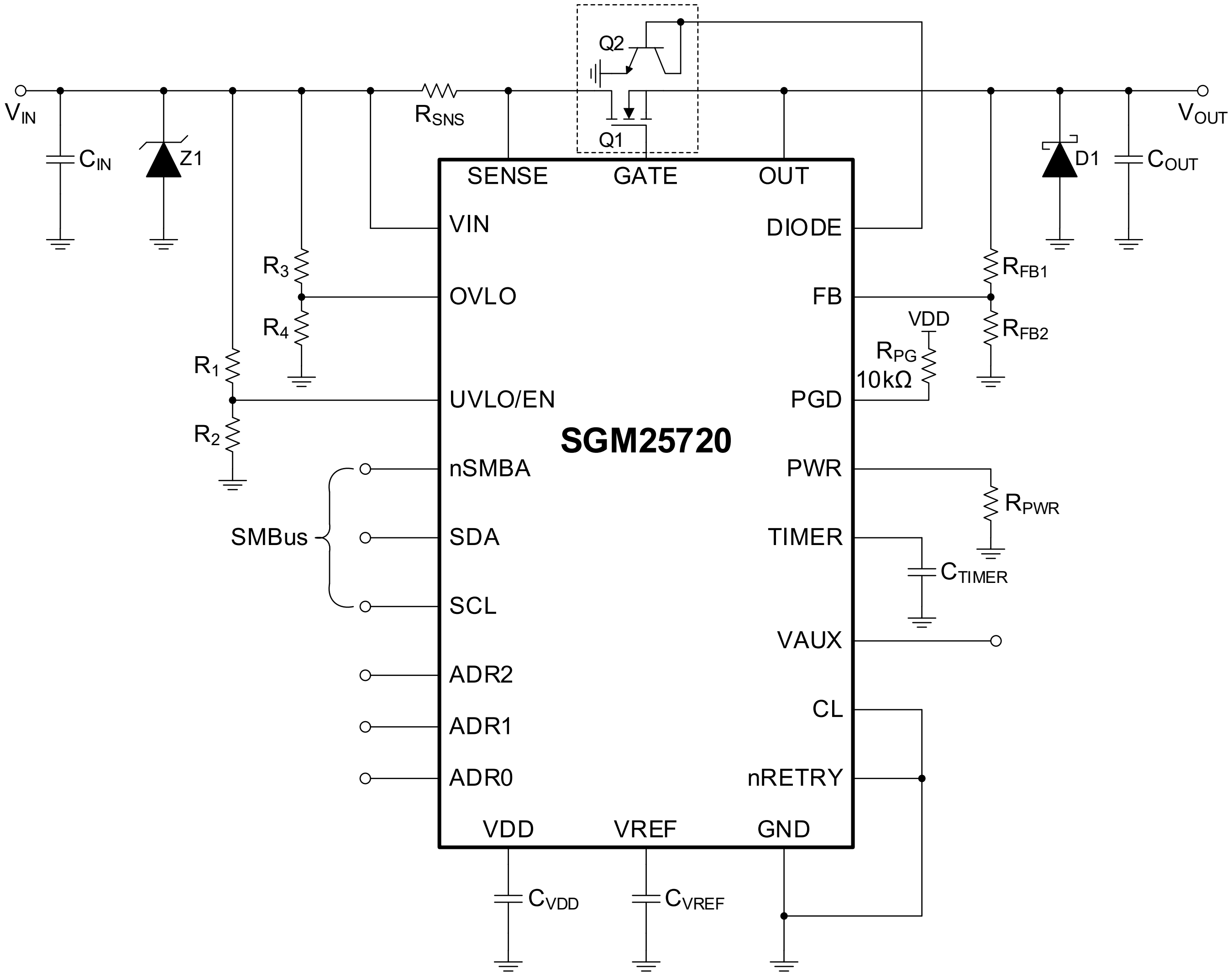
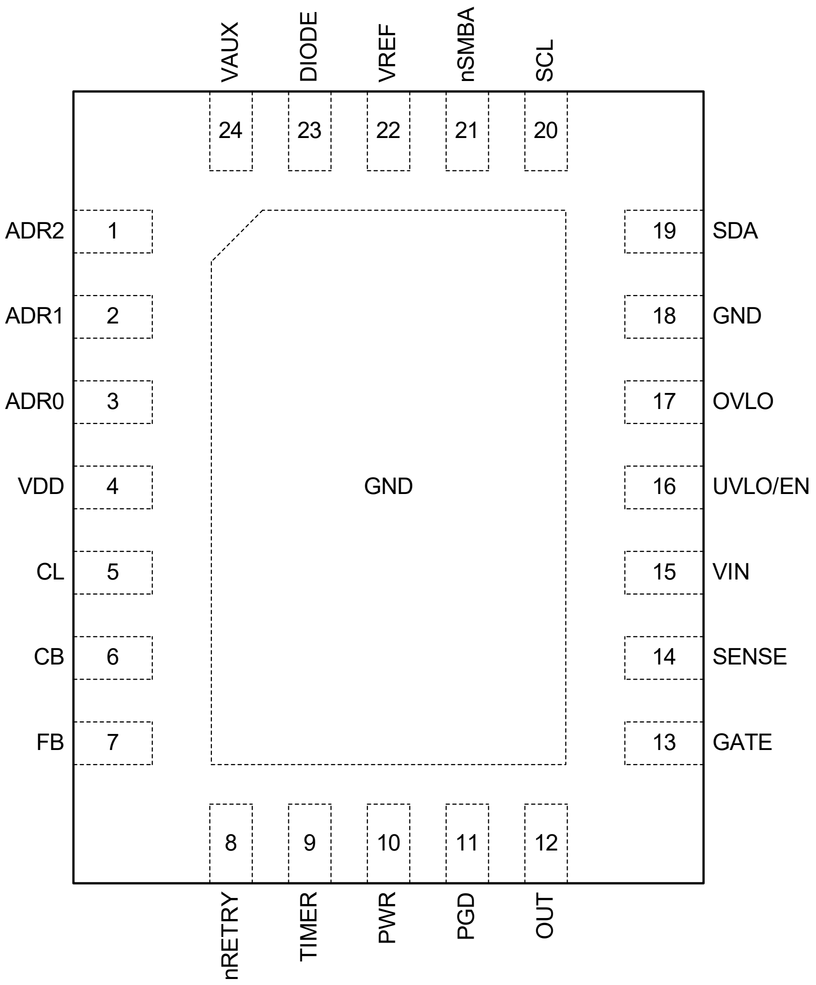


Figure 1. Simplified Schematic

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×5-24AL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	ADR2	SMBUS Address Line 2. 3-state address line. Should be connected to VDD or GND or left floating.
2	ADR1	SMBUS Address Line 1. 3-state address line. Should be connected to VDD or GND or left floating.
3	ADR0	SMBUS Address Line 0. 3-state address line. Should be connected to VDD or GND or left floating.
4	VDD	Internal Sub-Regulator Output. Internally sub-regulated 4.5V bias supply. Connect a 1μF capacitor between pin to ground.
5	CL	Current Limit Range. Connect this pin to GND to configure the over-current threshold at 24.5mV. When the pin is connected to VDD, the over-current threshold will be set to 45mV.
6	CB	Circuit Breaker Range. This pin determines the circuit breaker protection level relative to the over-current trip threshold. Connect this pin to GND configures the circuit breaker point at 1.8 times the over-current threshold. When the pin is connected to VDD, the circuit breaker trip level is set to 3.6 times the over-current threshold.
7	FB	Power Good Feedback. An external resistor divider connected to the OUT pin defines the output voltage that triggers the switching of the PGD pin. The pin's threshold voltage is specified as 1.163V. Hysteresis is added by an internal current source rated at 23μA.
8	nRETRY	Fault Retry Input. This pin sets the power-up fault retry functionality. Connecting this pin to GND, the device repeatedly attempts power engagement when a fault occurs. Connecting the pin to VDD will cause the device to latch-off upon detecting a fault.
9	TIMER	Timing Capacitor. An external capacitor connected to this pin configures the insertion time delay, fault timeout duration and restart timing.
10	PWR	Power Limit Set. An external resistor attached to this pin, together with the current sense resistor (R_{SNS}), determines the maximum permissible power dissipation of the external power MOSFET
11	PGD	Power Good Indicator. The pin stays high when the voltage at the FB pin exceeds 1.163V.
12	OUT	Output Feedback. Connect this pin to the output rail (the source of the external MOSFET). Internally, it is utilized to calculate the V_{DS} voltage of the MOSFET for power limiting purposes and to keep track of the output voltage.
13	GATE	Gate Drive Output. This pin is the gate drive of an external N-channel FET.
14	SENSE	Current Sense Input. The voltage drop across the current sense resistor (R_{SNS}) is detected between VIN pin and this pin. When the voltage across R_{SNS} meets or exceeds the over-current threshold, the load current is restricted and the fault timer is triggered.
15	VIN	Positive Supply Input. Connect a small ceramic bypass capacitor near this pin to suppress transients that arise when the load current is turned off.
16	UVLO/EN	Under-Voltage Lockout or Enable Control. An external resistor divider connected to the system input voltage configures the under-voltage turn-on threshold. Hysteresis is provided by an internal 23μA current source. The enable threshold voltage of this pin is specified as 1.16V. Additionally, this pin supports remote shutdown functionality.
17	OVLO	Over-Voltage Lockout. An external resistor divider linked to the system input voltage defines the over-voltage turn-off threshold. An internal current source rated at 23μA delivers hysteresis. The disable threshold voltage for this pin is specified as 1.16V.
18	GND	Circuit Ground.
19	SDA	SMBus Data Pin. Data pin for SMBus.
20	SCL	SMBus Clock. Clock pin for SMBus.
21	nSMBA	SMBus Alert Line. Alert pin for SMBus. Active low. This is an open-drain output that requires an external pull-up resistor connected to VDD or another voltage supply.
22	VREF	Internal Reference. An internally generated precision 2.73V reference is utilized for analog-to-digital conversion. A 1μF capacitor should be connected from this pin to ground for bypassing purposes.
23	DIODE	External Diode. Connecting this pin to an NPN transistor configured as a diode for temperature sensing. Ground the pin if it is not in use.
24	VAUX	Auxiliary Voltage Input. This pin allows voltage telemetry from an external source, with a full-scale input of 1.16V.
Exposed Pad	GND	Connect to Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = -40℃ to +125℃. Typical values are measured at T_J = +25℃, unless otherwise noted.) (1)(2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input (VIN Pin)						
Input Current, Enabled	I_{IN_EN}	V_{UVLO} = 2V and V_{OVLO} = 0.7V		2	4	mA
Power-On Reset Threshold at VIN	POR	V_{IN} increasing		2.7	2.89	V
POR_{EN} Hysteresis	POR_{HYS}	V_{IN} decreasing		100		mV
VDD Regulator (VDD Pin)						
VDD Regulator Output Voltage	V_{DD}	I_{VDD} = 5mA, V_{IN} = 12V	4.3	4.5	4.7	V
		I_{VDD} = 5mA, V_{IN} = 4.5V	4.2	4.4	4.6	V
VDD Current Limit	V_{DDILIM}		25	45		mA
UVLO/EN, OVLO Pins						
UVLO Threshold	$UVLO_{TH}$	V_{UVLO} falling	1.138	1.16	1.181	V
UVLO Hysteresis Current	$UVLO_{HYS}$	V_{UVLO} = 1V	18	23	28	μA
UVLO Delay	$UVLO_{DELAY}$	Delay to GATE high		8		μs
		Delay to GATE low		20		
UVLO Bias Current	$UVLO_{BIAS}$	V_{UVLO} = 3V			1	μA
OVLO Threshold	$OVLO_{TH}$	V_{OVLO} rising	1.138	1.16	1.181	V
OVLO Hysteresis Current	$OVLO_{HYS}$	V_{OVLO} = 3V	-28	-23	-18	μA
OVLO Delay	$OVLO_{DELAY}$	Delay to GATE high		20		μs
		Delay to GATE low		9		
OVLO Bias Current	$OVLO_{BIAS}$	V_{OVLO} = 1V			1	μA
Power Good (PGD Pin)						
Output Low Voltage	PGD_{VOL}	I_{SINK} = 2mA		27	60	mV
Off Leakage Current	PGD_{IOH}	V_{PGD} = 18V			1	μA
Power Good Delay	PGD_{DELAY}	V_{FB} to V_{PG}		170		ns
FB Pin						
FB Threshold	FB_{TH}	V_{FB} rising	1.132	1.163	1.193	V
FB Hysteresis Current	FB_{HYS}	V_{FB} = 3V	-28	-23	-18	μA
Off Leakage Current	FB_{LEAK}	V_{FB} = 1V			1	μA
Power Limit (PWR Pin)						
Power Limit Sense Voltage ($V_{IN-SENSE}$)	PWR_{LIM}	$V_{SENSE-OUT}$ = 12V, R_{PWR} = 25kΩ	10	12.5	15	mV
PWR Pin Current	I_{PWR}	V_{PWR} = 2.5V		-10		μA
PWR Pin Impedance when Disabled	R_{SAT_PWR}	V_{UVLO} = 1.0V, I_{PWR} = -2mA		190		Ω
Gate Control (GATE Pin)						
Source Current	I_{GATE}	V_{GATE} = 5V	-27.5	-21	-15.5	μA
Fault Sink Current		V_{UVLO} = 1V, V_{GATE} = 5V	1.5	2	2.5	mA
POR Circuit Breaker Sink Current		$V_{IN-SENSE}$ = 150mV, V_{GATE} = 5V	100	175	255	mA
Gate Output Voltage in Normal Operation	V_{GATE}	GATE voltage with respect to ground	17	18.8	20.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, T_A = -40℃ to +125℃. Typical values are measured at T_J = +25℃, unless otherwise noted.) (1)(2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT Pin						
OUT Bias Current, Enabled	I_{OUT_EN}	V_{OUT} = V_{IN}, normal operation		16		μA
OUT Bias Current, Disabled (3)	I_{OUT_DIS}	Disabled, V_{OUT} = 0V, V_{SENSE} = V_{IN}		-5		μA
Current Limit						
Threshold Voltage	V_{CL}	CL = GND	21.5	24.5	27.3	mV
		CL = VDD	40.5	45	49.3	
SENSE Input Current	I_{SENSE}	Enabled, SENSE = OUT		28		μA
		Disabled, OUT = 0V		45		
		Enabled, OUT = 0V		45		
Circuit Breaker						
Threshold Voltage × 1.8	V_{CB}	CL = GND, CB = GND	35	45	55	mV
CB:CL Ratio		V_{CB}/V_{CL}	1.6	1.8	2.0	
Threshold Voltage × 3.6	V_{CB}	CL = GND, CB = VDD	70	88	100	mV
CB:CL Ratio		V_{CB}/V_{CL}	3.3	3.6	3.7	
Timer (TIMER Pin)						
Upper Threshold	V_{TMRH}		1.54	1.7	1.86	V
Lower Threshold	V_{TMRL}	Restart cycles	0.85	1.0	1.085	V
		End of 8th cycle		0.3		
		Re-enable threshold		0.3		
Insertion Time Current	I_{TIMER}	TIMER pin = 2V	-8	-5.5	-3	μA
Sink Current, End of Insertion Time			1.4	1.8	2.4	mA
Fault Detection Current			-120	-90	-60	μA
Fault Sink Current				2.8		μA
Fault Restart Duty Cycle	DC_{FAULT}			0.67		%
Internal Reference						
Reference Voltage	V_{REF}	T_A = -40℃ to +85℃	2.703	2.73	2.757	V
ADC and MUX						
Resolution				12		Bits
Integral Non-Linearity	INL	ADC only		±1		LSB
Telemetry Accuracy						
Current Input Full-Scale Range	IIN_{FSR}	CL = GND		30.2		mV
		CL = VDD		60.4		mV
Current Input LSB	IIN_{LSB}	CL = GND		7.32		μV
		CL = VDD		14.64		μV
VAUX Input Full-Scale Range	$VAUX_{FSR}$			1.16		V
VAUX Input LSB	$VAUX_{LSB}$			283.2		μV
Input Voltage Full-Scale Range	VIN_{FSR}			18.7		V
Input Voltage LSB	VIN_{LSB}			4.54		mV
Input Current Accuracy (4)	IIN_{ACC}	T_A = -40℃ to +85℃, $V_{IN\text{-}SENSE}$ = 25mV, CL = GND	-1.8		1.8	%
VAUX, VIN, VOUT Accuracy (4)	V_{ACC}	T_A = -40℃ to +85℃, V_{IN}, V_{OUT} = 12V, V_{AUX} = 1V	-1		1	%
Input Power Accuracy (4)	PIN_{ACC}	T_A = -40℃ to +85℃, V_{IN} = 12V, $V_{IN\text{-}SENSE}$ = 25mV, CL = GND	-2.2		2.2	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, T_A = -40℃ to +125℃. Typical values are measured at T_J = +25℃, unless otherwise noted.) (1)(2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Remote Diode Temperature Sensor						
Temperature Accuracy Using Local Diode (5)	T_{ACC}			2	10	℃
Remote Diode Resolution				9		Bits
External Diode Current Source	I_{DIODE}	High level		260	300	μA
		Low level		10		μA
Diode Current Ratio				26		
PMBus Pin Thresholds (nSMBA, SDA, SCL)						
Data, Clock Input Low Voltage	V_{IL}				0.8	V
Data, Clock Input High Voltage	V_{IH}		2.1		5.5	V
Data Output Low Voltage	V_{OL}	I_{PULLUP} = 500μA	0		0.4	V
Input Leakage Current	I_{LEAK}	SDA, nSMBA, SCL = 5V			1	μA
Configuration Pin Thresholds (CB, CL, nRETRY)						
Threshold Voltage	V_{IH}		3			V
Input Leakage Current	I_{LEAK}	CL, CB, nRETRY = 5V			100	μA

NOTE:

1. A negative value is used to denote the current flowing out of a pin.

2. All limits are defined. During production, all electrical characteristics with room-temperature limits are tested at an ambient temperature (T_A) of +25℃. All high and low temperature limits are established by correlating electrical characteristics with process and temperature fluctuations, along with the implementation of statistical process control.

3. OUT bias current results from leakage current passing through an internal 0.9MΩ resistor connecting SENSE to VOUT.

4. Initial accuracy.

5. This parameter is guaranteed by design and characterization; not production tested.

SWITCHING CHARACTERISTICS

(Typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit						
Response Time	t_{CL}	$V_{IN-SENSE}$ stepped from 0mV to 80mV		1.2		μs
Circuit Breaker						
Response Time	t_{CB}	$V_{IN-SENSE}$ stepped from 0mV to 150mV, time to GATE low, no load		0.4	1.2	μs
Timer (TIMER Pin)						
Upper Threshold to GATE Low Delay	t_{FAULT_DELAY}	TIMER pin trigger the upper threshold		17		μs
ADC and MUX						
Acquisition + Conversion Time	t_{AQUIRE}	Any channel		120		μs
Acquisition Round Robin Time	t_{RR}	Cycle all channels		1		ms

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SMBus Operating Frequency	f_{SMB}	10		400	kHz
Bus Free Time from Stop to Start Condition	t_{BUF}	1.3			μs
Start Hold Time	t_{HD_STA}	0.6			μs
Repeated Start Condition Setup Time	t_{SU_STA}	0.6			μs
Stop Condition Setup Time	t_{SU_STO}	0.6			μs
Data Hold Time	t_{HD_DAT}	300			ns
Data Setup Time	t_{SU_DAT}	100			ns
Clock Low Time-Out (1)	$t_{TIMEOUT}$	25		35	ms
Clock Low Period	t_{LOW}	1.5			μs
Clock High Period (2)	t_{HIGH}	0.6			μs
Cumulative Clock Low Extend Time (Slave Device) (3)	t_{LOW_SEXT}			25	ms
Cumulative Low Extend Time (Master Device) (4)	t_{LOW_MEXT}			10	ms
Clock or Data Fall Time (5)	t_F	20		300	ns
Clock or Data Rise Time (5)	t_R	20		300	ns

NOTES:

1. Device involved in a data transfer will trigger a timeout if the clock remains low for longer than the minimum timeout value ($t_{TIMEOUT\_MIN}$) of 25ms. Upon detecting a timeout, devices must reset the communication process no later than the maximum timeout threshold ($t_{TIMEOUT\_MAX}$) of 35ms. Strict adherence to this aggregate ceiling is mandatory for both the master and slave devices, as it encompasses the cumulative clock stretching allowances of 10ms and 25ms, respectively.

2. The maximum high time (t_{HIGH_MAX}) serves as a straightforward means for devices to identify bus idle states.

3. The parameter t_{LOW_SEXT} defines the maximum permissible clock stretching duration a slave device may assert during a complete transmission cycle (Start-to-Stop). Should this threshold be breached, the device is required to relinquish control of the SDA and SCL lines and perform an internal reset.

4. t_{LOW_MEXT} denotes the total time a master device is allowed to extend its clock cycles within each byte of a message, as specified from Start-to-Acknowledgment, Acknowledgment-to-Acknowledgment, or Acknowledgment-to-Stop.

5. Rise time (t_R) and fall time (t_F) are defined as follows: t_R spans from (V_{ILMAX} - 0.15V) to (V_{IHMIN} + 0.15V), and t_F ranges from 0.9 × V_{DD} to (V_{ILMAX} - 0.15V).

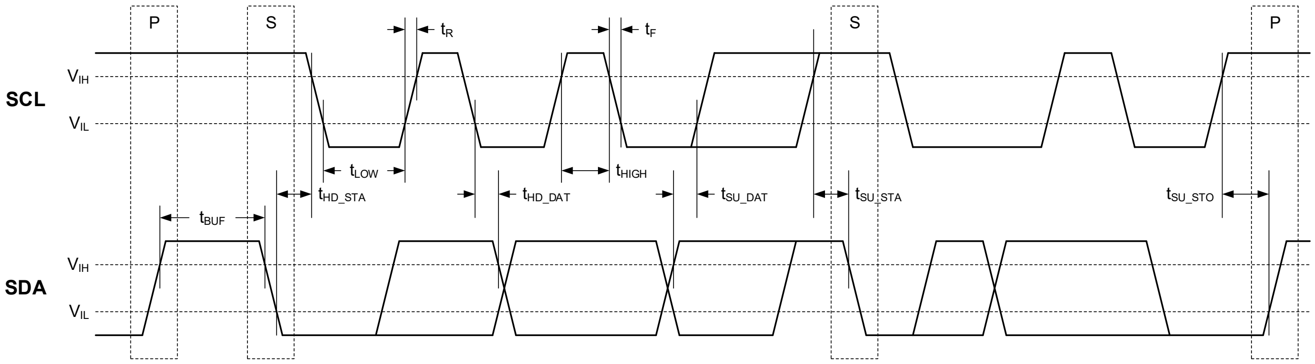
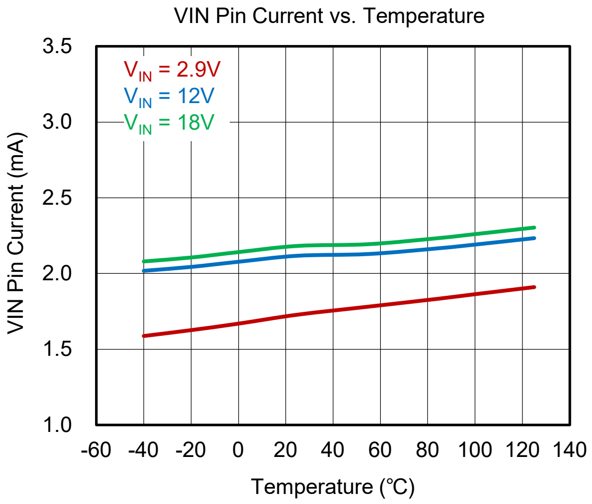
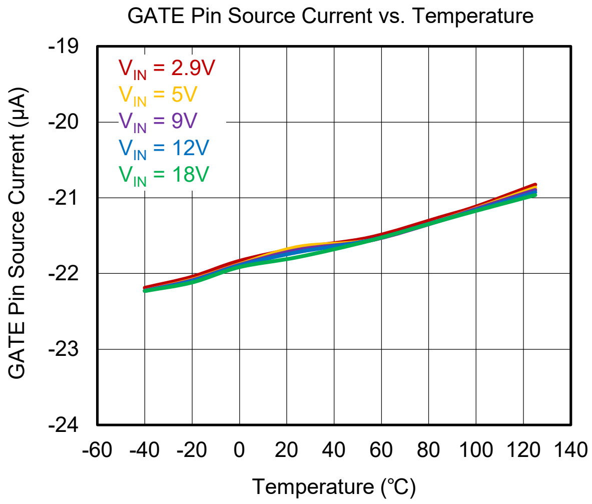


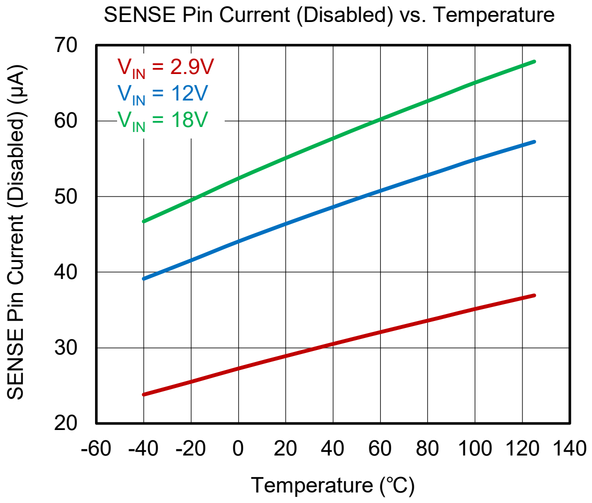
Figure 2. SMBus Timing Diagram

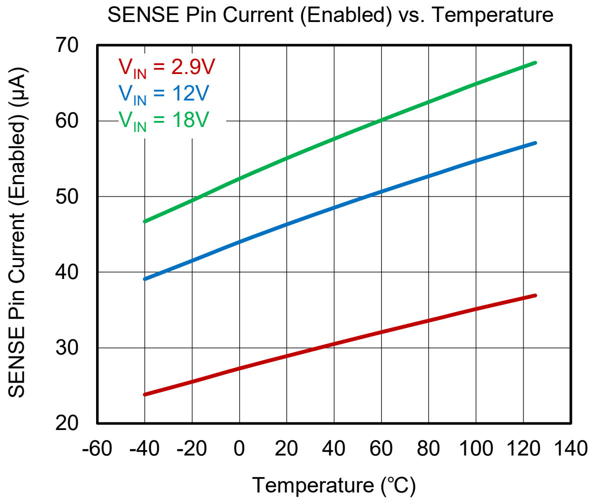
TYPICAL PERFORMANCE CHARACTERISTICS

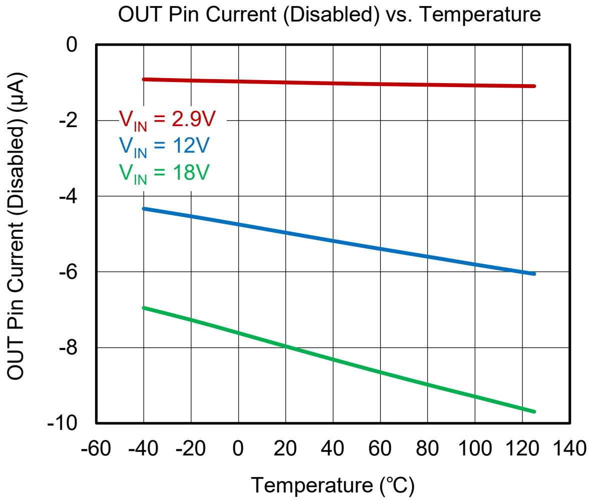
T_A = +25℃, unless otherwise noted.

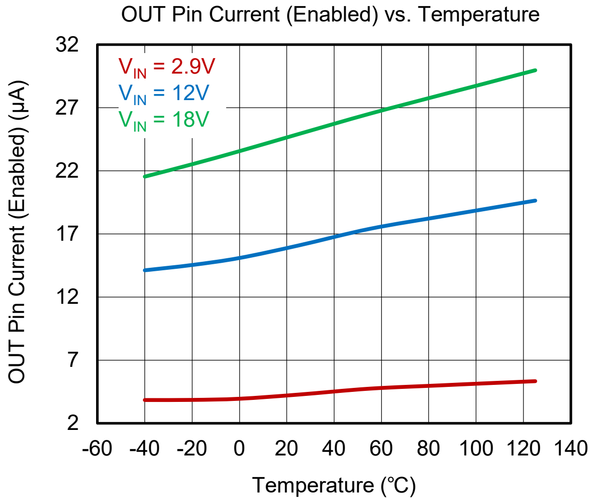






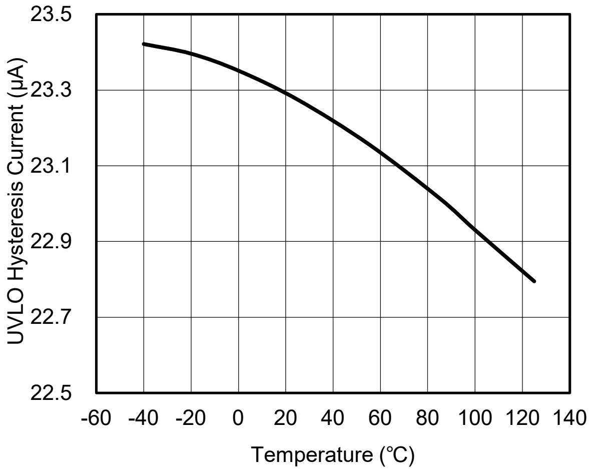


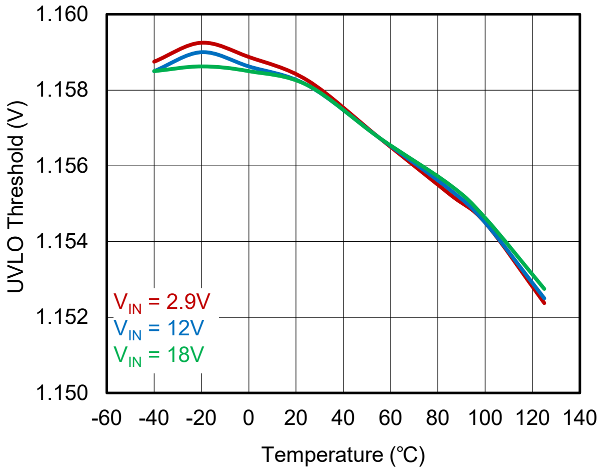


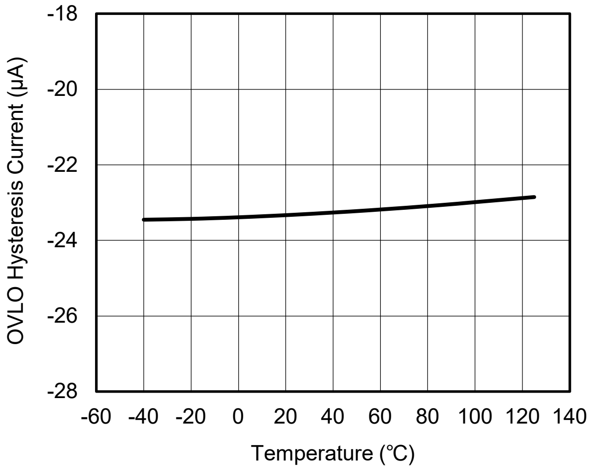


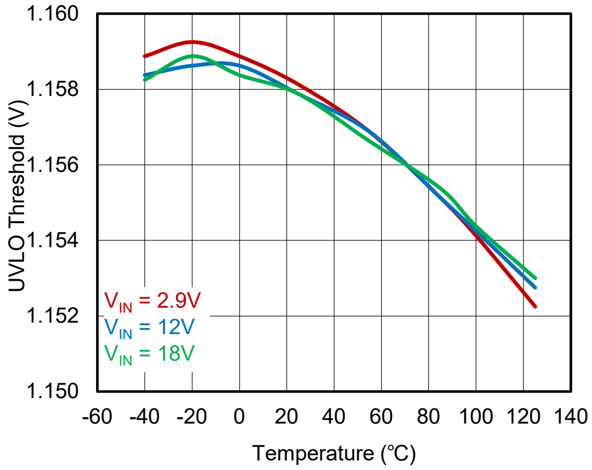
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

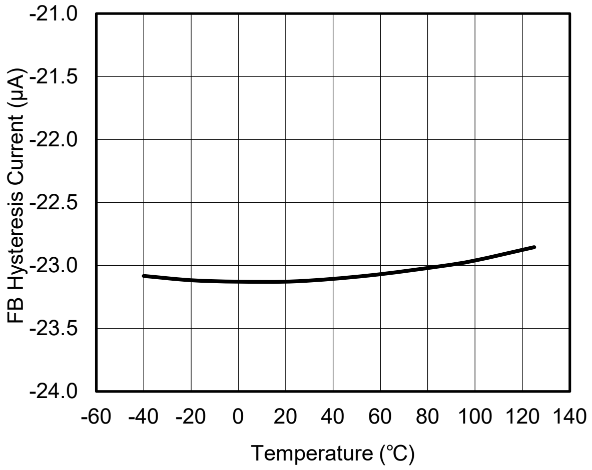
T_A = +25℃, unless otherwise noted.

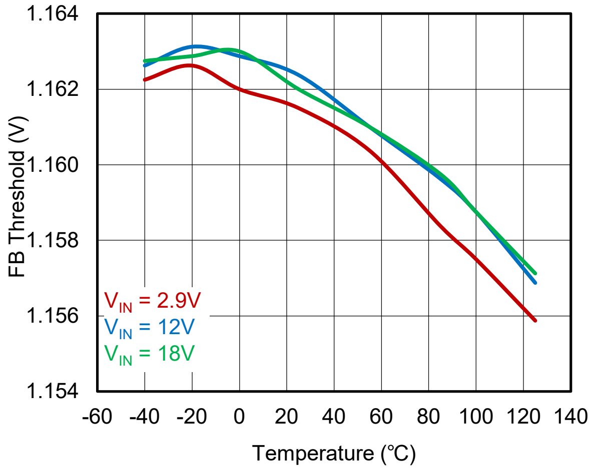

UVLO Hysteresis Current vs. Temperature


UVLO Threshold vs. Temperature


OVLO Hysteresis Current vs. Temperature

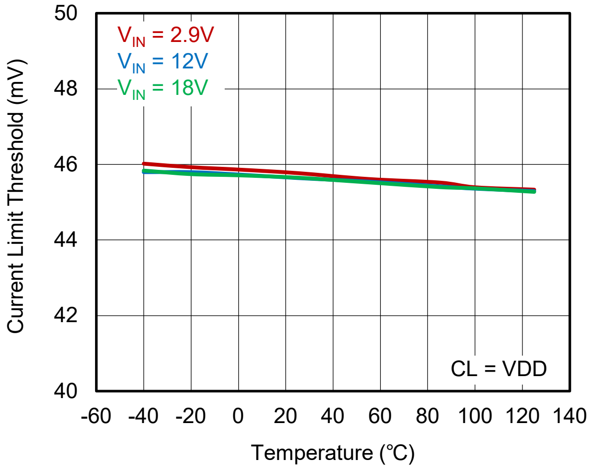

OVLO Threshold vs. Temperature


FB Hysteresis Current vs. Temperature

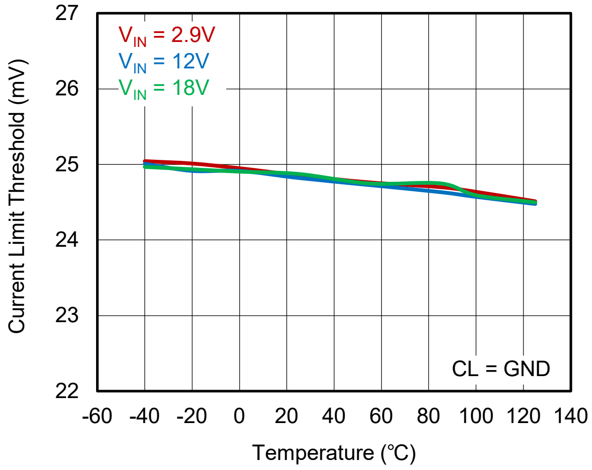

FB Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

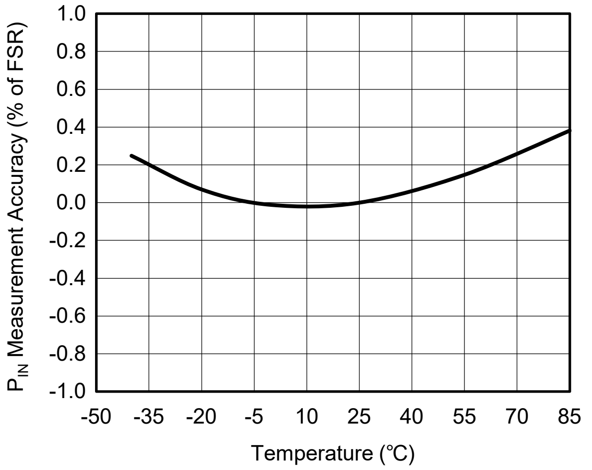
T_A = +25℃, unless otherwise noted.



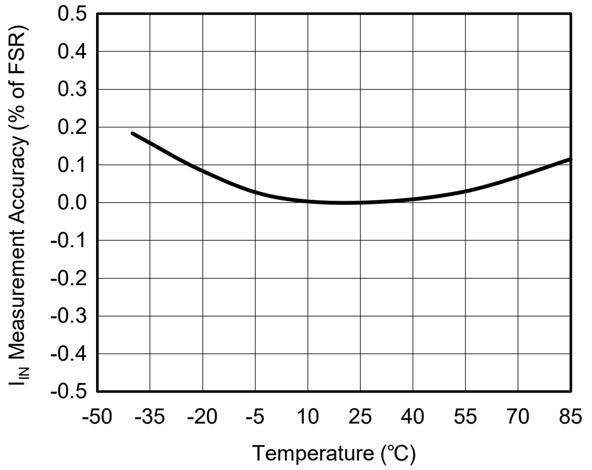
Current Limit Threshold vs. Temperature



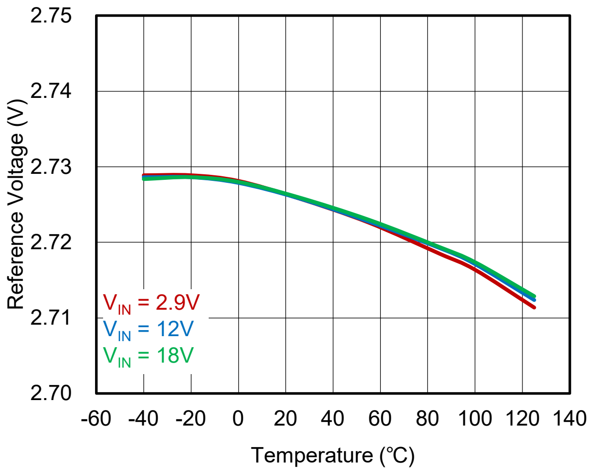
Current Limit Threshold vs. Temperature



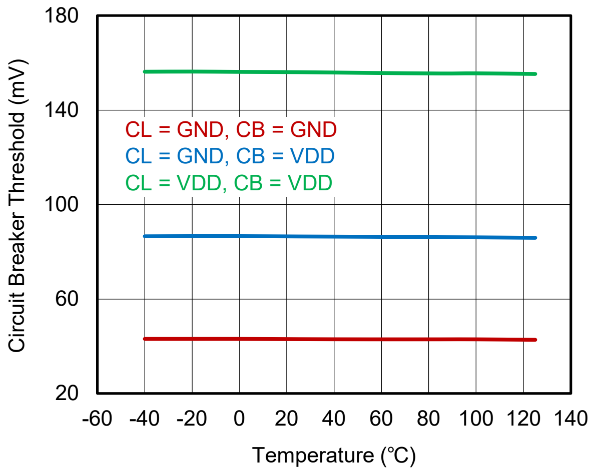
P_{IN} Measurement Accuracy vs. Temperature



I_{IN} Measurement Accuracy vs. Temperature



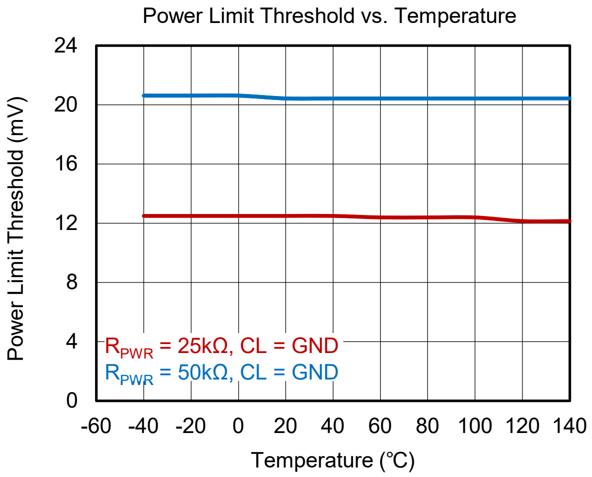
Reference Voltage vs. Temperature

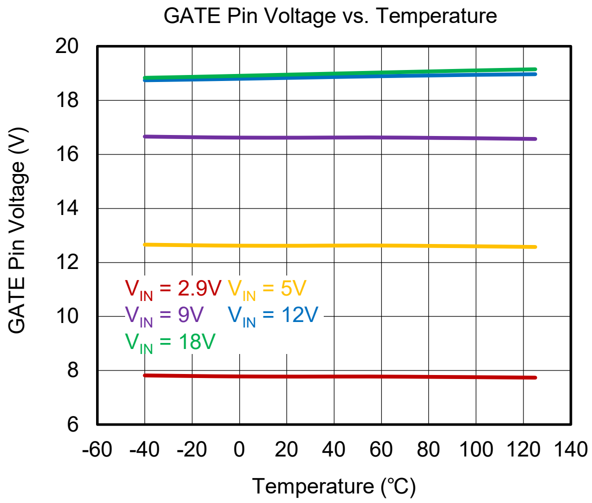


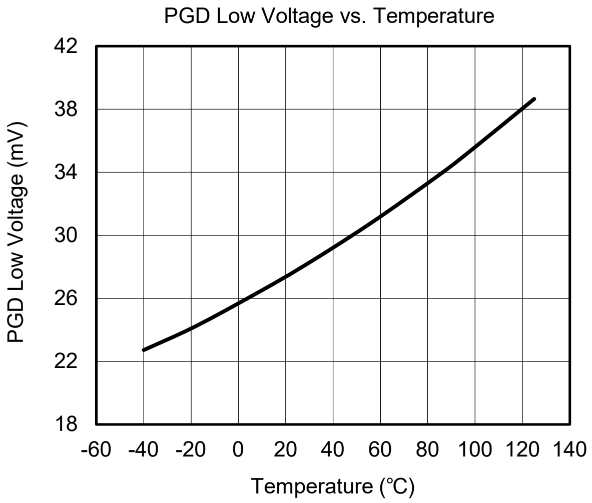
Circuit Breaker Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.



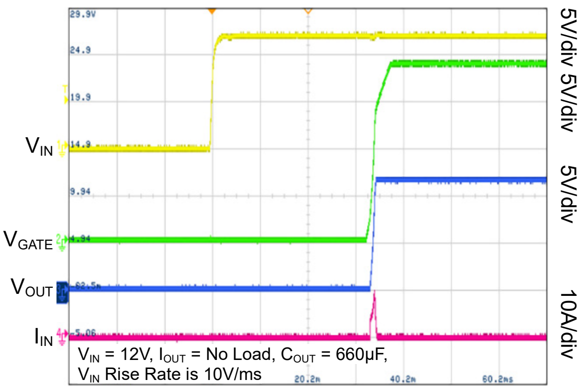




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

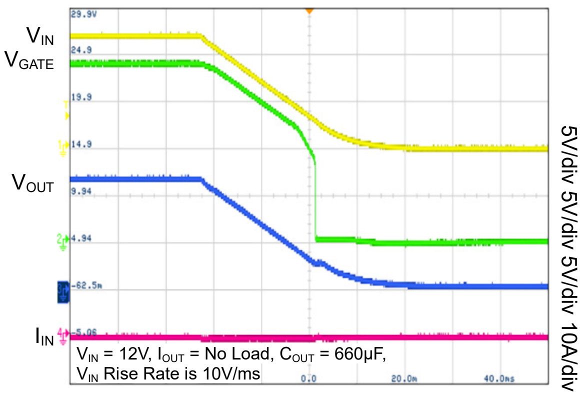
T_A = +25℃, R_{SNS} = 1mΩ, C_{TIMER} = 100nF, CL = GND and R_{PWR} = 6.98kΩ, unless otherwise noted.

VIN Power On



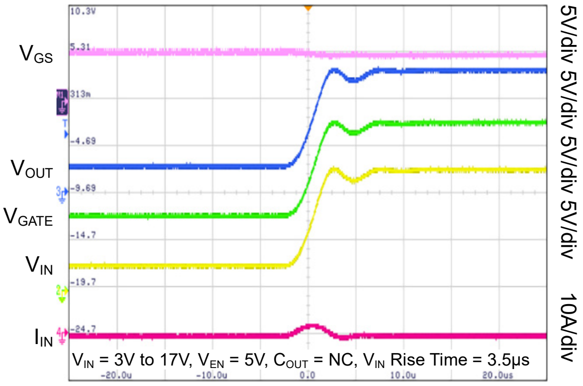
Time (10ms/div)

VIN Power Off



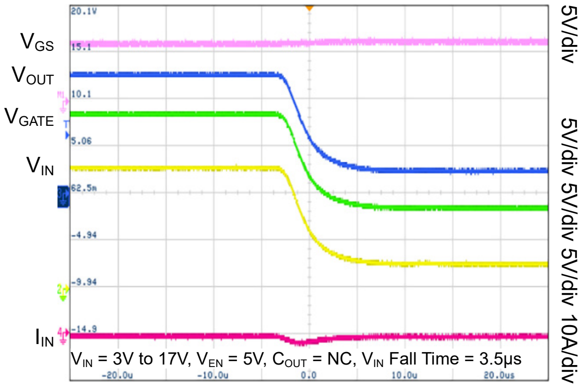
Time (10ms/div)

Line Transient



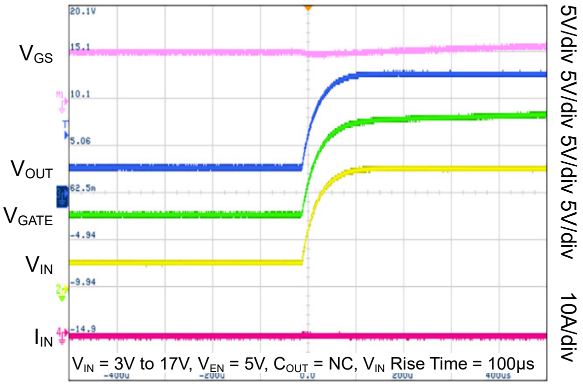
Time (5μs/div)

Line Transient



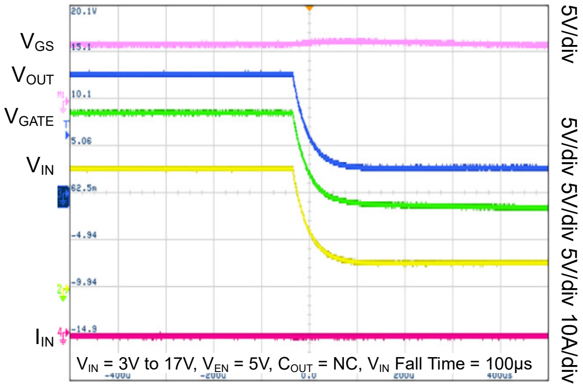
Time (5μs/div)

Line Transient



Time (100μs/div)

Line Transient

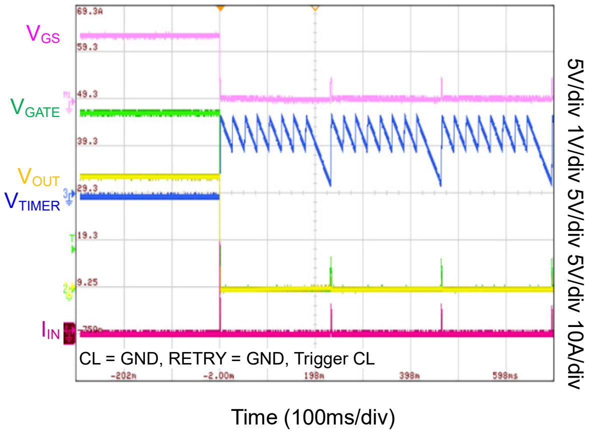


Time (100μs/div)

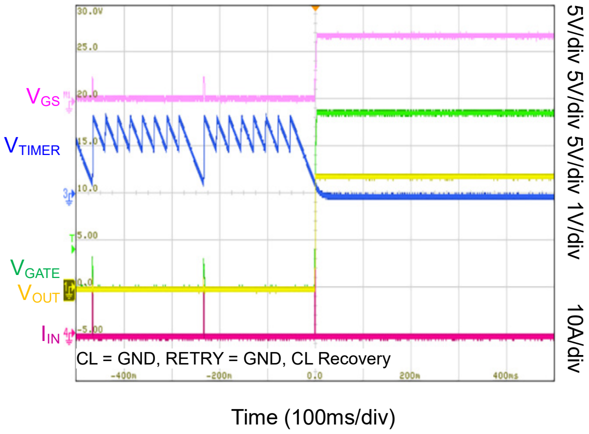
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{EN} = 5V, R_{SNS} = 2mΩ, C_{OUT} = 660μF, C_{TIMER} = 100nF and R_{PWR} = 100kΩ, unless otherwise noted.

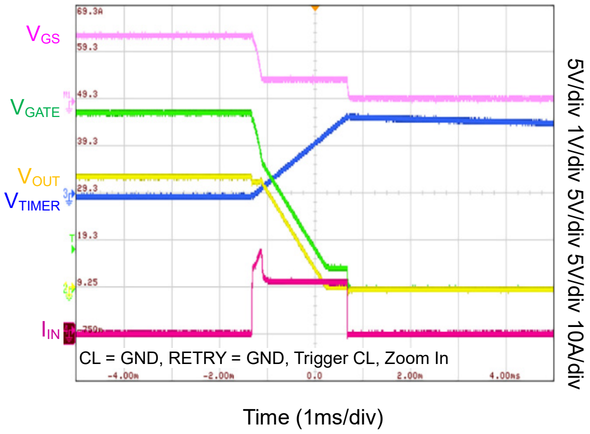
Over-Current Protection



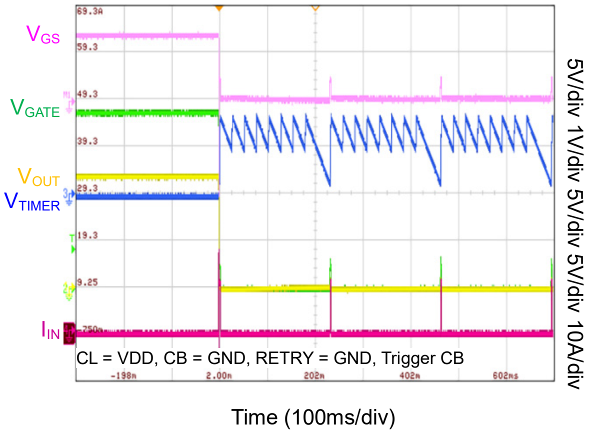
Over-Current Protection



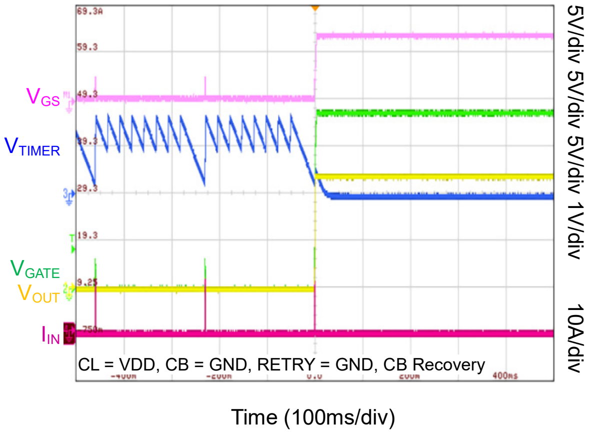
Over-Current Protection



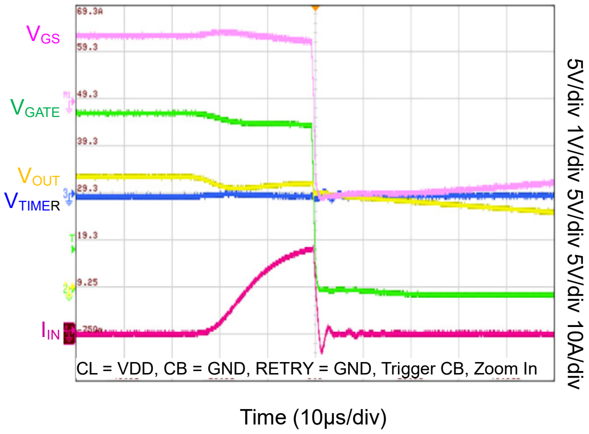
Short-Circuit Protection



Short-Circuit Protection



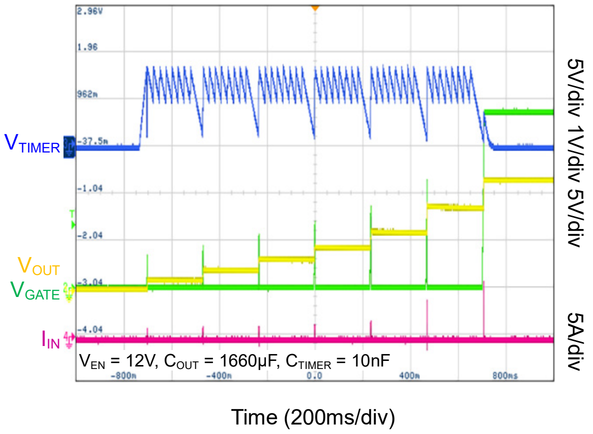
Short-Circuit Protection



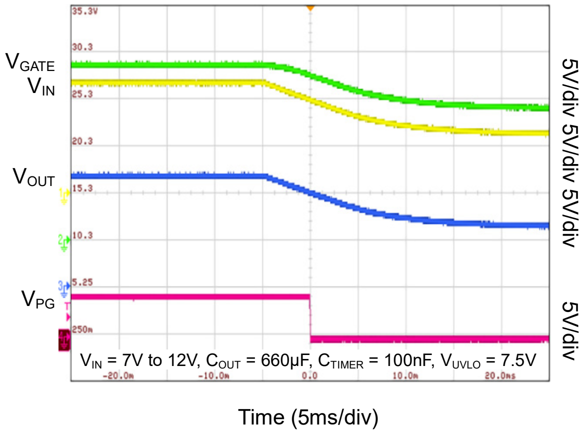
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, R_{SNS} = 2mΩ and R_{PWR} = 6.98kΩ, unless otherwise noted.

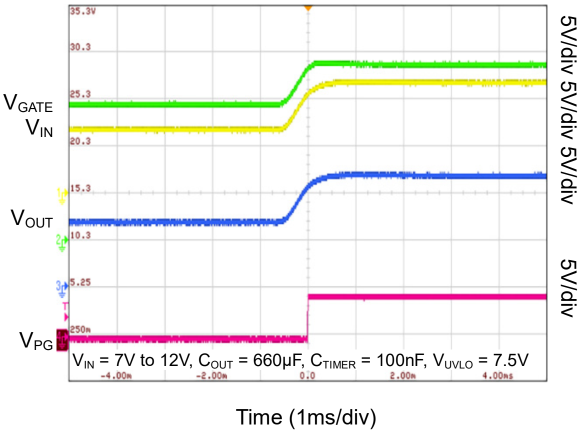
Over Power



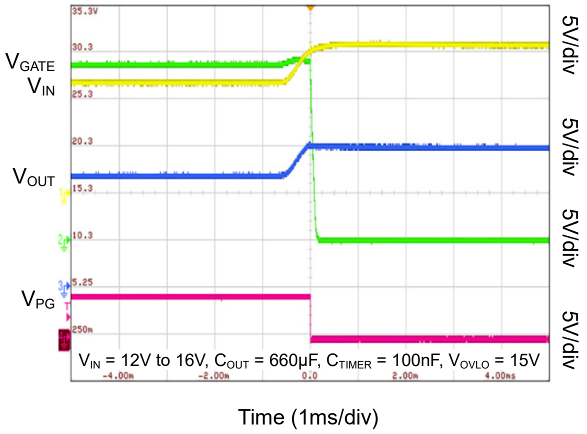
VIN UVLO Protection



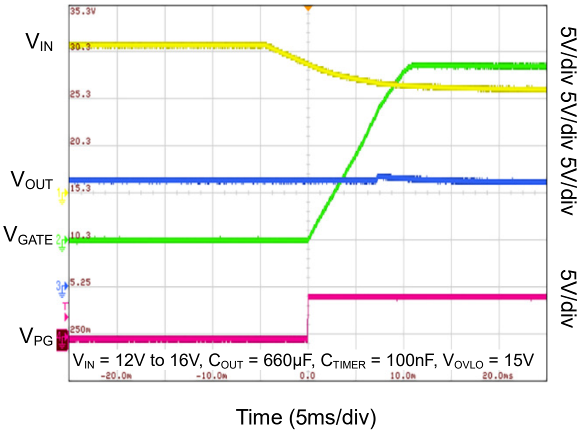
VIN UVLO Protection



VIN OVLO Protection



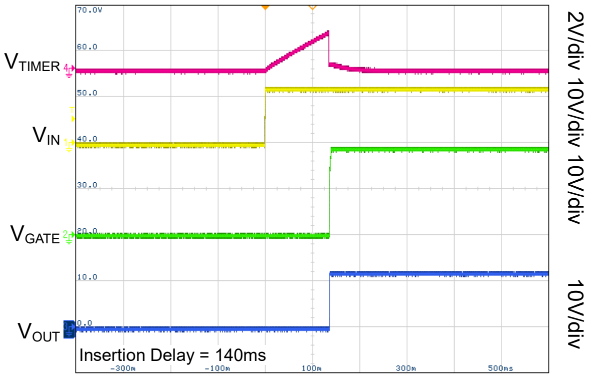
VIN OVLO Protection



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

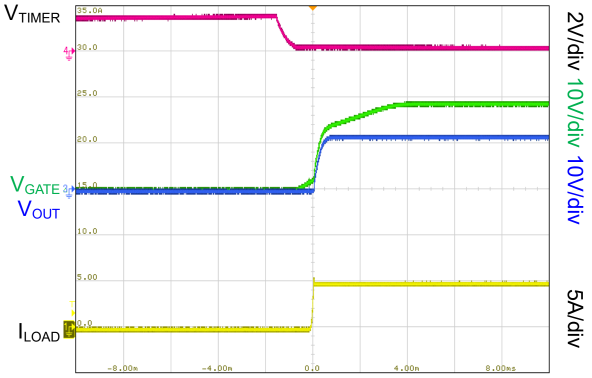
T_A = +25℃, R_{SNS} = 2mΩ and R_{PWR} = 6.98kΩ, unless otherwise noted.

Start-up (Insertion Delay)



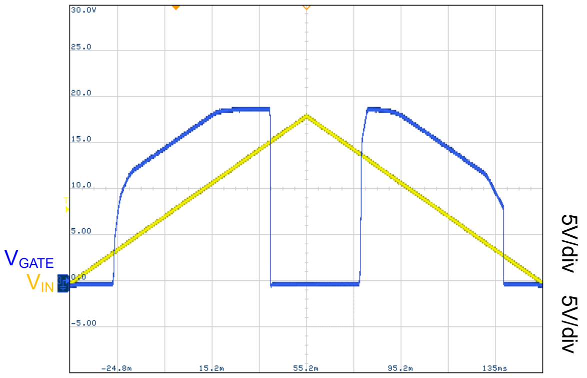
Time (100ms/div)

Start-up (5A Load)



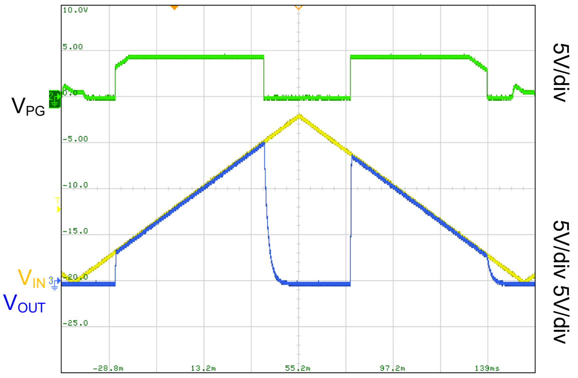
Time (2ms/div)

Start-up (UVLO, OVLO)



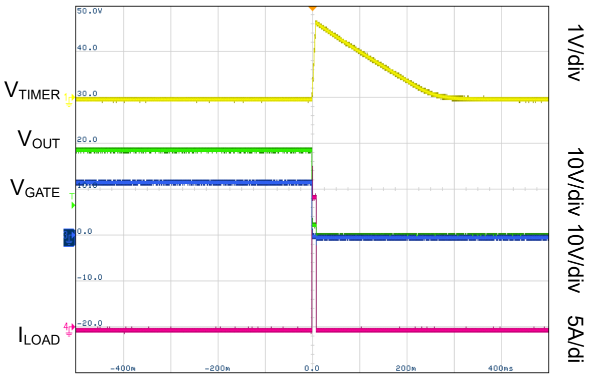
Time (20ms/div)

Start-up (PGOOD)



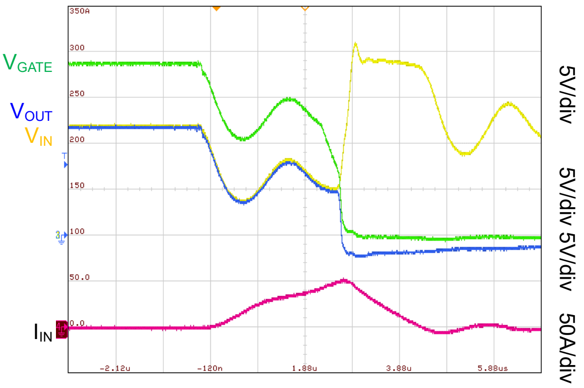
Time (21ms/div)

Latch Off (Retry = VDD)



Time (100ms/div)

Hot-Short on VOUT (Zoomed In)



Time (1μs/div)

FUNCTIONAL BLOCK DIAGRAM

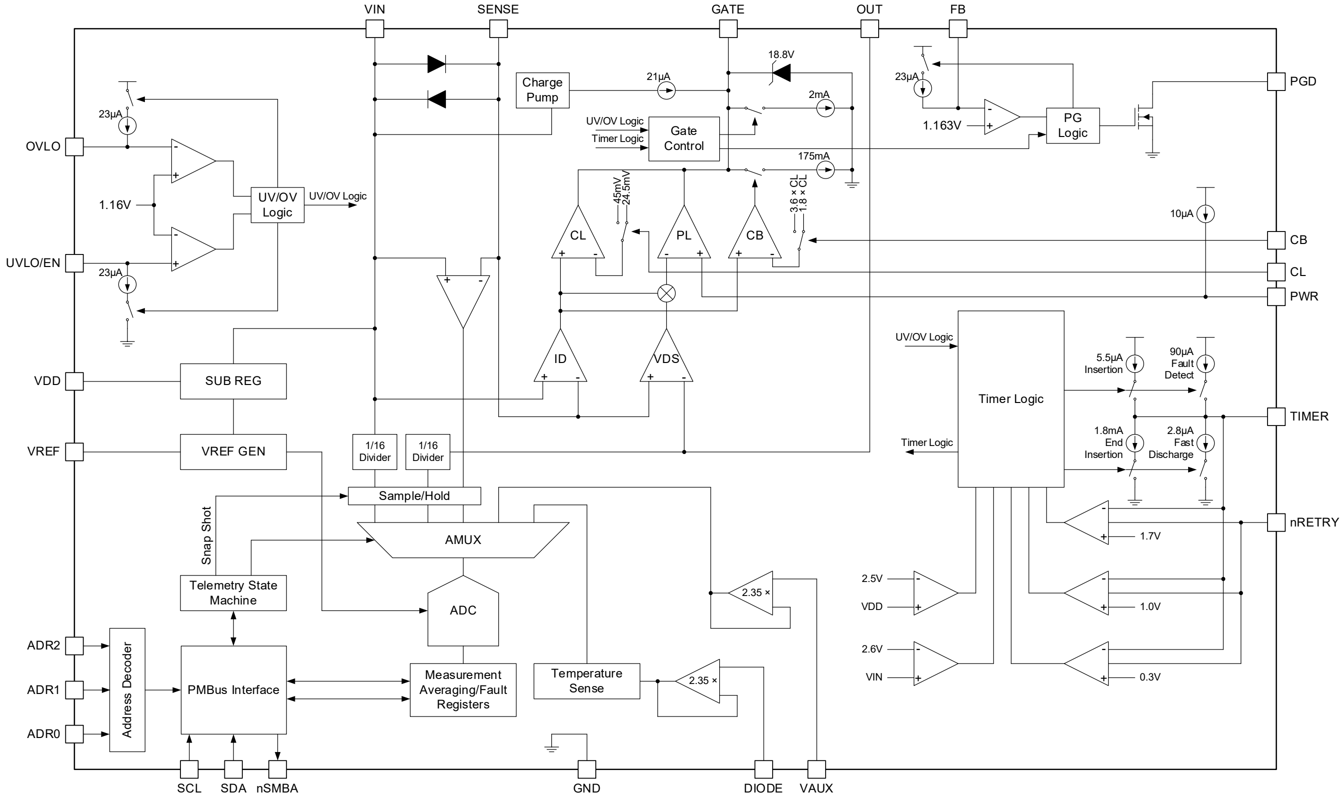


Figure 3. SGM25720 Block Diagram

PROGRAMMING

PMBus Command Support

SMBus interface is incorporated into the chip; relevant PMBus codes can configure alert limits and error masking while capturing VIN, VOUT, IIN, VAUX and PIN measurement data. See Table 1 for the complete PMBus command roster.

Table 1. Supported PMBus Commands

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
01h	OPERATION	Report or setting the operation status	R/W	1	80h
03h	CLEAR_FAULTS	Clears the status registers and re-arms the black box registers for updating	Send byte	0	
19h	CAPABILITY	Report the device capability	R	1	B0h
43h	VOUT_UV_WARN_LIMIT	Report or setting output under-voltage warn limit threshold	R/W	2	0000h
4Fh	OT_FAULT_LIMIT	Report or setting over-temperature fault limit threshold	R/W	2	0960h (150℃)
51h	OT_WARN_LIMIT	Report or setting over-temperature warn limit threshold	R/W	2	07D0h (125℃)
57h	VIN_OV_WARN_LIMIT	Report or setting input over-voltage warn limit threshold	R/W	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Report or setting input under-voltage warn limit threshold	R/W	2	0000h
78h	STATUS_BYTE	Report information about the parts operating status	R	1	01h
79h	STATUS_WORD	Report information about the parts operating status	R	2	3849h
7Ah	STATUS_VOUT	Report information about output voltage status	R	1	00h
7Ch	STATUS_INPUT	Report information about input status	R	1	10h
7Dh	STATUS_TEMPERATURE	Report information about temperature status	R	1	00h
7Eh	STATUS_CML	Report information about communications status	R	1	00h
80h	STATUS_MFR_SPECIFIC	Report information about circuit breaker and MOSFET shorted status	R	1	10h
88h	READ_VIN	Report input voltage measurement	R	2	0000h
8Bh	READ_VOUT	Report output voltage measurement	R	2	0000h
8Dh	READ_TEMPERATURE_1	Report temperature measurement	R	2	0190h
99h	MFR_ID	Report manufacturer ID in ASCII characters (MGS)	R	3	53h 47h 4Dh
9Ah	MFR_MODEL	Report part number in ASCII characters. (SGM25720)	R	8	32h 35h 37h 31h 36h 00h 00h 00h
9Bh	MFR_REVISION	Report part revision letter or number in ASCII (for example, 00)	R	2	00h 00h
D0h	MFR_SPECIFIC_00: READ_VAUX	Report auxiliary voltage measurement	R	2	0000h
D1h	MFR_SPECIFIC_01: MFR_READ_IIN	Report input current measurement	R	2	0000h
D2h	MFR_SPECIFIC_02: MFR_READ_PIN	Report input power measurement	R	2	0000h
D3h	MFR_SPECIFIC_03: MFR_IIN_OC_WARN_LIMIT	Report or setting input current limit warn threshold	R/W	2	0FFFh
D4h	MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT	Report or setting input power limit warn threshold	R/W	2	0FFFh
D5h	MFR_SPECIFIC_05: READ_PIN_PEAK	Report measured peak input power measurement	R	2	0000h

PROGRAMMING (continued)

Table 1. Supported PMBus Commands (continued)

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
D6h	MFR_SPECIFIC_06: CLEAR_PIN_PEAK	Resets the contents of the peak input power register to 0	Send byte	0	
D7h	MFR_SPECIFIC_07: GATE_MASK	Disables external MOSFET gate control for FAULTs	R/W	1	0000h
D8h	MFR_SPECIFIC_08: ALERT_MASK	Report or setting user nSMBA fault mask	R/W	2	0820h
D9h	MFR_SPECIFIC_09: DEVICE_SETUP	Report or stores information about number of retry attempts	R/W	1	0000h
DAh	MFR_SPECIFIC_10: BLOCK_READ	Report most recent diagnostic and telemetry information in a single transaction	R	12	0460h 0000h 0000h 0000h 0000h 0000h
DBh	MFR_SPECIFIC_11: SAMPLES_FOR_AVG	Exponent value AVGN for number of samples to be averaged (N = 2^{AVGN}), range = 00h to 0Ch	R/W	1	00h
DCh	MFR_SPECIFIC_12: READ_AVG_VIN	Report averaged input voltage measurement	R	2	0000h
DDh	MFR_SPECIFIC_13: READ_AVG_VOUT	Report averaged output voltage measurement	R	2	0000h
DEh	MFR_SPECIFIC_14: READ_AVG_IIN	Report averaged input current measurement	R	2	0000h
DFh	MFR_SPECIFIC_15: READ_AVG_PIN	Report averaged input power measurement	R	2	0000h
E0h	MFR_SPECIFIC_16: BLACK_BOX_READ	Captures diagnostic and telemetry information, which are latched when the first nSMBA event occurs after faults are cleared	R	12	0000h 0000h 0000h 0000h 0000h 0000h
E1h	MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD	STATUS_WORD has a manufacturer-customized parallel variant to output all fault/warning contents through a sole bus access operation.	R	2	0460h
E2h	MFR_SPECIFIC_18: AVG_BLOCK_READ	Report most recent average telemetry and diagnostic information in a single transaction	R	12	0460h 0000h 0000h 0000h 0000h 0000h

Standard PMBus Commands

0x01: OPERATION

The OPERATION command is a standard PMBus instruction designed to control MOSFET switching functions. It allows the host system to remotely turn the MOSFET on or off. Additionally, this command serves to reactivate the MOSFET after it shuts down due to a fault condition. Sending an OFF then ON sequence resets all fault flags and returns the unit to regular working status. By comparison, a standalone ON trigger post fault-triggered shutdown fails to clear fault registers or reactivate equipment. This instruction is delivered via the single-byte-write communication protocol.

Table 2. Recognized OPERATION Command Values

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ON/OFF_STATE	1	R/W	0: The MOSFET is off 1: The MOSFET is on
D[6:0]	Reserved	000 0000	R/W	Reserved

PROGRAMMING (continued)

0x03: CLEAR_FAULTS

CLEAR_FAULTS is a regular PMBus order designed to erase all cached fault/warning flags and release the nSMBA signal. In cases where fault or alarm abnormalities are still ongoing at command issuance, nSMBA either stays asserted or restores its active state promptly. Importantly, issuing CLEAR_FAULTS alone does not turn the MOSFET back on after a fault-induced shutdown; restoring the output requires sending an OPERATION command once the underlying fault has been resolved. This command is transmitted via the PMBus send-byte protocol.

0x19: CAPABILITY

The CAPABILITY command is a standard PMBus instruction that reports which PMBus functions the SGM25720 device supports. This command is accessed using the PMBus read-byte protocol.

Table 3. CAPABILITY Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PACKET_ERROR_CHECKING	1	R	Packet Error Checking is supported
D[6:5]	MAXIMUM_BUS_SPEED[1:0]	01	R	Maximum supported bus speed is 400kHz
D[4]	nSMBALERT#	1	R	The device does have a nSMBALERT# pin and does support the SMBus Alert Response protocol
D[3]	DATA_TYPE	0	R	Numeric data is in LINEAR11, ULINEAR16 or DIRECT format
D[2]	AVSBus_SUPPORT	0	R	AVSBus Not Supported
D[1:0]	CML[1:0]	0	R	A communication fault has occurred
D[0]	Reserved	0	R	Reserved

0x43: VOUT_UV_WARN_LIMIT

VOUT_UV_WARN_LIMIT belongs to standardized PMBus codes for defining the output threshold (sampled from output or sense terminals) that activates the output under-voltage alert. Such alert is suppressed before the device ramps up to its preset output setting; meanwhile, the alert function gets blocked while the chip is switched off. Data interaction for this register follows PMBus read-word or write-word transmission rules. All read/write operations adopt the scaling parameters listed in Table 41. Once the actual sampled VOUT falls beneath the preset threshold value inside this register, the V_{OUT} under-voltage warning bits will set and pull the nSMBA interrupt line high.

Table 4. VOUT_UV_WARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VOUT_UV_WARN_LIMIT[15:0]	0000h (disabled)	R	0000h: V_{OUT} under-voltage warning disabled 0001h~0FFFh: V_{OUT} under-voltage warning detection threshold

0x4F: OT_FAULT_LIMIT

The OT_FAULT_LIMIT command is a standard PMBus instruction that configures or reads the threshold for over-temperature fault detection. All register read/write operations require conversion factors specified in Table 41, with register access limited to PMBus read-word/write-word protocols. Once measured temperature surpasses the predefined limit, an over-temperature fault activates: the power MOSFET shuts down, OT_FAULT bits latch, and the nSMBA pin goes active. After temperature drops beneath the set-point, running the OPERATION command restores MOSFET conduction.

Table 5. OT_FAULT_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	OT_FAULT_LIMIT[15:0]	0960h (+150℃)	R/W	0000h~0FFEh: Over-temperature fault threshold value 0FFFh: Over-temperature fault detection disabled

PROGRAMMING (continued)

0x51: OT_WARN_LIMIT

OT_WARN_LIMIT is a standard PMBus command used to configure or read the over-temperature warning threshold. Any register read or write must adopt conversion factors from Table 41 and follow PMBus read-word/write-word protocols. Measured temperatures above this programmed limit trigger an over-temperature warning, activate OT_WARN status bits and pull the nSMBA alert signal active.

Table 6. OT_WARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	OT_WARN_LIMIT[15:0]	07D0h (+125℃)	R/W	0000h~0FFEh: Over-temperature warn threshold value 0FFFh: Over-temperature warn detection disabled

0x57: VIN_OV_WARN_LIMIT

The VIN_OV_WARN_LIMIT command represents a standard PMBus instruction used for setting or retrieving the threshold value associated with V_{IN} over-voltage warning detection. When reading from or writing to this register, the coefficient values specified in Table 41 must be applied. All access operations for this command shall follow the PMBus read-word/write-word protocols. In the event that the sensed V_{IN} measurement exceeds the value stored in this register, the corresponding V_{IN} over-voltage warning flags will be triggered in the relevant registers, and the nSMBA signal will be activated.

Table 7. VIN_OV_WARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VIN_OV_WARN_LIMIT[15:0]	0FFFh (disabled)	R/W	0000h~0FFEh: V_{IN} over-voltage warning detection threshold 0FFFh: V_{IN} over-voltage warning disabled

0x58: VIN_UV_WARN_LIMIT

VIN_UV_WARN_LIMIT serves as a standard PMBus command designed for configuring and reading the threshold level for V_{IN} under-voltage warning monitoring. The coefficients provided in Table 41 shall be applied for both read and write operations to this register. All communications for this command shall follow PMBus read-word/write-word specifications. Once sampled V_{IN} falls below the register-defined threshold, relevant V_{IN} under-voltage warning bits get latched and the nSMBA alert pin activates.

Table 8. VIN_UV_WARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	VIN_UV_WARN_LIMIT[15:0]	0000h (disabled)	R/W	0000h: V_{IN} under-voltage warning disabled 0001h~0FFFh: V_{IN} under-voltage warning detection threshold

0x78: STATUS_BYTE

The STATUS_BYTE command is a standard PMBus instruction that outputs a set of flag bits reflecting the operating status of the SGM25720. The command must be accessed using the PMBus read-byte protocol. To reset the bits within this register, the relevant system fault condition must be resolved first, followed by the issuance of a CLEAR_FAULTS command.

Table 9. STATUS_BYTE Definitions

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	BUSY	0	R	Not supported, always 0
D[6]	OFF	1	R	This status gets high whenever the MOSFET fails to turn on due to any abnormal cause.
D[5]	VOUT_OV	0	R	Not supported, always 0
D[4]	IOUT_OC	0	R	Not supported, always 0
D[3]	VIN_UV_FAULT	1	R	A V_{IN} under-voltage fault has occurred
D[2]	TEMPERATURE	0	R	A temperature fault or warning has occurred
D[1]	CML	0	R	A communication fault has occurred
D[0]	None of the above	1	R	A fault or warning not listed in bits [7:1] has occurred

PROGRAMMING (continued)

0x79: STATUS_WORD

The STATUS_WORD is a standard PMBus command that outputs a series of status flags reflecting the operating condition of the SGM25720 device. This command must be accessed in accordance with the PMBus read-word protocol. Clearing the bits within this register required to remove the originating fault condition followed by execution of the CLEAR_FAULTS command. Notably, the INPUT and VIN_UV flags are set to logic 1 by default at power on and UVLO is below the threshold; these bits are automatically reset to 0 once the input voltage first rises above the resistor configured UVLO threshold.

Table 10. STATUS_WORD Definitions

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT	0	R	The output voltage has generated a corresponding fault or alarm.
D[14]	IOUT/POUT	0	R	Not supported, always 0
D[13]	INPUT	1	R	An input voltage or current fault has occurred
D[12]	FET_FAIL	1	R	FET is shorted
D[11]	nPOWER_GOOD	1	R	The Power Good signal has been negated
D[10]	FANS	0	R	Not supported, always 0
D[9]	CB_FAULT	0	R	Circuit breaker fault triggered
D[8]	UNKNOWN	0	R	Not supported, always 0
D[7]	BUSY	0	R	Not supported, always 0
D[6]	OFF	1	R	This bit is asserted if the MOSFET is not switched on for any reason.
D[5]	VOUT_OV	0	R	Not supported, always 0
D[4]	IOUT_OC	0	R	Not supported, always 0
D[3]	VIN_UV	1	R	A V_{IN} under-voltage fault has occurred
D[2]	TEMPERATURE	0	R	A temperature fault or warning has occurred
D[1]	CML	0	R	A communication fault has occurred
D[0]	None of the above	1	R	A fault or warning not listed in bits [7:1] has occurred

0x7A: STATUS_VOUT

STATUS_VOUT is a conventional PMBus register command dedicated to indicating the status flag for output under-voltage alerts. All read operations on this register comply with PMBus's read-byte specification. Prior to clearing its stored status bits, users need to eliminate the existing fault trigger and subsequently issue the CLEAR_FAULTS PMBus order.

Table 11. STATUS_VOUT Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VOUT_OV_FAULT	0	R	Not supported, always 0
D[6]	VOUT_OV_WARN	0	R	Not supported, always 0
D[5]	VOUT_UV_WARN	0	R	A V_{OUT} under-voltage warning has occurred
D[4]	VOUT_UV_FAULT	0	R	Not supported, always 0
D[3]	VOUT_MAX	0	R	Not supported, always 0
D[2]	TON_MAX_FAULT	0	R	Not supported, always 0
D[1]	TOFF_MAX_FAULT	0	R	Not supported, always 0
D[0]	VOUT_TRACKING_ERROR	0	R	Not supported, always 0

PROGRAMMING (continued)

0x7C: STATUS_INPUT

STATUS_INPUT is a regular PMBus instruction used to fetch flag states of input voltage, current and power. Only PMBus read-byte protocol is available for data reading. Users need to clear existing faults and send CLEAR_FAULTS to reset the register bits. The V_{IN} under-voltage warning flag is initialized to 1 at input power-on; it is then set to 0 once the input voltage first rises above the resistor-configured UVLO threshold.

Table 12. STATUS_INPUT Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	VIN_OV_FAULT	0	R	A V_{IN} over-voltage fault has occurred
D[6]	VIN_OV_WARN	0	R	A V_{IN} over-voltage warning has occurred
D[5]	VIN_UV_WARN	1	R	A V_{IN} under-voltage warning has occurred
D[4]	VIN_UV_FAULT	0	R	A V_{IN} under-voltage fault has occurred
D[3]	INSUFFICIENT_VOLTAGE	0	R	Not supported, always 0
D[2]	IIN_OC_FAULT	0	R	An I_{IN} over-current fault has occurred
D[1]	IIN_OC_WARN	0	R	An I_{IN} over-current warning has occurred
D[0]	PIN_OP_WARN	0	R	A P_{IN} overpower warning has occurred

0x7D: STATUS_TEMPERATURE

STATUS_TEMPERATURE, a typical PMBus code, retrieves flag information derived from temperature monitoring measurements. All register reads are limited to PMBus read-byte mode. Users have to fix original abnormal conditions then trigger CLEAR_FAULTS to reset internal register bits.

Table 13. STATUS_TEMPERATURE Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	OVERTEMP_FAULT	0	R	An over-temperature fault has occurred
D[6]	OVERTEMP_WARN	0	R	An over-temperature warning has occurred
D[5]	UNDERTEMP_WARN	0	R	Not supported, always 0
D[4]	UNDERTEMP_FAULT	0	R	Not supported, always 0
D[3]	Reserved	0	R	Not supported, always 0
D[2]	Reserved	0	R	Not supported, always 0
D[1]	Reserved	0	R	Not supported, always 0
D[0]	Reserved	0	R	Not supported, always 0

0x7E: STATUS_CML

STATUS_CML is a standard PMBus command that provides various status flags indicative of communication-related faults. This command must be read using the PMBus read-byte protocol. Issuing a CLEAR_FAULTS command is required to clear the bits within this register.

Table 14. STATUS_CML Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	STATUS_CML[7]	0	R	Invalid or unsupported command received
D[6]	STATUS_CML[6]	0	R	Invalid or unsupported data received
D[5]	STATUS_CML[5]	0	R	Packet error check failed
D[4]	STATUS_CML[4]	0	R	Not supported, always 0
D[3]	STATUS_CML[3]	0	R	Not supported, always 0
D[2]	STATUS_CML[2]	0	R	Not supported, always 0
D[1]	STATUS_CML[1]	0	R	Miscellaneous communications fault has occurred
D[0]	STATUS_CML[0]	0	R	Not supported, always 0

PROGRAMMING (continued)

0x80: STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command serves as a standardized PMBus instruction used to store status data unique to individual manufacturers. Reading data from this register is limited to PMBus read-byte mode. Resolving the pertinent fault issue and transmitting CLEAR_FAULTS is required to erase stored register bits.

Table 15. STATUS_MFR_SPECIFIC Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	STATUS_MFR_SPECIFIC[7]	0	R	Circuit breaker fault
D[6]	STATUS_MFR_SPECIFIC[6]	0	R	External MOSFET shorted fault
D[5]	STATUS_MFR_SPECIFIC[5]	0	R	Not supported, always 0
D[4]	STATUS_MFR_SPECIFIC[4]	1	R	Defaults loaded
D[3]	STATUS_MFR_SPECIFIC[3]	0	R	Not supported, always 0
D[2]	STATUS_MFR_SPECIFIC[2]	0	R	Not supported, always 0
D[1]	STATUS_MFR_SPECIFIC[1]	0	R	Not supported, always 0
D[0]	STATUS_MFR_SPECIFIC[0]	0	R	Not supported, always 0

0x88: READ_VIN

READ_VIN is a standard PMBus command that provides a 12 bits digital result representing the measured input voltage. Retrieval of this register requires the use of the coefficients specified in Table 41 and must follow the PMBus read-word protocol. Internally, this measured value is also employed to detect over-voltage and under-voltage warning conditions for the input voltage.

Table 16. READ_VIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VIN[15:0]	0000h	R	0000h~0FFFh: Measured value for V_{IN}

0x8B: READ_VOUT

The READ_VOUT command represents a standard PMBus instruction that outputs a 12 bits sampled measurement of the output voltage. When reading this register, the coefficient values provided in Table 41 shall be applied. All register access for this instruction shall conform to PMBus read-word specifications. The sampled numerical data is also leveraged inside the chip to identify occurrences of output under-voltage alerts.

Table 17. READ_VOUT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VOUT[15:0]	0000h	R	0000h~0FFFh: Measured value for V_{OUT}

0x8D: READ_TEMPERATURE_1

READ_TEMPERATURE_1 is a formal PMBus register code delivering signed temperature readings captured via an off-chip thermal sensing diode. Any register readout needs the conversion parameters specified in Table 41 and must abide by PMBus read-word transmission standards. The obtained thermal reading is further employed by internal circuitry to flag over temperature fault and alarm occurrences. After coefficient conversion, the valid range of this data spans from -256℃ to +255℃.

Table 18. READ_TEMPERATURE_1 Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_TEMPERATURE_1[15:0]	0000h	R	0000h~0FFFh: Measured value for TEMPERATURE

PROGRAMMING (continued)

0x99: MFR_ID

The MFR_ID command functions as a standard PMBus command that reports the manufacturer's identification code. To retrieve the MFR_ID information, the PMBus block-read protocol should be employed.

Table 19. MFR_ID Register

BYTE	BYTE NAME	DEFAULT	TYPE	DESCRIPTION
3	‘M'	4Dh	R	MFR ID-3
2	‘G'	47h	R	MFR ID-2
1	‘S’	53h	R	MFR ID-1
0		03h	R	Number of bytes

0x9A: MFR_MODEL

MFR_MODEL constitutes a conventional PMBus register code for retrieving the component's part identifier. Block Read defined by the PMBus specification is the only allowed method to fetch data from this register.

Table 20. MFR_MODEL Register

BYTE	BYTE NAME	DEFAULT	TYPE	DESCRIPTION
8		00h	R	MFR ID-8
7		00h	R	MFR ID-7
6		00h	R	MFR ID-6
5	‘0’	36h	R	MFR ID-5
4	‘2’	31h	R	MFR ID-4
3	‘7’	37h	R	MFR ID-3
2	‘5’	35h	R	MFR ID-2
1	‘2’	32h	R	MFR ID-1
0		05h	R	Number of bytes

0x9B: MFR_REVISION

MFR_REVISION is a conventional PMBus register code designed to output the component's hardware and firmware revision information. PMBus block-read protocol is compulsory for all read access to this register address.

Table 21. MFR_REVISION Register

BYTE	BYTE NAME	DEFAULT	TYPE	DESCRIPTION
2	‘0’	00h	R	MFR ID-2
1	‘0’	00h	R	MFR ID-1
0		02h	R	Number of bytes

PROGRAMMING (continued)

Manufacturer Specific PMBus Commands

0xD0: MFR_SPECIFIC_00: READ_VAUX

The READ_VAUX command outputs a 12 bits ADC measurement of the auxiliary voltage. Any voltage at or above 2.97V relative to ground is reported as full-scale value 0FFFh. Voltages at or below 0V with respect to ground are indicated as 0000h. The PMBus read-word protocol shall be used when retrieving data via the READ_VAUX command.

Table 22. READ_VAUX Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_VAUX[15:0]	0000h	R	0000h~0FFFh: Measured value for VAUX input

0xD1: MFR_SPECIFIC_01: MFR_READ_IIN

The MFR_READ_IIN command provides a 12 bits ADC measurement of the current sense voltage. Data from this command must be read using the PMBus read-word protocol, and the conversion coefficients specified in Table 41 should be applied when interpreting this register. Refer to the section on Reading and Writing Telemetry Data and Warning Thresholds for the proper calculation methodology.

Table 23. MFR_READ_IIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_READ_IIN[15:0]	0000h	R	0000h~0FFFh: Measured value for input current sense voltage

0xD2: MFR_SPECIFIC_02: MFR_READ_PIN

The MFR_READ_PIN command outputs the upper 12 bits of the product of V_{IN} × I_{IN}, captured by a 12 bits ADC. The PMBus read-word protocol is used to access data from this command. When reading this register, the coefficients listed in Table 41 must be applied. For guidance on computing the corresponding values, refer to the section Reading and Writing Telemetry Data and Warning Thresholds.

Table 24. MFR_READ_PIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_READ_PIN[15:0]	0000h	R	0000h~0FFFh: VALUE for input current × input voltage

0xD3: MFR_SPECIFIC_03: MFR_IN_OC_WARN_LIMIT

The MFR_IIN_OC_WARN_LIMIT is a PMBus command used to configure the input over current warning threshold. If the input current exceeds the threshold programmed in this register, the corresponding I_{IN} over-current warning flags will be set in the relevant registers, and the nSMBA signal will be asserted. This register can be accessed using the PMBus read-word/write-word protocols, and the coefficients provided in Table 41 should be applied for both read and write operations.

Table 25. MFR_IIN_OC_WARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_IIN_OC_WARN_LIMIT[15:0]	0FFFh	R/W	0000h~0FFEh: Value for input over-current warn limit 0FFFh: Input over-current warning disabled

0xD4: MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT

MFR_PIN_OP_WARN_LIMIT, one standardized PMBus code, sets the threshold value for input overpower alert. Once actual input power surpasses the preset limit stored inside this register, dedicated PIN overpower status bits get latched in corresponding registers alongside assertion of the nSMBA interrupt line. All read and write transactions for this register comply with PMBus read-word/write-word protocols, with conversion factors tabulated in Table 41 implemented during every access.

Table 26. MFR_PIN_OPWARN_LIMIT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	MFR_PIN_OP_WARN_LIMIT[15:0]	0FFFh	R/W	0000h~0FFEh: Value for input over power warn limit 0FFFh: Input over power warning disabled

PROGRAMMING (continued)

0xD5: MFR_SPECIFIC_05: READ_PIN_PEAK

READ_PIN_PEAK retrieves the peak input power captured since either device power-up reset or the latest execution of CLEAR_PIN_PEAK instruction. All data fetching for this register must adopt PMBus read-word specification and apply the conversion parameters listed within Table 41.

Table 27. READ_PIN_PEAK Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_PIN_PEAK[15:0]	0000h	R	0000h~0FFFh: Maximum value for input current × input voltage since reset or last clear

0xD6: MFR_SPECIFIC_06: CLEAR_PIN_PEAK

The CLEAR_PIN_PEAK instruction is designed to reset the PIN_PEAK register. This command operates using the PMBus send-byte protocol.

0xD7: MFR_SPECIFIC_07: GATE_MASK

GATE_MASK implements hardware masking so faults cannot switch off the MOSFET. A high logic level on any bit decouples its corresponding fault from MOSFET gate control. STATUS, DIAGNOSTIC and other status registers refresh as usual, and nSMBA interrupt still triggers under qualified faults. Users configure or read the register in compliance with PMBus read-byte/write-byte protocols.

NOTE: Preventing the MOSFET from shutting down during over-current or circuit-breaker fault events may lead to permanent damage of the MOSFET. This feature must be applied with extreme caution and proper supervision.

Table 28. MFR_SPECIFIC_07 Gate Mask Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Not used, always 0	0	R/W	
D[6]	Not used, always 0	0	R/W	
D[5]	VIN_UV_FAULT	0	R/W	If turning off the MOSFET when V_{IN} under-voltage fault happened 0: Turning off 1: No
D[4]	VIN_OV_FAULT	0	R/W	If turning off the MOSFET when V_{IN} over-voltage fault happened 0: Turning off 1: No
D[3]	Not used, do not write to bit	-	R	
D[2]	OVERTEMP_FAULT	0	R/W	If turning off the MOSFET when over-temperature fault happened 0: Turning off 1: No
D[1]	Not used, always 0	0	R/W	
D[0]	Not used, do not write to bit	-	R	

The IIN/PFET fault covers both the input current fault and the MOSFET power dissipation fault. The device does not implement input power fault detection, but only input power warning detection.

0xD8: MFR_SPECIFIC_08: ALERT_MASK

The ALERT_MASK PMBus setting inhibits nSMBA output for selected fault and alarm events. Fourteen available bits each represent an individual analog or digital alert that ordinarily pulls nSMBA high. Setting a bit high disables nSMBA response from its paired fault. STATUS and DIAGNOSTIC_WORD registers still log faults normally, and key faults like VIN over-voltage/under-voltage, IIN/PFET, CB and over-temperature faults continue controlling external MOSFET gates. Register configuration and reading comply with PMBus Read/Write Word rules. The VIN UV fault bit powers up as 1 and clears to 0 after input voltage surpasses resistor-programmed UVLO for the first startup cycle.

PROGRAMMING (continued)

Table 29. ALERT_MASK Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT_UNDERVOLTAGE_WARN	0	R	If masking nSMBA signal pulled down when V_{OUT} under-voltage warning happened 0: No mask 1: Mask
D[14]	IIN_LIMIT_WARN	0	R	If masking nSMBA signal pulled down when input current exceeds current limit threshold 0: No mask 1: Mask
D[13]	VIN_UNDERVOLTAGE_WARN	0	R	If masking nSMBA signal pulled down when V_{OUT} under-voltage warning happened 0: No mask 1: Mask
D[12]	VIN_OVERVOLTAGE_WARN	0	R	If masking nSMBA signal pulled down when V_{IN} over-voltage warning happened 0: No mask 1: Mask
D[11]	nPOWER_GOOD	1	R	If masking nSMBA signal pulled down when power good signal is low voltage. 0: No mask 1: Mask
D[10]	OVERTEMP_WARN	0	R	If masking nSMBA signal pulled down when over-temperature warning happened. 0: No mask 1: Mask
D[9]	Not used	0	R	Reserved
D[8]	OVERPOWER_LIMIT_WARN	0	R	If masking nSMBA signal pulled down when over power limit warning happened. 0: No mask 1: Mask
D[7]	Not used	0	R	Reserved
D[6]	EXT_MOSFET_SHORTED	0	R	If masking nSMBA signal pulled down when external MOSFET shorted. 0: No mask 1: Mask
D[5]	VIN_UNDERVOLTAGE_FAULT	1	R	If masking nSMBA signal pulled down when V_{IN} under-voltage fault happened. 0: No mask 1: Mask
D[4]	VIN_OVERVOLTAGE_FAULT	0	R	If masking nSMBA signal pulled down when V_{IN} over-voltage fault happened. 0: No mask 1: Mask
D[3]	IIN/PFET_FAULT	0	R	If masking nSMBA signal pulled down when over-current or power fault happened. 0: No mask 1: Mask
D[2]	OVERTEMPERATURE_FAULT	0	R	If masking nSMBA signal pulled down when over-temperature fault happened. 0: No mask 1: Mask
D[1]	CML_FAULT	0	R	If masking nSMBA signal pulled down when communication fault happened. 0: No mask 1: Mask
D[0]	CIRCUIT_BREAKER_FAULT	0	R	If masking nSMBA signal pulled down when circuit breaker fault happened. 0: No mask 1: Mask

PROGRAMMING (continued)

0xD9: MFR_SPECIFIC_09: DEVICE_SETUP

The DEVICE_SETUP command allows the host to override the pin configurations and define the operating mode of the SGM25720. This command is accessed using the PMBus read-byte/write-byte protocols.

Table 30. DEVICE_SETUP Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	RETRY_SETTING[2:0]	000	R/W	000: Pin configured retries 001: No retries 010: Retry 1 time 011: Retry 2 times 100: Retry 4 times 101: Retry 8 times 110: Retry 16 times 111: Unlimited retries
D[4]	CURRENT_LIMIT_SETTING	0	R/W	0: Low setting (24.5mV) 1: High setting (45mV)
D[3]	CB/CL_RATIO	0	R/W	0: Low setting (1.8x) 1: High setting (3.6x)
D[2]	CURRENT_LIMIT_CONFIGURATION	0	R/W	0: Use pin settings 1: Use SMBus settings
D[1]	Unused	0	R/W	Reserved
D[0]	Unused	0	R/W	Reserved

To configure the current limit via this register, the current limit configuration bit 2 must be set to 1, allowing the register to control the current limit function. Meanwhile, bit 4 is used to select the target current limit level. If the current limit configuration bit is disabled, the device will follow the hardware pin settings instead.

The circuit-breaker to current-limit ratio is configured by the CB/CL_RATIO bit 3. Note that modifying the current limit configuration does not reset the sampling data for the telemetry averaging function. SGMICRO recommends waiting for a complete averaging update cycle under the new current limit configuration before processing the averaged results.

It should also be noted that the current limit configuration influences the scaling coefficients applied to current and power measurements as well as the corresponding warning registers.

0xDA: MFR_SPECIFIC_10: BLOCK_READ

The BLOCK_READ function packs DIAGNOSTIC_WORD, power rail telemetry and temperature data together; this design lets users collect all working parameters for SGM25720 in one-time SMBus readout. This data block has a length of 12 bytes, and the telemetry values are transmitted in the same format as individual READ_* commands (as illustrated in Table 31). The contents of this block-read register are refreshed every clock cycle of 1μs. The BLOCK_READ function also ensures that measurements for V_{IN}, V_{OUT}, I_{IN}, and P_{IN} are fully time-synchronized.

When using separate read commands, individual samples may lose time alignment due to inherent communication delays in the protocol. This block-read operation is performed using the PMBus block-read protocol.

Table 31. BLOCK_READ Register

BYTE	BYTE NAME	DEFAULT	TYPE	DESCRIPTION
word 1	DIAGNOSTIC_WORD	0460h	R	Report all of the SGM25720 faults and warnings
word 2	IIN_BLOCK	0000h	R	Report the 12-bit ADC measured current sense voltage
word 3	VOUT_BLOCK	0000h	R	Report the 12-bit ADC measured output voltage
word 4	VIN_BLOCK	0000h	R	Report the 12-bit ADC measured input voltage
word 5	PIN_BLOCK	0000h	R	Report the 12-bit ADC measured $V_{IN} \times I_{IN}$
word 6	TEMP_BLOCK	0000h	R	Report the 12-bit ADC measured temperature

PROGRAMMING (continued)

0xDB: MFR_SPECIFIC_11: SAMPLES_FOR_AVG

The decimal value corresponding to the AVGN nibble represents the exponent of 2 that determines the sample count; for instance, AVGN = 12 corresponds to an averaging window of 4096 samples. The SGM25720 supports the following sample counts: 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, and 4096. The configured sample count applies uniformly and simultaneously to the average computations of I_{IN}, V_{IN}, V_{OUT}, and P_{IN}.

The device implements straightforward arithmetic averaging: consecutive sampled results are accumulated up to the programmed number of samples, and the sum is then divided by the sample count.

The averaging process follows the formula below:

$$Y = (X_N + X_{N-1} + ... + X_0) / N \quad (1)$$

Once an averaging cycle is completed (e.g., after 4096 samples), a new averaging cycle restarts from scratch.

The same number of new samples must be acquired before the updated average value becomes valid.

Table 32. SAMPLES_FOR_AVG Register

AVGN (b)	N = 2^{AVGN}	Averaging/Register Update Period (ms)
0000b	1	1
0001b	2	2
0010b	4	4
0011b	8	8
0100b	16	16
0101b	32	32
0110b	64	64
0111b	128	128
1000b	256	256
1001b	512	512
1010b	1024	1024
1011b	2048	2048
1100b	4096	4096

Modifications to the SAMPLES_FOR_AVG register via PMBus byte read/write operations take effect on averaged telemetry only after the current averaging cycle finishes.

able 33. SAMPLES_FOR_AVG Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	SAMPLES_FOR_AVG[15:0]	0000h	R/W	0000h~000Ch: Exponent (AVGN) for number of samples to average over

PROGRAMMING (continued)

0xDC: MFR_SPECIFIC_12: READ_AVG_VIN

The READ_AVG_VIN command provides the 12 bits ADC measurement of the averaged input voltage. In cases where new data is not available, the previously stored averaged value will be returned as the result. Should no prior averaged data exist, a default value of 0000h is provided instead. This register is accessed via the PMBus read-word protocol, and the coefficients specified in Table 41 shall be applied for data conversion.

Table 34. READ_AVG_VIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_VIN[15:0]	0000h	R	0000h~0FFFh: Average of measured values for input voltage

0xDD: MFR_SPECIFIC_13: READ_AVG_VOUT

Executed via the PMBus read-word protocol, the READ_AVG_VOUT command returns the 12-bit ADC-averaged current sense voltage. If averaging is incomplete, it defaults to returning either 0000h or the last known valid measurement. Refer to Table 41 for the conversion coefficients required to decode this data.

Table 35. READ_AVG_VOUT Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_VOUT[15:0]	0000h	R	0000h~0FFFh: Average of measured values for output voltage

0xDE: MFR_SPECIFIC_14: READ_AVG_IIN

The READ_AVG_IIN command outputs the averaged current sense voltage acquired by the 12 bits ADC. If the averaged measurement is not yet valid, the device returns either the default value 0000h or the last valid set of data. This parameter is read using the PMBus read-word protocol, and the coefficients listed in Table 41 apply to this register.

Table 36. READ_AVG_IIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_IIN[15:0]	0000h	R	0000h~0FFFh: Average of measured values for current sense voltage

0xDF: MFR_SPECIFIC_15: READ_AVG_PIN

Accessed through the PMBus read-word protocol, the READ_AVG_PIN command retrieves the upper 12 bits of the ADC-averaged V_{IN} × I_{IN} product. If the new averaged data is pending, the register will supply either a default value of 0000h or the last computed result. To correctly decode this register, the conversion coefficients specified in Table 41 must be applied.

Table 37. READ_AVG_PIN Register

BITS	BITS NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	READ_AVG_PIN[15:0]	0000h	R	0000h~0FFFh: Average of measured value for input voltage × input current sense voltage

0xE0: MFR_SPECIFIC_16: BLACK_BOX_READ

Retrieved via the PMBus block-read protocol, the BLACK_BOX_READ command captures the data latched by the SGM25720 at the initial assertion of the nSMBA signal. This function remains disabled until a CLEAR_FAULTS command is issued. Although it shares the identical format with standard BLOCK_READ registers, its content refreshes exclusively upon the nSMBA edge rather than the internal clock cycle.

PROGRAMMING (continued)

0xE1: MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD

The READ_DIAGNOSTIC_WORD PMBus command consolidates all fault and warning statuses of the SGM25720 into a single-word-read operation, thereby replacing the traditional practice of issuing multiple read requests to status registers in response to the assertion of the nSMBA signal. This command must be executed using the PMBus read-word protocol and, once queried, its diagnostic data is accessible through BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations, enabling centralized system monitoring and simplified fault diagnostics.

Table 38. DIAGNOSTIC_WORD Register

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	VOUT_UNDERVOLTAGE_WARN	0	R	A V_{OUT} under-voltage warning has occurred
D[14]	IIN_OP_WARN	0	R	An I_{IN} over-current or over power warning has occurred
D[13]	VIN_UNDERVOLTAGE_WARN	0	R	A V_{IN} under-voltage warning has occurred
D[12]	VIN_OVERVOLTAGE_WARN	0	R	A V_{IN} over-voltage warning has occurred
D[11]	nPOWER_GOOD	1	R	The Power Good signal has been negated
D[10]	OVER_TEMPERATURE_WARN	0	R	An over-temperature warning has occurred
D[9]	TIMER_LATCHED_OFF	0	R	Communication time out has occurred
D[8]	EXT_MOSFET_SHORTED	0	R	An external MOSFET shorted has occurred
D[7]	CONFIG_PRESET	1	R	Defaults loaded
D[6]	DEVICE_OFF	1	R	MOSFET is not switched on for any reason.
D[5]	VIN_UNDERVOLTAGE_FAULT	1	R	A V_{IN} under-voltage fault has occurred
D[4]	VIN_OVERVOLTAGE_FAULT	0	R	A V_{IN} over-voltage fault has occurred
D[3]	IIN_OC/PFET_OP_FAULT	0	R	An I_{IN} over-current or over power fault has occurred
D[2]	OVER_TEMPERATURE_FAULT	0	R	An over-temperature fault has occurred
D[1]	CML_FAULT	0	R	A communication fault has occurred
D[0]	CIRCUIT_BREAKER_FAULT	0	R	A circuit breaker fault has occurred

0xE2: MFR_SPECIFIC_18: AVG_BLOCK_READ

The AVG_BLOCK_READ command integrates diagnostic data from the DIAGNOSTIC_WORD register with averaged telemetry values, including input and output current (I_{IN}), output voltage (V_{OUT}), input voltage (V_{IN}), power (P_{IN}), and temperature, into a single PMBus data transfer. This consolidated operation enables retrieval of all device operating parameters through a singular communication transaction, streamlining system monitoring and diagnostics efficiency. This data block is 12 bytes in length, and the telemetry values are transmitted in the same format as individual READ_AVG_* commands, as detailed in Table 39. The AVG_BLOCK_READ function also ensures time alignment among V_{IN}, V_{OUT} and I_{IN} measurements, which may not be guaranteed when reading these values through separate PMBus commands. The SMBus block-read protocol is used to access data from the AVG_BLOCK_READ command.

Table 39. AVG_BLOCK_READ Register

BYTE	BYTE NAME	DEFAULT	TYPE	DESCRIPTION
1 byte	DIAGNOSTIC_WORD	08E0h	R	Report all of the SGM25720 faults and warnings
1 byte	AVG_IIN	0000h	R	Report the 12-bit ADC measured average current sense voltage
1 byte	AVG_VOUT	0000h	R	Report the 12-bit ADC measured average output voltage
1 byte	AVG_VIN	0000h	R	Report the 12-bit ADC measured average input voltage
1 byte	AVG_PIN	0000h	R	Report the 12-bit ADC measured average V_{IN} × I_{IN}
1 byte	TEMPERATURE	0000h	R	Report the 12-bit ADC measured average temperature

PROGRAMMING (continued)

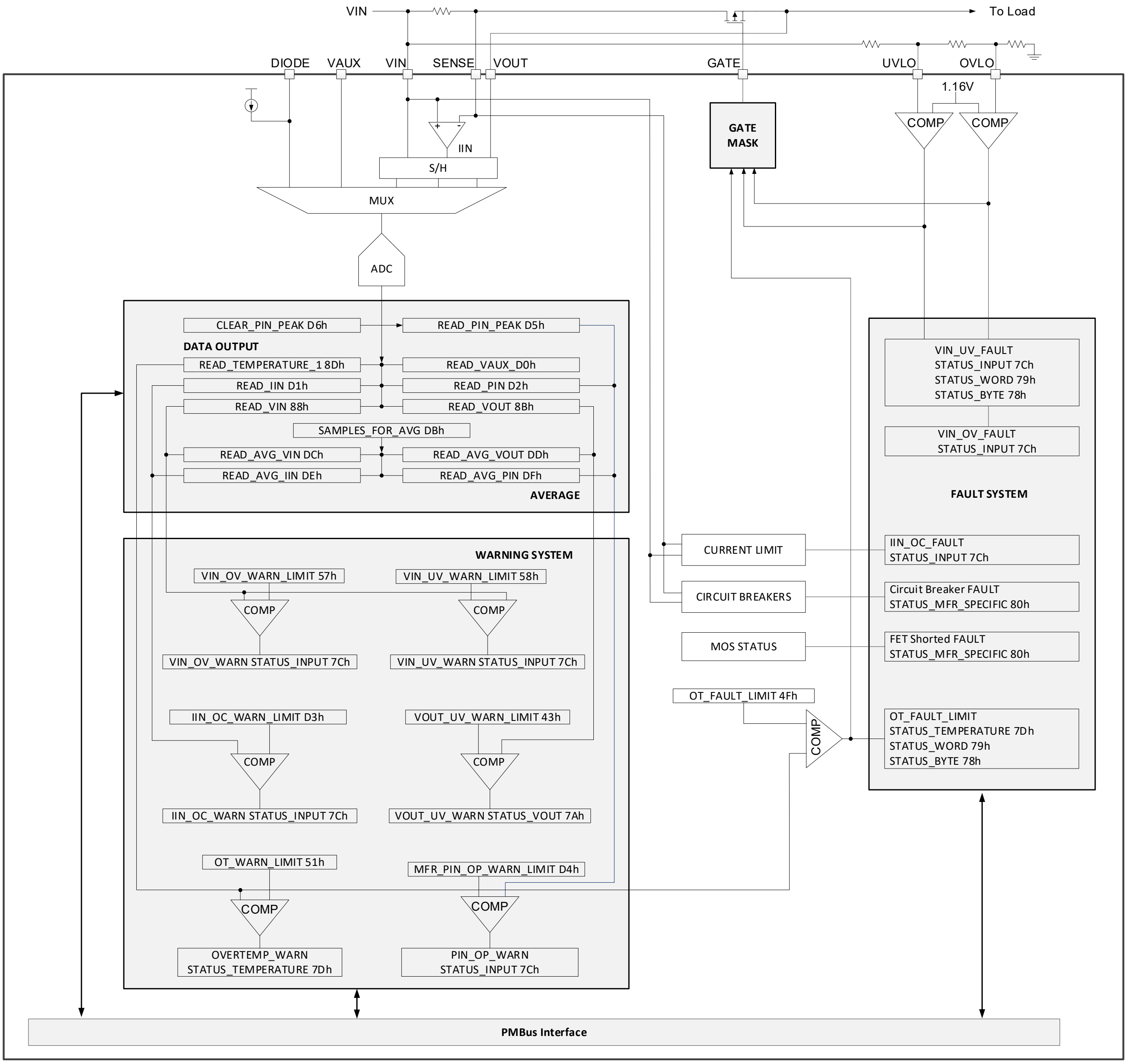


Figure 4. Command/Register and Alert Flow Diagram

PROGRAMMING (continued)

Reading and Writing Telemetry Data and Warning Thresholds

A 12-bit ADC is adopted to capture all telemetry parameters. Collected measurement data as well as user-defined warning threshold values are exchanged in the format of 16-bit two's complement signed numbers. All read/write transactions proceed in 2-byte steps per the DIRECT specification detailed in Section 8.3.3 of PMBus Power System Management Protocol Spec V1.1 (Part II). Table 40 defines the bit arrangement of telemetry and threshold words, with Bit11 as MSB and Bit0 as LSB. Except for temperature data, all converted decimal values of relevant registers fall in the 0 ~ 4095 range; temperature's decimal equivalent covers 0 to 65535 entirely.

Table 40. Telemetry and Warning Word Format

BYTE	B7	B6	B5	B4	B3	B2	B1	B0
1	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0
2	0	0	0	0	Bit_11	Bit_10	Bit_9	Bit_8

To translate DIRECT-formatted raw data into practical voltage, current, power and temperature readings, relevant coefficients shall be computed in line with PMBus V1.1 (Part II) Clause7.2.1. The host employs Equation 2 to convert acquired data into corresponding physical engineering units.

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \qquad (2)$$

where:

- X: the derived practical value (expressed in volts, amps, watts, etc.)
- m: the slope coefficient, encoded as a two-byte signed integer in two's complement format
- Y: a 16-bit signed integer (in two's complement format) received from the device
- b: the offset, given as a two-byte signed integer in two's complement format
- R: the exponent, encoded as a single-byte signed integer in two's complement format
- R This is only needed in systems where m must be an integer - for instance, when m is stored in a register within an integrated circuit. In such cases, R merely needs to be sufficiently large to achieve the required accuracy.

PROGRAMMING (continued)

Table 41. Telemetry and Warning Conversion Coefficients (R_{SNS} in mΩ)

COMMANDS	CONDITION	FORMAT	NUMBER OF DATA BYTES	m	b	R	UNITS
READ_VIN, READ_AVG_VIN, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT		DIRECT	2	22031	-300	-2	V
READ_VOUT, READ_AVG_VOUT, VOUT_UV_WARN_LIMIT		DIRECT	2	22031	-300	-2	V
READ_VAUX		DIRECT	2	3525	0	0	V
*READ_IIN, READ_AVG_IIN, MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	13571 × R_S	-2000	-2	A
*READ_IIN, READ_AVG_IIN, MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	6786 × R_S	-1500	-2	A
*READ_PIN, READ_AVG_PIN, READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	730 × R_S	-1000	-2	W
*READ_PIN, READ_AVG_PIN, READ_PIN_PEAK, MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	365 × R_S	-500	-2	W
READ_TEMPERATURE_1, OT_WARN_LIMIT, OT_FAULT_LIMIT		DIRECT	2	16000	0	-3	°C

Determining Telemetry Coefficients Empirically with Linear Fit

The calibration constants listed in Table 41 work well for most common-use scenarios of telemetry sampling and fault threshold setup. However, current and power-related coefficients require custom calculation for each design, as their values hinge on the selected sense resistor (R_{SNS}). These tabulated parameters are finalized from multi-device temperature cycling characterization to deliver ideal baseline performance.

Unlike other monitoring channels, current and power readings rely on low-amplitude signal acquisition, making them more vulnerable to PCB stray parasitic effects. Component tolerance spread on RS and the SGM25720 IC itself further shifts the ideal M/B/R conversion factors needed to translate DIRECT-format digital codes into real ampere/watt physical values. To boost measurement precision, users can perform board-specific empirical coefficient tuning to offset inaccuracies induced by PCB parasitics, RS deviation and device intrinsic variance.

Copying calibration coefficients characterized from a single PCB to all mass-produced boards is inadvisable: every assembly uses randomly picked R_{SNS} and SGM25720 parts which fail to reflect average statistical characteristics. Designers have two valid options: apply per-board individual calibration, or directly adopt Table 41's default coefficient set.

Follow the steps below to calculate customized optimal current coefficients per PCB:

1. With SGM25720 running normally, regulate load current and capture R_{SNS} voltage via Kelvin probing paired with high-precision DVM. Meanwhile fetch integer data from the READ_AVG_IIN register (set SAMPLES_FOR_AVG > 0) under no less than two distinct R_{SNS} voltage levels. For optimal precision, pick test points covering nearly full current range (e.g., R_{SNS} voltage at 5mV and 20mV).

2. Derive actual current readings by dividing sampled R_{SNS} voltage with the real measured R_{SNS} resistance; Table 42's calculation baseline is defined around a 5mΩ sense resistor.

Table 42. Measurements for Linear Fit Determination of Current Coefficients

MEASURED VOLTAGE ACROSS R_{SNS} (V)	MEASURED CURRENT (A)	READ_AVG_IIN (INTERGER VALUE)
0.005	1	648
0.01	2	1331
0.02	4	2698

PROGRAMMING (continued)

3. Calculate the slope and vertical intercept linking actual measured current and READ_AVG_IIN digital output via spreadsheet or mathematical calculation software. Table 42 follows this linear formula:

- READ_AVG_IIN value = slope × (Measured Current) + (y-intercept)
- slope = 683.4
- y-intercept = -35.5

4. The m factor is obtained by adjusting the slope's decimal position to get an integer (usually four significant digits) within the numeric range -32768 ~ +32767; such decimal displacement directly defines parameter R. For the above slope example, shifting the decimal one position right results in R = -1.

5. After fixing the R coefficient, compute b by multiplying the intercept value by 10^{-R}. Using the given data yields of b = -355.

Calculated Current Coefficients:

- m = 6834
- b = -355
- R = -1

$$X = \frac{1}{m} \times \left(Y \times 10^{-R} - b\right) \tag{3}$$

where:

- X: the derived practical value (expressed in volts, amps, watts, etc.)
- m: the slope coefficient, encoded as a two-byte signed integer in two's complement format
- Y: a 16-bit signed integer (in two's complement format) received from the device
- b: the offset, given as a two-byte signed integer in two's complement format
- R: the exponent, encoded as a single-byte signed integer in two's complement format
- This process can be reused for any telemetry channel by swapping the measured current with another quantity like voltage, power, etc.to compute its respective coefficients.

Writing Telemetry Data

Several registers require data to be written if their optional features are to be enabled. In such cases, use the same coefficients already computed for your application and apply them according to the method outlined in Section 7.2.2 of the *PMBus Power System Management Protocol Specification, Part II – Command Language, Revision 1.2.*

$$Y = \left(mX + b\right) \times 10^{R} \tag{4}$$

where:

- X: the derived practical value (expressed in volts, amps, watts, etc.)
- m: the slope coefficient, encoded as a two-byte signed integer in two's complement format
- Y: a 16-bit signed integer (in two's complement format) received from the device
- b: the offset, given as a two-byte signed integer in two's complement format
- R: the exponent, encoded as a single-byte signed integer in two's complement format

PROGRAMMING (continued)

PMBus Address Lines (ADR0, ADR1, ADR2)

The SGM25720 offers 27 possible I²C addresses, determined by setting each of its three address pins to either VDD (high), GND (low), or left open (floating). Table 43 provides the resulting 7-bit addresses, with the eighth bit used for the read/write control.

Table 43. Device Addressing

ADR2	ADR1	ADR0	DECODED ADDRESS
Z	Z	Z	40h
Z	Z	0	41h
Z	Z	1	42h
Z	0	Z	43h
Z	0	0	44h
Z	0	1	45h
Z	1	Z	46h
Z	1	0	47h
Z	1	1	10h
0	Z	Z	11h
0	Z	0	12h
0	Z	1	13h
0	0	Z	14h
0	0	0	15h
0	0	1	16h
0	1	Z	17h
0	1	0	50h
0	1	1	51h
1	Z	Z	52h
1	Z	0	53h
1	Z	1	54h
1	0	Z	55h
1	0	0	56h
1	0	1	57h
1	1	Z	58h
1	1	0	59h
1	1	1	5Ah

PROGRAMMING (continued)

nSMBA Response

The nSMBA effectively has two masks:

1. The Alert Mask Register at D8h;
2. The ARA Automatic Mask.

The ARA Automatic Mask is a feature that activates automatically when a device successfully answers an Alert Response Address (ARA) read request. During an ARA transaction, the PMBus™ master retrieves the address of the lowest-numbered device on the bus whose nSMBA pin is currently active. If this device's address is returned, it confirms that it was the one that responded. In response, the device releases its nSMBA signal. Once all devices with asserted nSMBA have reported their addresses through ARA, the common nSMBA line returns to an inactive state.

In the SGM25720, this release is achieved by internally masking all fault conditions present at the time of the ARA read via the ARA Automatic Mask bit. While these faults remain visible in the status registers, they will not reassert nSMBA unless the mask is cleared—typically by the host issuing a Clear Faults command. As a best practice, this clear operation should be performed whenever servicing an nSMBA event, regardless of whether an actual ARA read took place. A schematic overview of this process is shown in Figure 5:

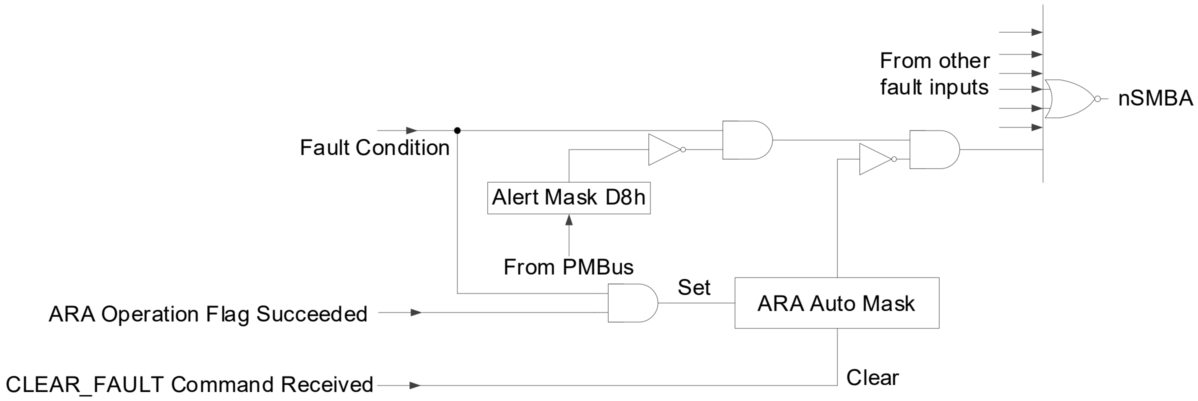


Figure 5. Typical Flow Schematic for nSMBA Fault

DETAILED DESCRIPTION

Overview

The SGM25720 is designed to limit the generated inrush current when the circuit card is plugged into and removed from the live backplane or hot power supply, reduce the voltage sag and dV/dt on the load during power-on, and avoid unnecessary reset and other impacts. The SGM25720 not only has current limit function, but also detects power dissipation when used in series to ensure the operations within SOA. Once the current limit or power-limiting exceeds the preset value, the SGM25720 components will repeatedly try to recover until the faults are removed, and the SGM25720 will latch off. When the input voltage range exceeds EN/UVLO and OVLO ranges, the device breaks during the period.

Equipped with multi-channel measurement functions, the SGM25720 tracks input/output voltages, input current, input power, chip temperature and one auxiliary analog signal. This chip can record peak input power values and implement user-defined hardware average filtering for input voltage, output voltage, input current and input power. Designers can configure alert limits through the PMBus communication port to pull the nSMBA alert pin high/low once voltage, current, power or temperature exceeds preset ranges. Moreover, the device incorporates detection logic to spot breakdown issues of the external Q1 MOSFET.

Current Limit

Current limiting threshold triggers once the voltage drop across sense resistor R_S (between VIN and SENSE pins) surpasses an internal reference of either 24.5mV or 45mV. This preset internal voltage is selected via CL pin wiring: 24.5mV with CL tied to ground, and 45mV when CL connects to VDD. When current limiting engages, the IC regulates the Q1 MOSFET's gate potential to cap its conduction current.

Concurrent with active current-limit protection, the device's fault countdown timer starts working per specifications listed under Fault Timer and Restart. Should load current drop below the threshold ahead of the programmed fault timeout window, the SGM25720 automatically returns to regular operating mode. In contrast, continuous over-current lasting beyond the timeout duration (configured via timing capacitor C_T) triggers multiple fault flag assertions: the IIN_OC_FAULT flag inside MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h), the INPUT flag within STATUS_WORD (79h), alongside the IIN_OC/PFET_OP_FAULT bit all switch to logic high. Meanwhile, the nSMBA pin is pulled low, unless users disable this alert function through the MFR_SPECIFIC_08: ALERT_MASK (D8h) register.

To guarantee stable performance, R_S resistance must stay under 200mΩ; larger resistance values risk destabilizing the closed-loop current-limit control circuit. Users can also overwrite the default current-limit threshold by configuring corresponding configuration bits in MFR_SPECIFIC_09: DEVICE_SETUP (D9h).

Circuit Breaker

In cases of fast load current surges (such as load short-circuit faults), the current flowing through the sense resistor RS may surpass the current limit threshold prior to the response of the current limit control loop. Once the current rises to 1.8 or 3.6 times the threshold (user-configurable values), the 175mA gate pull-down current instantly turns off the MOSFET Q1, initiating the device's fault timeout cycle.

The 175mA gate pull-down function deactivates when the R_S voltage drops back below the threshold. Following this, Q1's gate voltage is regulated by either the current limit or power limit control mechanism. If the voltage at the TIMER pin rises to 1.7V while the current or power limiting state remains active, a 2mA gate pull-down current will shut down Q1, complying with the fault timer and restart operating rules.

A circuit breaker fault sets the CIRCUIT_BREAKER_FAULT bits to high in both STATUS_MFR_SPECIFIC (80h) and MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h). The nSMBA pin is simultaneously pulled low, and this alert can be disabled by configuring the ALERT_MASK (D8h) register. Default circuit breaker pin behavior may also be reconfigured via the DEVICE_SETUP (D9h) register.

DETAILED DESCRIPTION (continued)

Power-Limiting

The SGM25720 integrates a key MOSFET power limiting function, which constrains the maximum power dissipation of MOSFET Q1 within the device's safe operating area (SOA) specifications. The chip calculates the real-time power dissipation of Q1 by sampling the drain-source voltage across the SENSE and OUT pins and the drain current detected via the R_S sense resistor between VIN and SENSE pins. The measured power value is compared against the power limit threshold, which is preset through the external resistor connected to the PWR pin.

Upon exceeding the preset thermal dissipation threshold, the integrated circuit dynamically adjusts the gate voltage to regulate the MOSFET's drain current, maintaining optimal power stability. The fault monitoring timer is automatically initiated as soon as the power limiting mechanism becomes active, in strict compliance with the specified fault response and recovery protocols.

When the over-power condition persists beyond the configured fault detection period (determined by the CT timing capacitor), a comprehensive fault indication sequence is triggered.

Specifically, the IIN_OC_FAULT bit in STATUS_INPUT (7Ch), the INPUT bit in STATUS_WORD (79h), and the IIN_OC/PFET_OP_FAULT bit in MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h) are all set to logical high. Concurrently, the nSMBA output is driven low to signal the fault condition, unless the fault indication feature has been disabled via the MFR_SPECIFIC_08: ALERT_MASK (D8h) register setting. This fault signaling mechanism ensures immediate system awareness of critical power conditions while providing flexible configuration options for different operational requirements.

UVLO/EN

The SGM25720 turns on the series pass MOSFET Q1 only when the system input voltage V_{SYS} falls between the user-programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) operating boundaries. As illustrated in Figure 7, the V_{SYS} UVLO threshold is generally configured via an external resistor divider network consisting of R_1, R_2 and R_3. Per the device block diagram, a V_{SYS} voltage below the UVLO threshold activates the internal 23μA UVLO current source and disables the OVLO current source, while a 2mA gate pull-down current keeps Q1 in the off state.

As V_{SYS} rises and pushes the UVLO/EN pin voltage beyond its threshold, the 23μA UVLO current source turns off, elevating the UVLO/EN pin voltage and introducing threshold hysteresis. Once the UVLO/EN pin exceeds its valid threshold and the preset insertion delay time elapses, a 21μA gate current source activates Q1. The calculation workflow for threshold-setting resistors R_1 to R_3 is provided in the **Typical Application** section. Tying the UVLO/EN pin directly to VIN pin sets the device's minimum V_{SYS} UVLO level, where Q1 activates after the insertion delay once VIN crosses the power-on reset (POR) threshold.

After device power-up, a UVLO fault condition sets the VIN_UV_FAULT bit in STATUS_INPUT (7Ch), the INPUT bit in STATUS_WORD (79h), and the VIN_UNDERVOLTAGE_FAULT bit in MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h) to a high logic state. This fault event also pulls the nSMBA pin low, which can be masked by disabling the corresponding alert function through the MFR_SPECIFIC_08: ALERT_MASK (D8h) register.

OVLO

The series pass MOSFET (Q1) is turned on as long as the input supply voltage (V_{SYS}) remains between the programmable UVLO and OVLO limits. If V_{SYS} drives the OVLO pin above its trip point, the gate of Q1 is actively pulled down by a 2mA current, disabling the FET and stopping power delivery to the load. Once the OVLO threshold is crossed, an internal 23μA current source turns on to raise the OVLO pin voltage slightly, introducing hysteresis. Q1 resumes conduction only after VSYS falls below the OVLO threshold again.

An OVLO condition asserts the VIN_OV_FAULT bit in STATUS_INPUT (7Ch), sets the INPUT flag in STATUS_WORD (79h), and raises the VIN_OVERVOLTAGE_FAULT bit in MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h). The nSMBA pin is also driven low unless alert masking is enabled through the MFR_SPECIFIC_08: ALERT_MASK register (D8h). Resistor selection for setting the OVLO threshold is detailed in the **Typical Application** section.

DETAILED DESCRIPTION (continued)

Power Good Pin

The SGM25720 integrates an internal N-channel MOSFET for the Power Good (PGD) indicator, which withstands 18V steady-state off-state voltage and up to 20V transient voltage. An external pull-up resistor connected to a suitable supply rail is mandatory for the PGD pin, enabling it to deliver valid operating status signals to subsequent circuits. The PGD pin's voltage in the off state may lie above or below the voltages at VIN and OUT.

The PGD pin outputs a high logic level once the feedback (FB) pin voltage surpasses the predefined PGD threshold. The monitored threshold is commonly configured through an output-to-FB resistor divider network, while the device supports flexible voltage monitoring. Users can monitor other voltage signals provided that the FB pin voltage never exceeds its maximum rated value.

According to the device block diagram, the internal 23μA FB current source remains inactive when the FB pin voltage is below the threshold. As the monitored voltage increases and drives the FB pin above its threshold, the current source activates, sourcing current from the FB pin to establish hysteresis and ensure operational stability. The PGD pin is pulled low automatically if either the UVLO/EN pin voltage dips below its threshold or the OVLO pin voltage goes above its threshold. The current PGD status is accessible via the PMBus interface by reading the corresponding bits in STATUS_WORD (79h) and MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h).

VDD

The SGM25720 is equipped with a built-in linear sub-regulator that steps down the input voltage to produce a stable 4.5V supply for the device's low-voltage internal circuits. When the input voltage falls below 4.5V, the VDD rail follows the VIN voltage level. To prevent sub-regulator dropout at input voltages of 3.3V or lower, the VDD pin must be directly connected to VIN pin.

The internal VDD sub-regulator is the recommended pull-up power source for pins configured to a high state, including CL, CB, RETRY, ADR2, ADR1 and ADR0. It can also serve as the pull-up supply for the PGD pin and SMBus communication signals, namely SDA, SCL and nSMBA.

Designed exclusively for low-current auxiliary power supply, the VDD sub-regulator is not capable of driving high-current loads or external integrated circuits. For short-circuit protection, the VDD pin incorporates a 45mA current limit to safeguard the SGM25720 from damage. A bypass capacitor of 1μF to 4.7μF is also needed for the sub-regulator and must be positioned near the VDD pin on the PCB to ensure stability.

Remote Temperature Sensing

The SGM25720 supports remote temperature sensing via an external MMBT3904 NPN transistor. For proper sensing wiring, the transistor's base and collector terminals connect to the device's DIODE pin, while its emitter is tied to ground. This sensor transistor needs to be positioned adjacent to the target device for temperature monitoring. To accurately monitor the temperature of the hot-swap pass MOSFET Q1, mount the MMBT3904 as close to Q1 as the PCB layout permits.

Temperature detection is implemented by capturing the diode voltage variation induced by current excitation from the DIODE pin. The DIODE pin outputs a steady 10μA baseline current and injects a 260μA pulsed current every millisecond to sample the transistor temperature. To guarantee measurement accuracy, the PCB layout should minimize parasitic resistance between the DIODE pin and the MMBT3904 transistor to prevent accuracy loss in temperature measurements. A 1000pF bypass capacitor is recommended in parallel with the transistor to mitigate high-frequency noise.

Temperature readings are accessible via the PMBus command READ_TEMPERATURE_1 (8Dh). By default, the SGM25720 pulls the nSMBA pin low when the sensed temperature exceeds +125 °C and turns off the hot-swap MOSFET Q1 if the temperature climbs above +150 °C. These over-temperature thresholds can be reconfigured through PMBus using the OT_WARN_LIMIT (51h) and OT_FAULT_LIMIT (4Fh) commands. If remote temperature sensing and associated protection is not needed, the DIODE pin should be tied directly to ground.

DETAILED DESCRIPTION (continued)

Damaged MOSFET Detection

The SGM25720 provides built-in fault detection for external MOSFET Q1 damage under specific operating scenarios. When the voltage across the sense resistor surpasses 4mV with a low gate voltage, or when internal logic commands the gate to remain low, the device triggers an external MOSFET fault. This fault condition sets the EXT_MOSFET_SHORTED flag high in both the STATUS_MFR_SPECIFIC (80h) and MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h) registers, while pulling the nSMBA pin low. Users can disable this alert function by configuring the MFR_SPECIFIC_08: ALERT_MASK (D8h) register. This detection mechanism reliably identifies Q1 failures caused by drain-gate or drain-source short-circuit faults in the external MOSFET.

Power-Up Sequence

The SGM25720 operates with an input voltage range of 2.9V to 18V and can withstand transient voltage spikes up to 24V. As illustrated in Figure 6 below, a 175mA internal gate pull-down current keeps the external N-channel MOSFET Q1 off during the initial rise of VIN. This robust pull-down avoids unintended MOSFET turn-on while charging the device's gate-drain Miller capacitance, and the TIMER pin is held at ground in this initial state.

When V_{IN} rises above the power-on reset (POR) threshold, the device initiates the insertion delay period. During this time, the TIMER capacitor (C_T) is charged by a 5.5μA current source, and a 2mA gate pull-down current keeps Q1 firmly off, regardless of any variations in the input voltage. This delay stabilizes VIN ringing and transients to ensure safe MOSFET activation. The insertion period terminates when the TIMER pin voltage hits 1.7V, after which C_T is rapidly discharged via a 1.8mA internal pull-down current.

Subsequently, the GATE pin activates Q1 if the system input voltage V_{SYS} exceeds the UVLO threshold. If V_{SYS} satisfies the UVLO requirement upon completion of the insertion delay, Q1 turns on immediately. An internal charge pump delivers 21μA of current to charge Q1's gate capacitance, with an integrated 18.8V Zener diode capping the maximum ground-referenced GATE pin voltage.

As the OUT pin voltage ramps up, the SGM25720 keeps track of Q1's drain current and power dissipation in real time, using inrush and power-limiting control loops to dynamically adjust the load current. During the inrush limiting interval (t2 in Figure 6), C_T is charged by an internal 90μA current source. If, before the TIMER pin reaches 1.7V, both the input current and Q1's power consumption drop below their set limits, the 90μA source turns off and CT is discharged through a 2.8μA internal sink (t3 in Figure 6). The PGD pin goes high once the FB pin voltage crosses its rising threshold of 1.163V.

Should the TIMER pin voltage hit 1.7V while the device is still in inrush or power limiting during the Inrush Limit phase, a fault is triggered and Q1 is disabled. Detailed fault mode operations are elaborated in the Fault Timer and Restart section.

After V_{IN} exceeds the POR threshold, the SGM25720 pulls the nSMBA pin low to signal that all volatile memory and device parameters have loaded their default values. The CONFIG_PRESET bit in the STATUS_MFR_SPECIFIC (80h) register indicates default threshold and operational configurations, and remains asserted until the device receives a CLEAR_FAULTS command.

DETAILED DESCRIPTION (continued)

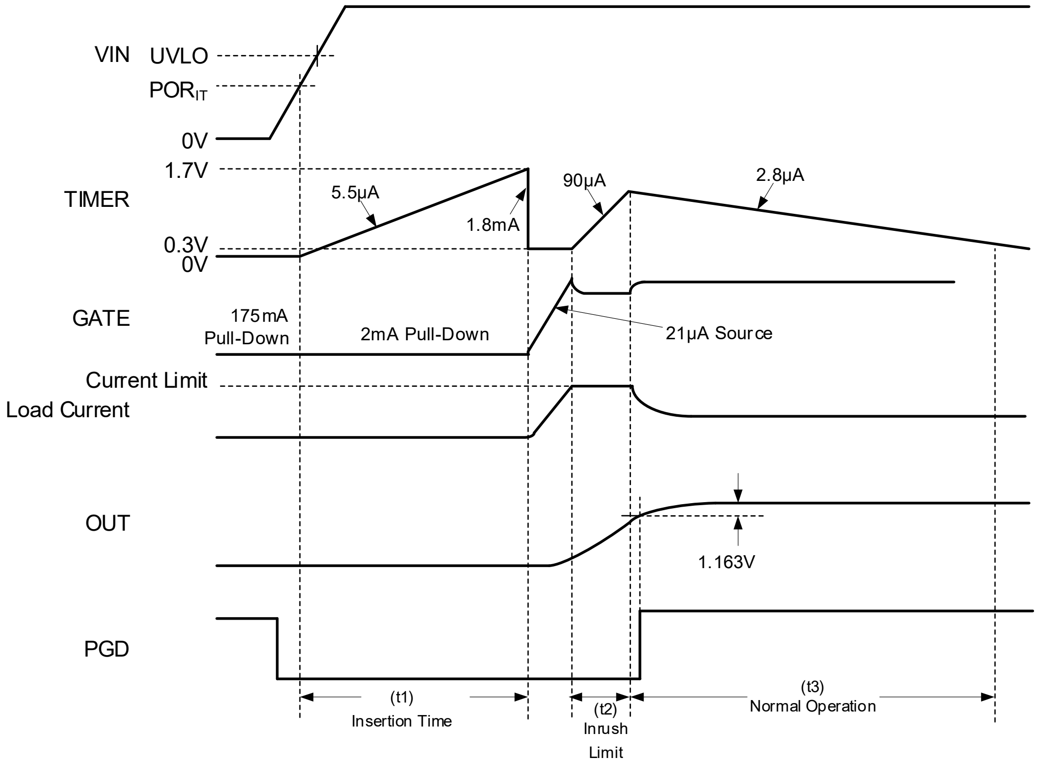


Figure 6. Power-Up Sequence (Power-Limiting Only)

Gate Control

An integrated charge pump supplies voltage to the GATE pin to fully drive the external N-channel MOSFET. Under steady-state normal operation (t3 in Figure 6), a 21μA internal current source sustains the charge on Q1's gate terminal. An embedded 18.8V Zener diode clamps the maximum ground-referenced GATE pin voltage, as characterized in ***GATE Pin Voltage vs. Temperature*** of the Typical Characteristics curves. Since Q1 may endure a gate-source voltage up to 18.8V under operating conditions, an external Zener diode between the GATE and OUT pins is mandatory if the selected MOSFET's maximum V_{GS} rating is lower than 18.8V. This supplementary Zener device requires a minimum forward current capability of 175mA.

At initial system power-up, a 175mA pull-down current keeps the GATE pin low. This mechanism eliminates unintended MOSFET turn-on caused by voltage coupling through the drain-gate parasitic capacitance during input voltage ramp-up. During the insertion delay phase (t1 in Figure 6), a 2mA pull-down current holds the GATE pin low, keeping Q1 consistently off independent of V_{IN} and UVLO voltage states throughout the Insertion Time period.

Upon completion of the insertion delay (t2 in Figure 6), the device dynamically adjusts Q1's gate voltage to confine the load current and MOSFET power dissipation within preset limits. The TIMER capacitor charges continuously while the device operates in current or power limiting mode. Once current and power regulation conditions terminate before the TIMER pin reaches 1.7V, the capacitor discharges and the system resumes standard operating mode.

If the inrush limiting state persists long enough to drive the TIMER pin voltage to 1.7V within the Inrush Limit interval, a 175mA pull-down current forces the GATE pin low. Q1 remains off until either a manual power-up reset is triggered by pulling the RETRY pin to VDD or an automatic restart is initiated with the RETRY pin grounded, with detailed rules specified in the Fault Timer and Restart section. Furthermore, the 2mA GATE pull-down current activates to turn off Q1 when the system input voltage drops below the UVLO threshold or exceeds the OVLO threshold.

DETAILED DESCRIPTION (continued)

Shutdown Control

In addition, the remote control device can be turned off and safely started by connecting an open collector device or an open-drain device on the UVLO/EN pin, as shown in the Figure 7.

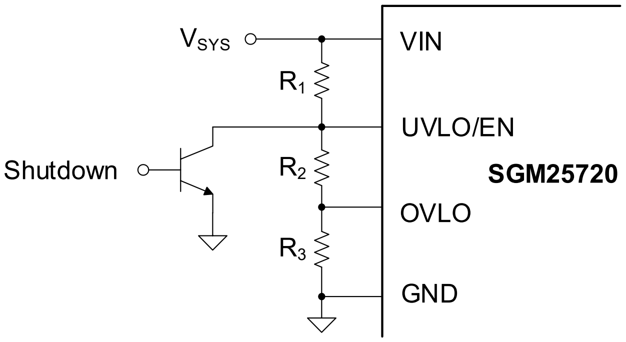


Figure 7. Shutdown Control

Fault Timer and Restart

During device turn-on or fault events that trigger current or power limit activation, the SGM25720 adjusts Q1's gate-source voltage to stabilize the load current and restrict the MOSFET's power consumption. While either protection loop is engaged, a 90μA fault timer current source charges the external TIMER capacitor C_T to initiate the fault timeout sequence, as illustrated in Figure 6.

If the abnormal operating condition clears before the TIMER pin ramps to 1.7V within the timeout window, the device reverts to normal operation, and a 1.8mA current sink fully discharges the C_T capacitor. In contrast, the device shuts down Q1 via a 2mA GATE pull-down current once the TIMER pin voltage reaches 1.7V, with the subsequent restart behavior determined by the RETRY pin configuration.

When the RETRY pin is set high, the SGM25720 latches the GATE pin low upon fault timeout completion. Meanwhile, a 2.8μA fault current sink discharges the CT capacitor to ground. The 2mA pull-down current maintains the GATE pin low continuously until an external reset is performed, either by cycling the system input voltage V_{SYS} or temporarily pulling the UVLO/EN pin below its threshold through an open-collector or open-drain circuit (Figure 8). Valid restart operations require the TIMER pin voltage to stay below 0.3V. The TIMER_LATCHED_OFF bit in the MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h) register remains logic-high for the entire duration of the latched-off fault state.

The SGM25720 features a built-in automatic restart mechanism. Following a fault timeout event, the TIMER pin cycles between 1.7V and 1V for seven consecutive times, as depicted in Figure 9. Each cycle duration is defined by the 90μA charging current, the 2.8μA discharging current and the capacitance value of the external CT capacitor. During the eighth high-to-low voltage transition, the TIMER pin drops to 0.3V, which activates the 21μA gate current source to turn Q1 back on. If the fault persists after device reactivation, the fault timeout and restart sequence will repeat cyclically.

The RETRY pin configures the device for either disabled retries or unlimited automatic retries. For more flexible and precise retry configuration, users can program the MFR_SPECIFIC_09: DEVICE_SETUP (D9h) register. This register supports configurable retry counts of 0, 1, 2, 4, 8, 16 cycles or continuous infinite retries via corresponding bit settings.

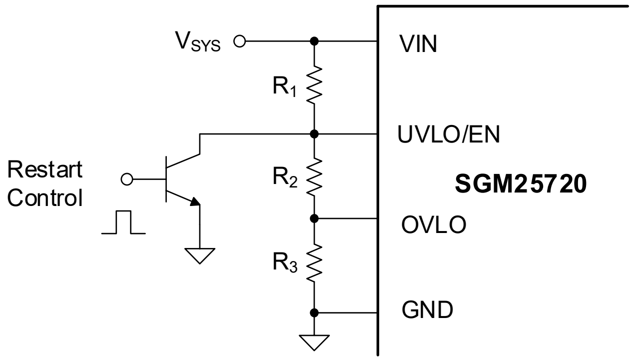


Figure 8. Latched Fault Restart Control

DETAILED DESCRIPTION (continued)

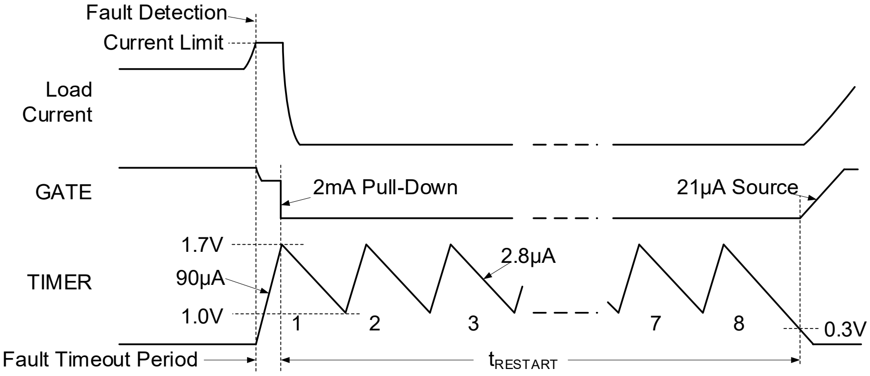


Figure 9. Restart Sequence

Enabling/Disabling and Resetting

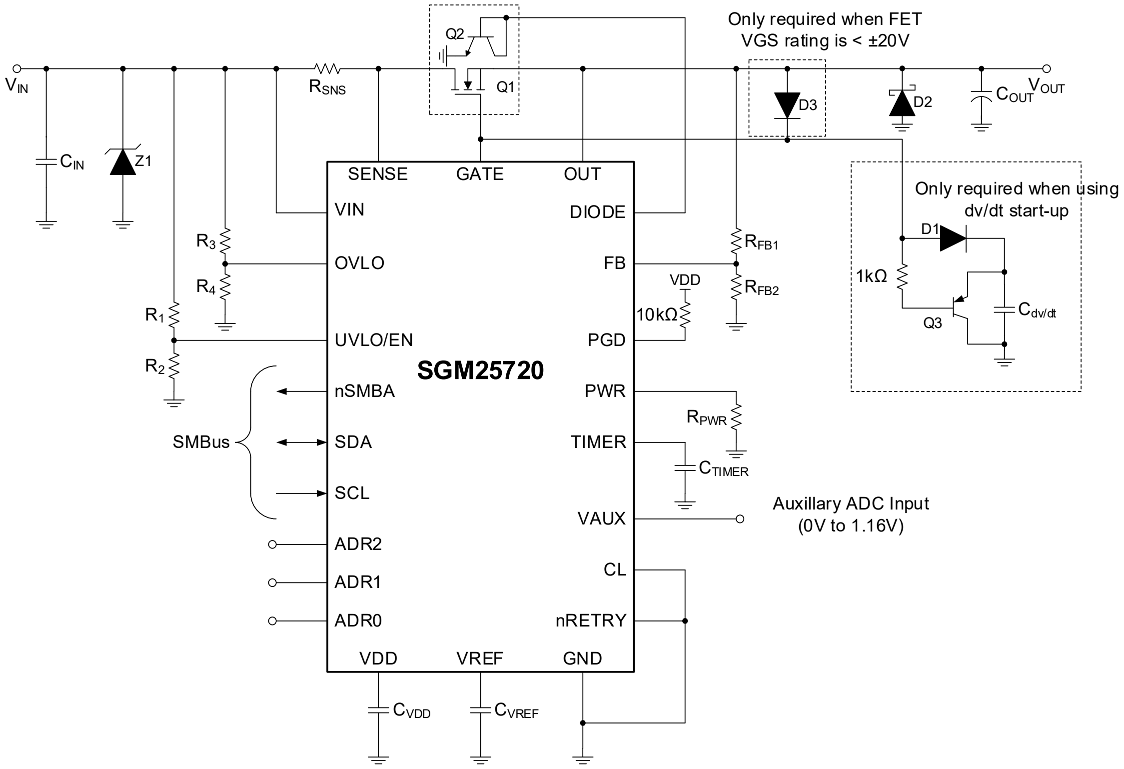
Under normal operating conditions, the SGM25720's output can be turned off at any moment by driving the UVLO/EN pin below its activation threshold or driving the OVLO pin above its threshold. Either operation forces the device's GATE pin low through a 2mA pull-down current. Toggling the UVLO/EN pin serves as a reset method for the device to exit the latched-off state, which occurs when overcurrent or overpower faults exhaust the maximum retry times. Notably, disabling the output through UVLO/EN or OVLO pins does not alter the device's volatile memory or address settings. All user-defined configurations, including device address, operating parameters, fault thresholds and warning levels programmed via SMBus, remain intact as long as the chip stays powered, independent of UVLO/EN and OVLO pin states.

Alternatively, users can enable or disable the output by writing 80h or 0h to the OPERATION (03h) register respectively. To restore normal output after a fault shutdown, the existing fault state must first be cleared, followed by writing 0h and then 80h sequentially to the OPERATION (03h) register.

The SGM25720 captures its SMBus address based on the power-up logic states of the ADR0, ADR1 and ADR2 pins (GND, NC, VDD). This address value is locked into a volatile register after VDD rises above its 2.7V POR threshold. Holding the VREF pin low allows users to delay or reconfigure the address capture process, while also resetting internal logic and clearing the device's volatile memory. When the VREF pin is released, its voltage ramps up gradually, and the SMBus address is latched into the volatile register once the VREF pin voltage exceeds 2.4V.

APPLICATION INFORMATION

Typical Application


Only required when FET VGS rating is < ±20V

Only required when using dv/dt start-up

Auxillary ADC Input (0V to 1.16V)

Figure 10. Typical Application Circuit

Design Requirements

Table 44 summarizes the key design parameters that must be established before implementing a hot-swap circuit. When the output capacitor is charged through the hot-swap MOSFET, the energy dissipated in the FET equals the energy stored in the capacitor, expressed as (½CV²). Consequently, the input voltage and output capacitance jointly determine the stress on the MOSFET. The peak load current sets the required current-limit threshold and dictates the sense resistor value. This current, together with the maximum ambient temperature and the PCB's case-to-ambient thermal resistance ($R_{\theta CA}$), influences the choice of MOSFET R_{DSON} and whether paralleling multiple FETs is necessary. ($R_{\theta CA}$), is strongly affected by layout, especially the copper area connected to the MOSFET drain. Because the drain is not electrically connected to the ground plane, the ground plane cannot aid in heat removal. For this example, ($R_{\theta CA}$) = 30°C/W is used, aligning with the SGM25720 evaluation module. It is advisable to measure the actual ($R_{\theta CA}$), once physical PCBs are available.

Finally, clearly defining the test conditions the hot-swap circuit must meet is critical. In most cases, the design should reliably survive both a "Hot-Short" and a "Start-into-Short," as detailed earlier. Additionally, the load should remain off until the hot-swap controller has fully powered up. Activating the load too early imposes excessive stress on the MOSFET and may cause startup failures or permanent damage.

Table 44. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	10V to 14V
Maximum load current	45A
Maximum output capacitance of the hotswap	5600μF
Maximum ambient temperature	55℃
MOSFET $R_{\theta CA}$ (function of layout)	30℃/W
Pass a Hot-Short on output?	Yes
Pass a Start-into-Short?	Yes
Is the load OFF until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

APPLICATION INFORMATION (continued)

Detailed Design Procedure

Select R_{SNS} and CL setting

The SGM25720 offers two current-limit sense thresholds: 24.5mV and 45mV. Choosing the lower 24.5mV setting typically allows for a smaller sense resistor (R_{SNS}) and reduces I^2R conduction losses. In this design, the 24.5mV mode is selected by tying the CL pin directly to GND. To ensure reliable operation despite device tolerances, the current limit should be set at least 8% higher than the maximum anticipated load current. With a target trip point of 49A, the required sense resistor value is determined using Equation 5:

$$R_{SNS} = \frac{V_{CL}}{I_{LIM}} = \frac{24.5mV}{49A} = 0.5m\Omega \tag{5}$$

Since sense resistors are typically available only in standard discrete values, achieving an exact current limit may require additional circuitry. For improved accuracy, a combination of a sense resistor and a resistor divider - configured as shown in Figure 11 - can be employed to fine-tune the effective current-sense voltage and thus set a more precise current limit.

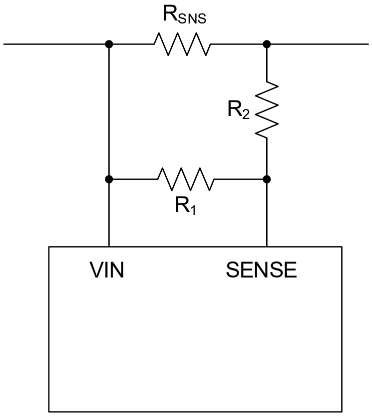


Figure 11. SENSE Resistor Divider

If a resistor divider is used, the next higher standard-value sense resistor should be selected (e.g., 1mΩ). The ratio of R_1 to R_2 can then be determined using Equation 6:

$$\frac{R_1}{R_2} = \frac{R_{SNS\_CLC}}{R_{SNS} - R_{SNS\_CLC}} = \frac{0.5m\Omega}{1m\Omega - 0.5m\Omega} = 1 \tag{6}$$

The SENSE pin sources a 28μA current, which introduces a voltage offset across R_2. To reduce this offset, it is advisable to limit R_2 to less than 10Ω. Additionally, the use of 1% tolerance resistors will impact the overall accuracy of current monitoring. When implementing a resistor divider, the effective sense resistance (R_{SNS_EFF}) must be calculated using Equation 7 and used in place of R_{SNS} for all subsequent computations.

$$R_{SNS\_EFF} = \frac{R_{SNS} \times R_1}{R_1 + R_2} \tag{7}$$

For many applications, tight current-limit accuracy isn't essential. In such cases, opting for the next lower standard-value sense resistor simplifies the design. Here, a 0.5mΩ resistor can be used to target a current limit of roughly 49A.

Selecting the Hot-Swap MOSFET(s)

Selecting the right MOSFET for hot-swap applications is critical. Please ensure that the device meets the requirements as below:

- The MOSFET's VDS rating should be adequate to tolerate the highest expected system voltage, including transient overshoots or ringing. For standard 12V systems, a 30V MOSFET is typically sufficient.
- The SOA (Safe Operating Area) of the MOSFET must be adequate to handle all operational scenarios, including startup, Hot-Short, and Start-into-Short conditions.
- R_{DSON} should be low enough to keep both the junction and case temperatures below the MOSFET's maximum rated limits. In real-world operation, the MOSFET's steady-state temperature should be kept below +125℃ to allow sufficient thermal margin for transient events.
- The MOSFET's continuous drain current rating should be higher than the peak expected load current, and its pulsed current handling capability must exceed the circuit breaker's trip point. In most cases, MOSFETs that satisfy the first three requirements - VDS rating, SOA, and R_{DSON} - will inherently meet these two current-related criteria as well.
- A VGS rating of ±20V is required because the SGM25720 can drive the gate up to 16V above the source. Alternatively, for MOSFETs with a lower ±12V VGS rating, a protective diode (such as D3 in Figure 10) can be added to clamp the gate-source voltage and prevent overstress.

APPLICATION INFORMATION (continued)

For this design, the CSD17556Q5B was chosen due to its low R_{DSON} and robust Safe Operating Area (SOA). Once the MOSFET is selected, the maximum steady-state case temperature can be calculated using Equation 8:

$$T_{C\_MAX} = T_{A\_MAX} + R_{\theta CA} \times I^2_{LOAD\_MAX} \times R_{DSON}\ (T_J) \tag{8}$$

Note that R_{DSON} varies significantly with junction temperature, which for most MOSFETs closely matches the case temperature. Therefore, the calculation process may need to be repeated several times to converge on a consistent pair of values for R_{DSON} and the maximum case temperature $T_{C.MAX.}$ The CSD17556Q5B datasheet indicates that at +85℃, R_{DSON} is about 30% higher than its room-temperature R_{DSON} value. Equation 9 uses this thermally adjusted resistance to estimate $T_{C\_MAX.}$

$$T_{C\_MAX} = 55°C + 30\frac{°C}{W} \times (45A)^2 \times 1.3 \times 1.4m\Omega = 165.6°C \tag{9}$$

The estimated maximum steady-state case temperature implies that a second MOSFET might be needed to distribute and reduce power dissipation under typical operating conditions. With MOSFETs paralleled, the peak steady-state case temperature can be predicted using Equation 10.

$$T_{C\_MAX} = T_{A\_MAX} + R_{\theta CA} \times \left(\frac{I_{LOAD\_MAX}}{\#\text{ of MOSFETs}}\right)^2 \times R_{DSON}(T_J) \tag{10}$$

Therefore, paralleling two CSD17556Q5B devices yields a steady-state case temperature of:

$$T_{C\_MAX} = 55°C + 30\frac{°C}{W} \times \left(\frac{45A}{2}\right)^2 \times 1.3 \times 1.4m\Omega = 82.6°C \tag{11}$$

The resulting T_{C_MAX} aligns closely with the junction temperature used to determine R_{DSON} eliminating the need for further iterative calculations.

Select Power-Limiting

As a rule of thumb, setting a lower power limit helps reduce MOSFET stress. However, if the SGM25720 is configured with an excessively low power threshold, it forces the device to regulate the FET current - and thus the sense resistor voltage (V_{SNS}) to a very small level. The resulting V_{SNS} can be computed using Equation 12:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \tag{12}$$

To prevent significant degradation of power-limiting accuracy, a V_{SNS} below 4mV is not advised. Based on this constraint, the minimum allowable power limit can be derived using Equation 13:

$$P_{LIM\_MIN} = \frac{V_{SNS\_MIN} \times V_{IN\_MAX}}{R_{SNS}} = \frac{4mV \times 14V}{0.5m\Omega} = 112W \tag{13}$$

In typical applications, the power limit can be set to P_{LIM_MIN} using Equation 14, where R_{SNS} and R_{PWR} are expressed in ohms (Ω) and P_{LIM} is in watts.

$$R_{PWR} = 2.05 \times 10^5 \times R_{SNS} \times \left(P_{LIM} - 1.7mV \times \frac{V_{DS}}{R_{SNS}}\right) \tag{14}$$

Note that the minimum value of R_{PWR} occurs when $V_{DS} = V_{IN\_MAX.}$ Under this worst case condition, the smallest allowable R_{PWR} can be determined using Equation 15:

$$\begin{aligned} R_{PWR} &= 2.05 \times 10^5 \times 0.5m\Omega \times \left(112W - 1.7mV \times \frac{14V}{0.5m\Omega}\right) \\ &= 6.6k\Omega \end{aligned} \tag{15}$$

A standard resistor value just above the calculated minimum should be used. Here, a 6.6kΩ resistor was selected, establishing a power limit of approximately 112W.

APPLICATION INFORMATION (continued)

Set Fault Timer

The fault timer is active whenever the hot-swap circuit operates in power-limit or current-limit mode conditions commonly encountered during startup. To avoid unintended shutdowns, the timer must be set with sufficient margin to accommodate the full startup transient. In the worst-case scenario where the device powers up directly into current limit (i.e., $I_{LIM} \times V_{DS} < P_{LIM}$), the maximum allowable startup time can be calculated using Equation 16:

$$t_{START\_MAX} = \frac{C_{OUT} \times V_{IN\_MAX}}{I_{LIM}} \tag{16}$$

For this example, the device enters a conversion from power-limiting to current limit during startup. The startup time can be estimated according to Equation 17.

$$t_{START} = \frac{C_{OUT}}{2} \times \left(\frac{V_{IN\_MAX}{}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}{}^2} \right) = \frac{5600\mu F}{2} \times \left(\frac{14V^2}{112W} + \frac{112W}{49A^2} \right) = 5.03ms \tag{17}$$

Please note that the time calculated above is the ideal constant power conversion to constant current startup. Because power-limiting is a function of V_{DS}, the actual startup time will be longer than calculated time. In addition, it needs to consider errors introduced by some device specifications, such as C_{TIMER} and constant current source, power-limiting value, etc., and also needs an additional 50% time margin to ensure that the startup time does not time out. Therefore, use Equation 18 to determine the value of the fault timer capacitance.

$$C_{TIMER} = \frac{t_{FLT} \times I_{TIMER}}{V_{TIMER}} = \frac{10.06ms \times 90\mu A}{1.7V} = 533nF \tag{18}$$

The capacitor of 560nF with a slightly larger capacitance can be selected to calculate the programming time of the fault timer according to Equation 19.

$$t_{FLT} = \frac{C_{TIMER} \times V_{TIMER}}{I_{TIMER}} = \frac{560nF \times 1.7V}{90\mu A} = 10.58ms \tag{19}$$

Check MOSFET SOA

After setting the power limit and fault timer, it’s crucial to confirm the MOSFET remains within its Safe Operating Area (SOA) across all specified stress conditions.

In a “Hot-Short” scenario, the circuit breaker trips, causing the SGM25720 to re-enter power-limit mode and remain there until the fault timer expires. The worst-case stress occurs when $V_{DS} = V_{IN\_MAX}$, $I_D = P_{LIM}/V_{IN\_MAX,}$ and this condition lasts for the full fault timeout duration (t_{FLT}), For this design, the MOSFET endures 14V and 8A for 10.58ms. Per the CSD17556Q5B datasheet, the part supports 14V at 10A for 10ms and 14V at 3A for 100ms. Since 10.58ms falls between these two points, the SOA at this specific duration can be estimated by approximating the SOA - time curve as a power-law function, as outlined in Equations 20 through 23:

$$I_{SOA}(t) = a \times t^m \tag{20}$$

$$m = \frac{\ln\left(\frac{I_{SOA}(t_1)}{I_{SOA}(t_2)} \right)}{\ln\left(\frac{t_1}{t_2} \right)} = \frac{\ln\left(\frac{10A}{3A} \right)}{\ln\left(\frac{10ms}{100ms} \right)} = -0.523 \tag{21}$$

$$a = \frac{I_{SOA}(t_1)}{t_1{}^m} = \frac{10A}{10ms^{-0.523}} = 10A \times 10ms^{0.523} \tag{22}$$

$$I_{SOA}(10.58ms) = 10A \times 10ms^{0.523} \times 10.58ms^{-0.523} = 9.71A \tag{23}$$

Note that the current calculated above is an ideal calculation considering the MOSFET case temperature to be +25℃. A certain ambient temperature and thermal increase during operation can make the MOSFET more possible to Hot-Short. It can use Equation 24 to calculate the approximate current.

$$\begin{aligned} I_{SOA}(10.58ms, T_{C\_MAX}) &= I_{SOA}(10.58ms, 25°C) \times \frac{T_{J\_ABSMAX} - T_{C\_MAX}}{T_{J\_ABSMAX} - 25°C} \\ &= 9.71A \times \frac{150°C - 82.6°C}{150°C - 25°C} = 5.24A \end{aligned} \tag{24}$$

APPLICATION INFORMATION (continued)

The calculation shows that, at elevated case temperatures, the MOSFET can only safely handle 14V at 5.24A for 10.58ms yet the “Hot-Short” scenario requires it to endure 8A under identical conditions. This gap implies a real risk of device failure during such an event. To ensure reliability, it’s generally recommended that the MOSFET be rated to withstand at least 30% more power than the worst-case Hot-Short demand. This safety margin compensates for variations in the actual power-limit setting, fault timer tolerance, and thermal environment, helping to prevent SOA violations in production units.

Switching to dV/dt Based Start-up

In systems with very high load currents and large output capacitances, using a power-limit-based startup strategy often becomes impractical. Higher load currents require a smaller sense resistor to keep losses low—but this forces the minimum power limit to rise, since the controller can’t regulate accurately below a certain sense voltage. At the same time, a larger output capacitor means the inrush charging phase lasts longer, which demands a longer fault timer to avoid false triggering during normal startup. The combination of a higher power limit and an extended fault duration significantly increases the stress on the MOSFET during worst-case events like a “Hot-Short” or “Start-into-Short.” Eventually, the required robustness exceeds what even the best available MOSFETs can handle, leaving no viable device that can reliably survive these conditions—making pure power-limit control unsuitable for such demanding designs.

To avoid these limitations, a dV/dt limiting capacitor ($C_{dv/dt}$) can be introduced to control the gate drive slew rate—thereby slowing the rise of the output voltage. By reducing how fast ramps up, the inrush current can be made arbitrarily small, effectively decoupling startup stress from the size of the load capacitance or the magnitude of the steady-state load current. In this configuration, the power limit is set just high enough to satisfy the controller’s minimum requirement and ensure the fault timer never triggers during normal startup. This is achieved by making sure the current equivalent of the power limit (P_{LIM} /V_{IN_MAX}) exceeds the actual inrush current. Because the timer remains inactive during startup, it can be kept short minimizing the duration of stress on the MOSFET during worst-case faults like “Start-into-Short” or “Hot-Short.”

Diode D2 plays a critical role: it isolates the charge on $C_{dV/dt}$ from the power-limit feedback loop during a Hot-Short, preventing unwanted interaction that could destabilize regulation. Meanwhile, transistor Q3 provides a discharge path for $C_{dV/dt}$ when the hot-swap gate is turned off, ensuring a rapid and controlled reset for the next startup cycle.

To ensure safe operation, the inrush current must be limited so the MOSFET stays well within its Safe Operating Area (SOA) during startup. A key insight is that the total energy dissipated in the MOSFET during startup is essentially fixed—it’s determined by the input voltage and output capacitance, not by how fast the transition occurs. Therefore, as long as the load remains off during startup, slowing down the voltage ramp (i.e., reducing the slew rate) spreads that fixed energy over a longer duration, which always lowers peak power stress on the device.

When selecting a target slew rate, start with a practical baseline such as 0.25V/ms, then evaluate the resulting operating point against the MOSFET’s SOA. If the device approaches its limits, simply reduce the slew rate further to add margin. Using 0.25V/ms as an initial reference, the corresponding inrush current can be estimated as follows:

$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} = 5600\mu F \times \frac{0.25V}{ms} = 1.4A \tag{25}$$

Assuming a maximum input voltage of 14V and a slew rate of 0.25V/ms, the startup will take approximately 56ms. During this time, the MOSFET’s power dissipation begins at its peak V_{IN_MAX} × I_{INR} and gradually tapers to zero as V_{DS} across the device decreases.

APPLICATION INFORMATION (continued)

Since SOA curves are typically defined for constant-power rectangular pulses, a conservative way to assess real-world startup stress is to model the actual triangular-like power profile as an equivalent rectangular pulse with the same energy. A common simplification is to assume the MOSFET dissipates the peak power ($P_{FET} = V_{IN\_MAX} \times I_{INR}$) for half the total startup duration i.e., $t = t_{startup}/2$. In this case, that translates to evaluating the SOA at 14V, 1.4A, for 28ms. Using the same interpolation method described earlier for SOA validation (e.g., power-law fitting between known points), the MOSFET's capability under this equivalent pulse can be estimated using Equation 26.

$$I_{SOA}\left(28ms\right) = 10A \times 10ms^{0.523} \times 28ms^{-0.523} = 5.84A \tag{26}$$

This SOA-derived current limit must also be derated for temperature. In this analysis, we conservatively assume the MOSFET's case temperature (T_C) could immediately reach the maximum ambient temperature (T_{A_MAX}) at the moment the board is plugged in such as when hot-plugging into a high-temperature environment (e.g., inside an enclosed chassis or industrial setting).

Since SOA curves in datasheets are typically specified at a reference junction or case temperature (often 25 °C), operating at elevated temperatures reduces the device's safe current-handling capability. Therefore, the allowable current from Equation 27 should be further scaled down using the manufacturer's recommended thermal derating guidelines to ensure reliable operation under worst-case thermal conditions.

$$\begin{aligned} I_{SOA}\left(28ms, T_{A\_MAX}\right) &= I_{SOA}\left(28ms, 25°C\right) \times \frac{T_{JABS\_MAX} - T_{A\_MAX}}{T_{JABS\_MAX} - 25°C} \\ &= 5.84A \times \frac{150°C - 55°C}{150°C - 25°C} = 4.44A \end{aligned} \tag{27}$$

The calculation confirms the MOSFET can support 4.44A at 14V for 28ms under elevated ambient temperature, which is more than sufficient compared to the actual requirement of 1.4A. This ensures the device remains well within its Safe Operating Area (SOA) during startup, as long as the input voltage slew rate is limited to 0.25V/ms or lower. It should be noted that when the load is disabled during startup, the total energy dissipated in the MOSFET is independent of the slew rate. However, a slower slew rate reduces peak power dissipation, thereby minimizing stress on the device. To cap the slew rate at 0.25V/ms, size the gate-drive timing capacitor using Equation 28, which defines the required $C_{dV/dt}$ relationship.

$$C_{dV/dt} = \times \frac{I_{SOURCE\_MAX}}{0.25V/ms} = \frac{22\mu A}{0.25V/ms} = 88nF \tag{28}$$

The next higher standard $C_{dV/dt}$ value is selected as 100nF, resulting in a typical slew rate of 0.22V/ms and a startup time of 55ms for a 12V input.

$$V_{OUT,dV/dt} = \times \frac{I_{SOURCE}}{C_{dV/dt}} = \frac{22\mu A}{100nF} = 0.22V/ms \tag{29}$$

In certain cases, temperature derating may be based on T_{C_MAX} rather than T_{A_MAX} typically only in the worst-case situation where a board is hot-unplugged and reinserted before returning to ambient temperature. For the majority of applications, using T_{A_MAX} for derating is appropriate.

$$\begin{aligned} I_{SOA}\left(28ms, T_{C\_MAX}\right) &= I_{SOA}\left(28ms, 25°C\right) \times \frac{T_{J\_ABSMAX} - T_{C\_MAX}}{T_{J\_ABSMAX} - 25°C} \\ &= 5.84A \times \frac{150°C - 82.6°C}{150°C - 25°C} = 3.15A \end{aligned} \tag{30}$$

With derating based on T_{C_MAX} the MOSFET is capable of supporting 3.15A at 14V for 28ms under elevated case temperature, significantly exceeding the 1.4A requirement. This ensures ample SOA margin during startup as long as the slew rate remains at or below 0.25V/ms.

APPLICATION INFORMATION (continued)

Select Power Limit and Fault Timer

When selecting the power limit, two key requirements must be satisfied:

a. Maintain sufficient sense voltage: The power limit must be high enough to keep the voltage across the sense resistor (V_{SNS}) at or above 4mV during normal operation. Going below this threshold can degrade regulation accuracy and compromise current monitoring.
b. Prevent fault timer activation during startup: The power limit should be set well above the peak inrush power demand to ensure the fault timer never triggers under normal startup conditions. A robust design practice is to size the power limit to at least twice the worst-case inrush power that is, 2 × I_{INR_MAX} × V_{IN_MAX}.

Thus, the minimum allowable power limit is determined using Equation 31.

$$\begin{aligned} P_{LIM\_MIN} &= MAX\left(\frac{V_{SNS\_MIN} \times V_{IN\_MAX}}{R_{SNS}}, 2 \times V_{IN\_MAX} \times I_{INR\_MAX}\right) \\ &= MAX(112W, 39.2W) = 112W \end{aligned} \tag{31}$$

Next, the power limit is configured to P_{LIM_MIN}, using the following equation, with R_{SNS} and R_{PWR} expressed in ohms (Ω) and P_{LIM} in Watts (W).

$$\begin{aligned} R_{PWR} &= 2.05 \times 10^5 \times R_{SNS} \times \left(P_{LIM} - 1.7mV \times \frac{V_{DS}}{R_{SNS}}\right) \\ &= 2.05 \times 10^5 \times 0.5m\Omega \times \left(112W - 1.7mV \times \frac{14V}{0.5m\Omega}\right) \\ &= 6.6k\Omega \end{aligned} \tag{32}$$

Select the closest standard resistor value available. For this design, a 6.6kΩ resistor was used.

Next, a fault timer value should be selected. As a general guideline, the timer should be reduced as much as possible while still maintaining sufficient margin between the MOSFET's available Safe Operating Area (SOA) and the actual power pulse it experiences during a Hot-Short event.

For this design, a 22nF capacitor was chosen for C_{TIMER}, which corresponds to a fault time of 420μs. The available SOA at this duration was estimated using the same extrapolation method described earlier.

$$I_{SOA}(t) = a \times t^m \tag{33}$$

$$m = \frac{\ln\left(\frac{I_{SOA}(t_1)}{I_{SOA}(t_2)}\right)}{\ln\left(\frac{t_1}{t_2}\right)} = \frac{\ln\left(\frac{100A}{30A}\right)}{\ln\left(\frac{0.1ms}{1ms}\right)} = -0.52 \tag{34}$$

$$a = \frac{I_{SOA}(t_2)}{{t_2}^m} = \frac{30A}{1ms^{-0.52}} = 30A \times 1ms^{0.52} \tag{35}$$

$$I_{SOA}(0.52ms, 25°C) = 30A \times 1ms^{0.52} \times 0.52ms^{-0.52} = 42.3A \tag{36}$$

Next, the available SOA is derated for temperature.

$$I_{SOA}(0.52ms, T_{C\_MAX}) = 42.3A \times \frac{175°C - 114°C}{175°C - 25°C} = 17.17A \tag{37}$$

The design requires only 4A, while the MOSFET after temperature SOA derating can safely handle up to 17.17A. This significant headroom confirms a robust design with ample safety margin.

APPLICATION INFORMATION (continued)

Set Under-Voltage and Over-Voltage Threshold

The SGM25720 controls the series pass device (Q1) based on user-programmed UVLO and OVLO thresholds. Q1 is enabled only when the input supply voltage (V_{SYS}) remains within the specified operating range. If V_{SYS} drops below the UVLO threshold or exceeds the OVLO threshold, Q1 is immediately disabled, cutting off power to the load for protection. Both thresholds incorporate hysteresis to prevent chatter and ensure stable operation during voltage transients near the trip points.

Option A

The configuration shown in Figure 12 uses three resistors R_1, R_2 and R_3 to set the UVLO and OVLO thresholds. These resistors form a voltage divider network that programs the precise input voltage levels at which the SGM25720 enables or disables the series pass device Q1.

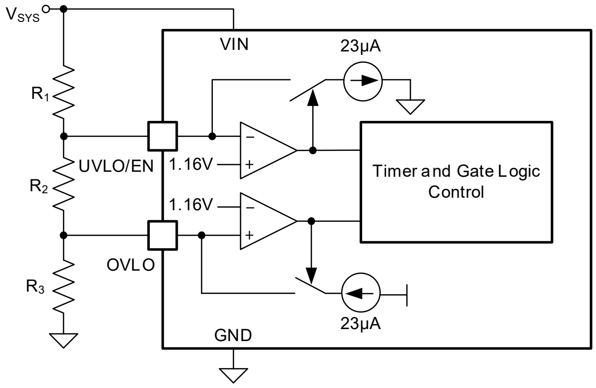


Figure 12. UVLO and OVLO Thresholds Set By R1-R3

The resistor values are calculated using the following procedure:

- Define the upper UVLO trip point (V_{UVH}) and the lower UVLO trip point (V_{UVL}).
- Define the upper OVLO threshold (V_{OVH}).
- Note that the lower OVLO threshold (V_{OVL}) cannot be independently set in this configuration—it is determined once R_1, R_2, and R_3 are calculated. If precise control of V_{OVL} is also required, along with the other three thresholds, refer to *Option B* below.

$$R_1 = \frac{V_{UVH} - V_{UVL}}{23\mu A} = \frac{V_{UV\_HYS}}{23\mu A} \tag{38}$$

$$R_3 = \frac{1.16V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 1.16V)} \tag{39}$$

$$R_2 = \frac{1.16V \times R_1}{V_{UVL} - 1.16V} - R_3 \tag{40}$$

The lower OVLO threshold is derived from:

$$V_{OVL} = \left[(R_1 + R_2) \times \left(\frac{1.16V}{R_3} - 23\mu A\right)\right] + 1.16V \tag{41}$$

As an example, suppose the application specifies the following thresholds: V_{UVH} = 8V, V_{UVL} = 7V, V_{OVH} = 15V.

$$R_1 = \frac{8V - 7V}{23\mu A} = \frac{1V}{23\mu A} = 43.5k\Omega \tag{42}$$

$$R_3 = \frac{1.16V \times R_1 \times 7V}{15V \times (7V - 1.16V)} = 4.03k\Omega \tag{43}$$

$$R_2 = \frac{1.16V \times R_1}{7V - 1.16V} - R_3 = 4.61k\Omega \tag{44}$$

The lower OVLO threshold comes out to 12.03V, resulting in an OVLO hysteresis of 2.97V. In this setup, the OVLO hysteresis is consistently somewhat larger than the UVLO hysteresis. With R_1, R_2, R_3 known, the actual threshold voltages and hysteresis values are obtained from the following expressions:

$$V_{OVL} = \left[(R_1 + R_2) \times \left(\frac{1.16V}{R_3} - 23\mu A\right)\right] + 1.16V \tag{45}$$

$$V_{OV\_HYS} = (R_1 + R_2) \times 23\mu A \tag{46}$$

$$V_{UVH} = 1.16V + \left[R_1 \times \left(23\mu A + \frac{1.16V}{R_2 + R_3}\right)\right] \tag{47}$$

$$V_{UVL} = \frac{1.16V \times (R_1 + R_2 + R_3)}{R_2 + R_3} \tag{48}$$

$$V_{UV\_HYS} = R_1 \times 23\mu A \tag{49}$$

$$V_{OVH} = \frac{1.16V \times (R_1 + R_2 + R_3)}{R_3} \tag{50}$$

APPLICATION INFORMATION (continued)

Option B

If all four thresholds must be accurately defined, the Figure 13 configuration in can be used.

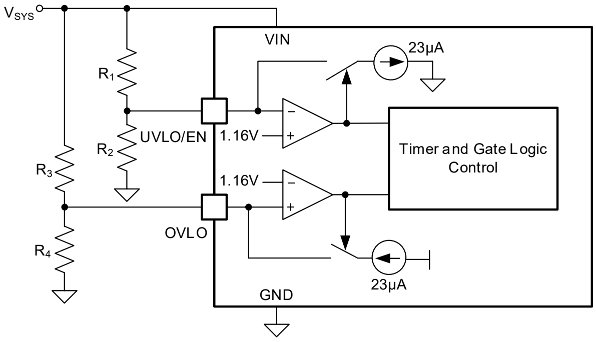


Figure 13. Programming the Four Thresholds

The values of the four resistors are determined as follows:

- Select the upper and lower UVLO thresholds, denoted as V_{UVH} and V_{UVL}.

$$R_1 = \frac{V_{UVH} - V_{UVL}}{23\mu A} = \frac{V_{UV\_HYS}}{23\mu A} \tag{51}$$

$$R_2 = \frac{1.16V \times R_1}{(V_{UVL} - 1.16V)} \tag{52}$$

- Select the upper and lower OVLO thresholds, denoted as VOVH and VOVL.

$$R_3 = \frac{V_{OVH} - V_{OVL}}{23\mu A} = \frac{V_{OV\_HYS}}{23\mu A} \tag{53}$$

$$R_4 = \frac{1.16V \times R_3}{(V_{OVH} - 1.16V)} \tag{54}$$

For instance, consider an application with the following required thresholds: V_{UVH} = 8V, V_{UVL} = 7V, V_{OVH} = 15.5V, and V_{OVL} = 14V. This results in a UVLO hysteresis of 1V and an OVLO hysteresis of 1.5V. The resistor values are then calculated as follows:

$$R_1 = 43.5k\Omega,\ R_2 = 8.64k\Omega \tag{55}$$

$$R_3 = 65.2k\Omega,\ R_4 = 5.27k\Omega \tag{56}$$

Once the values of R_1 through R_4 are determined, the threshold voltages and hysteresis can be computed using the following expressions:

$$V_{UVH} = 1.16V + \left[R_1 \times \left(\frac{1.16V}{R_2} + 23\mu A\right)\right] \tag{57}$$

$$V_{UVL} = \frac{1.16V \times (R_1 + R_2)}{R_2} \tag{58}$$

$$V_{UV\_HYS} = R_1 \times 23\mu A \tag{59}$$

$$V_{OVH} = \frac{1.16V \times (R_3 + R_4)}{R_4} \tag{60}$$

$$V_{OVL} = 1.16V + \left[R_3 \times \left(\frac{1.16V}{R_4} - 23\mu A\right)\right] \tag{61}$$

$$V_{OV\_HYS} = R_3 \times 23\mu A \tag{62}$$

Option C

The lowest UVLO setting is realized by tying the UVLO/EN pin to VIN pin, per Figure 14. Here, Q1 activates once V_{IN} rises to the power-on-reset (POR) threshold - typically around 2.7V. The OVLO trip points are set via R_3 and R_4, with their values derived using the procedure described in *Option B.*

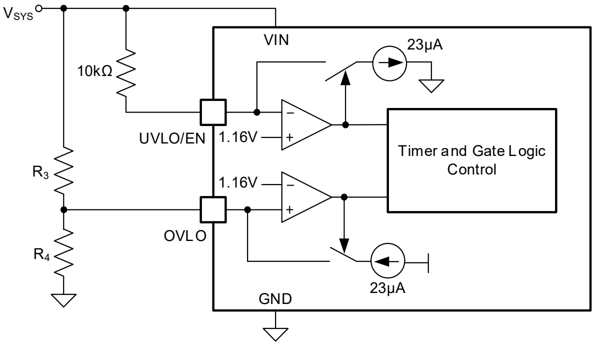


Figure 14. UVLO = POR

Option D

To disable OVLO, the OVLO pin is connected to ground. UVLO thresholds are configured per the guidelines in *Option B or Option C.*

This implementation follows Option B, with desired thresholds of V_{UVH} = 10V, VU_{VL} = 9V, V_{OVH} = 15V, and V_{OVL} = 14V. Resistor values R_1 through R_4 are obtained using the equations below:

$$R_1 = \frac{V_{UVH} - V_{UVL}}{23\mu A} = \frac{10V - 9V}{23\mu A} = 43.48k\Omega \tag{63}$$

$$R_2 = \frac{1.16V \times R_1}{(V_{UVL} - 1.16V)} = \frac{1.16V \times 43.48k\Omega}{(9V - 1.16V)} = 6.49k\Omega \tag{64}$$

$$R_3 = \frac{V_{OVH} - V_{OVL}}{23\mu A} = \frac{15V - 14V}{23\mu A} = 43.48k\Omega \tag{65}$$

$$R_4 = \frac{1.16V \times R_3}{(V_{OVH} - 1.16V)} = \frac{1.16V \times 43.48k\Omega}{(15V - 1.16V)} = 3.65k\Omega \tag{66}$$

Select the closest standard 1% resistor values: R_1 = 43.2kΩ, R_2 = 6.49kΩ, R_3 = 43.2kΩ, and R_4 = 3.65kΩ.

APPLICATION INFORMATION (continued)

Power Good Pin

When the FB pin voltage exceeds its threshold, the internal pull-down on PGD is turned off, letting PGD rise to V_{PGD} via the external pull-up resistor R_{PG}, as shown in Figure 15. The pull-up voltage (V_{PGD}) can go up to 17V and may differ from both V_{IN} and V_{OUT} either higher or lower. Selecting V_{DD} as V_{PGD} is a practical choice: it simplifies interfacing with low-voltage logic and prevents PGD glitches during startup.

If a delay on PGD is needed, refer to the circuits in Figure 16. In Figure 16A, capacitor C_{PG} delays only the rising edge, with no effect on the falling edge. In Figure 16B, the rising edge is slowed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed less, governed only by R_{PG2} and C_{PG}. Placing a diode across R_{PG2} (Figure 16C) allows either symmetrical delays on both edges or a brief rise delay with an extended fall delay, offering flexible timing control.

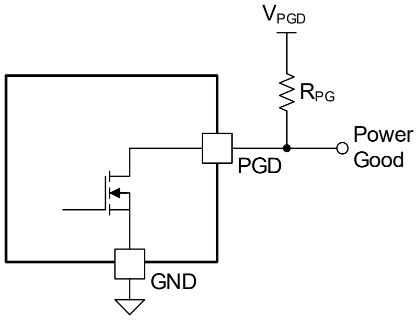
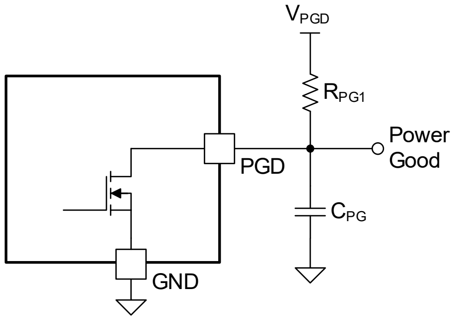
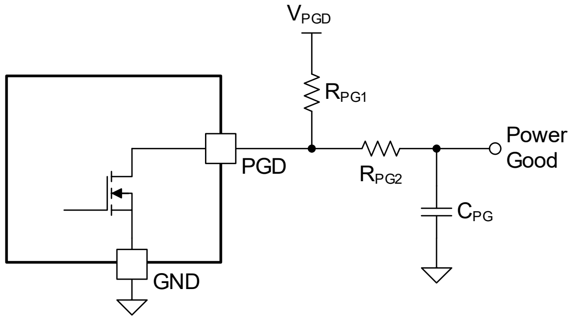


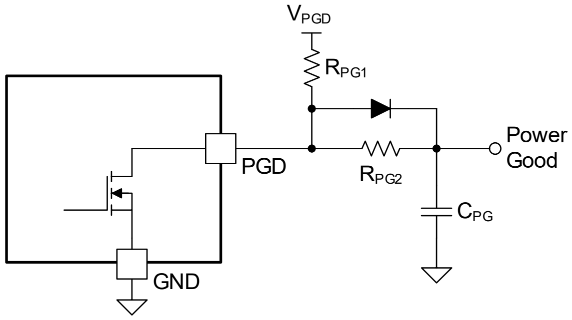
Figure 15. Power Good Output



A) Delay at Rising Edge Only



B) Long Delay at Rising Edge, Short Delay at Falling Edge



C) Short Delay at Rising Edge and Long Delay at Falling Edge or Equal Delays

Figure 16. Adding Delay to the Power Good Output Pin

APPLICATION INFORMATION (continued)

The PGD pin's output threshold is set using two resistors, R_{FB1} and R_{FB2}, per the arrangement in Figure 17. While the figure depicts monitoring of the output voltage, R_{FB1} can also be tied to any other voltage node that requires supervision.

The resistor values are determined as follows:

Specify the high and low PGD threshold voltages (V_{PGDH} and V_{PGDL}) with respect to V_{OUT}.

$$R_{FB1} = \frac{V_{PGDH} - V_{PGDL}}{23\mu A} = \frac{V_{PGD\_HYS}}{23\mu A} \tag{67}$$

$$R_{FB2} = \frac{1.163V \times R_{FB1}}{V_{PGDH} - 1.163V} \tag{68}$$

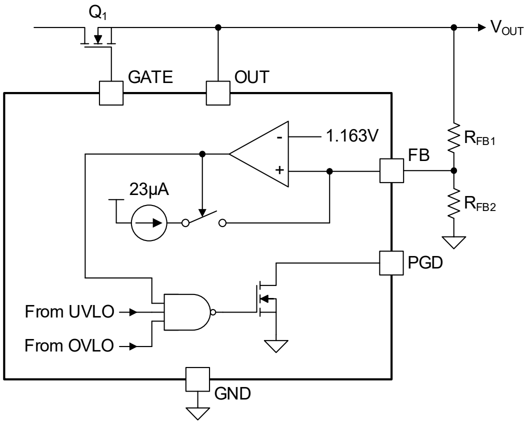


Figure 17. Programming the PGD Threshold

For this example, the desired PGD thresholds are set to 9.25V (V_{PGDH}) and 8.75V (V_{PGDL}). Resistors R_{FB1} and R_{FB2} are then determined using the equations below:

$$R_{FB1} = \frac{V_{PGDH} - V_{PGDL}}{23\mu A} = \frac{9.25V - 8.75V}{23\mu A} = 21.74k\Omega \tag{69}$$

$$R_{FB2} = \frac{1.163V \times R_{FB1}}{V_{PGDH} - 1.163V} = \frac{1.163V \times 21.74k\Omega}{9.25V - 1.163V} = 3.13k\Omega \tag{70}$$

Select the closest standard 1% resistor values: R_{FB1} = 21.74kΩ and R_{FB2} = 3.13kΩ.

APPLICATION INFORMATION (continued)

Input and Output Protection

For the SGM25720 hot-swap circuit to function correctly, a voltage-clamping device must be installed on the supply side of the mating connector. A transient voltage suppression (TVS) diode like the one shown in Figure 18 is ideal for this purpose. It absorbs voltage spikes created when the circuit rapidly disconnects load current, especially during a Hot-Short event where a high current is abruptly stopped as the FET turns off.

The TVS should be selected to have very low leakage at the maximum input voltage (V_{IN_MAX}) and must limit the clamped voltage to under 24V during such fault conditions. In numerous high-power applications, the 5.0SMDJ13A TVS meets these requirements effectively.

Furthermore, if the load powered through the SGM25720 contains inductive elements, a Schottky diode should be connected across the output, along with adequate local capacitance. This diode - capacitor pair helps suppress negative voltage under-shoot at the OUT pin that can occur when the load current is suddenly switched off.

System Considerations

As shown in Figure 18, the normal operation of SGM25720 requires a capacitor on the backplane side. The capacitor with live backplane needs to absorb the input surge voltage generated when the controller cuts off the load. If there is no capacitance, TVS needs to be placed in the input measurement to prevent large voltage generated during voltage transient from exceeding the maximum rated value of VIN pin.

When the output of SGM25720 is inductive load, it is necessary to reverse parallel diode on the load side. When the load is cut off, a reverse path is provided for the current of the inductive load to prevent negative voltage from damaging the device.

Power Supply Recommendations

Generally speaking, SGM25720 can provide stable power supply with reliable performance. However, when other card slots on the backplane are inserted, the high frequency dynamics on the backplane will appear. When this happens in the system, it is recommended to place a capacitor of 1μF on the drain of MOSFET. This will reduce the common mode voltage between VIN and SENSE pins, which needs to be suppressed to prevent over-current shutdown.

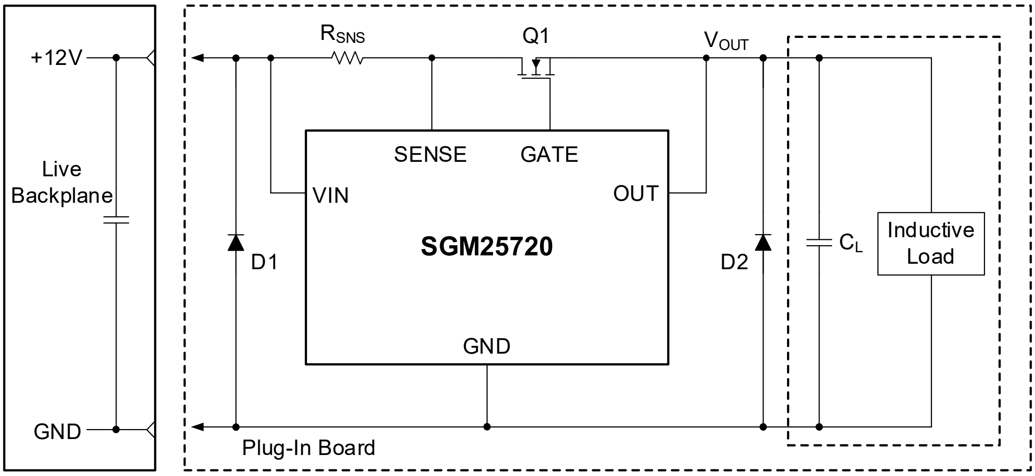


Figure 18. Output Diode Required for Inductive Loads

APPLICATION INFORMATION (continued)

Component Values

Figure 10 illustrates the schematic that fulfills the design requirements detailed in the prior section. Table 45 summarizes the finalized component values used to achieve the target specifications for a 12V, 45A hot-swap solution. The application waveforms presented in the next section are generated using these specific components. based on these device values.

Table 45. Final Component Values (12V, 45A Design)

COMPONENT	VALUE
R_{SNS}	0.5mΩ
R_1, R_3	43.2kΩ
R_2	6.49kΩ
R_4	3.65kΩ
R_{FB1}	21.74kΩ
R_{FB2}	3.13kΩ
R_{PWR}	6.6kΩ
$C_{dV/dt}$	100nF
C_{TIMER}	22nF
Z1	5.0MDJA15A
Q1	CSD17556Q5B
Q2	MMBT3904
Q3	MMBT3906
D1, D3	1N4148W-7-F
D2	SK153-TP

Layout Guidelines

SGM25720 should observe the following principles when laying PCB:

SGM25720 needs to be placed near the input connector to reduce the lead inductance from the connector to the power MOSFET.

The bypass capacitor of V_{IN} should be placed carefully. When MOSFET is turned off due to short-circuit, the input terminal has a very large dV/dt. When the capacitor is placed close to the VIN pin, the LC filter is formed due to the long routing from SENSE to VIN. At this time, a large voltage difference may be formed between VIN and SENSE pins. To prevent this, place the capacitor on the R_{SNS} terminal instead of VIN terminal.

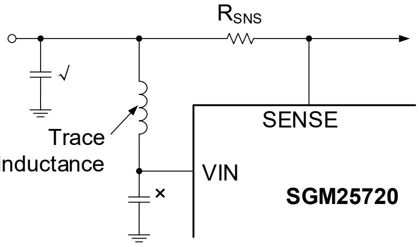


Figure 19. Layout Trace Inductance

- The R_{SNS} needs to be close to the controller chip and use the Kelvin connection.
- The current path and return path from the input to the load side should be parallel and close to each other to reduce the loop inductance.
- GND of components around SGM25720 can be connected with each other and connected with GND pin of SGM25720. Then connect GND to the system ground uniformly. Do not separately connect the ground of the devices around the chip to the ground of the system with high current.
- PCB layout provides good heat dissipation conditions for MOSFET Q1 to reduce the junction temperature when it is turned on and off.

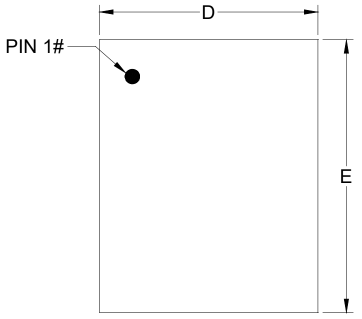
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

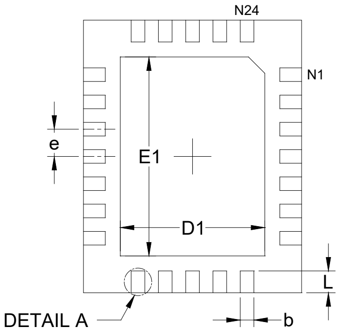
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

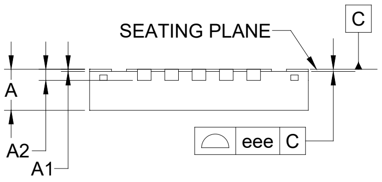
TQFN-4×5-24AL



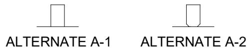
TOP VIEW



BOTTOM VIEW

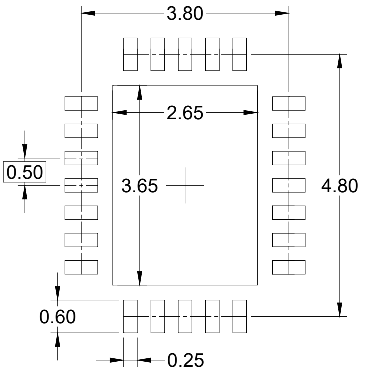


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL
CONSTRUCTION



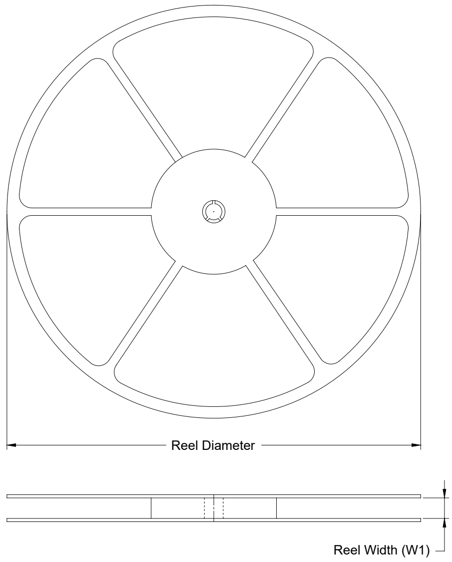
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**NOM**	**MAX**
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.900	-	4.100
E	4.900	-	5.100
D1	2.550	-	2.750
E1	3.550	-	3.750
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

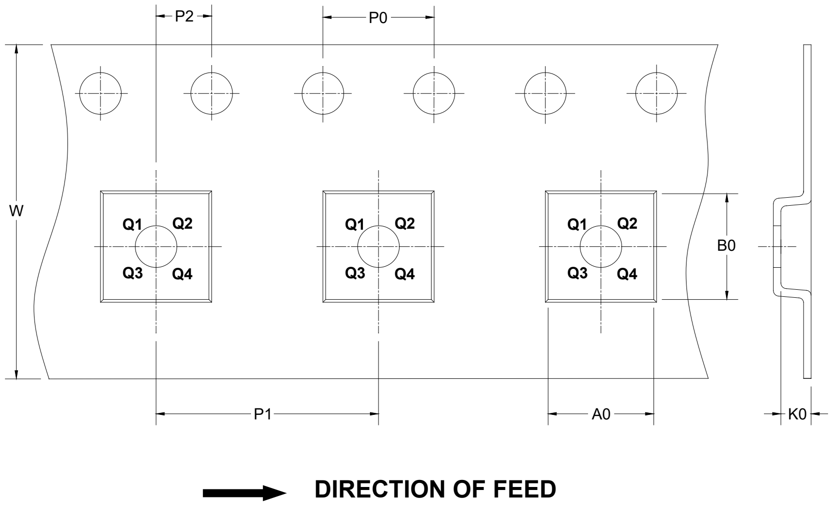
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



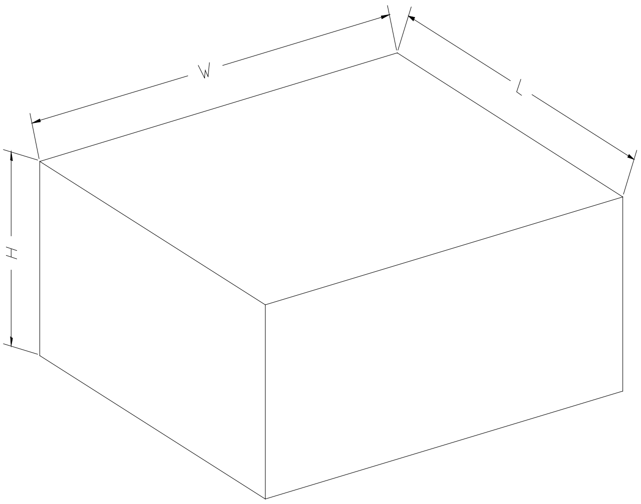
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×5-24AL	13"	12.4	4.30	5.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002