SGM856
Nano I_Q Precision Voltage Supervisor with Precision Timeout Watchdog Timer

GENERAL DESCRIPTION

The SGM856 is a high-precision voltage supervisor with ±1.2% accuracy over the operating temperature range. It only consumes 750nA (TYP) quiescent current and provides a timeout watchdog with fixed timeout period.

The SGM856 gives four available watchdog timeout period options, which are preset as a default value and can be configured by the users for setting different multiples of the default value by SET0. The watchdog function can be enabled or disabled by the WD_EN pin.

The output asserted times for nRESET are all preset. The SGM856xxD-x is a unique device that latches the output until an effective watchdog input is detected.

The SGM856 is available in a Green TDFN-1.5×1.5-6L package.

TYPICAL APPLICATION

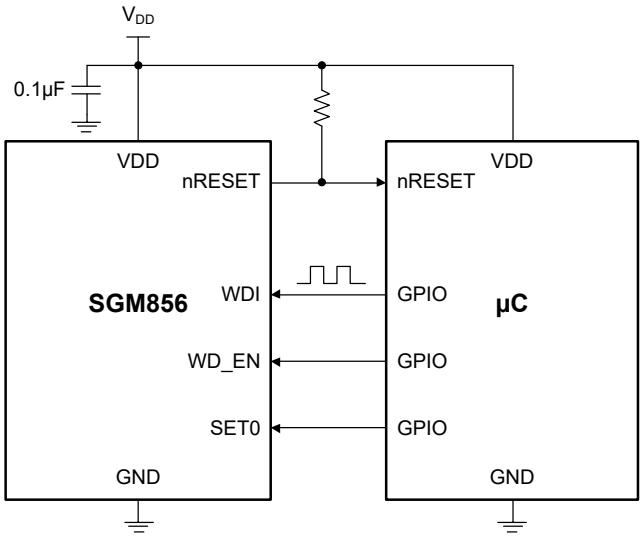


Figure 1. Typical Application Circuit

FEATURES

- **Factory-Programmed Watchdog Timeout**
  - **Factory-Programmed Options: 70ms, 1.12s, 4.48s, 17.92s**
- **Factory-Programmed Reset Delay with Scaling**
  - **Factory-Programmed Options: 11.2ms, 44.8ms, 179.2ms, Latched (t_D = 2.8ms)**
- **Supply Voltage Range: 1.6V to 6.5V**
- **Fixed Threshold Voltage: 2.3V, 3.0V, 4.6V**
  - **±1.2% (MAX) Voltage Threshold Accuracy**
  - **Built-in Hysteresis: 2.1% (TYP)**
- **Ultra-Low Supply Current: 750nA (TYP)**
- **Active-Low Open-Drain Outputs**
- **Various Programmability Options:**
  - **Watchdog Enable**
  - **On-the-Fly Timer Extension: 1X to 64X**
  - **Latched Output Option**
- **Available in a Green TDFN-1.5×1.5-6L Package**

APPLICATIONS

Robot Servo Drive
HVAC Control System
Electricity Meter
Hybrid I/O Module (Analog & Digital)
Infusion Pump
Surgical Equipment

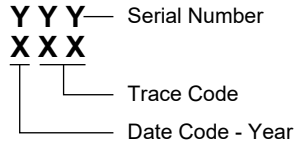
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM856AAB-2.3	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAB-2.3XTHR6G/TR	323 XXX	Tape and Reel, 3000
SGM856AAB-3.0	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAB-3.0XTHR6G/TR	324 XXX	Tape and Reel, 3000
SGM856AAB-4.6	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAB-4.6XTHR6G/TR	325 XXX	Tape and Reel, 3000
SGM856AAD-2.3	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAD-2.3XTHR6G/TR	327 XXX	Tape and Reel, 3000
SGM856AAD-3.0	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAD-3.0XTHR6G/TR	328 XXX	Tape and Reel, 3000
SGM856AAD-4.6	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856AAD-4.6XTHR6G/TR	329 XXX	Tape and Reel, 3000
SGM856BAB-2.3	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAB-2.3XTHR6G/TR	32B XXX	Tape and Reel, 3000
SGM856BAB-3.0	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAB-3.0XTHR6G/TR	32C XXX	Tape and Reel, 3000
SGM856BAB-4.6	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAB-4.6XTHR6G/TR	32D XXX	Tape and Reel, 3000
SGM856BAD-2.3	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAD-2.3XTHR6G/TR	26F XXX	Tape and Reel, 3000
SGM856BAD-3.0	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAD-3.0XTHR6G/TR	32F XXX	Tape and Reel, 3000
SGM856BAD-4.6	TDFN-1.5×1.5-6L	-40℃ to +125℃	SGM856BAD-4.6XTHR6G/TR	32G XXX	Tape and Reel, 3000

NOTE: For more models not listed above, please contact your local SGMICRO sales representatives.

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

PACKAGE/ORDERING INFORMATION (continued)

Device Naming Convention

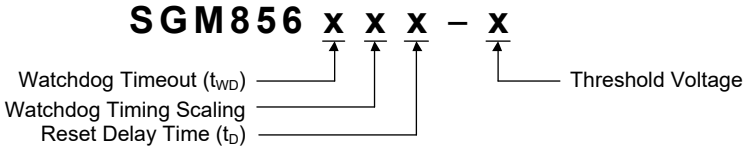


Table 1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Watchdog Timeout (t_{WD})	A	70ms
	B	1.12s
	C	4.48s
	D	17.92s
Watchdog Timing Scaling	A	1, 2
	B	1, 8
	C	1, 32
	D	1, 64
Reset Delay Time (t_D)	A	11.2ms
	B	44.8ms
	C	179.2ms
	D	Latched Output
Threshold Voltage	2.3	2.3V
	3.0	3.0V
	4.6	4.6V

ABSOLUTE MAXIMUM RATINGS

VDD Voltage ..... -0.3V to 7V
WD_EN, SET0, WDI ..... -0.3V to 7V
nRESET Voltage ..... -0.3V to 7V
nRESET Current ..... -20mA to 20mA
Package Thermal Resistance
TDFN-1.5×1.5-6L, θ_{JA} ..... 147.8℃/W
TDFN-1.5×1.5-6L, θ_{JB} ..... 54.6℃/W
TDFN-1.5×1.5-6L, θ_{JC} ..... 124.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VDD Voltage ..... 1.6V to 6.5V
WD_EN, SET0, WDI ..... 0V to V_{DD}
nRESET Voltage ..... 0V to 6.5V
nRESET Current ..... -5mA to 5mA
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

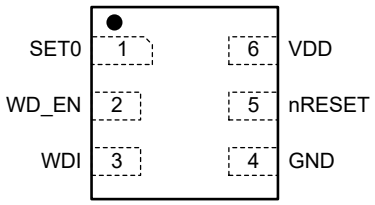
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-1.5×1.5-6L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SET0	I	Logic Input. SET0 determines the watchdog timeout ratio. Do not leave it floating.
2	WD_EN	I	Watchdog Enable Input. Logic high input enables the watchdog and logic low disables the watchdog. Do not leave it floating.
3	WDI	I	Watchdog Input. The watchdog timer is cleared every time a falling edge is detected at this pin. Do not leave it floating.
4	GND	G	Ground Pin.
5	nRESET	O	Reset and Watchdog Output. It is recommended to place a 100kΩ resistor to pull up this pin. This pin is asserted low once VDD is below under-voltage threshold (V_{IT-}). The nRESET signal is also asserted in occurence of any watchdog errors.
6	VDD	I	Supply Voltage Pin. For noisy systems, it is advised to place a 0.1μF ceramic capacitor between the VDD pin and GND.

NOTE: I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.6V to 6.5V, R_{nRESET} = 100kΩ to VDD, nRESET load C_{LOAD} = 10pF, VDD ramp rate ≤ 1V/μs, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common Parameters						
Input Supply Voltage	V_{DD}		1.6		6.5	V
Negative-Going Input Threshold Accuracy	V_{IT-}	V_{IT-} = 2.3V, 3.0V, 4.6V	-1.2	±0.5	1.2	%
Hysteresis	V_{HYS}		1	2.1	4	%
Supply Current into VDD Pin	I_{DD}	V_{DD} = 2.5V	0.3	0.75	1.7	μA
		V_{DD} = 6.5V	0.5	1.11	4	μA
Power-On Reset Voltage (1)	V_{POR}	V_{OL_MAX} = 300mV, I_{OUT_SINK} = 15μA			900	mV
Low-Level Input Voltage WD_EN, WDI, SET0	V_{IL}				0.25 × V_{DD}	V
High Level Input Voltage WD_EN, WDI, SET0	V_{IH}		0.8 × V_{DD}			V
nRESET						
Low-Level Output Voltage	V_{OL}	V_{DD} =1.6V, I_{OUT_SINK} = 500μA			300	mV
		V_{DD} = 3.3V, I_{OUT_SINK} = 2mA			300	mV
Open-Drain Output Leakage Current	I_{LKG}	V_{DD} = $V_{PULL-UP}$ = 6.5V			300	nA

NOTE: 1. V_{POR} is the minimum V_{DD} voltage level for a controlled output state.

TIMING REQUIREMENTS

(V_{DD} = 1.6V to 6.5V, R_{nRESET} = 100kΩ to VDD, nRESET load C_{LOAD} = 10pF, VDD ramp rate ≤ 1V/μs, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Glitch Immunity V_{IT-}	t_{GI_VIT-}	5% V_{IT-} overdrive (1)		21		μs
WDI Pulse Duration to Start Next Frame	t_{P-WD}	V_{DD} > V_{IT-}	1			μs
WD_EN Hold Time to Enable WD Operation	$t_{HD-WDEN}$	V_{DD} > V_{IT-}	200			μs
SET0 Hold Time to Change WD Timer Setting	$t_{HD-SET0}$	V_{DD} > V_{IT-}	150			μs
Watchdog Timeout Period	t_{WD}	SGM856Axx-x	56.4	70	82	ms
		SGM856Bxx-x	0.9	1.12	1.32	s
		SGM856Cxx-x	3.6	4.48	5.28	s
		SGM856Dxx-x	14.4	17.92	21.12	s
Startup Delay (2)	t_{STRT}			275		μs
nRESET Detect Delay for VDD Falling below V_{IT-}	t_{P_HL}	V_{DD} = (V_{IT+} + 10%) to (V_{IT-} - 10%) (3)		17	35	μs
Reset Time Delay	t_D	SGM856xxA-x	9	11	13.2	ms
		SGM856xxB-x	36	45	52.8	
		SGM856xxC-x	144	179	211.2	
Watchdog Timeout Delay	t_{nWDO}			t_D		s

NOTES:

1. Overdrive% = [(V_{DD}/V_{IT-}) - 1] × 100%

2. After rising above V_{IT+} from an initial voltage lower than the specified minimum V_{DD}, nRESET deassertion occurs after the cumulative duration of t_{STRT} and t_D.

3. t_{P_HL} is measured from threshold trip point (V_{IT-}) to nRESET assertion. V_{IT+} = V_{IT-} + V_{HYS}.

TIMING DIAGRAM

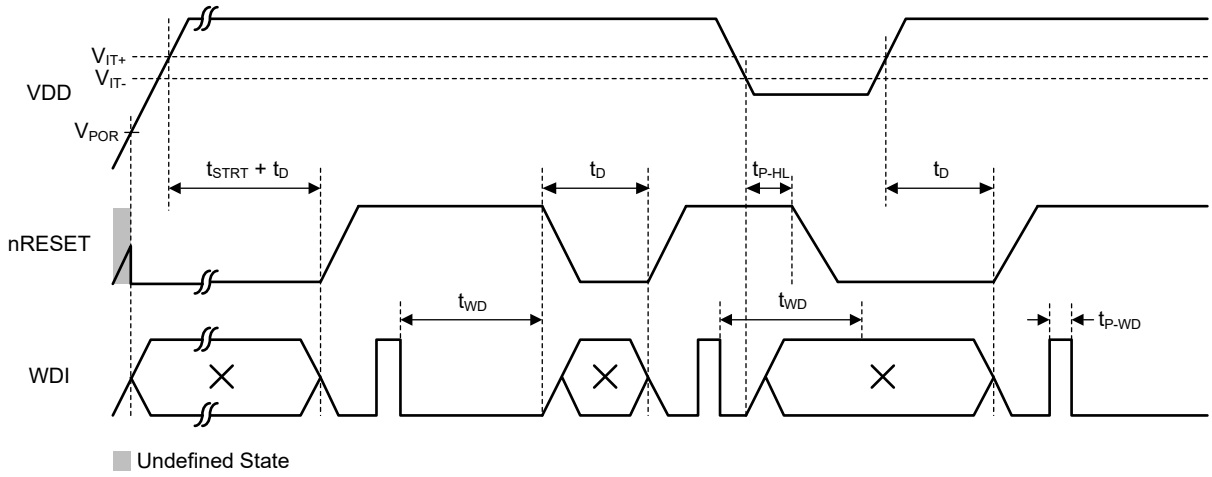


Figure 2. Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

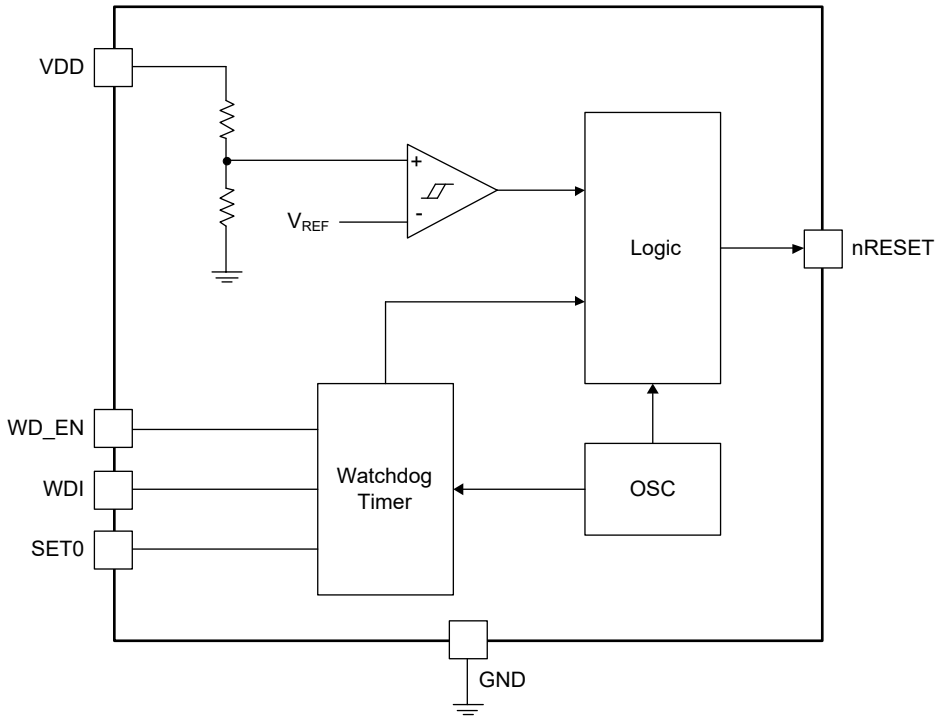
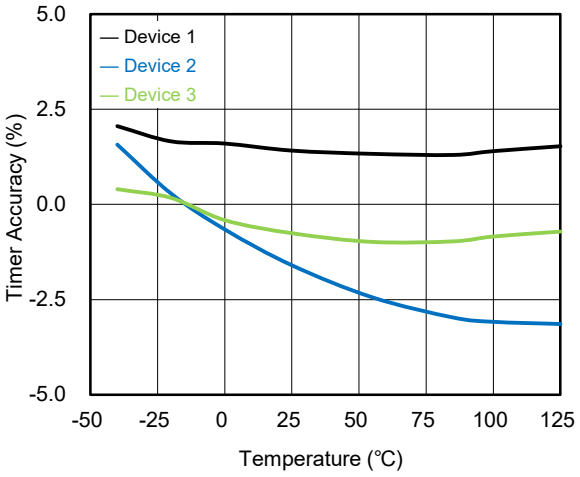


Figure 3. Block Diagram

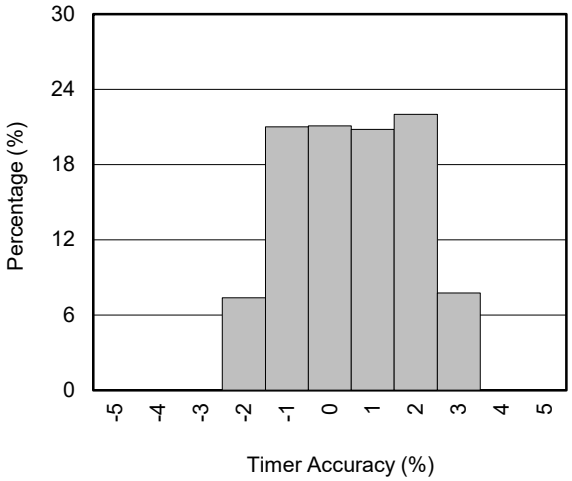
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

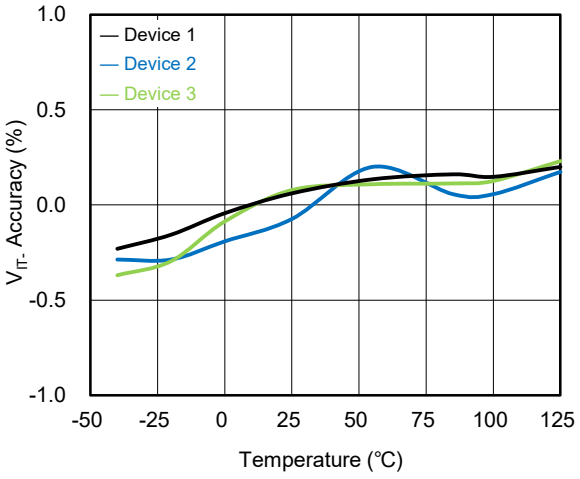
Timer Accuracy vs. Temperature



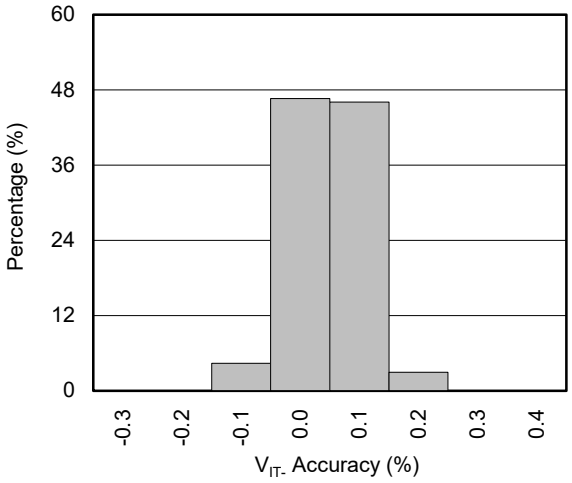
Timer Accuracy Histogram



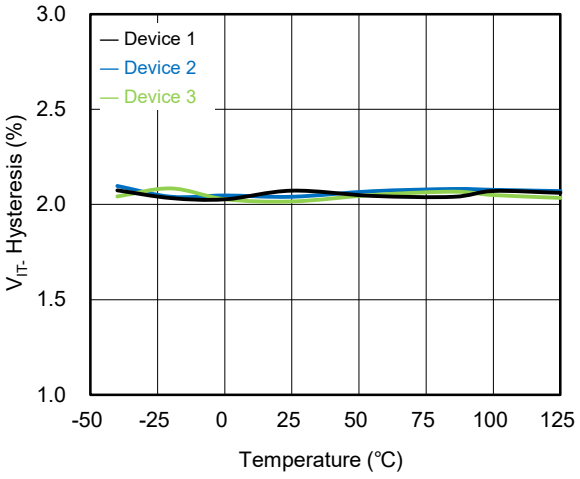
V_{IT-} Accuracy vs. Temperature



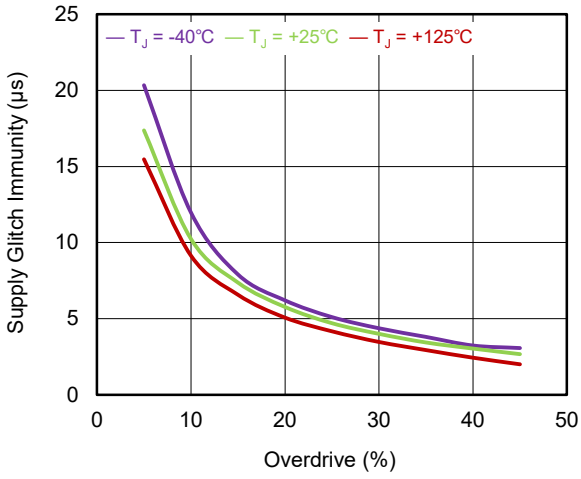
V_{IT-} Accuracy Histogram



V_{IT-} Hysteresis vs. Temperature



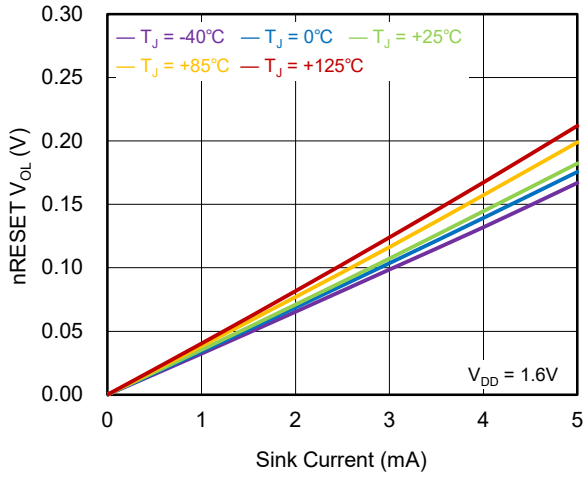
Supply Glitch Immunity vs. Overdrive



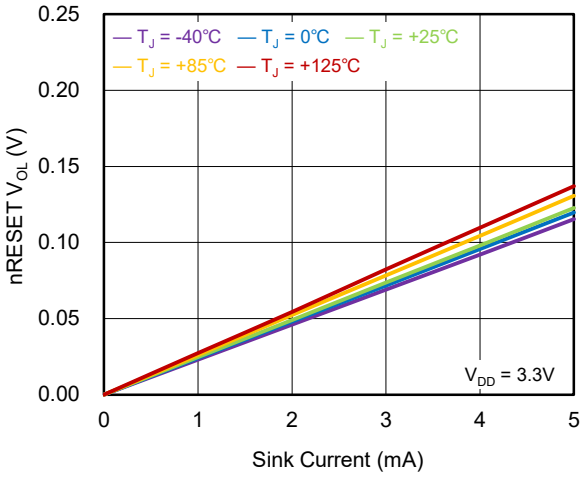
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

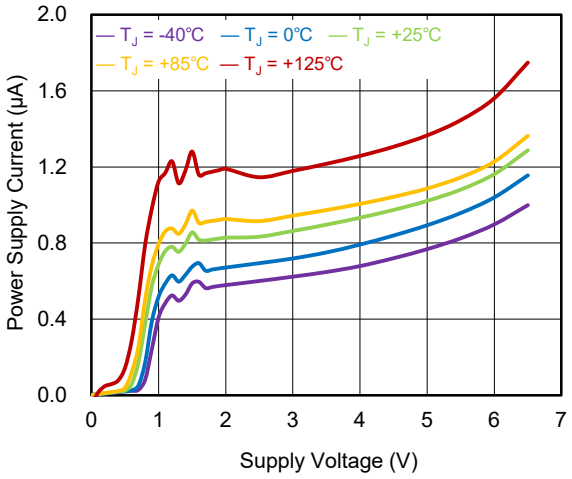
nRESET V_{OL} vs. I_{SINK}



nRESET V_{OL} vs. I_{SINK}



Supply Current vs. Power Supply Voltage



DETAILED DESCRIPTION

Overview

The SGM856 is a high-precision voltage supervisor, integrated with an accurate watchdog timer in the specified temperature range of -40℃ to +125℃. Besides, it ensures an accurate hysteresis of ±2.1% on the threshold, which makes it very suitable for systems that need small tolerance. It can also disable the watchdog function with the WD_EN pin and extend the watchdog scaling with the SET0 pin.

Feature Description

Voltage Supervisor

The SGM856 provides three fixed monitored voltage thresholds: 2.3V, 3.0V and 4.6V. It can precisely monitor voltages with quiescent current down to only 750nA. The nRESET pin is the ANDed output of the internal voltage supervisor and watchdog timer.

Figure 4 illustrates the timing diagram of the SGM856. When V_{DD} is lower than V_{POR}, the nRESET pin is floating. After V_{DD} rises above V_{POR}, the nRESET output is asserted low. If the V_{DD} continues to increase above the positive-going threshold (V_{IT+}), the nRESET will keep low for the time duration of t_{STRT} + t_D and then goes high. Once the nRESET is deasserted, the watchdog timer begins to work. The nRESET will maintain the deasserted state until the V_{DD} drops below the negative-going threshold V_{IT-}. Note that the device takes t_D to pull high the nRESET when V_{DD} ramps up from a point higher than V_{DD_MIN}.

Timeout Watchdog Timer

When V_{DD} > V_{IT-} + V_{HYS} and the nRESET is deasserted after the t_D time, the watchdog function becomes active.

The watchdog timer will be refreshed under the following conditions:

- A falling edge at the WDI pin;
- A falling/rising edge at the SET0 pin;
- A rising edge at nRESET or WD_EN is detected.

Once the watchdog does not receive a valid refresh signal during t_{WD}, the nRESET will be pulled low for t_D. Figure 5 shows the basic operation for timeout watchdog timer operation.

The SGM856 provides four kinds of timeout delay options: 70ms, 1.12s, 4.48s and 17.92s with ±20% accuracy. It also provides the opportunity to set multiples of t_{WD} through the SET0 pin. Details can be seen in SET0 Pin Behavior section.

Watchdog Enable/Disable Operation

In some applications, such as firmware update and step-by-step debug, disabling the watchdog function momentarily is necessary and significant. The SGM856 performs this task through the WD_EN pin. Pulling the WD_EN pin high can enable the watchdog function, while pulling it down can disable the watchdog function. The state transition for the WD_EN pin can be achieved at any time. If V_{DD} > V_{IT-} + V_{HYS}, nRESET will respond instantaneously to logic high once the WD_EN pin is pulled low.

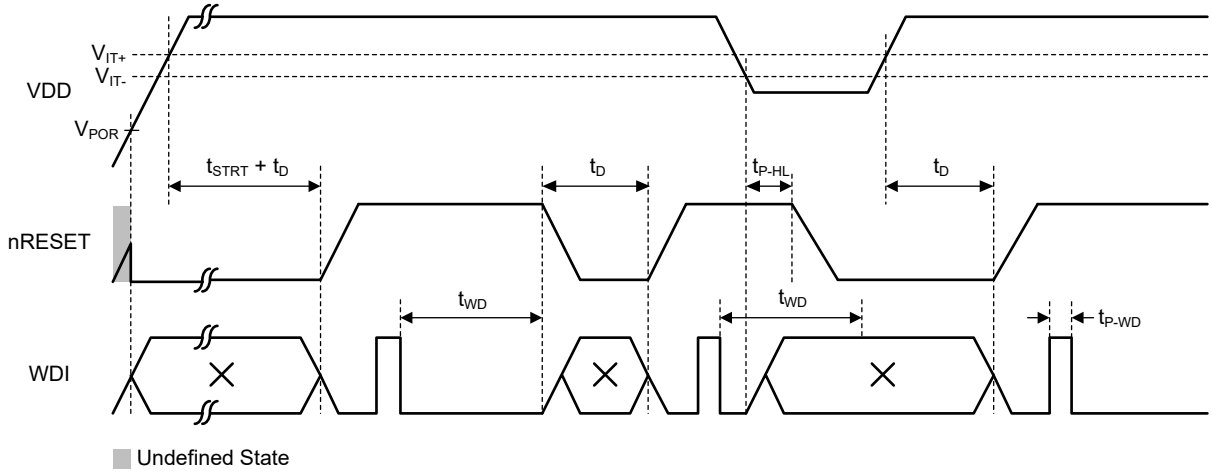


Figure 4. Voltage Supervisor Timing Diagram

DETAILED DESCRIPTION (continued)

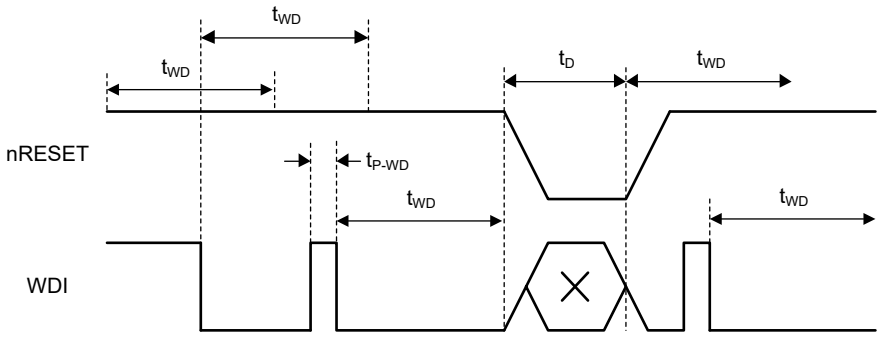


Figure 5. Timeout Watchdog Timer Operation

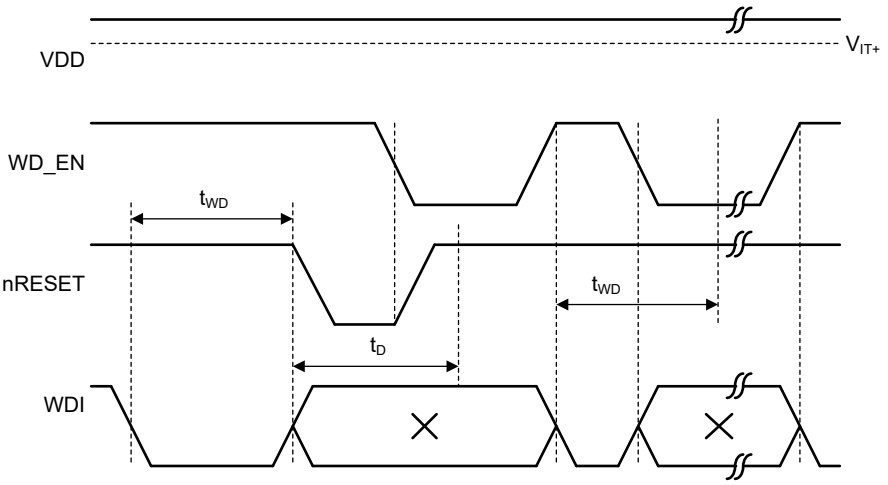


Figure 6. Watchdog Enable: WD_EN Pin Control

SET0 Pin Behavior

The SGM856 offers one SET pin for the TDFN package. Changing the logic level of SET0 pin allows for achieving integer multiple fundamental t_{WD} to meet various application requirements. The fundamental t_{WD} is determined by the used model which is described clearly in Device Naming Convention. The SET0 information is read and saved in the power on process and can be modified at any time in the normal operation. When the SET0 is modified, the watchdog timer is cleared and recounted as the new coding.

Table 2 presents an example of the t_{WD} values for different SET0 logic levels.

Table 2. t_{WD} Scaling with SET0 Pin

Watchdog Time Scaling Selection	t_{WD} Scaling Coefficient	
	SET0 = 0	SET0 = 1
A	× 1	× 2
B	× 1	× 8
C	× 1	× 32
D	× 1	× 64

DETAILED DESCRIPTION (continued)

Figure 7 and Figure 8 show the timing behavior with respect to SET0 status changes.

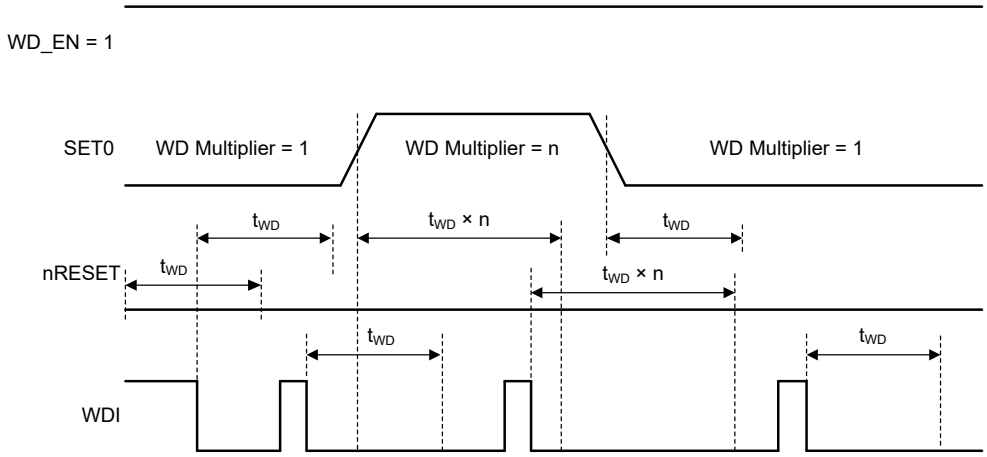
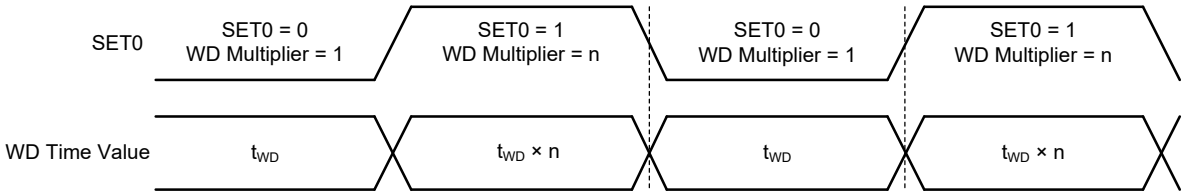


Figure 7. Watchdog Behavior with with SET0 Pin Status



t_{WD} = Fixed based on factory-set option.

n = Fixed based on time-set multiplier chosen.

Figure 8. Watchdog Operation with SET0 Pin

Device Functional Modes

Table 4 summarizes the functional modes of the SGM856. t_{PULSE} is the time between falling edges on WDI.

Table 3. Device Functional Modes

VDD	Watchdog Status	WDI	nRESET
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined
$V_{POR} \le V_{DD} < V_{IT-}$	Not Applicable	Ignored	Low
$V_{DD} \ge V_{IT+}$	Disabled	Ignored	High
	Enabled	$t_{PULSE} < t_{WD\_MIN}$	High
	Enabled	$t_{PULSE} > t_{WD\_MAX}$	Low

Watchdog Output Latch Function

The nRESET will be latched low due to the timeout error for SGM856xxD-x. To exit the latched state, the following actions can be taken:

- A new power cycle for the VDD pin;
- A valid WDI falling edge;
- Toggling WD_EN from logic high to logic low.

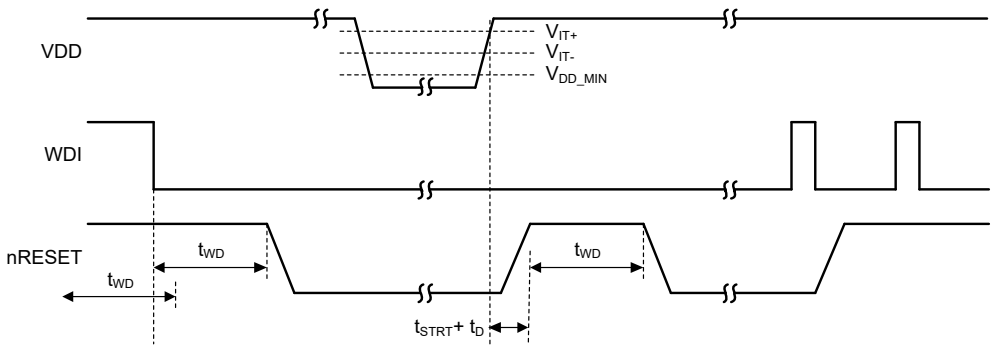


Figure 9. Output Latch Timing Behavior

APPLICATION INFORMATION

Calculating the nRESET Pull-up Resistor

The nRESET pin is an open-drain output, as shown in Figure 10. When selecting an appropriate pull-up resistor, the total system current consumption (including quiescent current flowing into VDD and currents flowing through the pull-up resistors), the low-level output voltage (V_{OL}), the capacitor between the nRESET and GND, and the leakage current of nRESET pin should be taken into consideration.

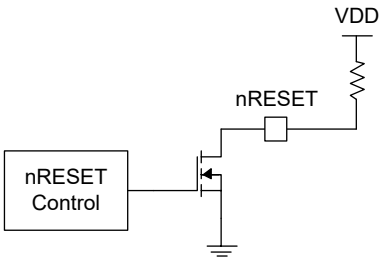


Figure 10. Open-Drain RESET Configuration

A tradeoff is made between V_{OL} and the current flowing into the nRESET pin (I_{nRST}). The constraint for V_{OL} is lower than 0.3V and for I_{nRST} is lower than 10mA. To be more exact, I_{nRST} should be kept below 2mA for $V_{DD} \geq 3V$ and 500μA for V_{DD} = 1.6V.

For example, when the power rail is pulled up to 2.5V, the pull-up resistor should be larger than 4.4kΩ due to V_{OL}. Take the pull-up resistor as 100kΩ, the obtained total current consumption is 25.75μA.

Power Supply Recommendations

This device is configured to function normally with an input voltage ranging from 1.6V to 6.5V. Note that incorporating a capacitor ranging from 0.1μF to 1μF between the VDD and GND pins is advisable, depending on the noise characteristics of the input voltage supply.

Layout Guidelines

Though not mandatory, placing a 0.1μF ceramic capacitor close to the VDD pin is recommended to suppress the noise or transient spikes.

Place the pull-up resistor for nRESET pin as close to the corresponding pin as possible.

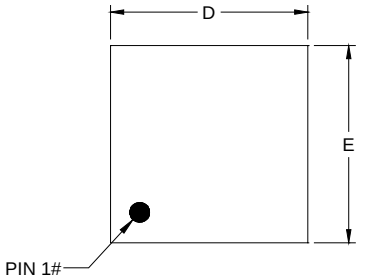
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

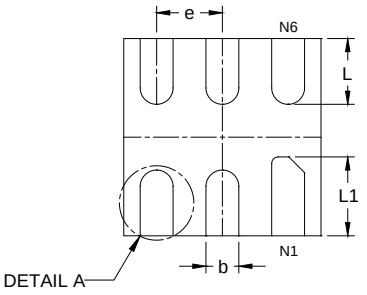
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

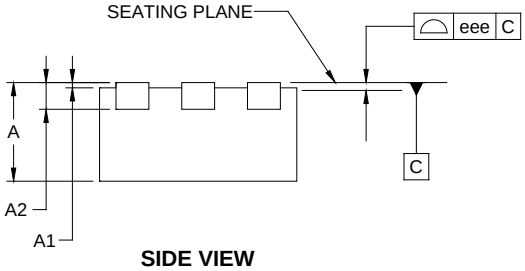
TDFN-1.5×1.5-6L



TOP VIEW



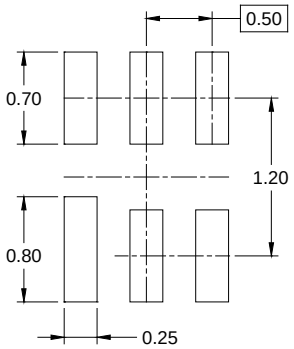
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



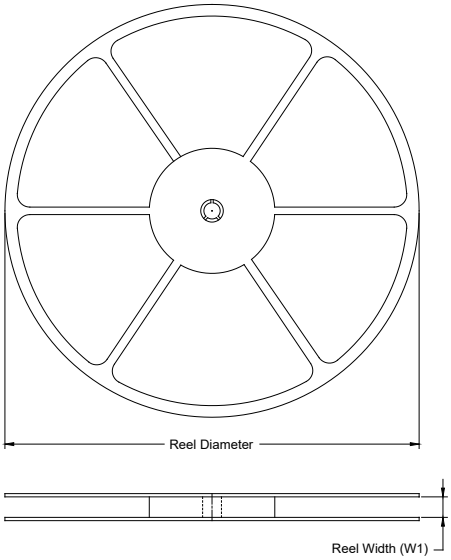
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
D	1.400	-	1.600
E	1.400	-	1.600
e		0.500 BSC	
L	0.400	-	0.600
L1	0.500	-	0.700
eee		0.080	

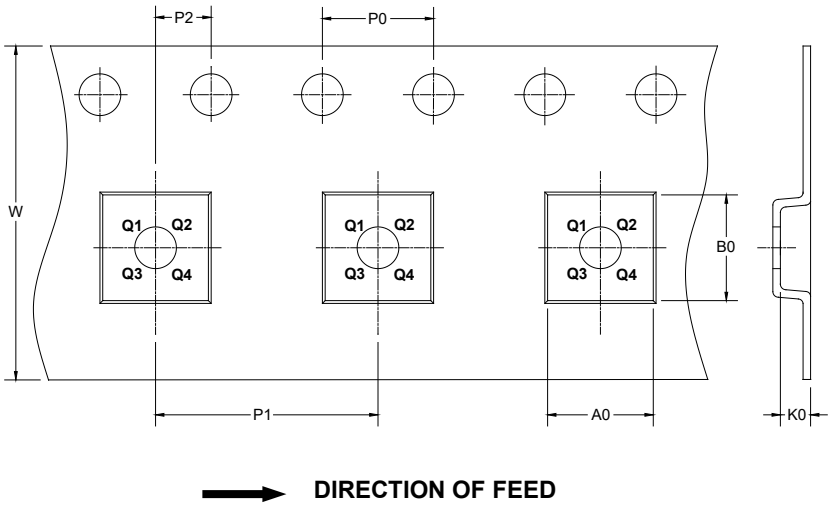
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



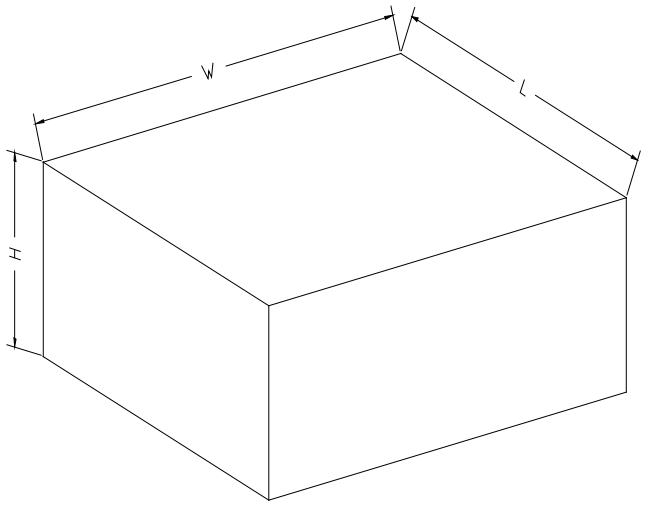
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-1.5×1.5-6L	7"	9.5	1.70	1.70	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002