TDT5118
8-Kbit Serial Presence Detect (SPD) EEPROM with Hub and Integrated Temperature Sensor

GENERAL DESCRIPTION

The TDT5118 is a SPD5 Hub device Compatible with JEDEC standard JESD300-5B.01. The SPD5 Hub device contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write-protected via software command. Write protection for each block may be overridden in an offline programmer environment while overrides are prevented in normal use. The SPD5 Hub device operates from 1.8V nominal power supply input. The SPD5 Hub device is intended to operate up to 12.5MHz on a 1.0V I3C Basic bus or up to 1MHz on a 1.0V to 3.3V I^2C bus. The SPD5 Hub device is intended to interface to I^2C/I3C Basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus.

The SPD5 Hub device responds to specific pre-defined I^2C/I3C Basic device select codes on a host interface bus. The SPD5 Hub device also incorporates a second local I^2C/I3C Basic bus and supports pass through of commands from the host bus onto the local bus for addressing of I^2C/I3C Basic devices on the local bus (Hub function).

The SPD5 Hub device incorporates thermal sensing capability which is controlled and read over I^2C/I3C Basic bus.

The TDT5118 is available in a Green TDFN-2×3-8EL package.

FEATURES

- **SPD5 Hub Device, JEDEC JESD300-5B.01 Compliant**
- **Two-wire Programmable I^2C or I3C Basic Bus Serial Interface**
- **Up to 12.5MHz Transfer Rate**
- **Power Supply: 1.8V V_{DDSPD}, 1.0V V_{DDIO}**
- **Supports 1.0V, 1.1V and 1.2V Push Pull IO Levels**
- **Supports 1.0V, 1.1V, 1.2V, 1.8V, 2.5V and 3.3V Open Drain IO Levels**
- **1024 Bytes of Non-volatile Memory (16 Blocks; 64 Bytes per Block)**
- **Write Protection for each Block of NVM**
- **Hub Function with 3 Address Bits Translation**
- **Integrated Temperature Sensor: +0.5℃ Accuracy with +0.25℃ Resolution**
- **Packet Error Check (PEC) Function**
- **Parity Error Check Function**
- **Bus Reset Function**
- **Up to 8 Unique Addressing**
- **In Band Interrupt (IBI)**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green TDFN-2×3-8EL Package**

APPLICATIONS

DDR5 DIMM Modules

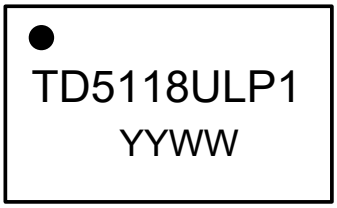
PC, Server Platforms

Industrial Temperature Monitors

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TDT5118	TDFN-2×3-8EL	-40℃ to +125℃	TDT5118-ULP1TR	TD5118ULP1 YYWW	Tape and Reel, 3000

MARKING INFORMATION



TD: SGMICRO Logo

TD5118ULP1: TDT5118-ULP1

YYWW: Date Code, YY = year, WW = week

Example: 2320 = year 2023, week 20

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DDIO} ..... -0.5V to 2.1V
Supply voltage, V_{DDSPD} ..... -0.5V to 2.1V
Voltage on HSA Pin, V_{HSA} ..... -0.5V to 2.1V
Voltage on HSCL, HSDA, LSCL, LSDA Pins, V_{IO} ..... -0.5V to 2.1V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

2. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage (1), V_{DDSPD} ..... 1.8V (TYP)
Input Supply Voltage (1), V_{DDSPD} ..... 1.7V to 1.98V
Input Supply Voltage (2), V_{DDIO} ..... 1.0V (TYP)
Input Supply Voltage (2), V_{DDIO} ..... 0.95V to 1.05V
Operating Ambient Temperature Range ..... -40℃ to +125℃

NOTES:

1. For DDR5 DIMM application, the DDR5 PMIC VOUT_1.8V setting should be selected such that absolute MIN and MAX values for SPD Hub specification are not violated.

2. For DDR5 DIMM application, the DDR5 PMIC VOUT_1.0V setting should be selected such that absolute MIN and MAX values for SPD Hub specification are not violated.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

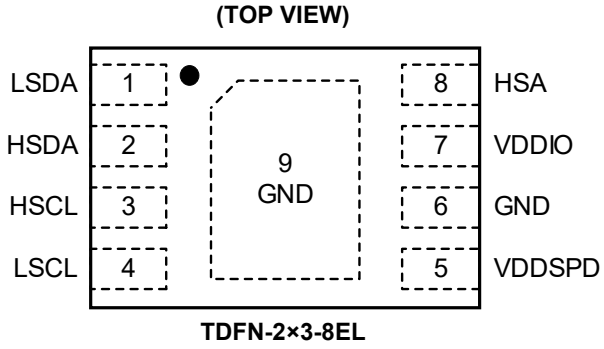
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	LSDA	I	Local Bus - I^2C/I3C Basic Data
2	HSDA	I/O	Host Bus - I^2C/I3C Basic Data
3	HSCL	I	Host Bus - I^2C/I3C Basic Input Clock
4	LSCL	O	Local Bus - I^2C/I3C Basic Output Clock
5	VDDSPD	P	1.8V Input Power Supply. Connect minimum of 1.0μF capacitor to GND
6	GND	G	GND
7	VDDIO	P	1.0V Input Power Supply. Connect minimum of 1.0μF capacitor to GND.
8	HSA	I	Host Bus - I^2C/I3C Basic Address Pin. See Table 1 for ID definition. Table 1 shows the HSA pin resistor values and corresponding 3-bit HID for SPD5 Hub device.
9	Thermal Pad, GND	G	Connected to GND Plane

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

Table 1. HSA Pin Resistor Value and ID - SPD5 Family

HSA PIN CONNECTION	3-BIT HID	COMMENT
10.0kΩ to GND	HID = 000	1% Resistor
15.4kΩ to GND	HID = 001	
23.2kΩ to GND	HID = 010	
35.7kΩ to GND	HID = 011	
54.9kΩ to GND	HID = 100	
84.5kΩ to GND	HID = 101	
127kΩ to GND	HID = 110	
196kΩ to GND	HID = 111	
Tied directly to GND	HID = 000	Offline mode; Write protect override enabled

ELECTRICAL CHARACTERISTICS

Write Endurance and Data Retention Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention at +25℃	D_R	100			Years
Write Endurance Cycles at +25℃	N_{W1}	≥ 100000			Cycles
Write Endurance Cycles at +95℃	N_{W2}	100000			Cycles

AC Measurement Conditions (1)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Load Capacitance	C_L	40		pF
Input Rise And Fall Times - Open Drain			120	ns
Input Rise And Fall Times - Push Pull			5	ns
Input Signal Swing Levels		0.2 to 0.8		V
Input Levels For Timing Reference		0.3 to 0.7		V

NOTE:
1. This AC measurement condition (***AC Measurement Conditions*** and Figure 1) is only for the test purpose in lab.

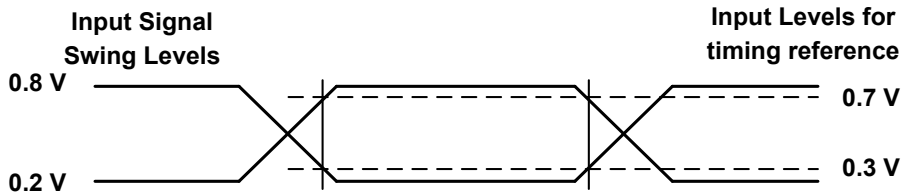


Figure 1. AC Measurement Waveform

Input Parameters

PARAMETER (1) (2)	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Capacitance (HSDA, HSCL, LSDA)	C_{IN}	-	-	5	pF
Pulse width of spikes which must be suppressed by the input filter in I^2C mode	t_{SP}	Single glitch, f ≤ 100kHz	-	-	ns
		Single glitch, f > 100kz	0	50	ns

NOTES:
1. T_A = +25℃, f = 400kHz.
2. Verified by design and characterization, not necessarily tested on all devices.

Output R_{ON} Specification

PARAMETER (1)	SYMBOL	MIN	MAX	UNITS
HSDA Output Pull-Up Driver Impedance	R_{ON_PUH}	10	45	Ω
HSDA Output Pull-Down Driver Impedance	R_{ON_PDH}	10	40	Ω
LSCL, LSDA Output Pull-Up and Pull-Down Driver Impedance	R_{ON_Local}	20	100	Ω

NOTE:
1. Pull-down $R_{ON} = V_{OUT}/I_{OUT}$; Pull-up $R_{ON} = (V_{IO} - V_{OUT})/I_{OUT}$.

ELECTRICAL CHARACTERISTICS (continued)

DC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Leakage Current	I_{LI}		-	±5	μA
Output Leakage Current	I_{LO}		-	±5	μA
Supply Current, Read Operation (1)	I_{DDR}	V_{DDSPD} = 1.8V, f_C = 12.5MHz	-	2	mA
Supply Current, Write Operation (1)	I_{DDW}	V_{DDSPD} = 1.8V, f_C = 12.5MHz	-	3	mA
Standby Supply Current	I_{DD1}	V_{IN} = V_{DDSPD} = 1.8V	-	50	μA
Input Low Voltage	V_{IL}		-0.35	0.3	V
Input High Voltage	V_{IH}		0.7	3.6	V
Output Low Voltage (2)	V_{OL}	3mA sink current	-	0.3	V
Output High Voltage	V_{OH}	3mA source current	0.75	-	V
Output Low Current (HSDA, LSDA, LSCL)	I_{OL}	V_{OL} = 0.3V	-3	-	mA
Output High Current (HSDA, LSDA, LSCL)	I_{OH}	V_{OH} = V_{DDIO} - 0.3V	-	-3	mA
Rising Output Slew Rate (3) (HSDA, LSDA, LSCL)	SR_R		0.1	1.0	V/ns
Falling Output Slew Rate (3) (HSDA, LSDA, LSCL)	SR_F		0.1	3.0	V/ns
Power-On Reset Threshold	V_{PON}	Monotonic rise between V_{PON} and $V_{DDSPD(min)}$ without ringback	1.6	-	V
Power Off Threshold for Warm Power On Cycle	V_{POFF}	No ringback above V_{POFF}	-	0.3	V

NOTES:

1. Thermal sensor is active.
2. Example calculation for V_{OL}= R_{ON} × ($I_{leakage}$ + I_{OUT}); where I_{OUT} = V_{DDIO}/(R_{pu} + R_{ON}); R_{pu} = Pull-up resistor with typical value of 1kΩ; Min and Max value of 750Ω and 1.5kΩ, respectively.
3. Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 5 and Figure 6 shows the timing measurement points. For slew rate measurements, the V_{OH} level shown in Figure 6 is a function of R_{ON} value; V_{OH} = {1.0/(R_{ON} + 50)} × 50.

AC Characteristics

PARAMETER	SYMBOL	I^2C MODE – OPEN DRAIN		I3C Basic – Push-Pull (1)		UNITS
		MIN	MAX	MIN	MAX	
Clock Frequency	f_{SCL}	0.01	1	0	12.5	MHz
Clock Pulse Width High Time	t_{HIGH}	260	-	35	-	ns
Clock Pulse Width Low Time	t_{LOW}	500	-	35	-	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$	10	50	10	50	ms
SDA Rise Time (2) (3)	t_R	-	120	-	5	ns
SDA Fall Time (2) (3)	t_F	-	120	-	5	ns
Data In Set-up Time (2)	$t_{SU:DAT}$	50	-	8	-	ns
Data In Hold Time (2)	$t_{HD:DI}$	0	-	3	-	ns
Start Condition Setup Time (2)	$t_{SU:STA}$	260	-	12	-	ns
Start Condition Hold Time (2)	$t_{HD:STA}$	260	-	30	-	ns
Stop Condition Setup Time (2)	$t_{SU:STO}$	260	-	12	-	ns
Time between Stop Condition and next Start Condition (2) (4)	t_{BUF}	500	-	500	-	ns
Write Time	t_W	See Maximum Recovery Time in MR6				
Warm Power Cycle Off Time	t_{POFF}	1	-	1	-	ms
Time from Valid 1.8V Supply to Sense HSA Pin for HID Code Assignment	t_{SENSE_HSA}	-	5	-	5	ms
Time from Power On to First Command	t_{INIT}	10	-	10	-	ms

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	SYMBOL	I^2C MODE – OPEN DRAIN		I3C Basic – Push-Pull (1)		UNITS
		MIN	MAX	MIN	MAX	
Bus Available Time (No Edges Seen on HSDA and HSCL)	t_{AVAL}	-	-	1	-	µs
Time to Issue IBI after an Event is Detected when Bus is Available	t_{IBI_ISSUE}	-	-	-	15	µs
Time from Clear Register Status to any I3C Operation with Start Condition to Avoid IBI Generation; PEC Disabled	$t_{CLR_I3C_CMD_DELAY}$	-	-	4	-	µs
Time from Clear Register Status to any I3C Operation with Start Condition to Avoid IBI Generation; PEC Enabled		-	-	15	-	µs
Propagation Delay, HSDA to LSDA and HSCL to LSCL (5)	t_{PDHL}	-	200	-	6	ns
Propagation Delay, LSDA to HSDA (5)	t_{PDLH}	-	200	-	6	ns
HSCL Falling Clock In to HSDA Data Out Hold Time (6)	$t_{HD:DAT}$	0.5	350	N/A	N/A	ns
HSCL Falling Clock In to HSDA Valid Data Out Time (7)	t_{DOUT}	N/A	N/A	0.5	12	ns
HSCL Rising Clock In to SDA Output Off (8)	t_{DOFFT}	N/A	N/A	0.5	12	ns
HSCL Rising Clock In to Controller SDA Output Off (9)	t_{DOFFC}	N/A	N/A	0.5	t_{HIGH}	ns
HSCL Rising Clock In to Controller Driving HSDA Low (10)	$t_{CL_r_DAT_f}$	N/A	N/A	40	-	ns
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay (11) (12) (13)	$t_{DEVCTRLCCC_DELAY_PEC_DIS}$	3	-	3	-	µs
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode (14) (15) (16)	$t_{WR_RD_DELAY_PEC_EN}$	N/A	N/A	8	-	µs
SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command Delay	$t_{I2C_CCC_UPDATE_DELAY}$	2.5	-	-	-	µs
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C_CCC_UPDATE_DELAY}$	-	-	2.5	-	µs
Any CCC to RSTDAA CCC delay	t_{CCC_DELAY}	N/A	N/A	2.5	-	µs

NOTES:

1. I3C mode with Open Drain operation follows timing values as shown in I^2C Mode - Open Drain column.
2. See Figure 2 for input timing parameter definition.
3. See Figure 7 for voltage threshold definition for rise and fall times.
4. If PEC is enabled, $t_{WR_RD_DELAY_PEC_EN}$ timing parameter also applies.
5. See Figure 8 for timing definition. See Figure 5 for output timing parameter measurement reference load.
6. See Figure 4 for output timing parameter definition.
7. The SPD5 Hub device must be in configured in I3C Basic mode to guarantee t_{DOUT} value. See Figure 3 for output timing parameter definition. See Figure 5 for output timing parameter measurement reference load.
8. The SPD5 Hub device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 19. See Figure 5 for output timing parameter measurement reference load. Also refer to MIPI Alliance Specification for I3C Basic Version 1.0-19 July 2018, section 5.1.2.3.2, Transition from Address ACK to Mandatory Byte during IBI.
9. The SPD5 Hub device must be configured in I3C Basic mode. The Host guarantees t_{DOFFC} value. See Figure 20. See Figure 5 for output timing parameter measurement reference load.
10. See Figure 22.
11. From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
12. The SPD5 Hub device may send ACK or NACK if Host does not satisfy $t_{DEVCTRLCCC_DELAY_PEC_DIS}$ timing parameter.
13. This timing parameter restriction is only applicable when PEC function is disabled in SPD5 Hub. If PEC is enabled, this timing parameter does not apply.
14. From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.
15. This timing parameter restriction is only applicable when PEC function is enabled in SPD5 Hub. If PEC is disabled, this timing parameter does not apply.
16. The SPD5 Hub device may send ACK or NACK if Host does not satisfy $t_{WR_RD_DELAY_PEC_EN}$ timing parameter.

ELECTRICAL CHARACTERISTICS (continued)

Temperature Sensor Performance

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Temperature Sensor Accuracy (Active Range)	T_{ACC}	+75℃ ≤ T_A ≤ +95℃	-	±0.5	±1.0	℃
Temperature Sensor Accuracy (Monitor Range)		+40℃ ≤ T_A ≤ +125℃	-	±1.0	±2.0	℃
Temperature Sensor Accuracy (Industrial Temperature Range)		-40℃ ≤ T_A ≤ +125℃	-	±2.0	±3.0	℃
Temperature Sensor Resolution	R_{TS}			0.25		℃
Conversion Time	t_{CONV}	Assumes 0.25℃ accuracy			68	ms
Hysteresis between Temperature Events	T_{HYST}		1	-	-	℃

AC TIMING DEFINITION

I²C or I3C Basic Bus Timing

The SPD5 Hub device follows the I²C or I3C Basic bus timing requirements. The Figure 2 and Figure 3 show the timing diagram for Data Bus Input and Data Output parameters.

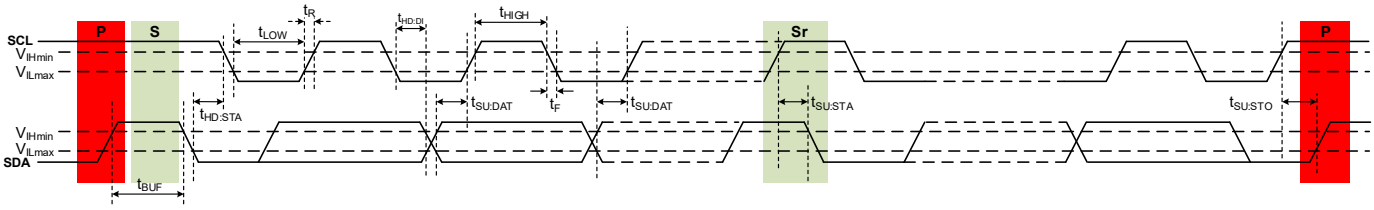


Figure 2. I²C or I3C Basic Bus AC Input Timing Parameter Definition

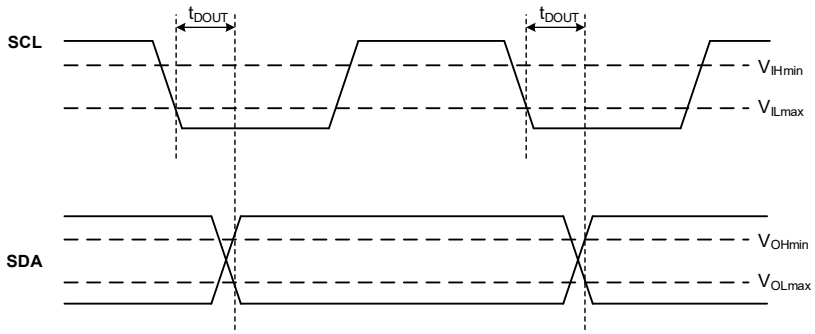


Figure 3. I3C Basic Bus AC Data Output Timing Parameter Definition

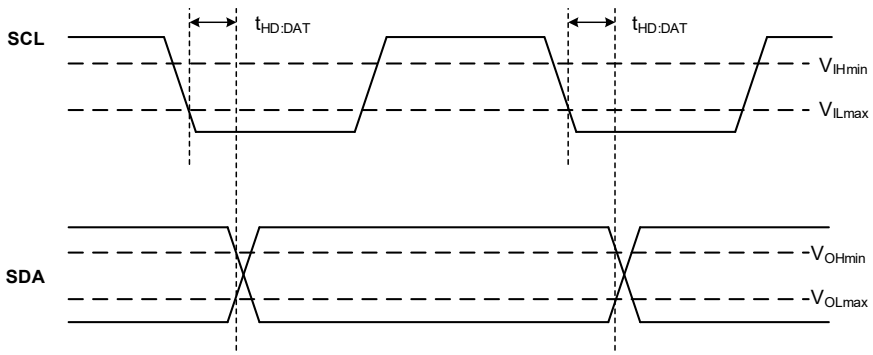


Figure 4. I²C Bus AC Data Output Timing Parameter Definition

AC TIMING DEFINITION (continued)

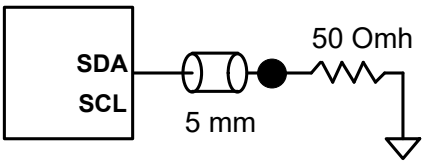


Figure 5. Output Slew Rate and Output Timing Reference Load

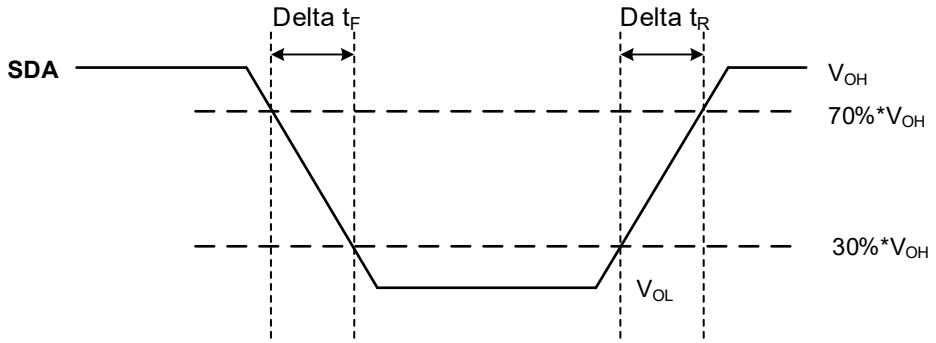


Figure 6. Output Slew Rate Measurement Points

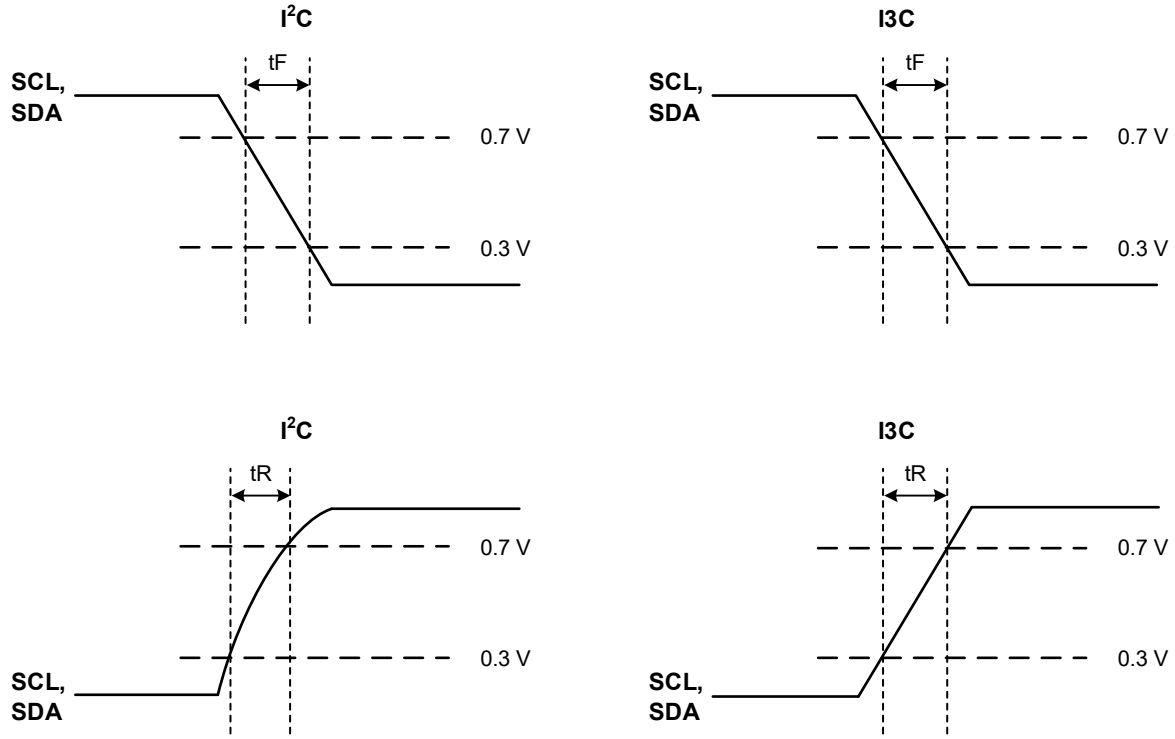


Figure 7. Rise and Fall Timing Parameter Definition

AC TIMING DEFINITION (continued)

HSCL Non Monotonicity

Due to non-deterministic loading (number of DIMMs populated) on an unterminated bus, there can be reflections on the bus, causing slope reversal on the HSCL signal on the input receiver of the SPD5 HUB.

The SPD5 Hub device must tolerate t_{SLPR} and t_{SLPR_PK2PK} slope reversal on HSCL in I3C mode as shown in Figure 8 to Figure 10.

Table 2. HSCL Slope Reversal Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS
Pulse width of slope reversal which must be suppressed (1) (2)	t_{SLPR}	0	2.6	ns
The Peak to Peak voltage of slope reversal which must be suppressed (1) (2)	SLPR_PK2PK	0	150	mV

NOTES:

1. Verified by design and characterization, not necessarily tested on all devices.
2. These parameters apply in I3C mode.

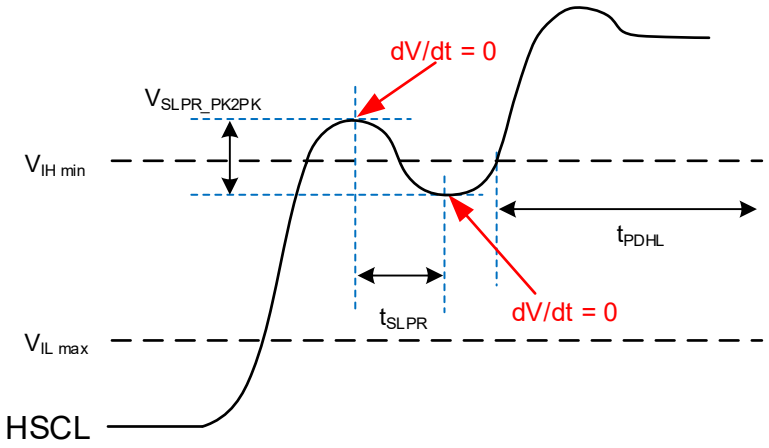


Figure 8. Slope Reversal on HSCL at V_{IH}

NOTE: t_{PDHL} is for reference only in this diagram; refer to measurement methodology for details on this parameter.

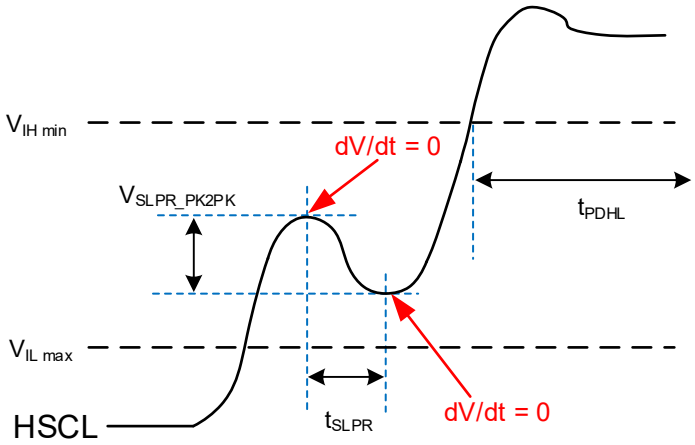


Figure 9. Slope Reversal on HSCL between V_{IL} and V_{IH}

NOTE: t_{PDHL} is for reference only in this diagram; refer to measurement methodology for details on this parameter.

AC TIMING DEFINITION (continued)

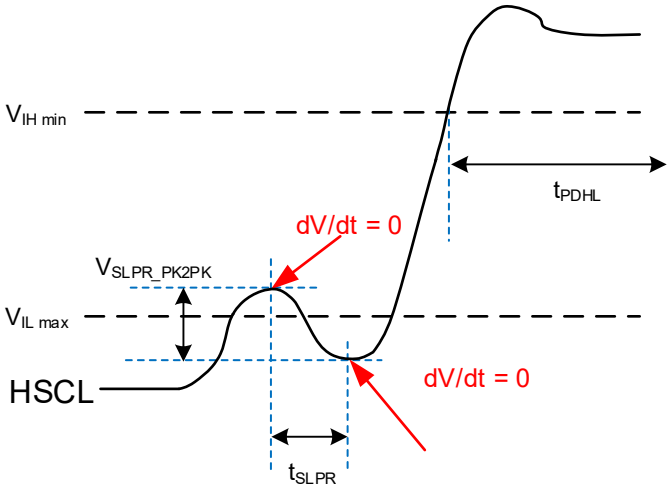


Figure 10. Slope Reversal on HSCL at V_{IL}

NOTE: t_{PDHL} is for reference only in this diagram; refer to measurement methodology for details on this parameter.

Hub Propagation Delay

The SPD5 Hub device has a propagation delay of t_{PDHL} for its host interface HSCL/HSDA input signals to the local interface LSCL/LSDA signals respectively.

Similarly, the SPD5 Hub device has a propagation delay of t_{PDLH} for its local interface LSDA input signal to the host interface HSDA signal.

AC TIMING DEFINITION (continued)

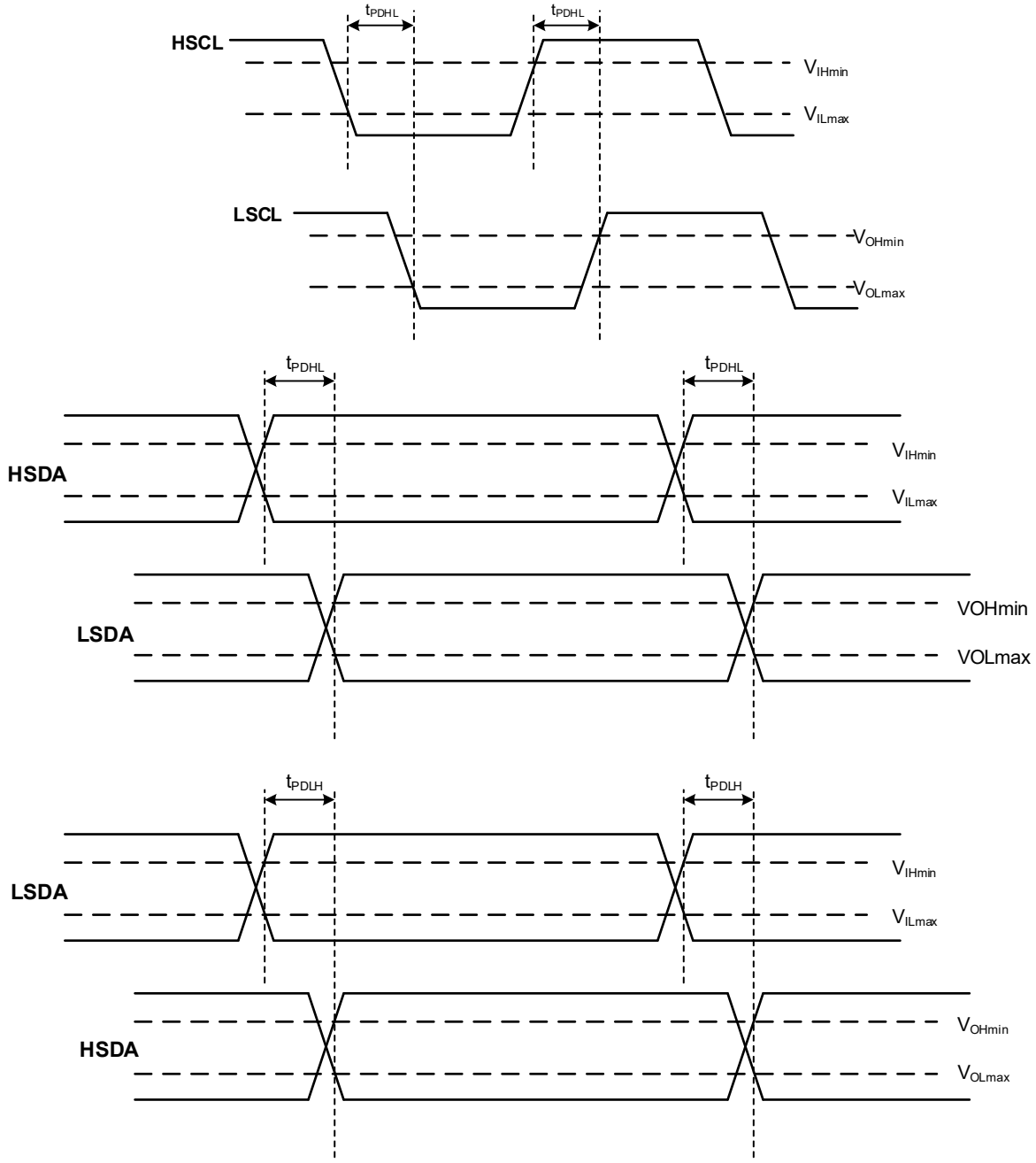


Figure 11. Propagation Delay through the SPD5 Hub Device

DEVICE POWER UP, RESET AND INITIALIZATION

Device Power Up

The SPD5 Hub device has one VDDSPD supply input.

In order to prevent inadvertent operations during power up, a Power-On Reset (POR) circuit is included. On cold power on, VDDSPD input supply must rise monotonically between V_{PON} and V_{DDSPD_MIN} and VDDIO input supply must rise monotonically to V_{DDIO_MIN} without ring back to ensure proper startup.

The SPD5 Hub device uses VDDIO supply for its IO levels and it must reach V_{DDIO_MIN} to ensure proper operation of I^2C or I3C Basic bus interface.

Once the VDDSPD and VDDIO supply is valid and stable, the SPD5 Hub device shall:

1. Once VDDSPD supply is valid and stable, within t_{SENSE_HSA} time, sense its HSA pin to determine if SPD5 Hub device is in application environment or in an offline tester program mode. Depending on what it senses on HSA pin, the SPD5 Hub device configures its HID code automatically based on what it detects on HSA pin at power up.

2. Enable I^2C interface within t_{INIT} time and be ready to receive the command from the Host. The SPD5 Hub device is ready for operation after t_{INIT} time.

The host interface HSDA and HSCL signal pins are pulled up to a pull-up voltage through a pull-up resistor on the platform or on the host controller. The pull-up voltage can be available before or after VDDSPD or VDDIO is valid and stable. If HSDA and HSCL pull-up voltage is available before VDDSPD or VDDIO is available, the HSDA and HSCL signal is high and remains high with no leakage path or damage to the SPD Hub device.

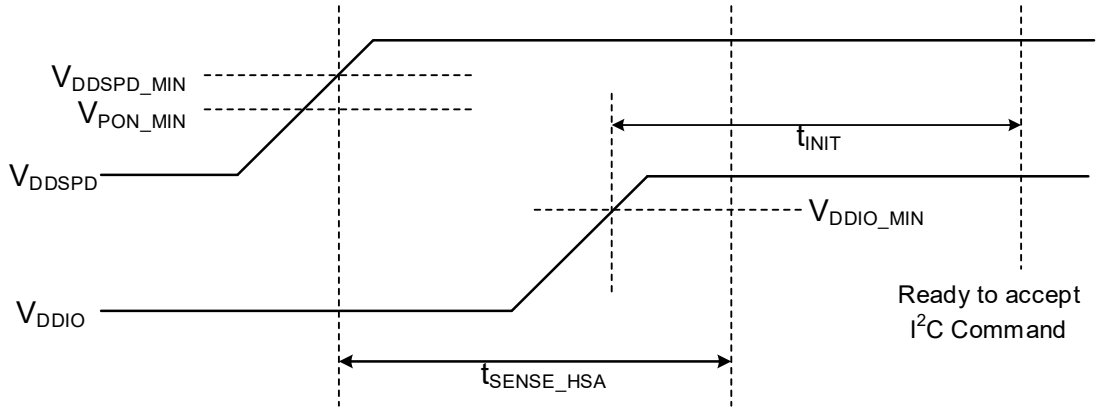


Figure 12. Device Power-Up Sequence

Device Reset and Initialization

At power down (phase during which VDDSPD input supply decreases continuously), as soon as VDDSPD input supply drops below the V_{DDSPD_MIN}, the SPD5 Hub device does not guarantee the operation.

On warm power cycling, the VDDSPD and VDDIO input supply must remain below VPOFF for t_{POFF} and must meet cold power-on reset timing when restoring the power.

Bus Clear

The SPD Hub device supports the following described Bus Clear feature in I^2C mode only. Any attempt by Host to perform I^2C Bus Clear on a Target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the Host abruptly stops clocking SCL while the Target device is in the middle of outputting data for read operation. For this type of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the Host. Eventually when the Host has control of the SCL clock, the Host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

DEVICE POWER UP, RESET AND INITIALIZATION (continued)

Bus Reset

To prevent a malfunctioning device from locking up the I^2C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on HSCL as shown in Figure 13 to force a device bus reset. All devices (All SPD5 Hub and all local Target devices behind the hub) on an I^2C or I3C Basic bus reset simultaneously. Bus reset operation works in the same way regardless of whether the device is operating in I^2C or I3C basic mode.

To guarantee the device resets I^2C bus or I3C Basic bus, the HSCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(MAX)}$.

The SPD5 Hub device does not reset I^2C bus or I3C Basic bus if the HSCL clock input Low time is less than $t_{TIMEOUT(MIN)}$.

If the HSCL clock input Low time is between $t_{TIMEOUT(MIN)}$ and $t_{TIMEOUT(MAX)}$, the SPD5 Hub device does not guarantee and it may or may not reset the I^2C bus or I3C Basic bus.

When RESET, the SPD5 Hub device takes the following actions:

1. Interface and any pending command or transactions are cleared.

2. All internal register values are preserved unless noted otherwise in item #3 below.

3. Device returns to I^2C mode of operation; MR18[7:5] resets to ‘000’; MR27[4] resets to ‘0’; MR52[1:0] resets to ‘00’.

4. Device does not re-sample HSA pin.

5. Device floats the HSDA such that it gets pulled High by external/other pull-up. The device pulls LSDA pin High.

6. Device treats bus resets as STOP operation.

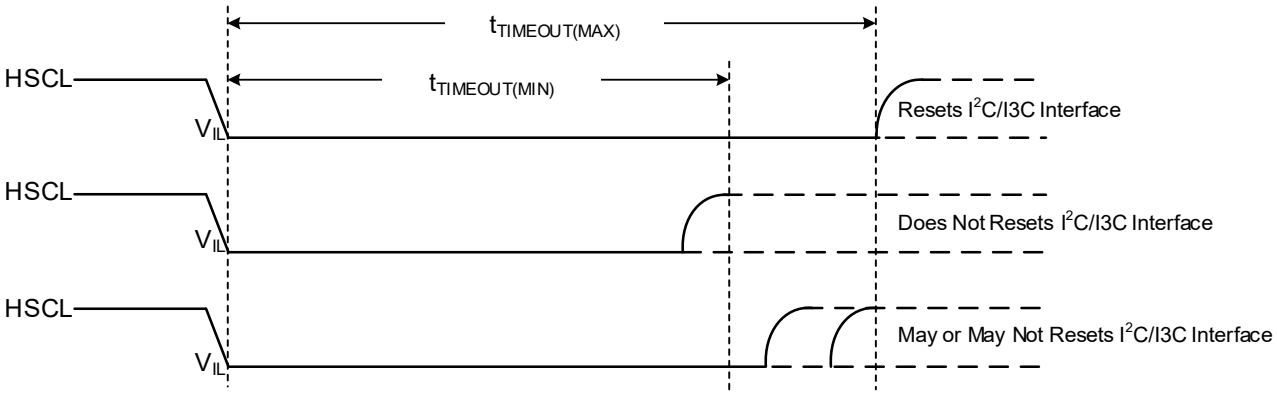


Figure 13. I^2C or I3C Basic Bus Reset - SPD5 Hub Device

DEVICE INTERFACE - IO VOLTAGE CONFIGURATION

The SPD5 Hub device supports configurable Open Drain and Push Pull IO levels to accommodate broad range of DDR5 platform.

Open Drain Interface w/Internal On Die Pull-up Resistor

Figure 14 below shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and Local side of the device. In this configuration, the SPD5 Hub device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 device can support IO levels from 1.0V to 3.3V depending on the supply rail Host may have pulled up the resistor to. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On Local side, the SPD5 device can support IO levels from 1.0V to 1.2V and register MR14[5] must be configured to '0'.

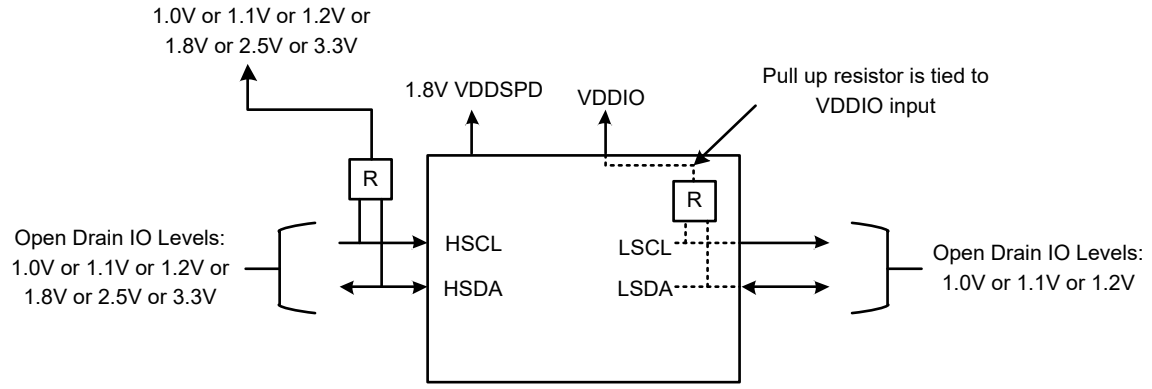


Figure 14. Open Drain Interface; Internal Pull-up Resistor

Open Drain Interface w/External Pull-up Resistor

Figure 15 below shows the SPD5 Hub device configuration options for Open Drain interface for both Host side and local side of the device. In this configuration, the SPD5 device supports Open Drain IO levels on both Host and Local side. However, the IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0V to 3.3V depending on the supply rail Host may have pulled up the resistor to. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On Local side, the SPD5 device can support IO levels from 1.0V to 3.3V and MR14[5] must be configured to '1'.

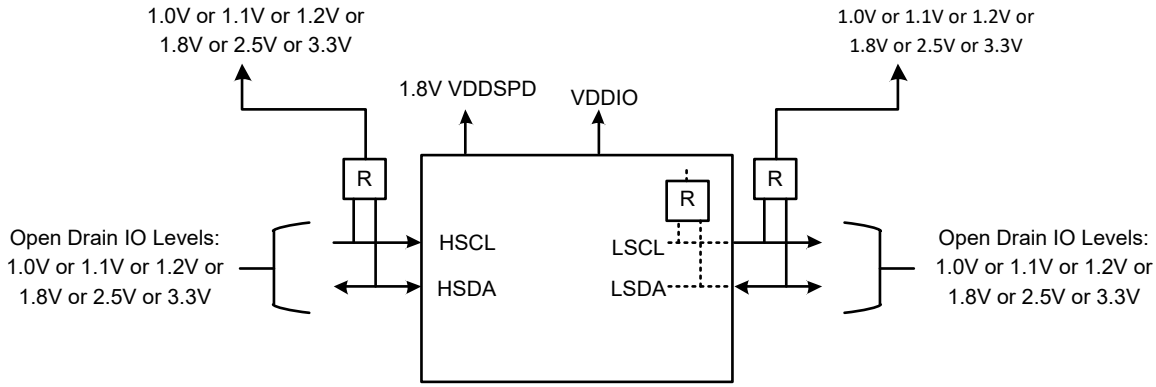


Figure 15. Open Drain Interface; External On Board Pull-up Resistor

DEVICE INTERFACE - IO VOLTAGE CONFIGURATION (continued)

Push Pull Interface w/Internal On Die Pull-up Resistor

The configuration option shown in Figure 16 is only supported when device is in I3C Basic mode. Figure 16 below shows the SPD5 Hub device configuration options for Push Pull interface for both Host side and Local side of the device. In this configuration, the SPD5 Hub device supports Push Pull IO levels on both Host and Local side. However, the pull-up IO voltage levels on Host side and Local side are independent and can be different.

On Host side, the SPD5 Hub device can support IO levels from 1.0V to 1.2V. The host side pull-up resistor can be on motherboard or on die inside the host logic device.

On Local side, the SPD5 Hub device can support IO levels from 1.0V to 1.2V and MR14[5] can be configured to '0' or '1'.

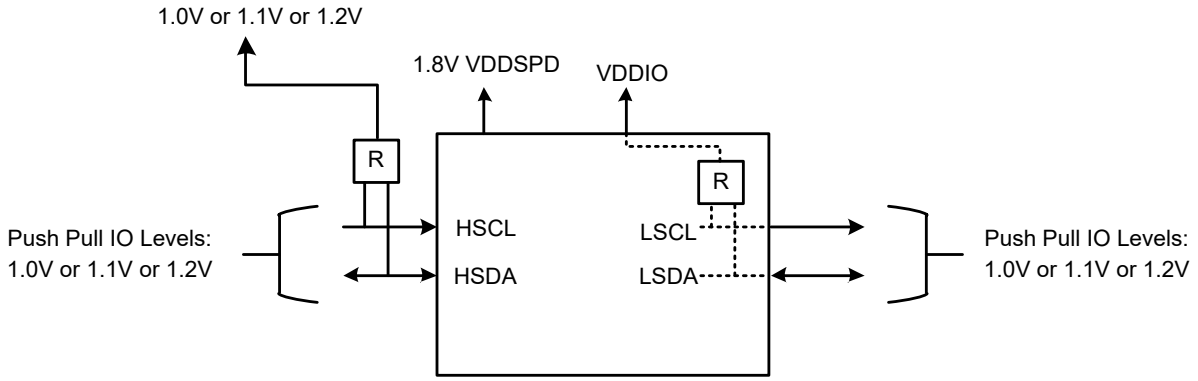


Figure 16. Push Pull Interface; On Die Pull-up

DEVICE INTERFACE - IO VOLTAGE CONFIGURATION (continued)

IO Operation

The SPD5 Hub device supports configurable IO operation scheme of either Open Drain or Push Pull on its Host side of the interface (HSCL and HSDA) and Local side of the interface (LSCL and LSDA). Further, the SPD5 Hub device supports independent IO configuration on Host side and Local side of the interface. The voltage levels for either Open Drain mode or Push Pull mode can also be independently configurable.

At power on, by default, the SPD5 Hub device comes up in legacy I^2C mode of operation with Open Drain IO for both its Host side and Local side of the interface. The maximum speed is limited to 1MHz and supported IO voltage levels are from 1.0V to 3.3V.

After power on, the Host may put the SPD5 Hub device in I3C mode of operation.

In I3C mode, the Host may drive the HSCL clock input of the SPD5 device using either push-pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the Host may always drive the HSCL clock input using a push-pull output driver.

To support in band interrupt, the SPD5 device supports dynamic switching between Open Drain mode and Push Pull mode on its HSDA and LSDA bus for various events. The Table 3 below describes the different mode of operation by the SPD5 device for each cycle.

Table 3. SPD5 Hub Device Dynamic IO Operation Mode Switching

FEATURES	OPEN DRAIN MODE	PUSH PULL MODE
START + Device Select Code	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7'h7E Header Byte	No	Yes
CCC Bytes (i.e after 7'h7E+W=0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

DEVICE INTERFACE - PROTOCOL

I²C and I3C Basic Operation

At power on, by default, the SPD5 Hub device comes up in I²C mode of operation. Following applies in I²C mode:

1. The maximum operation speed is limited to 1MHz.
2. In-band interrupts are not supported.
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The SPD5 Hub device shall operate in the I²C mode until put into I³C Basic mode via command.

The Host may put the SPD5 Hub device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C mode:

1. The maximum operation speed is up to 12.5MHz.
2. In-band interrupts are supported.
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

Serial Address of the SPD5 Hub Device

The 7-bit serial address of the SPD5 Hub device and all local devices behind the SPD5 Hub applies to both I²C and I3C Basic mode of operation identically.

The SPD5 Hub device type ID is 4-bit binary value of 1010b.

The SPD5 Hub device samples the status of the HSA pin on power up. The sampled status of the HSA pin determines the unique host ID (HID) of the device. The host identifier value (HID) is merged with the SPD5 Hub device type 1010 xxxb to establish the 7-bit address (SPD5 Hub DevID[6:0]) for the device on the I²C or I3C Basic bus as shown in Table 4. For example, if the value sensed on HSA pin identifier is 2 (010 binary), then the unique 7-bit address for this device is 1010 010b.

Table 4. 7-bit Address of SPD5 Hub Device

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	1	0	HID[2]	HID[1]	HID[0]	R/W
SPD5 Hub Device Type ID (LID)				Host ID (HID)			Read/Write

Serial Address of the Local Devices

Each local device behind the SPD5 Hub device has a unique 4-bit local device ID (LID) code. For example, the PMIC local device type ID is 4-bit binary value of 1001b.

The 3 HID bits of the local device type has a default value of '111' and is merged with its unique 4-bit local ID code to establish the 7-bit address (DevID[6:0]) for the local device on the I²C or I3C Basic bus as shown in Table 5. For example, the PMIC local device behind the SPD5 Hub has 7-bit address of 1001 111b.

Table 5. 7-bit Address of the Local Devices (e.g. PMIC Device)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	0	1	1	1	1	R/W
Local Device Type ID (LID)				Host ID (HID)			Read/Write

DEVICE INTERFACE - PROTOCOL (continued)

Switch from I^2C Mode to I3C Basic Mode

By default when SPD5 Hub first powers on, it operates in I^2C mode. The SPD5 Hub device shall operate in I^2C mode until put into I3C Basic mode via command.

In I^2C mode, the Host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the SPD5 Hub device may simply ignore it. The Host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The Host puts the SPD5 Hub device in I3C Basic mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the SPD5 Hub device, it updates the MR18[5] to '1'.

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device as explained in ***Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC).***

Switch from I3C Basic Mode to I^2C Mode

The Host can put the SPD5 Hub device back in I^2C mode from I3C mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the SPD5 Hub device, it updates the MR18[5] to '0'.

SPD5 Hub Device Selection

The Host can access any SPD5 Hub device as shown in Table 6 below in both I^2C mode and I3C Basic mode. The last 3 bits represent the HID bits.

Table 6. 7-bit Address of Each Hub Devices on I^2C/I3C Bus

HOST ACCESS TO:	7-BIT ADDRESS
DIMM 0 SPD Hub	1010 000
DIMM 1 SPD Hub	1010 001
DIMM 2 SPD Hub	1010 010
DIMM 3 SPD Hub	1010 011
DIMM 4 SPD Hub	1010 100
DIMM 5 SPD Hub	1010 101
DIMM 6 SPD Hub	1010 110
DIMM 7 SPD Hub	1010 111

DEVICE INTERFACE - PROTOCOL (continued)

Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC)

By default, the SPD5 Hub device and all local Target devices power up in I^2C mode of operation, prior to Host issuing SETHID CCC, the Host can access any local device behind the SPD5 Hub device. To access the local device, the Host sends 7-bit address that is made up of 4 bits of local device code (LID) followed by the 3 bits of HID code. The LID code represents which local device the Host is intended to target. The HID code represents which DIMM the local device resides on. The Table 7 below shows an example of four different local device address codes behind SPD5 Hub on each DIMM.

Table 7. 7-bit Address of Each Hub Devices on I^2C/I3C Bus

HOST ACCESS TO:	7-BIT ADDRESS LID = 1011 (RCD)	7-BIT ADDRESS LID = 1001 (PMIC)	7-BIT ADDRESS LID = 0010 (TS0)	7-BIT ADDRESS LID = 0110 (TS1)
DIMM 0 Local Device	1011 000	1001 000	0010 000	0110 000
DIMM 1 Local Device	1011 001	1001 001	0010 001	0110 001
DIMM 2 Local Device	1011 010	1001 010	0010 010	0110 010
DIMM 3 Local Device	1011 011	1001 011	0010 011	0110 011
DIMM 4 Local Device	1011 100	1001 100	0010 100	0110 100
DIMM 5 Local Device	1011 101	1001 101	0010 101	0110 101
DIMM 6 Local Device	1011 110	1001 110	0010 110	0110 110
DIMM 7 Local Device	1011 111	1001 111	0010 111	0110 111

The SPD5 Hub Device monitors the LID code coming from the Host. When it detects the Host access is for the Target device, it compares the last 3 bits of the HID information (shown in Red) coming from the Host against its own unique HID code that it has stored at power on. It compares each 3 bits one at a time. If there is a match, the SPD5 Hub device substitutes that bit with '1' and forwards it to the local device interface. If there is a mismatch, the SPD5 Hub device substitutes that bit with '0' and forwards it to the local device interface. As a result, only the targeted local device will see its last three HID bits as '111' and all non-targeted local devices will see their last three HID bits as anything other than '111' which is not a valid code as shown in Table 5.

There are two exceptions when SPD5 Hub device does not substitute its own HID code when it forwards it to the local Target interface:

1. Host issues Start followed by 7'h7E with W=0 (or Host issues Start followed by 0xFC).

2. After SPD5 Hub executes SETHID CCC command that Host issues. See ***Local Device Selection Through the SPD5 Hub Device (After SETHID CCC).***

Figure 17 gives an example of Host accessing local RCD Device on DIMM0. The figure shows Host sends 7-bit address '1011 000'. Each SPD5 Hub device receives this address. Each SPD5 Hub device forwards first four bits of binary address '1011' (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address '000' from the Host against its own unique HID code and substitutes the bits on the local device interface.

Figure 18 gives another example of Host accessing local Temperature Sensor 0 device on DIMM3. The figure shows Host sends 7-bit address '0010 011'. Each SPD5 Hub device receives this address. Each SDP5 Hub device forwards first four bits of binary address '0010' (LID) on the local device interface. Each SPD5 Hub compares last 3 bits of binary address '011' from the Host against its own unique HID code and substitutes the bits on the local device interface.

DEVICE INTERFACE - PROTOCOL (continued)

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58

Figure 17. Example: Host Accessing RCD on DIMM 0

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14	001 0100	14
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15	001 0101	15
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16	001 0110	16
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17	001 0111	17
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10	001 0000	10
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11	001 0001	11
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12	001 0010	12
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	001 0011	13												
Hub Sends			001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13	001 0011	13

Figure 18. Example: Host Accessing Temperature Sensor 0 on DIMM 3

DEVICE INTERFACE - PROTOCOL (continued)

Local Device Selection Through the SPD5 Hub Device (After SETHID CCC)

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device as explained in ***Local Device Selection Through the SPD5 Hub Device (Before SETHID CCC)***. After Host sends SETHID CCC, the Host still accesses all local Target devices behind the SPD5 Hub as shown in Table 7. There is no change in how Host accesses the SPD5 Hub device and all local Target devices behind the SPD5 Hub device before or after SETHID CCC.

I^2C Target Protocol - Host to SPD5 Hub Device

The SPD5 Hub devices operate on a standard I^2C serial interface. Transactions where the SPD5 Hub device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a read or write bit, R/W. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert an NACK.

The SPD5 Hub device does not allow any read or write operations to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The Host should either check MR48[3] register status or ensure that Write time (t_W) parameter is satisfied prior to performing another write or read operations to non-volatile memory. If Host violates this and performs either write or read operation to non-volatile memory, the SPD5 Hub device ACKs the address byte to allow possible volatile register access. However, the SPD5 Hub device NACKs the subsequent write or read operation if MemReg = '1' and sets the MR52[7] = '1'.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e. MemReg = '0') when it is busy with internal write operation to non-volatile memory.

To allow compatibility with legacy I^2C host controller, the SPD5 Hub device offers two ways to address 1024 bytes of non-volatile memory when it is operating in I^2C mode only. By default, the SPD5 Hub device accepts 1 byte of address which covers first 128 bytes of non-volatile memory. The Host must select the page pointer through volatile register MR11[2:0] to address the entire 1024 bytes of non-volatile memory.

Alternatively, at initial power on, the Host can set the MR11[3] = '1' to address the entire 1024 bytes of non-volatile memory with 2 bytes of address and hence not required to go through page selection to address entire non-volatile memory.

This two byte address mode is only applicable to SPD5 Hub device and it is not applicable to PMIC or TS or RCD device in I^2C mode.

The SPD5 Hub device volatile register space does not require the page selection process as all volatile registers are within first 128 bytes.

DEVICE INTERFACE - PROTOCOL (continued)

Write Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply Upper Address bits.

Table 8. Write Command Data Packet; MR11[3] = '0'

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	Data								A	
	…								A	
	Data								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.

Table 9. Write Command Data Packet; MR11[3] = '1'

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1] (2)				A	
	Data								A	
	…								A	
	Data								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.

Read Operation - Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply Upper Address bits.

Table 10. Read Command Data Packet; MR11[3] = '0'

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr[0]	Address[5:0]						A	
Sr	1	0	1	0	HID			R=1	A (2)	
	Data								A	
	…								A	
	Data								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. The device may eventually ACK.

DEVICE INTERFACE - PROTOCOL (continued)

Table 11. Read Command Data Packet; MR11[3] = '1'

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr[0]	Address[5:0]						A	
	0	0	0	0	Blk Addr[4:1] (2)				A	
Sr	1	0	1	0	HID			R=1	A (3)	
	Data								A	
	…								A	
	Data								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
3. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. The device may eventually ACK.

Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the Host periodically may poll critical information from the same location. An example may be the SPD5 Hub device's temperature readout. To help improve the efficiency of the I^2C bus protocol, the SPD5 Hub offers a default read address pointer mode so that whenever the SPD5 Hub device sees the STOP operation on its HSCL and HSDA bus, its read address pointer always resets to default address. The default read pointer address mode is enabled through register MR18[4] and default starting address for read operation is selectable through register MR18[3:2]. This allows Host to read the read command data packet as shown in Table 12 compared to as shown in Table 11. The default read address pointer reduces the packet overhead by 3 bytes. The Host typically enables this mode when the normal operation of the DDR5 DIMM begins. The default read address pointer mode is only applicable to volatile register space (i.e. MemReg = '0').

Table 12. Read Command Data Packet w/Default Address Pointer Mode

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr	1	0	1	0	HID			R=1	A	
	Data								A	
	…								A	
	Data								N	Sr or P

DEVICE INTERFACE - PROTOCOL (continued)

I²C Target Protocol - Host to Local Device through SPD5 Hub Device

Write Operation - Data Packet

Table 13. Write Command Data Packet (e.g. TS)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	0	0	1	0	HID			W=0	A	
	Address[7:0]								A	
	Data								A	
	Data								A	
	…								A	
	Data								A	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

Table 14. Write Command Data Packet (e.g. PMIC)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	0	1	HID			W=0	A	
	Address[7:0]								A	
	Data								A	
	Data								A	
	…								A	
	Data								A	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

When Host makes any write request to the RCD device, the RCD protocol has PEC check in the last byte. The SPD simply treats the last byte as Data like any other bytes as shown in Table 16. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I²C interface.

Table 15. Write Command Data Packet (e.g. RCD; PEC Disabled)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	1	HID			W=0	A	
	Data (I²C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num[7:0])								A	
	Data (Reg Num[7:0])								A	
	Data (Wr Data[31:24])								A	
	Data (Wr Data[23:16])								A	
	Data (Wr Data[15:8])								A	
	Data (Wr Data[7:0])								A	Sr or P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

DEVICE INTERFACE - PROTOCOL (continued)

Table 16. Write Command Data Packet (e.g. RCD; PEC Enabled)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=8)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num[7:0])								A	
	Data (Reg Num[7:0])								A	
	Data (Wr Data[31:24])								A	
	Data (Wr Data[23:16])								A	
	Data (Wr Data[15:8])								A	
	Data (Wr Data[7:0])								A	
	Data (PEC[7:0])								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.

Read Operation - Data Packet

When Host makes any read request to the RCD device, the RCD protocol has PEC check for the RCD address information as well as data returned by the RCD. The SPD5 Hub simply treats the PEC information as data byte like any other data byte as shown in Table 20. The SPD5 Hub device does not check for the PEC. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I^2C interface.

Table 17. Read Command Data Packet (e.g. TS)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	0	0	1	0	HID			W=0	A	
	Address[7:0]								A	
Sr	0	0	1	0	HID			R=1	A (2)	
	Data								A	
	Data								A	
	…								A	
	Data								N	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

DEVICE INTERFACE - PROTOCOL (continued)

Table 18. Read Command Data Packet (e.g. PMIC)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	0	1	HID			W=0	A	
	Address[7:0]								A	
Sr	1	0	0	1	HID			R=1	A (2)	
	Data								A	
	Data								A	
	…								A	
	Data								N	Sr or P

1. In I^{2}C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^{2}C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

Table 19. Read Command Data Packet (e.g. RCD; PEC Disabled; Legacy Format)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	1	HID			W=0	A	
	Data (I^{2}C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num[7:0])								A	
	Data (Reg Num[7:0])								A	P
S	1	0	1	1	HID			W=0	A	
	Data (I2C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A (2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data[31:24])								A	
	Data (Rd Data[23:16])								A	
	Data (Rd Data[15:8])								A	
	Data (Rd Data[7:0])								A	Sr or P

1. In I^{2}C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^{2}C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

DEVICE INTERFACE - PROTOCOL (continued)

Table 20. Read Command Data Packet (e.g. RCD; PEC Enabled; Legacy Format)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num[7:0])								A	
	Data (Reg Num[7:0])								A	
	Data (PEC[7:0])								A	P
S	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A (2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data[31:24])								A	
	Data (Rd Data[23:16])								A	
	Data (Rd Data[15:8])								A	
	Data (Rd Data[7:0])								A	
	Data (PEC[7:0])								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

Table 21. Read Command Data Packet (e.g. RCD; PEC Disabled; Optimized Format)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N	STOP
S or Sr (1)	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved; 0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page Num[7:0])								A	
	Data (Reg Num[7:0])								A	P
Sr	1	0	1	1	HID			R=1	A (2)	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data[31:24])								A	
	Data (Rd Data[23:16])								A	
	Data (Rd Data[15:8])								A	
	Data (Rd Data[7:0])								A	Sr or P

1. In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire.

DEVICE INTERFACE - PROTOCOL (continued)

I3C Basic Target Protocol - Host to SPD5 Hub Device

Write Operation Data Packet

The SPD5 Hub devices operate on a standard I3C serial interface. Transactions where the SPD5 Hub device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit SPD5 Hub device address then a write bit, R/W. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the SPD5 Hub device typically replies with an ACK unless there are conditions when it may passively assert an NACK. The 'T' bit carries Parity information from the Host for each byte.

The SPD5 Hub device does not allow any read or write operations to its non-volatile memory when it is busy with internal write operation to non-volatile memory. The Host should either check MR48[3] register status or ensure that Write time (t_W) parameter is satisfied prior to performing another write or read operations to non-volatile memory. If Host violates this and performs either write or read operation to non-volatile memory, the SPD5 Hub device always ACKs the address byte. In a subsequent byte, the device ignores the write operation if MemReg = '1' and sets the MR52[7] = '1' and requests IBI if IBI function is enabled. Subsequently, if Host continues to do the read operation with Repeat Start, the SPD5 Hub device NACKs.

The SPD5 Hub device does allow any read or write operation to its volatile memory (i.e. MemReg = '0') when it is busy with internal write operation to non-volatile memory.

The Packet Error Code (PEC) function is disabled by default when the SPD5 Hub device is put in I3C Basic mode.

The Host may enable this function through DEVCTRL CCC (RegMod = '0'). If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the Host must complete the burst length as indicated in CMD field. In other words, the Host must not interrupt the burst length pre-maturely for Write operation.

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply Upper Address bits.

Table 22. Write Command Data Packet; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			W=0	A (1) (2) (3)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	0	0	0	0	Blk Addr[4:1] (4)				T	
	Data								T	
	…								T	
	Data								T	Sr (5) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
5. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 23. Write Command Data Packet; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			W=0	A (1) (2) (3)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	CMD			W=0	Blk Addr[4:1] (4)				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr (5) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
5. Repeat Start or Repeat Start with 7'h7E.

The Host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic Host issuing a START condition followed by 7'h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. The Table 24 and Table 25 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled cases respectively. Note that in Table 25, PEC calculation does not include IBI header byte (7'h7E followed by W = 0).

Table 24. Write Command Data Packet w/IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A(1) (3)	
Sr	1	0	1	0	HID			W=0	A (2) (3) (4)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	0	0	0	0	Blk Addr[4:1] (5)				T	
	Data								T	
	…								T	
	Data								T	Sr (6) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
6. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 25. Write Command Data Packet w/IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A(1) (3)	
Sr	1	0	1	0	HID			W=0	A (2) (3) (4)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	CMD			W=0	Blk Addr[4:1] (5)				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr (6) or P

NOTES:

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
6. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Read Operation Data Packet

The transactions to SPD5 Hub Target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit SPD5 Hub device type identifier then a write bit. All I3C Basic bus data are transmitted with the most significant bit MSB first. During select code transmission, the SPD5 Hub device typically replies with an ACK unless there are exceptional conditions when it may passively assert an NACK. See Table 26. The 'T' bit carries Parity information from the Host prior to Repeated START. After Repeated START, 'T' bit carries information from SPD5 Hub device to Host indicating Continuous ('1') or Stop ('0') whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when SPD5 Hub device is put in I3C Basic mode. The Host may enable this function through DEVCTRL CCC (RegMod = '0'). If enabled, the PEC is appended as shown in Table 27. If PEC is enabled, the Host must complete the burst length as indicated in CMD field. In other words, the Host must not interrupt the burst length pre-maturely for Read operation.

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply Upper Address bits.

Table 26. Read Command Data Packet; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			W=0	A (1) (2) (3)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	0	0	0	0	Blk Addr[4:1] (4)				T	
S or Sr	1	0	1	0	HID			R=1	A/N (5) (6)	
	Data								T=1	
	…								T=1	
	Data								T=1 (7) (8)	Sr (9) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
5. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the SPD5 Hub may eventually ACK.
6. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
7. See Figure 22 to see how Host ends Target device operation.
8. For NVM read memory access (i.e. MemReg = '1'), when last byte is reached (1024 Byte) or for volatile memory access (i.e. MemReg = '0'), when last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
9. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 27. Read Command Data Packet; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			W=0	A (1) (2) (3)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	CMD			R=1	Blk Addr[4:1] (4)				T	
	PEC								T	
S or Sr	1	0	1	0	HID			R=1	A/N (5) (6)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (7)	Sr (8) or P

NOTES:

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
4. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
5. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD5 Hub may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
6. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
7. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
8. Repeat Start or Repeat Start with 7’h7E.

DEVICE INTERFACE - PROTOCOL (continued)

The Host may optionally allow SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic Host issuing a START condition followed by 7'h7E and then write bit. If SPD5 Hub device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If SPD5 Hub device has no pending IBI, there is no action taken by SPD5 Hub. The Table 28 and Table 29 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled cases respectively. Note that in Table 29, PEC calculation (from Host to SPD5 Hub) does not include IBI header byte (7'h7E followed by W=0).

Table 28. Read Command Data Packet w/IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A(1) (3)	
Sr	1	0	1	0	HID			W=0	A (2) (3) (4)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	0	0	0	0	Blk Addr[4:1] (5)				T	
Sr	1	0	1	0	HID			R=1	A/N (6) (7)	
	Data								T=1	
	…								T=1	
	Data								T=1 (8) (9)	Sr (10) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
6. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
7. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the SPD5 Hub may eventually ACK.
8. See Figure 22 to see how Host ends Target device operation.
9. For NVM read memory access (i.e. MemReg = '1'), when last byte is reached (1024 Byte) or for volatile memory access (i.e. MemReg = '0'), when last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
10. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 29. Read Command Data Packet w/IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A(1) (3)	
Sr	1	0	1	0	HID			W=0	A (2) (3) (4)	
	MemReg	Blk Addr[0]	Address[5:0]						T	
	CMD			R=1	Blk Addr[4:1] (5)				T	
	PEC								T	
Sr	1	0	1	0	HID			R=1	A/N (6) (7)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (8)	Sr (9) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
3. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
4. The SPD5 Hub does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match its own device code. The SPD5 Hub ignores the entire packet until STOP or next Repeat Start operation.
5. The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr[4] bit.
6. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
7. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there was no parity or PEC error, the SPD5 Hub may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat Start operation. If there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
8. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
9. Repeat Start or Repeat Start with 7'h7E.

Default Read Address Pointer Mode

This mode works the same exact way as explained in ***Default Read Address Pointer Mode*** in I^2C Target Protocol section. Table 30 and Table 31 show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, MR18[1] sets the number of bytes that SPD5 Hub device sends out followed by the PEC calculation. If PEC is enabled, the Host must complete the burst length as indicated in MR18[1] register. In other words, the Host must not interrupt the burst length pre-maturely for default address pointer read operation. The default read address pointer mode is only applicable to volatile register space (i.e. MemReg = '0').

Table 30. Read Command Data Packet w/Read Address Pointer Mode; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			R=1	A (1)	
	Data								T=1	
	…								T=1	
	Data								T=1 (2) (3)	Sr (4) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. See Figure 22 to see how Host ends Target device operation.
3. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
4. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 31. Read Command Data Packet w/Read Address Pointer Mode; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	0	HID			R=1	A (1)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (2)	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. See Figure 23 to see how Target device ends the operation followed by STOP operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 32. Read CMD Data Packet w/Read Address Pointer Mode and IBI Header; PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1) (2)	
Sr	1	0	1	0	HID			R=1	A (2) (3)	
	Data								T=1	
	…								T=1	
	Data								T=1 (4) (5)	Sr (6) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
4. See Figure 22 to see how Host ends Target device operation.
5. When last byte (i.e. MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
6. Repeat Start or Repeat Start with 7'h7E.

Table 33. Read CMD Data Packet w/Read Address Pointer Mode and IBI Header; PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1) (2)	
Sr	1	0	1	0	HID			R=1	A (2) (3)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (4)	Sr (5) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
4. See Figure 23 to see how Target device ends the operation followed by STOP operation.
5. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

I3C Basic Target Protocol - Host to Local Device (Through SPD5 Hub Device)

Write Operation - Data Packet

Table 34 to Table 39 shows examples of write command data packet for different types of local devices behind the SPD5 Hub. These examples do not show the optional IBI header byte that Host may choose to use. All local devices behind SPD5 Hub device also support the IBI header byte similar to as shown in Table 24 and Table 25.

Table 34. Write Command Data Packet (e.g. TS); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	0	1	0	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
	Data								T	
	Data								T	
	…								T	
	Data								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit[7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 35. Write Command Data Packet (e.g. TS); PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	0	1	0	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit [7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 36. Write Command Data Packet (e.g. PMIC); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	0	1	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
	Data								T	
	Data								T	
	…								T	
	Data								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit[7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 37. Write Command Data Packet (e.g. PMIC); PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	0	1	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit[7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I3C Basic interface.

DEVICE INTERFACE - PROTOCOL (continued)

Table 38. Write Command Data Packet (e.g. RCD); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	1	HID			W=0	A (1) (2) (3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count=8)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num[7:0])								T	
	Data (Reg Num[7:0])								T	
	Data (Wr Data[31:24])								T	
	Data (Wr Data[23:16])								T	
	Data (Wr Data[15:8])								T	
	Data (Wr Data[7:0])								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Data, bit[7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 39. Write Command Data Packet (e.g. RCD); PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	1	HID			W=0	A (1) (2) (3)	
	Data (I3C Bus Command)								T	
	Data (Byte Count=8)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num[7:0])								T	
	Data (Reg Num[7:0])								T	
	Data (Wr Data[31:24])								T	
	Data (Wr Data[23:16])								T	
	Data (Wr Data[15:8])								T	
	Data (Wr Data[7:0])								T	
	Data (PEC[7:0])								T	Sr (4) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Data, bit[7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Read Operation - Data Packet

Table 40 to Table 45 shows examples of read command data packet for different types of local devices behind the SPD5 Hub. These examples do not show the optional IBI header byte that Host may choose to use. All local devices behind SPD5 Hub device also support the IBI header byte similar to as shown in Table 28 and Table 29.

Table 40. Read Command Data Packet (e.g. TS); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	0	1	0	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
Sr	0	0	1	0	HID			R=1	A/N (4) (5)	
	Data								T=1	
	…								T=1	
	Data								T=1 (6) (7)	Sr (8) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 22 to see how Host ends Target device operation.
7. For volatile register access, when last byte (MR255) is reached (extreme rare case), the Target device sends T = ‘0’. See Figure 23 to see how Host ends Target device operation.
8. Repeat Start or Repeat Start with 7’h7E.

Table 41. Read Command Data Packet (e.g. TS); PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	0	0	1	0	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
Sr	0	0	1	0	HID			R=1	A/N (4) (5)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (6)	Sr (7) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The TS device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 22 to see how Target device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7’h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 42. Read Command Data Packet (e.g. PMIC); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	0	1	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
Sr	1	0	0	1	HID			R=1	A/N (4) (5)	
	Data								T=1	
	…								T=1	
	Data								T=1 (6) (7)	Sr (8) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 22 to see how Host ends Target device operation.
7. For volatile register access, when last byte is reached within the region (either Host region or DIMM Vendor region), it will continue to return the data but returned data is 0x00 if there is no valid password for DIMM vendor region or device vendor specific region. Once the address counter reaches R255, it resets to address R00 and it continues to return the data. Only Host can perform the STOP operation.
8. Repeat Start or Repeat Start with 7'h7E.

Table 43. Read Command Data Packet (e.g. PMIC); PEC Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	0	1	HID			W=0	A (1) (2) (3)	
	Address[7:0]								T	
Sr	1	0	0	1	HID			R=1	A/N (4) (5)	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0 (6)	Sr (7) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The TS device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset _n and Chip Select input (DCS_n) to allow any read or write access on its I3C Basic interface.

DEVICE INTERFACE - PROTOCOL (continued)

Table 44. Read Command Data Packet (e.g. RCD); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	1	HID			W=0	A (1) (2) (3)	
	Data (I^2C Bus Command)								T	
	Data (Byte Count=4)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num[7:0])								T	
	Data (Reg Num[7:0])								T	
Sr	1	0	1	1	HID			R=1	A/N (4) (5)	
	Data (Byte Count)								T=1	
	Data (Status)								T=1	
	Data (Rd Data[31:24])								T=1	
	Data (Rd Data[23:16])								T=1	
	Data (Rd Data[15:8])								T=1	
	Data (Rd Data[7:0])								T=0 (6)	Sr (7) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Data).
2. The RCD NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 45. Read Command Data Packet (e.g. RCD); PEC Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	0	1	1	HID			W=0	A (1) (2) (3)	
	Data (I^2C Bus Command)								T	
	Data (Byte Count=4)								T	
	Data (Reserved; 0x00)								T	
	Data (Dev/Channel Num)								T	
	Data (Page Num[7:0])								T	
	Data (Reg Num[7:0])								T	
Sr	1	0	1	1	HID			R=1	A/N (4) (5)	
	Data (Byte Count)								T=1	
	Data (Status)								T=1	
	Data (Rd Data[31:24])								T=1	
	Data (Rd Data[23:16])								T=1	
	Data (Rd Data[15:8])								T=1	
	Data (Rd Data[7:0])								T=1	
	Data (PEC [7:0])								T=0 (6)	Sr (7) or P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Data).
2. The RCD NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The RCD device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. If Target device NACKs during Repeat Start for any reason, the Host may re-try Repeat Start again. The Host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
5. See Figure 21 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
6. See Figure 23 to see how Target device ends the operation followed by Host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

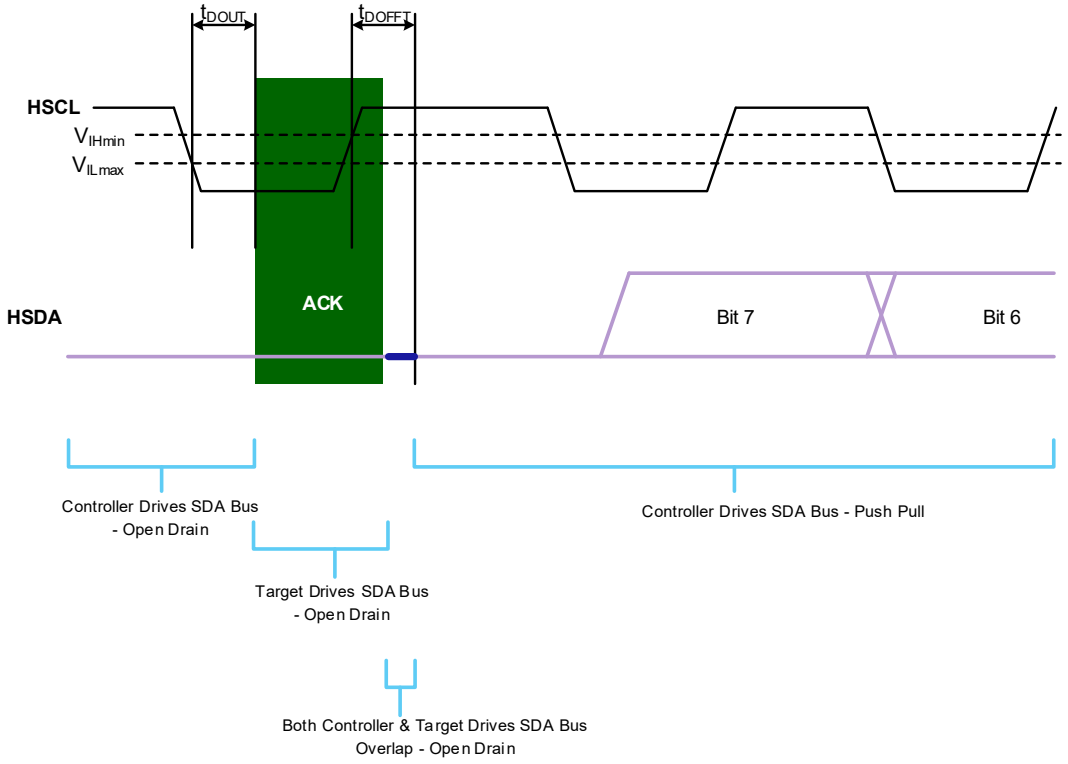


Figure 19. Target Open Drain to Host Push Pull Hand Off Operation

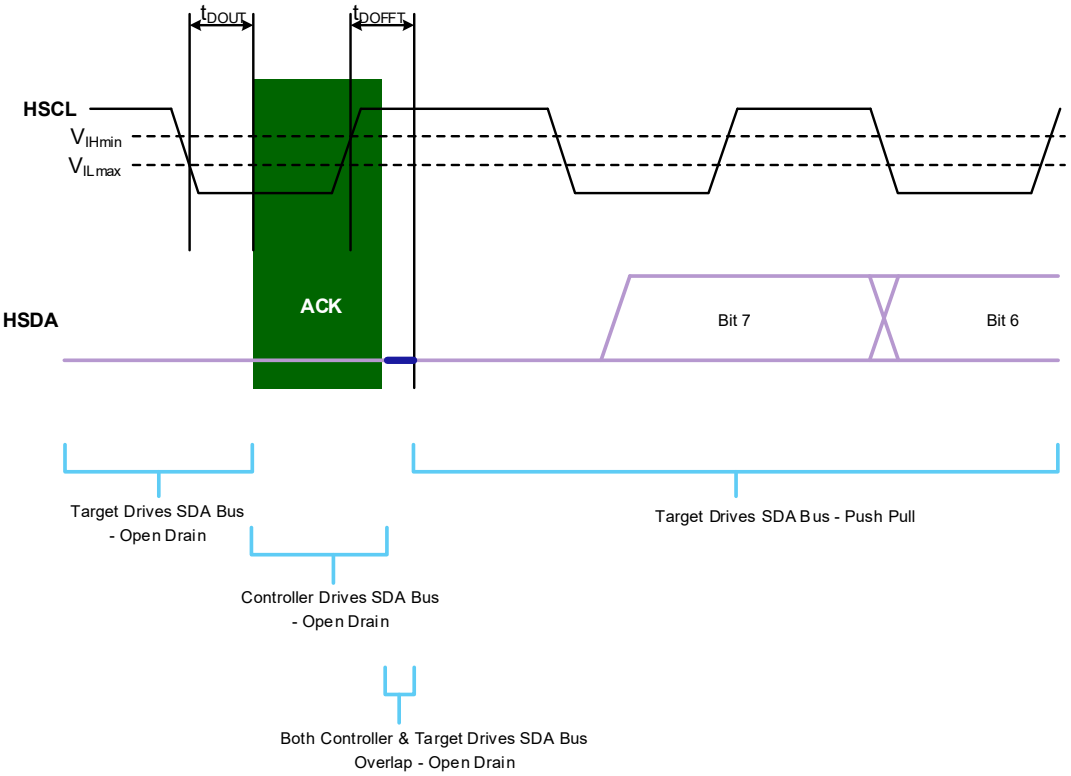


Figure 20. Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

DEVICE INTERFACE - PROTOCOL (continued)

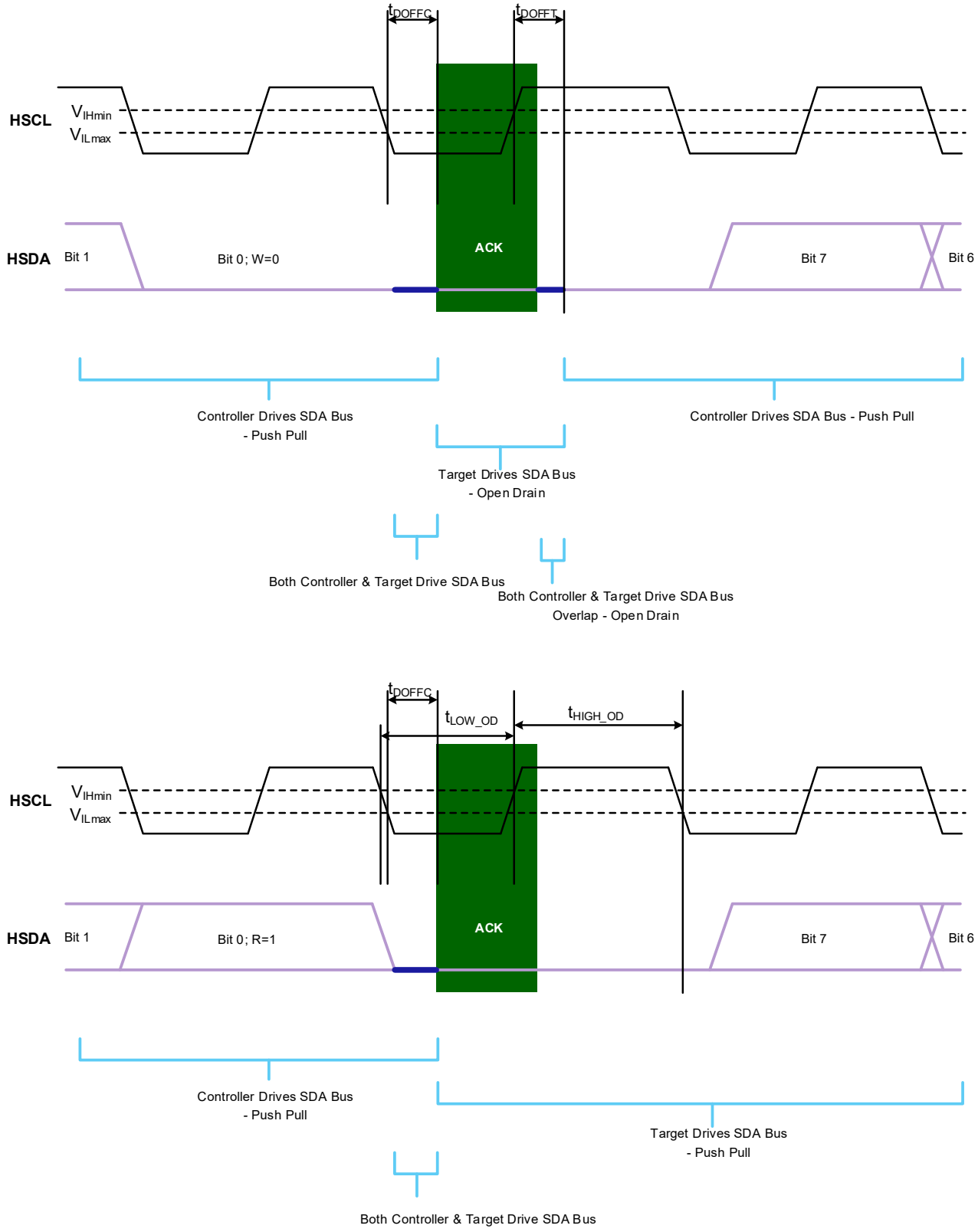


Figure 21. Controller Push Pull to Target Open Drain Hand Off Operation

DEVICE INTERFACE - PROTOCOL (continued)

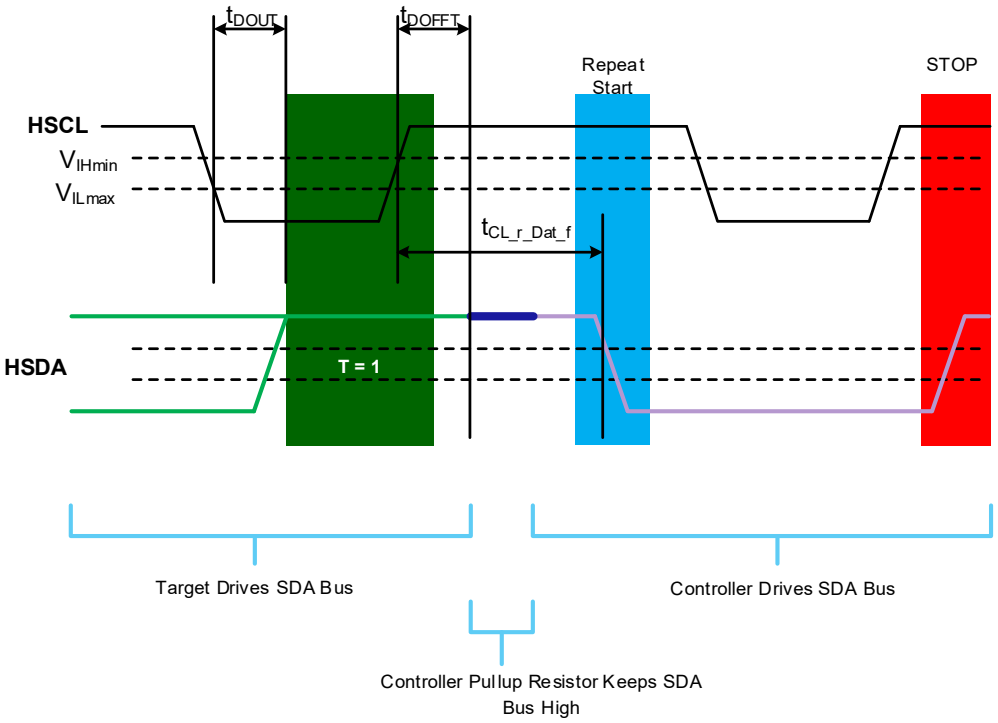


Figure 22. T = 1; Host Ends Read with Repeated START and STOP Waveform

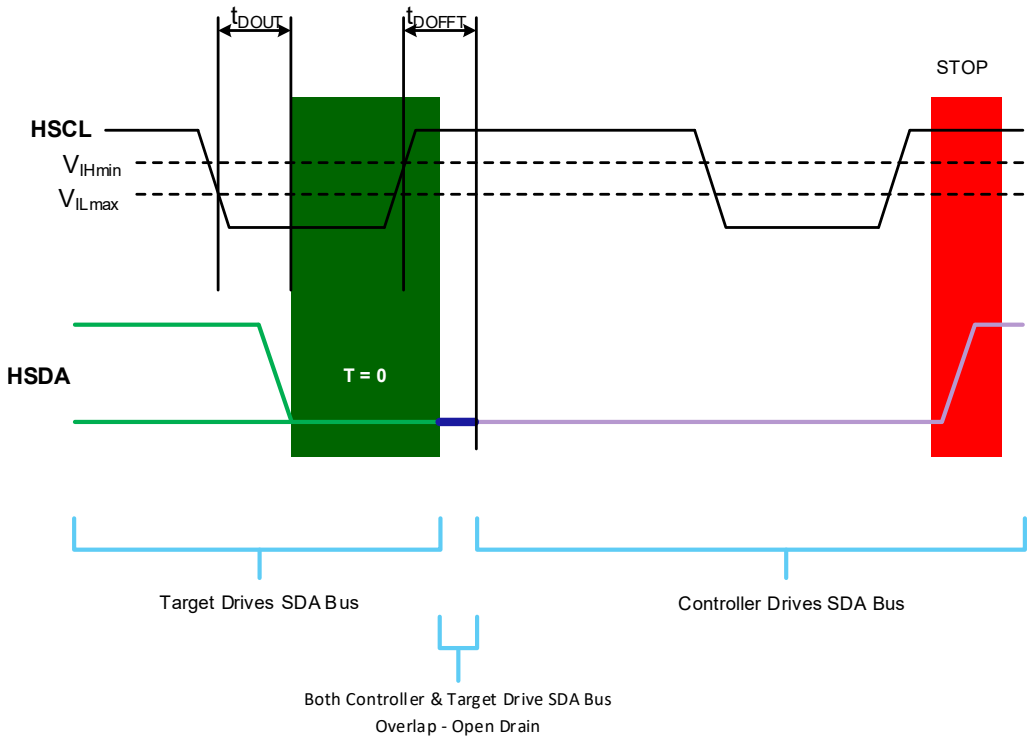


Figure 23. T = 0; Target Ends Read; Host Generates STOP

DEVICE INTERFACE - PROTOCOL (continued)

I3C Basic Common Command Codes (CCC)

The I3C Basic specification lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The SPD5 Hub device NACKs for all unsupported CCC. The SPD5 Hub supports CCC as listed in Table 46 below.

The SPD5 Hub device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The SPD5 Hub device also requires STOP operation between any direct CCC to broadcast CCC.

The SPD5 Hub device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

CCC is an I3C concept by definition, and shall always conform to I3C SDR timings, irrespective of whether the device has switched from I^2C mode or not.

Prior to dynamic address assignment (SETAASA/P), the Target device(s) may drive the ACK/NACK past the Open Drain SCL rising but before the next SCL falling transition, as a longer overlap in Open Drain is harmless. Immediately after the Open Drain ACK (upon the next SCL falling edge), the bus should transition to Push Pull mode (though still at 1MHz) as described in the MIPI *I3C Basic Specification V1.0, Section 5.1.2.3 "Handoff from Address ACK to SDR Controller Write Data" and Figure 32 "I3C Data Transfer - ACK by Target"*.

For additional details on how to handle the ACK transition, please refer to the *MIPI I3C Basic Specification V1.0, Section 5.1.2.3.1 "Transition from Address ACK to SDR Controller Write Data"*.

Table 46. SPD5 Hub CCC Support Requirement

CCC	MODE	CODE	DESCRIPTION
ENEC	Broadcast	0x00	Enable Event Interrupts
	Direct	0x80	
DISEC	Broadcast	0x01	Disable Event Interrupts
	Direct	0x81	
RSTDAA	Broadcast	0x06	Put the device in I^2C Mode (aka: Reset Dynamic Address Assignment)
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)
GETSTATUS	Direct	0x90	Get Device Status
DEVCAP (1)	Direct	0xE0	Get Device Capability
SETHID (1)	Broadcast	0x61	SPD5 Hub updates 3-bit HID field, updates 'T' bit with updated parity calculation for all devices behind Hub and stops 3-bit HID translation.
DEVCTRL (1)	Broadcast	0x62	Configure SPD5 Hub and all devices behind Hub

NOTE: 1. JEDEC specific CCC.

ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for Host to issue this CCC. When ENEC CCC is registered by the SPD5 Hub, it updates MR27[4] = '1' and it takes in effect at the next Start operation (i.e. after STOP condition). Table 47 to Table 50 shows an example of a single ENEC CCC. Table 51 shows the encoding definition for ENEC CCC.

DEVICE INTERFACE - PROTOCOL (continued)

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 47. ENEC CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x00 (Broadcast)								T	
	7'h00							ENINT	T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 48. ENEC CCC - Broadcast w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x00 (Broadcast)								T	
	7'h00							ENINT	T	
	PEC								T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 49. ENEC CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A (1) (2)	
	7'h00							ENINT	T	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 50. ENEC CCC - Direct w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A (1) (2)	
	7'h00							ENINT	T	
	PEC								T	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 51. ENEC CCC Byte Encoding

BIT	ENCODING	NOTES
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = '0'

DEVICE INTERFACE - PROTOCOL (continued)

DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for Host to issue this CCC. When DISEC CCC is registered by the SPD5 Hub, it updates MR27[4] = '0' and it takes in effect at the next Start operation (i.e. after STOP condition). Table 52 to Table 55 shows an example of a single DISEC CCC. Table 56 shows the encoding definition for DISEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 52. DISEC CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 53. DISEC CCC - Broadcast w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 54. DISEC CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A (1) (2)	
	7'h00							ENINT	T	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 55. DISEC CCC - Direct w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A (1) (2)	
	7'h00							DISINT	T	
	PEC								T	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 56. DISEC CCC Byte Encoding

BIT	ENCODING	NOTES
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'

RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I^2C mode, this CCC is ignored. When RSTDAA CCC is registered by the SPD5 Hub, it updates MR18[5] = '0' and it takes in effect at the next Start operation (i.e. after STOP condition). Further it disables IBI and PEC function (MR27[4] = '0', MR18[7] = '0' respectively) and clears parity function (MR18[6] = '0'). Table 57 to Table 58 shows an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 57. RSTDAA CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x06 (Broadcast)								T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 58. RSTDAA CCC - Broadcast w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x06 (Broadcast)								T	
	PEC								T	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

SETAASA CCC

The SETAASA CCC is only supported when device is in I^2C mode; however, it still follows I3C SDR timings compliant to CCC definitions. In I^2C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1MHz. In I3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the SPD5 Hub, it updates MR18[5] = '1'and it takes in effect at the next Start operation (i.e. after STOP condition). Table 59 shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I^2C mode and there is no PEC function in I^2C mode.

Table 59. SETAASA CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

DEVICE INTERFACE - PROTOCOL (continued)

GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e. it is not executed internally and GETSTATUS CCC code is not acknowledged and Host must do STOP operation). Table 60 to Table 61 shows an example of a single GETSTATUS CCC. Table 62 shows the encoding definition for GETSTATUS CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

When the SPD5 Hub device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The Host must explicitly clear the appropriate status register through Clear command by writing '1' to corresponding register or by issuing Global Clear command. Once the SPD5 Hub device clears the appropriate status register, the PEC_Err, P_err and Pending Interrupt Bits [3:0] get cleared.

After Host issues Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

Table 60. GETSTATUS CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R=1	A (1)	
	PEC_Err	0	0	0	0	0	0	0	T=1	
	0	0	P_Err	0	Pending Interrupt				T=0	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 61. GETSTATUS CCC - Direct w/PEC (1)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (2)	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A (1)	
	PEC_Err	0	0	0	0	0	0	0	T=1	
	0	0	P_Err	0	Pending Interrupt				T=1	
	PEC								T=0	Sr (3) or P

1. GETSTATUS CCC with PEC check is only supported in I3C Basic mode.
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. Repeat Start or Repeat Start with 7'h7E.

Table 62. GETSTATUS CCC Byte Encoding

BIT	ENCODING	NOTES
PEC_Err	0 = No Error 1 = PEC Error occurred	This register is cleared when Host issues clear command to MR20[1] for PEC error.
P_Err	0 = No Error 1 = Protocol Error; Parity Error occurred	This register is cleared when Host issues clear command to MR20[0] for Parity error.
Pending Interrupt	0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI status register to get cleared.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for Host to issue this CCC. Table 63 to Table 64 shows an example of a single DEVCAP CCC. Table 65 shows the encoding definition for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 63. DEVCAP CCC - Direct

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T=1	
	LSB (Each bit defines capability)								T=0	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 64. DEVCAP CCC - Direct w/PEC

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A (1)	
	MSB (Each bit defines capability)								T=1	
	LSB (Each bit defines capability)								T=1	
	PEC								T=0	Sr (2) or P

1. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 65. DEVCAP CCC Byte Encoding

BIT	ENCODING	NOTES
MSB[7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	SPD5 Hub hard codes to '1'
MSB[1:0]	RFU	Coded as '0'
LSB[7:0]	RFU	Coded as '0'

DEVICE INTERFACE - PROTOCOL (continued)

SETHID CCC

The SETHID CCC is supported only when device is in I^2C mode. In I^2C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1MHz. In I3C Basic mode, it is illegal for Host to issue this CCC. When SETHID CCC is registered by the SPD5 Hub, it stops 3-bit HID translation. Table 66 shows an example of a single SETHID CCC. The Host must send all '0' in the data byte followed by 'T' bit. The SPD5 Hub device forwards bits [7:4, 0] to local devices behind the SPD5 Hub as it receives from the Host. The SPD5 Hub device substitutes its own 3-bit HID code in bits [3:1] and forwards it to the local devices behind the SPD5 Hub. The SPD5 Hub device also re-calculates the parity information and forwards the updated parity information in 'T' bit. As the device is in I^2C mode when SETHID CCC is issued, the PEC function is not supported.

The Host may issue SETHID CCC more than one time.

Table 66. SETHID CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	0	0	0	0	T	P

DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub device, there are 4 local Target devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e. Packet Error Check), the Host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the Host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the Host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when the Host issues this CCC, to guarantee that this CCC is registered by the device without any error, the Host shall limit the maximum speed operation for this CCC to 1MHz. Table 67 to Table 68 shows an example of a single DEVCTRL CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

The Host shall pay attention to DEVCTRL CCC. The DEVCTRL CCC is limited to SPD5 Hub device's volatile register space only and should not be used for SPD5 Hub's NVM operation. If DEVCTRL CCC is used to access device specific registers (e.g. RegMod = '1'), the Host shall still follow any device specific register restriction. For example, if device specific register requires STOP operation for device to take in the effect of the setting, the Host must also use STOP operation when using DEVCTRL CCC to access device specific register.

In I^2C mode, DEVCTRL CCC must be limited to 1 byte addressing mode for SPD5 Hub device (i.e. MR11[3] = '0').

DEVICE INTERFACE - PROTOCOL (continued)

Table 67. DEVCTRL CCC - Broadcast

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (2)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr (3) or P

1. The SPD5 Hub NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. An exception is made for DEVCTRL CCC where device does report a parity error when it determines 7-bit device select code issued by the Host does not match with its own device code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 68. DEVCTRL CCC - Broadcast w/PEC (1)

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S or Sr	1	1	1	1	1	1	0	W=0	A (2)	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T (3)	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr (4) or P

1. DEVCTRL CCC with PEC check is only supported in I3C Basic mode.
2. The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. An exception is made for DEVCTRL CCC where device does report a parity error when it determines 7-bit device select code issued by the Host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

DEVICE INTERFACE - PROTOCOL (continued)

Table 69. DEVCTRL CCC Command Definition

PARAMETER	DEFINITION
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; SPD5 Hub device responds if DevID[6:0] field matches with SPD5 Hub device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; SPD5 Hub device and possible other device respond if DevID[6:3] field matches with SPD5 Hub device's own 4-bit LID address 111 = Broadcast Command; All devices respond to this command All other encodings are reserved.
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the Host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e. StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond. If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

Table 70. DEVCTRL CCC Data Payload Definition

BYTE #	BIT #	FUNCTION	DEFINITION	COMMENT
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	MR18[7] is updated
	[6]	Parity Disable	0 = Disable 1 = Enable	MR18[6] is updated
	[5:2]	RFU	RFU	
	[1]	RSVD	0 = RSVD 1 = RSVD	SPD5 Hub device always ignores this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No Action 1 = Clear All Event and pending IBI (1)	MR27[7] is updated.
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

1. After Target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCTRL CCC Examples - RegMod = '0'

Table 71 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C Basic bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The Host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices with DevID[6:3] that matches to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' with disable the parity function.

Table 71. DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 72 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The Host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices will enable PEC function.

Table 72. DEVCTRL CCC Example - Broadcast Command to all Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 73 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The Host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 73. DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

DEVICE INTERFACE - PROTOCOL (continued)

DEVCTRL CCC Examples - RegMod = '1'

Table 74 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of '1001' on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 74. DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

Table 75 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 75. DEVCTRL CCC Example - Multicast Command to '1001' Devices

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	1	1	1	1	1	0	W=0	A (1)	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

1. See Figure 19 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

IN BAND INTERRUPT (IBI)

In I^2C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

Enabling and Disabling In Band Event Interrupt Function

By default, all interrupt sources are disabled (i.e. set to '0'). The Host may enable following interrupts in the SPD5 Hub device. Once enabled, the SPD5 Hub device sends an IBI when that event occurs.

1. Error Interrupt Enable in MR27[4]:

- When MR27[4] = '1', the device sends the IBI at next available opportunity when any of the register bit in MR52[7:5, 1:0] is set to '1' and sets MR48[7] = '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC.
- When MR27[4] = '0', the device does not send the IBI regardless of the register bit status in MR52[7:5, 1:0]. However, the device does set MR48[7] = '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC.

2. Temperature sensor interrupt enable in MR27[3:0]: The Host can set any combination of register bits to '1':

- When any of the register bits in MR27[3:0] = '1' and if MR27[4] = '1', the device sends the IBI at next available opportunity when the corresponding register bit in MR51[3:0] is set to '1' and sets MR48[7] = '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC.
- When any of the register bits in MR27[3:0] = '0' or MR27[4] = '0', the device does not send the interrupt regardless of the corresponding register bit status in MR51[3:0]. However, the device does set MR48[7] = '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC if any of the bits in MR27[3:0] = '1' and MR27[4] = '0'.

Mechanics of Interrupt Generation - SPD5 Hub Device

Event interrupts may be generated by the SPD5 Hub device if IBI is enabled. When there is a pending interrupt (i.e. MR48[7] = '1 and MR27[4] = '1'), the SPD5 Hub requests an interrupt after detecting Start condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If the SPD5 Hub detects no Start condition but if the Host to the SPD5 Hub device bus (HSDA and HSCL) has been inactive (no edges seen) for t_{AVAL} period, then the SPD5 Hub device may assert HSDA low by t_{IBI_ISSUE} time to request an interrupt. When the SPD5 Hub device requests an interrupt, the Host toggles the HSCL. The SPD5 Hub device transmits its 7-bit binary address, '1010' followed by 3 HID bits, and then sets the R/W bit = '1'.

When the SPD5 Hub device requests an interrupt, the Host may take one of the two actions below.

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the SPD5 Hub confirms that it has won the arbitration, the SPD5 Hub device transmits the IBI payload as shown in Table 76 and Table 77 for PEC disabled and PEC enabled configuration, respectively. See Figure 24. It just shows only first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by 8-bit register contents of MR51 and MR52 in order. The Host then issues the Stop command. Note the timing waveform in Figure 24. The Host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The Host can interrupt the IBI payload at 'T'. If Host stops the IBI payload at 'T' bit in the middle of payload, the SPD5 Hub device retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits[3:0] internally and waits for the next opportunity to request an interrupt. If the SPD5 Hub device successfully transmits the entire IBI payload, it then clears IBI status flag MR48[7] = '0' and Pending Interrupt Bits[3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 25 followed by a Stop command. In this case, the SPD5 Hub device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent a NACK, it does have a knowledge of which SPD5 Hub device sent the IBI request. The SPD5 Hub retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits[3:0] = '0001'.

IN BAND INTERRUPT (IBI) (continued)

Table 76. Hub IBI Payload Packet; PEC is Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	0	1	0	HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	MR51[7:0]								T = 1	
	MR52[7:0]								T = 0 (2)	P

1. See Figure 20 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 23 to see how Target device ends the operation followed by Host Stop operation.

Table 77. Hub IBI Payload Packet; PEC is Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	1	0	1	0	HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	MR51[7:0]								T = 1	
	MR52[7:0]								T = 1	
	PEC								T = 0 (2)	P

1. See Figure 20 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 23 to see how Target device ends the operation followed by Host Stop operation.

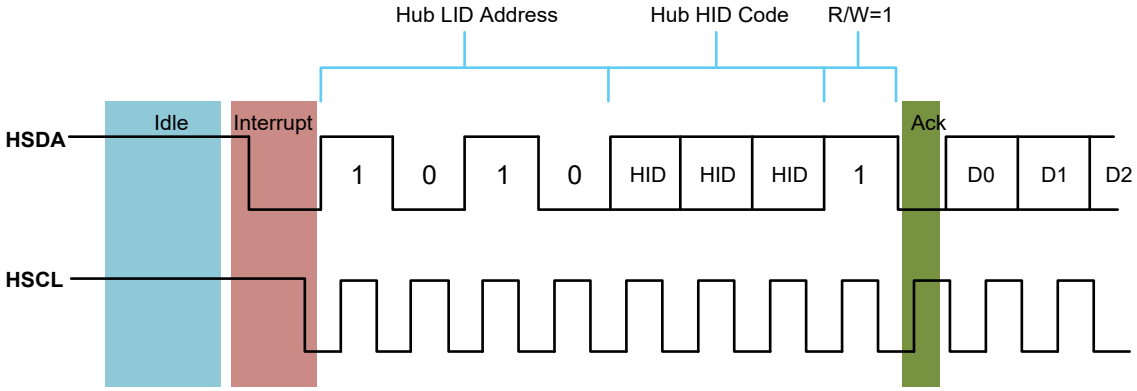


Figure 24. SPD5 Hub Interrupt; Host ACK followed by SPD5 Hub Device IBI Payload

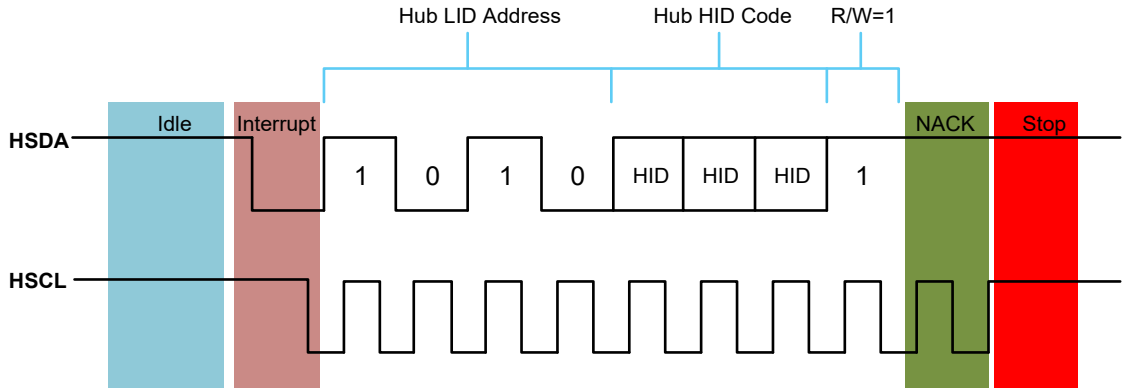


Figure 25. SPD5 Hub Interrupt; Host NACK followed by Stop

IN BAND INTERRUPT (IBI) (continued)

Mechanics of Interrupt Generation - Local Target Device

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt in any local device and if IBI is enabled, the local device requests an interrupt after detecting Start condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If the local device detects no Start condition but if the Host to the local Target device (through the SPD5 Hub device) bus (LSDA and LSCL) has been inactive (no edges seen) for t_{AVAL} period, then any local device may assert LSDA low by t_{IBI_ISSUE} time to request an interrupt. When the local device requests an interrupt, the SPD5 Hub device propagates the LSDA to HSDA to Host. The Host toggles the HSCL. The local device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' to the SPD5 Hub device. This is shown in Figure 26 top waveform.

The SPD5 Hub device forwards LID bits it receives from the local device to the Host. The SPD5 Hub device substitutes its own HID code in place of the HID bits it receives from the local device and sends to the Host if Host has not issued SETHID CCC previously. This is shown in Figure 26 middle waveform. The SPD5 Hub device forwards HID bits it receives from the local device to the Host if Host has issued SETHID CCC previously. This is shown in Figure 26 bottom waveform. The SPD5 Hub device forwards the R/W bit = '1' to the Host.

When the local device requests an interrupt, the Host may take one of the two actions below.

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the local device confirms that it has won the arbitration, the local device transmits the IBI payload as shown in Table 78 and Table 79 for PEC disabled and PEC enabled configuration respectively. See Figure 26. It just shows only first two data bits of MDB byte to illustrate the timing. The interrupt payload contains MDB followed by appropriate Target device error register contents in order. The Host then issues the Stop command. Note the timing waveform in Figure 26. The Host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The Host can interrupt the IBI payload at 'T' bit. If Host stops the IBI payload at 'T' bit in the middle of payload, the local device retains the IBI status flag and Pending Interrupt Bits[3:0] internally and waits for the next opportunity to request an interrupt. If the local device successfully transmits the entire IBI payload, it then clears IBI status flag and Pending Interrupt Bits[3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 27 followed by a Stop command. In this case, the local device does not transmit the IBI payload and waits for the next opportunity to request an interrupt.

At this point, though Host sent a NACK, it does have a knowledge of which local device sent the IBI request. The local device retains the IBI status flag and Pending Interrupt Bits[3:0] = '0001'.

Table 78. Target Device IBI Payload Packet; PEC is Disabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	LID				HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	First Error Code Byte								T = 1	
	Second Error Code Byte								T = 1	
	…								T = 0 (2)	P

1. See Figure 20 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 23 to see how Target device ends the operation followed by Host Stop operation.

Table 79. Target Device IBI Payload Packet; PEC is Enabled

START	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	A/N/T	STOP
S	LID				HID			R = 1	A (1)	
	MDB = 0x00								T = 1	
	First Error Code Byte								T = 1	
	Second Error Code Byte								T = 1	
	…								T = 1	
	PEC								T = 0 (2)	P

1. See Figure 20 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
2. See Figure 23 to see how Target device ends the operation followed by Host Stop operation.

IN BAND INTERRUPT (IBI) (continued)

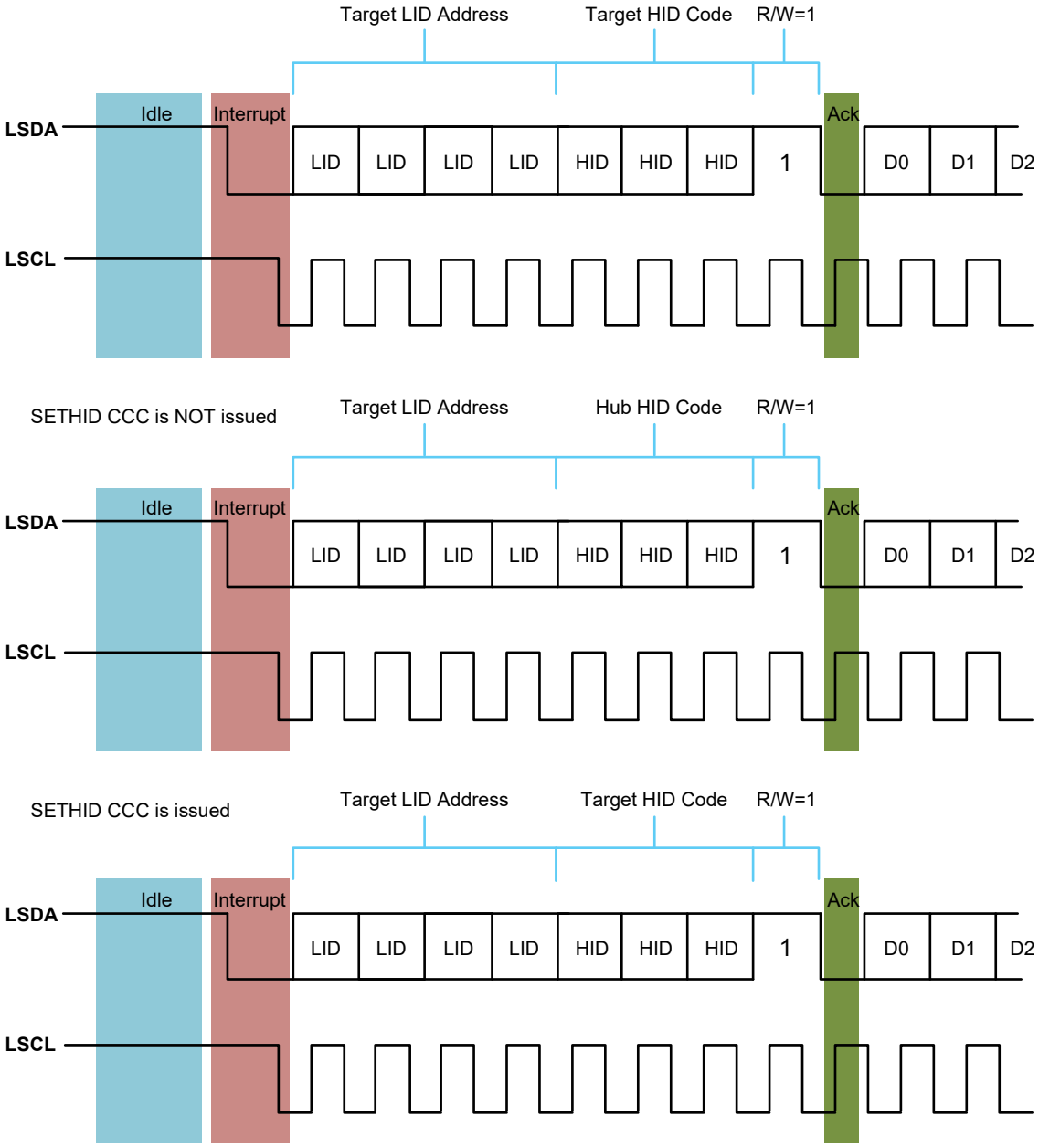


Figure 26. Local Device Interrupt; Host ACK followed by Target Device IBI Payload

IN BAND INTERRUPT (IBI) (continued)

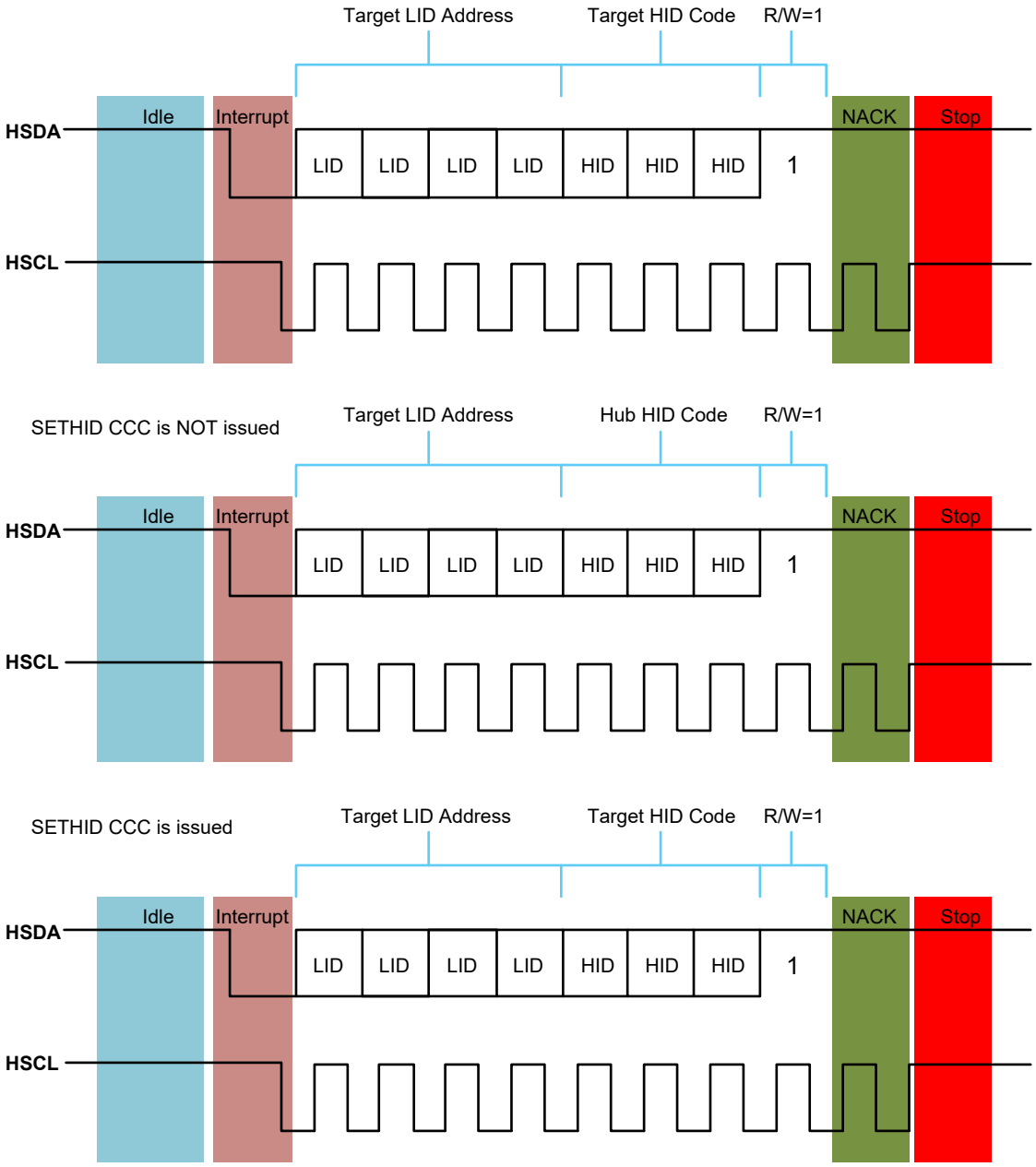


Figure 27. Local Device Interrupt; Host NACK followed by Stop

IN BAND INTERRUPT (IBI) (continued)

Interrupt Arbitration; SETHID CCC is Not Issued by Host

As there are multiple local Target devices behind the SPD5 Hub and there are multiple SPD5 Hub devices on I3C Basic bus, multiple devices may request an interrupt when the I3C Basic bus is inactive for t_{AVAL} period. Arbitration process is required.

Interrupt Arbitration - Among SPD5 Hub Devices

This section explains the interrupt arbitration among the SPD5 Hub devices only. There are up to 8 SPD5 Hub devices on the I3C Basic bus.

As all SPD5 Hub devices have the same 4-bit LID code of '1010', the arbitration is always won by the lower HID code. For example, if one SPD5 Hub device has HID code of '000' and other SPD5 Hub device has a HID code of '011', through the arbitration process, the HID code of '000' wins. The SPD5 Hub device with a HID code of '011 must release the bus and wait for next opportunity to request an interrupt. Table 80 shows the arbitration priority based on the HID code for the SPD5 Hub device.

Table 80. Interrupt Arbitration - Among SPD5 Hub Devices

HUB DEVICE LID CODE	HUB DEVICE HID CODE	ARBITRATION PRIORITY
1010	000	1
1010	001	2
1010	010	3
1010	011	4
1010	100	5
1010	101	6
1010	110	7
1010	111	8

Interrupt Arbitration - Among Local Target Devices behind One SPD5 Hub Devices

This section explains the interrupt arbitration among the local devices only behind the SPD5 Hub. There are up to 13 local devices behind the SPD5 Hub.

As all local Target devices behind the SPD5 Hub devices have the same 3-bit HID code, hence the arbitration is always won by the 4-bit LID code. For example, if one local Target device has LID code of '1001' and other local Target device has a LID code of '0010', through the arbitration process, the LID code of '0010' wins. The local device with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt. Table 81 shows the arbitration priority based on the LID code for the local devices. The Green color cells in Table 81 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM.

During the interrupt arbitration phase, the SPD5 Hub device forwards the winning 4-bit LID code one digit at a time that it receives from the local Target devices to the Host.

The SPD5 Hub device discards the 3-bit '111' HID code received from the local Target device. Instead the SPD5 Hub device forwards its own unique 3-bit HID code one digit at a time to the Host. As a result, the Host can identify the winning device based on the 4-bit LID code (Local Target device) and 3-bit HID code (the DIMM). Also, when the SPD5 Hub device substitutes its own unique 3-bit HID code to the Host, its own receiver will see that at the input and it compares each 3 bits one at a time as it if the Host sent those 3 bits. If there is a match, the SPD5 Hub device forwards '1' to the local device interface and if there is a mismatch, the SPD5 Hub device forwards '0' to the local device interface. Because the local Target device sends '111' as its 3 bit HID code, the local device knows that it won the arbitration.

IN BAND INTERRUPT (IBI) (continued)

Table 81. Interrupt Arbitration - Among Local Target Devices

DEVICE	TARGET DEVICE LID CODE	TARGET DEVICE HID CODE	ARBITRATION PRIORITY
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	HID	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

Interrupt Arbitration - Between SPD5 Hub Device and Local Target Devices behind the Hub

This section explains the interrupt arbitration among the SPD5 Hub device and all local devices behind that SPD5 Hub. There are up to 13 local devices behind each SPD5 Hub.

As the SPD5 Hub device LID code of '1010', any local Target devices with a lower LID code always wins the arbitration process as shown in Table 81. The local Target devices with a higher LID code than '1010', the SPD5 Hub device wins the arbitration process. As an example, for a typical DDR5 RDIMM/LRDIMM, the RCD always has the lowest priority for winning the interrupt arbitration.

Interrupt Arbitration - Among Local Target Devices behind Different SPD5 Hub Devices

This section explains the interrupt arbitration among the SPD5 Hub devices and all local devices behind any SPD5 Hub devices. There are up to 8 SPD5 Hub devices on the I3C bus and up to 13 local devices behind each SPD5 Hub.

The arbitration process is hybrid of the ***Interrupt Arbitration - Among SPD5 Hub Devices*** and ***Interrupt Arbitration - Between SPD5 Hub Device and Local Target Devices behind the Hub*** section. The device with the lowest 4 bit LID code across all local Target devices and across all SPD5 Hub devices always wins the arbitration process. The HID code for that lowest LID code represents the SPD5 Hub device code.

Table 82 shows four examples. In each example, the Target LID code column represents local Target device behind Hub which has HID code value of '111'; the Hub HID code column represents the SPD5 Hub device which has LID code of '1010' followed by its own unique HID code; the winning device column represent the final winner among all devices (either SPD Hub device or local Target devices) during the arbitration phase.

Example 1:

There are total 5 devices (4 local Target devices and 1 Hub device) that are requesting an interrupt. These 5 devices are shown in the RED color text. The devices that are in the Black color text are not requesting an interrupt. The winning device is the local device LID code of '0010' and HID code of '111'. This is because the LID code of '0010' is the lowest among three other local Target device code and its HID code is '111'.

IN BAND INTERRUPT (IBI) (continued)

Example 2:

There are total 4 devices (2 local Target devices and 2 Hub devices) that are requesting an interrupt. These 4 devices are shown in the RED color text. The devices that are in the Black color text are not requesting an interrupt. The winning device is the local device LID code of ‘1001’ and HID code of ‘100’. This is because the LID code of ‘1001’ is the lowest among one other local Target device code and its HID code is ‘100’.

Example 3:

There are total of 3 devices (2 local Target devices and 1 Hub device) that are requesting an interrupt. These 3 devices are shown in the RED color text. The devices that are in Black color text are not requesting an interrupt. The winning device is the Hub device on DIMM0 with LID code of ‘1010’ and HID code of ‘000’. This is because LID code ‘1010’ is lower than two other local Target device code and its HID code is ‘000’.

Example 4:

There are total of 2 devices (2 local Target devices) that are requesting an interrupt. These 2 devices are shown in RED color text. The devices that are in Black color text are not requesting an interrupt. This example is unique as two identical Target devices across two different DIMM devices are requesting an interrupt. The winning device is the local Target device on DIMM 0 with LID code of ‘0010’ and DIMM 0 HID code of ‘000’. This is because DIMM0 HID code ‘000’ is lower than DIMM2 HID code of ‘010’. See ***Interrupt Arbitration - Among Local Target Devices behind Different SPD5 Hub Devices*** section.

Table 82. Interrupt Arbitration - Among Local Target and SPD5 Hub Devices

EXAMPLE 1			EXAMPLE 2			EXAMPLE 3			EXAMPLE 4		
TARGET LID CODE	HUB HID CODE	WINNING DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE
0010 0110 1001 1011	000		0010 0110 1001 1011	000		0010 0110 1001 1011	000	1010 000	0010 0110 1001 1011	000	0010 000
0010 0110 1001 1011	001		0010 0110 1001 1011	001		0010 0110 1001 1011	001		0010 0110 1001 1011	001	
0010 0110 1001 1011	010		0010 0110 1001 1011	010		0010 0110 1001 1011	010		0010 0110 1001 1011	010	
0010 0110 1001 1011	011		0010 0110 1001 1011	011		0010 0110 1001 1011	011		0010 0110 1001 1011	011	
0010 0110 1001 1011	100		0010 0110 1001 1011	100	1001 100	0010 0110 1001 1011	100		0010 0110 1001 1011	100	
0010 0110 1001 1011	101		0010 0110 1001 1011	101		0010 0110 1001 1011	101		0010 0110 1001 1011	101	
0010 0110 1001 1011	110		0010 0110 1001 1011	110		0010 0110 1001 1011	110		0010 0110 1001 1011	110	
0010 0110 1001 1011	111	0010 111	0010 0110 1001 1011	111		0010 0110 1001 1011	111		0010 0110 1001 1011	111	

IN BAND INTERRUPT (IBI) (continued)

Interrupt Arbitration - Between Host and Any SPD5 Hub or Any Local Target Devices behind Hub

When the bus is idle for t_{AVAL} time, any SPD5 Hub device or any local device behind the Hub can request an interrupt by pulling the SDA bus low.

In an uncommon but possible scenario would be that at the exact same time as when the SPD5 Hub or local Target devices are requesting an interrupt, the Host is starting an operation to the Hub or local Target devices. When this happens, Host also gets involved in the arbitration process along with the Hub or the local Target devices. During the arbitration phase, there will be always only one winning device and it could be either the Hub or the local Target device or the Host.

If the Host wins during the arbitration phase, it continues with normal operation. The losing Hub or local Target device waits for next opportunity to send an interrupt.

If the Host loses during the arbitration phase, it must let go of the bus. When the Host loses during the arbitration, the Host must let the Hub or local Target device finish sending its 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the Host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning SDP5 Hub or local Target device. After the IBI payload, the Host issues Stop operation.
- Host sends an NACK followed by Stop operation.

In a rare but still possible scenario would be that at the exact same time as when the Hub or local Target device is requesting an interrupt, the Host is starting an operation to that same exact Hub or local Target device. When this happens, neither Host nor the Hub or local Target device knows it is a winner until the 8th bit and Host always wins. This is because, the Hub or local Target device sends R = 1 (8th bit) during the interrupt. The Host sets W=0 (8th bit) during the operation. As a result, the Host wins and the Hub or local Target device must let go of the bus and wait for the next opportunity to send an interrupt. This is shown as example 3 in Table 83.

Table 83 shows three examples. In each example, the Target LID code column represents local Target device behind Hub which has HID code value of '111'; the Hub HID code column represents the SPD5 Hub device which has LID code of '1010' followed by its own unique HID code; the winning device column represents the final winner among all devices (either Host or SPD5 Hub device or local Target devices) during the arbitration phase.

Example 1:

There are total of 5 devices (1 Hub device and 4 local Target devices) are requesting an interrupt at exactly same time as when the Host is starting an operation to Hub device on DIMM 3 (1010 011). The winning device is local Target device '0010 111' because it has the lower 4-bit LID code.

Example 2:

There are total of 4 devices (2 Hub devices 2 local Target devices) are requesting an interrupt at exactly same time as when the Host is requesting an operation to the local Target device on DIMM5 (0110 101). The Host is the winner because its intended Target device has the lower 4-bit LID code than devices that are requesting an interrupt.

Example 3:

There is one Hub device on DIMM 2 is requesting an interrupt at exactly the same time as when Host is requesting an operation to the same exact Hub device on DIMM2. In this case, the Host is the winner because the 8-bit will be driven low by the Host (W = 0) while the Hub device drives it high (R = 1) during the interrupt.

In an extreme rare but still possible scenario would be that at the exact same time as when the Hub or local Target device is requesting an interrupt, the Host is requesting a read operation with default read address pointer mode to the same exact Hub or local Target device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the Hub or local Target device sends R = 1 (8th bit) during the interrupt and Host also sends R = 1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the Hub or the local Target devices, are waiting for other device to ACK. In this case, no devices will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeated Start. When it repeats the read request with Repeat Start, the Hub or local Target device does not send an interrupt because of Repeated Start.

IN BAND INTERRUPT (IBI) (continued)

Table 83. Interrupt Arbitration - Between Host and Local Target and SPD5 Hub Devices

EXAMPLE 1				EXAMPLE 2				EXAMPLE 3			
HOST TARGET DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE	HOST TARGET DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE	HOST TARGET DEVICE	TARGET LID CODE	HUB HID CODE	WINNING DEVICE
1010 011	0010 0110 1001 1011	000		0110 101	0010 0110 1001 1011	000		1010 010	0010 0110 1001 1011	000	
	0010 0110 1001 1011	001			0010 0110 1001 1011	001			0010 0110 1001 1011	001	
	0010 0110 1001 1011	010			0010 0110 1001 1011	010			0010 0110 1001 1011	010	Host operation to 1010 010
	0010 0110 1001 1011	011			0010 0110 1001 1011	011			0010 0110 1001 1011	011	
	0010 0110 1001 1011	100			0010 0110 1001 1011	100			0010 0110 1001 1011	100	
	0010 0110 1001 1011	101			0010 0110 1001 1011	101	Host operation to 0110 101		0010 0110 1001 1011	101	
	0010 0110 1001 1011	110			0010 0110 1001 1011	110			0010 0110 1001 1011	110	
	0010 0110 1001 1011	111	0011 111		0010 0110 1001 1011	111			0010 0110 1001 1011	111	

Interrupt Arbitration; SETHID CCC is Issued by Host

The interrupt arbitration process works similar way as defined in ***Interrupt Arbitration; SETHID CCC is Not Issued by Host*** section but with a simplification. It is assumed that in this case, all Target devices behind Hub across all DIMMs on I3C Basic bus have a unique 7-bit device select code. Further, it assumes that all devices on a DIMM have the same 3-bit HID code.

The SPD5 Hub device forwards the 4-bit LID code and 3-bit HID code one digit at a time that it receives from the local Target devices to the Host. The SPD5 Hub device's own receiver will see the same input and it forwards it back to the local device interface.

Interrupt Arbitration - Between SPD5 Hub Device and Local Target Devices behind Hub

On an any given DIMM, the arbitration is always won by the device that has the lowest 4-bit LID code since all devices on the DIMM has same 3-bit HID code.

Interrupt Arbitration - Between all SPD5 Hub Devices and all Local Target Devices behind Hub

Across multiple DIMMs, the arbitration is always won by the device that has the lowest 7-bit address (4-bit LID + 3-bit HID).

IN BAND INTERRUPT (IBI) (continued)

Interrupt Arbitration - Between Host and All Devices

In an uncommon but possible scenario would be that at the exact same time as when the Target device is requesting an interrupt, the Host is starting an operation to the Target device. When this happens, Host also gets involved in the arbitration process along with the Target devices. During the arbitration phase, there will be always only one winning device and it could be either the Host or the Target device.

If the Host wins during the arbitration phase, it continues with normal operation. The losing Target device waits for next opportunity to send an interrupt.

If the Host loses during the arbitration phase, it must let go of the bus. When Host loses during the arbitration, the Host must let the Target device finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the Host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Target device. After the IBI payload, the Host issues Stop operation.
- Host sends an NACK followed by Stop operation.

In a rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the Host is starting an operation to that same SPD5 Hub device. When this happens, neither Host or nor the SPD5 Hub device knows it is a winner until the 8th bit and Host always wins. This is because, the SPD5 hub device sends R = 1 (8th bit) during the interrupt. The Host sets W = 0 (8th bit) during the operation. As a result, the Host wins and the SPD5 Hub device must let go of the bus and wait for the next opportunity to send an interrupt.

In an extreme rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the Host is requesting a read operation with default read address pointer mode to the SPD5 Hub device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the SPD5 Hub device sends R = 1 (8th bit) during the interrupt and Host also sends R = 1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the SPD5 Hub devices, are waiting for other device to ACK. In this case, no devices will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeat Start. When it repeats the read request with Repeat Start, the SPD5 Hub device does not send an interrupt because of Repeat Start.

Clearing Device Status and IBI Status Registers

The SPD5 Hub device provides the IBI status in MR48[7] by setting it to '1'. The SPD5 Hub device clears the IBI status register MR48[7] to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits[3:0] to '0000'. Once IBI status register is cleared, the SPD5 Hub does not request for an IBI again unless another event occurs.

The SPD5 Hub device provides the device status in MR51 and MR52 registers. The status information in MR51 and MR52 are latched and remains set even after the SPD5 Hub device sends IBI payload and clears the IBI status register MR48[7] to '0'. The Host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global Clear command.

After Host issues Clear command, if the condition is no longer present, the SPD5 Hub device clears the appropriate status register, clears the IBI status register to '0' and Pending Interrupt Bits[3:0] to '0000' even if the SPD5 Hub device has not sent the IBI. After Host issues Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits[3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

ERROR CHECK FUNCTION

Packet Error Check (PEC) Function

In I^2C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The SPD5 Hub device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC. The PEC is a CRC-8 value calculated on all the message bytes except for Start, Repeat Start, Stop conditions or 'T' bits, ACK and NACK and IBI header (7'h7E followed by W = 0) bits.

The polynomial for CRC-8 calculations is:

$$C(X) = X^8 + X^2 + X^1 + 1$$

The seed value for PEC function is all zero.

When Host calculates PEC for SPD5 Hub device, it includes LID and HID bits followed by R/W bit.

Parity Error Check Function

In I^2C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when SPD5 Hub device is put in I3C Basic mode, parity function is automatically enabled. The Host can disable the function after it is enabled. Host can only disable the parity function with DEVCTRL CCC (RegMod = '0'). When parity function is disabled, the SPD5 Hub device simply ignores the 'T' bit information from the Host. The Host may actually choose to compute the parity and send that information during 'T' bit or simply drive static low or high in 'T' bit.

The SPD5 Hub device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'.

If even number of bits in the byte are '1', the parity bit value is '1'. The Host computes the parity and sends it during 'T' bit.

Packet Error Check and Parity Error Handling

There are two types of error checking done by the SPD5 Hub device: parity error checking and packet error checking. By default, the parity error checking is always enabled and packet error checking is disabled when the SPD5 Hub device is put in I3C Basic mode. The Host may enable the packet error checking at any time. The parity error is calculated for each byte. The Host sends parity error information in 'T' bit.

I3C Basic defines TE0, TE1, TE2, TE3, TE4, TE5, TE6 error detection for Target devices. Only TE1 and TE2 error detection is supported by the SPD5 Hub for parity checking. All other errors are not supported and not applicable.

Write Command Data Packet Error Handling - PEC Disabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host as shown in Table 22.

Write command - if no parity error:

The SPD5 Hub device executes the command.

Write command - if parity error:

- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards all subsequent bytes in that packet until the Stop operation. The SPD5 Hub device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the SPD5 Hub device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The SPD5 Hub device sets the MR52[0], MR48[7] and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits[3:0] to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

ERROR CHECK FUNCTION (continued)

Read Command Data Packet Error Handling - PEC Disabled

The SPD5 Hub device checks for parity error for each byte in a packet except for the device select code byte that it receives from the Host prior to Repeat Start as shown in Table 26.

The SPD5 Hub device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes that SPD5 Hub device sends. The SPD5 Hub device sends Continuous (‘1’) or Stop (‘0’) information during ‘T’ bit.

Read Command - If no parity error:

- The SPD5 Hub sends ACK back to the Host when Host performs Repeat Start operation.
- The SPD5 Hub device executes the command and sends the data as shown in Table 26.
- Read Command - If parity error:
- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards second byte in that packet if the parity error occurred in first byte. The SPD5 Hub device may or may not check the parity for second byte in that packet.
- The SPD5 Hub sends NACK back to the Host when Host performs a Repeat Start operation. This is shown in the RED color cell in Table 26. The NACK represents either a parity error in one of the two bytes or that SPD5 Hub is not able to start the read operation. The Host may re-try Repeat Start again. The Host may do the Repeat Start as many times as it may desire. If the SPD5 Hub device NACKs due to parity error in a previous byte from the Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The SPD5 Hub does not send the data shown in Table 26 and instead expects Host to perform Stop operation.
- The SPD5 Hub device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send an in band interrupt if IBI is enabled.

Write Command Data Packet Error Handling - PEC Enabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host as shown in Table 23. Further, the SPD5 Hub device checks for the packet error for the entire packet (from Start condition until last byte of Data) that receives from the Host as shown in Table 23.

Write command - if no parity error:

- The SPD5 Hub device waits for the entire packet. If no error in packet, the SPD5 Hub device executes the command. If there is an error in the packet, the SPD5 Hub device discards the entire packet and does not execute that packet and waits for Stop, sets the MR52[1] and MR48[7] to ‘1’ and PEC_Err in GETSTATUS CCC to ‘1’ and updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send in band interrupt if IBI is enabled.

Write command - if parity error:

- The SPD5 Hub device discards that byte and the entire packet until Stop operation.
- The SPD5 Hub device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send in band interrupt if IBI is enabled.
- The SPD5 Hub device may or may not check the error for the packet. If the SPD5 Hub device checks for the packet error, likely it will detect an error in the packet and the device may also set MR52[1] and PEC_Err in GETSTATUS CCC to ‘1’ as well.

Read Command Data Packet Error Handling - PEC Enabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the Host prior to Repeat Start as shown in Table 27.

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ERROR CHECK FUNCTION (continued)

The SPD5 Hub device does not compute the parity when it sends the data to the Host. It does not check for parity error for the bytes shown in Table 27. The SPD5 Hub device sends Continuous (‘1’) or Stop (‘0’) information during ‘T’ bit when SPD5 Hub device is sending the read data.

The SPD5 Hub device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from first device select code followed by the address offset and CMD byte).

The SPD5 Hub device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data SPD5 Hub device transmits back to Host)

Read command - If no parity error and no PEC error:

- The SPD5 Hub sends ACK back to the Host when Host performs a Repeat Start operation.
- The SPD5 Hub device executes the command and sends the data as shown in Table 27.
- The SPD5 Hub computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in Table 27.
- Read command - if parity error or PEC error:
- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards second byte in that packet if a parity error occurred in first byte. The SPD5
- Hub device may or may not check parity for the second byte in that packet.
- The SPD5 Hub device discards the packet if there is a PEC error.
- The SPD5 Hub sends NACK back to the host when Host performs Repeat Start operation. This is shown in the RED color cell in Table 27. The NACK represents either PEC error or a parity error in one of the three bytes or that SPD5 Hub is not able to start the read operation. The Host may re-try Repeat Start again. The Host may do the Repeat Start as many times it may desire. The PEC calculation by SPD5 Hub device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the SPD5 Hub device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the SPD5 Hub device NACKs due to PEC error or a parity error in previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The SPD5 Hub does not send any data shown in Table 27 and instead expects Host to perform Stop operation.
- The SPD5 Hub device sets MR52[0] and MR48[7] and P_Err in GETSTATUS CCC to ‘1’ for parity error and MR52[1] and MR48[7] and PEC_Err in GETSTATUS CCC to ‘1’ for PEC error. Further, the SPD5 Hub updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send an in band interrupt if IBI is enabled.

CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled in the same way as described for normal Read/Write operations.

Error Reporting

All error conditions including PEC error check and parity error check detected by the SPD5 Hub devices are captured in MR51 and MR52 registers.

There are three different possible ways error information can be communicated to the Host.

The Host makes the read request to MR51 and MR52 registers.

The Host starts any transaction with 7’h7E IBI header (only applicable in I3C mode).

The SPD5 Hub device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time (only applicable in I3C Basic mode).

SPD5 HUB DEVICE - WRITE AND READ

In both I^2C and I3C mode, any read or write access to SPD5 Hub NVM memory must be followed by Stop operation (i.e. not Repeat Start) before launching new access to SPD5 Hub volatile memory registers. Conversely, any read or write access to SPD5 Hub volatile memory registers must be followed by Stop operation (i.e. not Repeat Start) before launching new access to SPD5 Hub NVM memory.

Command Truth Table

The command truth table as shown in Table 84 only applies in I3C Basic mode with PEC enabled. In I^2C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 84. For I3C Basic Mode Only w/PEC Enabled - Command Truth Table

SPD5 COMMAND	COMMAND NAME	COMMAND CODE	RW	MEMREG	BLOCK ADDRESS	ADDRESS
		2^{ND} BYTE BITS [7:5]	2^{ND} BYTE BIT [4]	1^{ST} BYTE BIT [7]	2^{ND} BYTE BITS [3:0] 1^{ST} BYTE BITS [6]	1^{ST} BYTE BITS [5:0]
Write 1 Byte to Register	W1R	000	0	0	V	V
Read 1 Byte from Register	R1R		1	0	V	V
Write 1 Byte to NVM	W1M		0	1	V	V
Read 1 Byte from NVM	R1M		1	1	V	V
Write 2 Byte to Register	W2R	001	0	0	V	V
Read 2 Byte from Register	R2R		1	0	V	V
Write 2 Byte to NVM	W2M		0	1	V	V
Read 2 Byte from NVM	R2M		1	1	V	V
Write 4 Byte to Register	W8R	010	0	0	V	V
Read 4 Byte from Register	R8R		1	0	V	V
Write 4 Byte to NVM	W8M		0	1	V	V
Read 4 Byte from NVM	R8M		1	1	V	V
Write 16 Byte to Register	W16R	011	0	0	V	V
Read 16 Byte from Register	R16R		1	0	V	V
Write 16 Byte to NVM	W16M		0	1	V	V
Read 16 Byte from NVM	R16M		1	1	V	V
Reserved	RSVD	011 to 111	RSVD	RSVD	RSVD	RSVD

SPD5 HUB DEVICE - WRITE AND READ (continued)

Write and Read Access - NVM Memory

For I^2C mode and I3C mode with PEC disabled, the Write access to NVM memory is done within 16 byte boundary in a block. Once the last address within 16 byte boundary in a block is reached, the device stops the operation. The write operation to remaining addresses is not executed by the SPD5 Hub device. The SPD5 Hub device does not loop to first address within the 16 byte boundary in that block. The SPD5 Hub device does not set any register to inform this to the Host and does not generate any interrupt to the Host.

For I3C mode with PEC enabled, if for a given Write access (either W2M, W4M, W16M) to NVM memory reaches the last address within the 16 byte boundary in a block, (i.e. Byte 15, Byte 31, Byte 47, Byte 63), the device stops the operation. The write operation to remaining addresses is not executed by the SPD5 Hub device. The SPD5 Hub device does not loop to first address within the 16 byte boundary in that block. The SPD5 Hub device does not set any register to inform this to the Host and does not generate any interrupt to the Host.

Unlike Write access to NVM memory, any Read access to NVM memory does not impose 16 byte boundary or block boundary. The Read access to NVM memory is treated as continuous address space even if it crosses 16 byte boundary or block boundary in I^2C mode or I3C Basic mode (w/ or w/o PEC enabled). The last byte for NVM memory is 1024^{th} byte and when the address pointer reaches to the last byte, the SPD5 Hub device does not return any data. In I^2C mode and I3C Basic mode with PEC disabled, the Host must do the Stop operation.

Write and Read Access - Register Memory

There is no concept of “Block Address”. The “Block Address” is treated is simply as upper address bit when MemReg = ‘0’ by the SPD5 Hub device.

For I^2C mode and I3C Basic mode with PEC disabled or PEC enabled, any access to read or write to register memory is continuous address space even if it appears crossing 16 byte boundary or “Block Address” boundary. The last byte is MR255 and when the address pointer reaches to MR255, the SPD5 Hub device does not return any data.

In I^2C mode and I3C Basic mode with PEC disabled, the Host must do the Stop operation.

Write Protection of Non-Volatile Memory

Normal Run Time Operation

In Normal Run Time Operation mode, by HSA Pin tied to GND via a resistor value, the SPD5 Hub device offers a write protection for its NVM memory. The MR12[7:0] and MR13[7:0] register contains a bit map for write protection status of each 64 byte block of NVM memory.

The MR12 7:0] and MR13[7:0] registers can be written to ‘1’ at any time. When any bit in MR12 or MR13 is set to ‘1’, further writes to that corresponding block of NVM are ignored and MR52[6] bit is set to ‘1’.

Once any bit is written to ‘1’ in MR12 and MR13, clearing that bit in normal run time mode is not allowed. Any attempt to clear the bit in MR12 and MR13 is ignored and MR52[5] bit is set to ‘1’.

Offline Tester Operation

In Offline Tester Operation mode, by HSA Pin tied directly to GND with no resistor value, the SPD5 Hub device allows to clear any bit in MR12 and MR13 registers.

Once cleared, the SPD5 Hub device allows to modify the corresponding block of NVM memory.

Suggested Steps to Program SPD5 Hub Devices

The recommended steps to program the SPD Hub devices are:

1. Connect HSA Pin directly to GND (without a resistor).
2. Power up the device. The device senses HSA pin. It sets MR48[2] = ‘1’ and enables write protection override.
3. Program MR12 and MR13 to enable desired NVM blocks to be written.
4. Program desired NVM blocks.
5. Program MR12 and MR13 to set the write protection as desired.

REGISTERS

Register Attribute Definition

All volatile registers have Base Attributes as defined in Table 85. Some register attributes are further modified with Attribute Modifiers, as defined in Table 86.

The volatile register space has a continuous address. Unlike non-volatile memory in SPD5 Hub device, there is no concept of "Block" memory in volatile register space. When writing to and reading from volatile register space (i.e. MemReg = 0), the "Block Address bits" are treated simply as Upper address bits.

Table 85. Register Base Attributes

ATTRIBUTE	ABBREVIATION	DESCRIPTION
Read Only	R	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by software.
Write Only	W	This bit can only be written by software.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by software. The bit will return '0' when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 86. Register Attribute Modifier

ATTRIBUTE	ABBREVIATION	DESCRIPTION
Write 1 Only	1O	This bit can only be set (i.e. write '1') but not reset (i.e. write '0')
Persistent	E	Persistent.

REGISTERS (continued)

Table 87. Register Map

REGISTER NAME	REGISTER ADDRESS (HEX)	ATTRIBUTE	DESCRIPTION
MR0	0x00	ROE	Device Type; Most Significant Byte
MR1	0x01	ROE	Device Type; Least Significant Byte
MR2	0x02	ROE	Device Revision
MR3	0x03	ROE	Vendor ID Byte 0
MR4	0x04	ROE	Vendor ID Byte 1
MR5	0x05	ROE	Device Capability
MR6	0x06	ROE	Device Write Recovery Time Capability
MR7 - MR10	0x07 - 0x0A	RV	Reserved
MR11	0x0B	RW	I^2C Legacy Mode Device Configuration
MR12	0x0C	RWE	Write Protection For NVM Blocks [7:0]
MR13	0x0D	RWE	Write Protection for NVM Blocks [15:8]
MR14	0x0E	RWE	Device Configuration - Host and Local Interface IO; DO NOT USE [4:0]
MR15	0x0F	RV	DO NOT USE
MR16 - MR17	0x10 - 0x11	RV	Reserved
MR18	0x12	RO, RW	Device Configuration
MR19	0x13	1O	Clear Register MR51 Temperature Status Command
MR20	0x14	1O	Clear Register MR52 Error Status Command
MR21 - MR25	0x15 - 0x19	RV	Reserved
MR26	0x1A	RW	TS Configuration
MR27	0x1B	1O, RO, RW	Interrupt Configurations
MR28	0x1C	RW	TS Temperature High Limit Configuration - Low Byte
MR29	0x1D	RW	TS Temperature High Limit Configuration - High Byte
MR30	0x1E	RW	TS Temperature Low Limit Configuration - Low Byte
MR31	0x1F	RW	TS Temperature Low Limit Configuration - High Byte
MR32	0x20	RW	TS Critical Temperature High Limit Configuration – Low Byte
MR33	0x21	RW	TS Critical Temperature High Limit Configuration – High Byte
MR34	0x22	RW	TS Critical Temperature Low Limit Configuration – Low Byte
MR35	0x23	RW	TS Critical Temperature Low Limit Configuration – High Byte
MR36 - MR47	0x24 - 0x2F	RV	Reserved for Device Configuration Type of Registers
MR48	0x30	RO	Device Status
MR49	0x31	RO	TS Current Sensed Temperature - Low Byte
MR50	0x32	RO	TS Current Sensed Temperature - High Byte
MR51	0x33	RO	TS Temperature Status
MR52	0x34	RO	Hub, Thermal and NVM Error Status
MR53 - MR127	0x35 - 0x7F	RV	Reserved
MR128 - MR255	0x80 - 0xFF	RV	Reserved for Vendor Specific Registers

REGISTERS (continued)

Thermal Sensor Registers Read Out Mechanism

All thermal registers are 16-bit quantities stored in two consecutive registers; low byte first and then high byte. Five bits are reserved for future use. Reserved bits are Read only bits and must be set to '0' when Host writes to low and high bytes. The device returns '0' in reserved bits when Host reads from the low and high bytes. Remaining 11 bits in these paired registers form a signed value of multiples of 0.25 ranging from -256.00 to + 255.75. Units for all thermal registers are ℃.

The format of each pair of thermal registers is shown in Table 88 below.

Table 88.Thermal Register - Low Byte and High Byte

REGISTER		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MRX	Low Byte	8	4	2	1	0.5	0.25	Reserved	Reserved
MRX + 1	High Byte	Reserved	Reserved	Reserved	Sign	128	64	32	16

Bit 'Sign' decides whether the readout temperature is positive or negative. The examples (reserved bits in grey, sign bit highlighted in blue) is shown in Table 89 below.

Table 89. Thermal Register Examples

HIGH BYTE	LOW BYTE	VALUE	UNITS
0000 0101	1111 0000	+95.00	℃
0000 0101	0101 0000	+85.00	℃
0000 0100	1011 0000	+75.00	℃
0000 0000	0001 0000	+1.00	℃
0000 0000	0000 1100	+0.75	℃
0000 0000	0000 1000	+0.50	℃
0000 0000	0000 0100	+0.25	℃
0000 0000	0000 0000	0.00	℃
0001 1111	1111 1100	-0.25	℃
0001 1111	1111 1000	-0.50	℃
0001 1111	1111 0100	-0.75	℃
0001 1111	1111 0000	-1.00	℃
0001 1101	1000 0000	-40.00	℃

REGISTER DESCRIPTION

REG0x00: MR0 Register: Device Type; Most Significant Byte (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	MSB_DEV_TYPE[7:0]	ROE	0x51	0x51: Temperature Sensor without Serial Number

1. The code in this register is used in conjunction with any device type in MR1 register.

REG0x01: MR1 Register: Device Type; Least Significant Byte (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	LSB_DEV_TYPE[7:0]	ROE	0x18	Device Type 0x18: with Temperature Sensor; SPD5 Hub Device

1. The code in this register is used in conjunction with any device type in MR0 register.

REG0x02: MR2 Register: Device Revision

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:6]	Reserved	RV	0	Reserved
D[5:4]	DEV_REV_MAJOR[1:0]	ROE	00	Major Revision 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
D[3:1]	DEV_REV_MINOR[2:0]	ROE	011	Minor Revision 000 = Revision 0 001 = Revision 1 010 = Revision 2 … 111 = Revision 7
D[0]	Reserved	RV	0	Reserved

REG0x03: MR3 Register: Vendor ID Byte 0

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	VENDOR_ID_BYTE0[7:0]	ROE	0x0E	Vendor ID Byte 0

REG0x04: MR4 Register: Vendor ID Byte 1

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	VENDOR_ID_BYTE1[7:0]	ROE	0x8F	Vendor ID Byte 1

REG0x05: MR5 Register: Device Capability

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:2]	Reserved	RV	0	Reserved
D[1]	TS_SUPPORT	ROE	1	Internal Temperature Sensor Support 0 = Does not support Temperature Sensor 1 = Supports Temperature Sensor
D[0]	HUB_SUPPORT	ROE	1	Hub Function Support 0 = Does not support Hub function 1 = Supports Hub function

REGISTER DESCRIPTION (continued)

REG0x06: MR6 Register: Write Recovery Time

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	WR_REC_UNIT[3:0]	ROE	0101	Write Recovery Unit 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 50 1100 = 100 1101 = 200 1110 = 500 1111 = Reserved
D[3:2]	Reserved	RV	0	Reserved
D[1:0]	WR_REC_UNIT_TIME[1:0]	ROE	10	Write Recovery Time Unit 00 = ns 01 = μs 10 = ms 11 = Reserved

REG0x0B: MR11 Register: I^2C Legacy Mode Device Configuration

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0	Reserved
D[3]	I^2C_LEGACY_MODE_ADDR	RW	0	SPD5 Hub Device - I^2C Legacy Mode Addressing 0 = 1 Byte Addressing for SPD5 Hub Device Memory 1 = 2 Bytes Addressing for SPD5 Hub Device Memory
D[2:0]	I^2C_LEGACY_MODE_ADDR_POINTER	RW	000	MR11[2:0]: I^2C_LEGACY_MODE_ADDR_POINTER SPD5 Device - Non Volatile Memory Address Page Pointer in I^2C Legacy Mode (1) (2) (3) 000 = Page 0 (0x00 to 0x7F) 001 = Page 1 (0x80 to 0xFF) 010 = Page 2 (0x100 to 0x17F) 011 = Page 3 (0x180 to 0x1FF) 100 = Page 4 (0x200 to 0x27F) 101 = Page 5 (0x280 to 0x2FF) 110 = Page 6 (0x300 to 0x37F) 111 = Page 7 (0x380 to 0x3FF)

1. This register is only applicable if bit [3] = '0' and MR18[5] = '0'. The SPD5 Hub device does not incur any delay to switch from one page to another page.
2. This register only applies to non-volatile memory (1024 Bytes) access of SPD5 Hub device. For volatile memory access, this register must be programmed to '000'.
3. See ***Write and Read Access - NVM Memory*** section for the NVM Write and Read operation when device reaches the last byte of the 16 byte block boundary.

REGISTER DESCRIPTION (continued)

REG0x0C: MR12 Register: NVM Protection Configuration for Blocks [7:0] (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	WP_BLK_7	RWE	-	Write Protect - Block 7 0 = Not Protected 1 = Protected
D[6]	WP_BLK_6	RWE	-	Write Protect - Block 6 0 = Not Protected 1 = Protected
D[5]	WP_BLK_5	RWE	-	Write Protect - Block 5 0 = Not Protected 1 = Protected
D[4]	WP_BLK_4	RWE	-	Write Protect - Block 4 0 = Not Protected 1 = Protected
D[3]	WP_BLK_3	RWE	-	Write Protect - Block 3 0 = Not Protected 1 = Protected
D[2]	WP_BLK_2	RWE	-	Write Protect - Block 2 0 = Not Protected 1 = Protected
D[1]	WP_BLK_1	RWE	-	Write Protect - Block 1 0 = Not Protected 1 = Protected
D[0]	WP_BLK_0	RWE	-	Write Protect - Block 0 0 = Not Protected 1 = Protected

1. Once any register bit is set to '1', it can only be cleared when the SPD5 Hub device is in offline tester mode of operation.
2. The write (or update) transaction to this register must be followed by Stop operation to allow SPD5 Hub device to update the setting.

REG0x0D: MR13 Register: NVM Protection Configuration for Blocks [15:8] (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	WP_BLK_15	RWE	-	Write Protect - Block 15 0 = Not Protected 1 = Protected
D[6]	WP_BLK_14	RWE	-	Write Protect - Block 14 0 = Not Protected 1 = Protected
D[5]	WP_BLK_13	RWE	-	Write Protect - Block 13 0 = Not Protected 1 = Protected
D[4]	WP_BLK_12	RWE	-	Write Protect - Block 12 0 = Not Protected 1 = Protected
D[3]	WP_BLK_11	RWE	-	Write Protect – Block 11 0 = Not Protected 1 = Protected
D[2]	WP_BLK_10	RWE	-	Write Protect - Block 10 0 = Not Protected 1 = Protected
D[1]	WP_BLK_9	RWE	-	Write Protect - Block 9 0 = Not Protected 1 = Protected
D[0]	WP_BLK_8	RWE	-	Write Protect - Block 8 0 = Not Protected 1 = Protected

1. Once any register bit is set to '1', it can only be cleared when the SPD5 Hub device is in offline tester mode of operation.
2. The write (or update) transaction to this register must be followed by Stop operation to allow SPD5 Hub device to update the setting.

REGISTER DESCRIPTION (continued)

REG0x0E: MR14 Register: Device Configuration - Local Interface (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:6]	Reserved	RV	0	Reserved
D[5]	LOCAL_INF_PULLUP_CONF	RWE	0	Local Interface – Pull-Up Resistor Configuration 0 = Internal (on die) Pull-up Resistor (3) 1 = External (board) Pull-up Resistor
D[4:0]	DO NOT USE	RV	0	DO NOT USE

1. DIMM Vendor configures this register during assembly based on the DIMM design. After SPD Hub device is powered up, the Host can alter the setting through this register.
2. The write (or update) transaction to this register must be followed by Stop operation to allow SPD5 Hub device to update the setting.
3. Typical value of on die pull-up resistor is 1KΩ. The minimum and maximum on die pull-up resistor value is 750Ω and 1.5kΩ respectively.

REG0x0F: MR15 Register: DO NOT USE

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	DO NOT USE	RV	0	DO NOT USE

REG0x12: MR18 Register: Device Configuration (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	PEC_EN	RO	0	PEC Enable (2) (3) 0 = Disable 1 = Enable
D[6]	PAR_DIS	RO	0	Parity (T bit) Disable (3) (4) 0 = Enable 1 = Disable
D[5]	INF_SEL	RO	0	Interface Selection 0 = I^2C Protocol (Max speed of 1 MHz) 1 = I3C Basic Protocol (5)
D[4]	DEF_RD_ADDR_POINT_EN	RW	0	Default Read Address Pointer Enable 0 = Disable Default Read Address Pointer (Address pointer is set by the Host) (6) 1 = Enable Default Read Address Pointer; Address selected by register bits [3:2]
D[3:2]	DEF_RD_ADDR_POINT_Start[1:0]	RW	00	Default Read Pointer Starting Address (7) 00 = MR49 01 = Reserved 10 = Reserved 11 = Reserved
D[1]	DEF_RD_ADDR_POINT_BL	RW	0	Burst Length for Read Pointer Address for PEC Calculation (8) 0 = 2 Bytes 1 = 4 Bytes
D[0]	Reserved	RV	0	Reserved

1. The write (or update) transaction to this register must be followed by Stop operation to allow the SPD5 Hub device to update the setting.
2. This register is only applicable if MR18[5] = '1'.
3. This register is updated when RSTDAA CCC is registered by SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in Bus Reset section.
4. This register is only applicable if MR18[5] = '1'. When Parity function is disabled, the SPD5 Hub device simply ignores the 'T' bit information from the Host. The Host may actually choose to compute the parity and send that information in 'T' bit or simply drive static low or high in 'T' bit.
5. This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in Bus Reset section. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I^2C mode or I3C Basic mode of operation. When this register is updated, it takes in effect when there is a next Start operation (i.e. after Stop operation).
6. The setting in register MR18[3:1] is don't care.
7. This register is only applicable if MR18[4] = '1'.
8. This register is only applicable if MR18[7, 4] = '11'.

REGISTER DESCRIPTION (continued)

REG0x13: MR19 Register: Clear Register Command (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0	Reserved
D[3]	CLR_TS_CRIT_LOW	1O	0	Clear Temperature Sensor Critical Low Status 1 = Clear MR51[3] Register
D[2]	CLR_TS_CRIT_HIGH	1O	0	Clear Temperature Sensor Critical High Status 1 = Clear MR51[2] Register
D[1]	CLR_TS_LOW	1O	0	Clear Temperature Sensor Low Status 1 = Clear MR51[1] Register
D[0]	CLR_TS_HIGH	1O	0	Clear Temperature Sensor High Status 1 = Clear MR51[0] Register

1. This entire register is self-clearing register after corresponding register is cleared.

REG0x14: MR20 Register: Clear Register Command (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	CLR_SPD_BUSY_ERROR	1O	0	Clear Write or Read Attempt while SPD Device Busy Error Status 1 = Clear MR52[7] Register
D[6]	CLR_WR_NVM_BLK_ERROR	1O	0	Clear Write Attempt to Protected NVM Block Error Status 1 = Clear MR52[6] Register
D[5]	CLR_WR_NVM_PRO_REG_ERROR	1O	0	Clear Write Attempt to NVM Protection Register Error Status 1 = Clear MR52[5] Register
D[4:3]	Reserved	RV	0	Reserved
D[1]	CLR_PEC_ERROR	1O	0	Clear Packet Error Status 1 = Clear MR52[1] Register
D[0]	CLR_PAR_ERROR	1O	0	Clear Parity Error Status 1 = Clear MR52[0] Register

1. This entire register is self-clearing register after corresponding register is cleared.

REG0x1A: MR26 Register: Thermal Sensor Configuration

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:1]	Reserved	RV	0	Reserved
D[0]	DIS_TS	RW	0	Disable Temperature Sensor (1) (2) 0 = Enable thermal sensor 1 = Disable thermal sensor

1. This register is only applicable if MR1[7:0] programmed value is 0x18.
2. If this bit is set to '1' and then reset to '0', the Host must wait minimum of t_{INIT} before accessing samples on the thermal sensor.

REGISTER DESCRIPTION (continued)

REG0x1B: MR27 Register: Interrupt Configuration

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	CLR_GLOBAL	1O	0	Global Clear Event Status and In Band Interrupt Status1,2 1 = Clear MR48[7], MR51[3:0] and MR52[7:5, 1:0] Register
D[6:5]	Reserved	RV	0	Reserved
D[4]	IBI_ERROR_EN	RO	0	In Band Error Interrupt Enable for MR52 Error Log3 0 = Disable; Errors logged in MR52[7:5, 1:0] registers do not generate an IBI to Host 1 = Enable; Errors logged in MR52[7:5, 1:0] registers generates an IBI to Host
D[3]	IBI_TS_CRIT_LOW_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Critical Low 0 = Disable; MR51[3] = '1' does not generate an IBI to Host 1 = Enable; MR51[3] = '1' and MR27[4] = '1' generates an IBI to Host
D[2]	IBI_TS_CRIT_HIGH_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Critical High 0 = Disable; MR51[2] = '1' does not generate an IBI to Host 1 = Enable; MR51[2] = '1' and MR27[4] = '1' generates an IBI to Host
D[1]	IBI_TS_LOW_EN	RW	0	In Band Error Interrupt Enable for Temperature Sensor Low 0 = Disable; MR51[1] = '1' does not generate an IBI to Host 1 = Enable; MR51[1] = '1' and MR27[4] = '1' generates an IBI to Host
D[0]	IBI_TS_HIGH_EN	RV	0	In Band Error Interrupt Enable for Temperature Sensor High 0 = Disable; MR51[0] = '1' does not generate an IBI to Host 1 = Enable; MR51[0] = '1' and MR27[4] = '1' generates an IBI to Host

1. This register is a self-clearing register after corresponding registers are cleared. Writing '0' in this register has no effect.
2. After this command is issued, the device does not generate an IBI for any pending event. But if new event occurs, the device does generate an IBI.
3. This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in Bus Reset section. This register can be read by the Host through normal read operation but cannot be written with normal write operation either in I^2C mode or I3C Basic mode. When this register is updated, it takes effect when there is a next Start operation (i.e. after Stop operation).

REG0x1C: MR28 Register: Thermal Sensor High Limit Configuration - Low Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_HIGH_LIMIT_LOW[7:0]	RW	0x70	MR28 and MR29 - 16 bit thermal registers define the high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28[7:0] and MR29[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x1D: MR29 Register: Thermal Sensor High Limit Configuration - High Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_HIGH_LIMIT_HIGH[7:0]	RW	0x03	MR28 and MR29 - 16 bit thermal registers define the high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

4. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
5. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28[7:0] and MR29[7:0]).
6. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REGISTER DESCRIPTION (continued)

REG0x1E: MR30 Register: Thermal Sensor Low Limit Configuration - Low Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_LOW_LIMIT_LOW[7:0]	RW	0	MR30 and MR31 - 16 bit thermal registers define the low limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR30[7:0] and MR31[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x1F: MR31 Register: Thermal Sensor Low Limit Configuration - High Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_LOW_LIMIT_HIGH[7:0]	RW	0	MR30 and MR31 - 16 bit thermal registers define the low limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR30[7:0] and MR31[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x20: MR32 Register: Thermal Sensor Critical Temperature High Limit Configuration - Low Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_HIGH_LIMIT_LOW[7:0]	RW	0x50	MR32 and MR33 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28[7:0] and MR29[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x21: MR33 Register: Thermal Sensor Critical Temperature High Limit Configuration - High Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_HIGH_LIMIT_HIGH[7:0]	RV	0x05	MR32 and MR33 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR28[7:0] and MR29[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x22: MR34 Register: Thermal Sensor Critical Temperature Low Limit Configuration - Low Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_LOW_LIMIT_LOW[7:0]	RW	0	MR34 and MR35 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR30[7:0] and MR31[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REGISTER DESCRIPTION (continued)

REG0x23: MR35 Register: Thermal Sensor Critical Temperature Low Limit Configuration - Low Byte (1) (2) (3)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_CRIT_LOW_LIMIT_HIGH[7:0]	RW	0	MR34 and MR35 - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. Critical temperature High Limit value must have a higher value than temperature High Limit (MR30[7:0] and MR31[7:0]).
3. The Reserved bits are Read Only bits. The Host must write '0' in reserved bits when writing and device always returns '0' from reserved bits when reads this byte.

REG0x30: MR48 Register: Device Status

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	IBI_STATUS	RO	0	Device Event In Band Interrupt Status 0 = No pending IBI 1 = Pending IBI
D[6:4]	Reserved	RV	0	Reserved
D[3]	WR_OP_STATUS	RO	0	Write Operation Status 0 = No internal write operation is on-going; 1 = Internal write operation is on-going; Device ignores Host Write command if Host attempts to write when this bit is '1'. The device self clears this bit to '0' when its completes internal write operation
D[2]	WP_OVERRIDE_STATUS	RO	-	Write Protect Override Status 0 = Override of write protect bits in MR12 and MR13 are blocked 1 = Override of write protect bits in MR12 and MR13 are allowed The default state of this register reflects the sensing of HSA pin during power on. This bit is set to '1' if HSA pin is directly tied to GND. This bit is set to '0' if HSA pin is connected to GND through a resistor.
D[1:0]	Reserved	RV	0	Reserved

REG0x31: MR49 Register: Current Sensed Temperature - Low Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_SENSE_LOW[7:0]	RO	-	MR49 and MR50 - 16 bit thermal registers return the most recent conversion of the thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. The device always returns '0' from reserved bits.

REG0x32: MR50 Register: Current Sensed Temperature - High Byte (1) (2)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:0]	TS_SENSE_HIGH[7:0]	RO	0	MR49 and MR50 - 16 bit thermal registers return the most recent conversion of the thermal sensor. See Table Thermal Register - Low Byte and High Byte.

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.
2. The device always returns '0' from reserved bits.

REGISTER DESCRIPTION (continued)

REG0x33: MR51 Register: Thermal Sensor Temperature Status (1)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7:4]	Reserved	RV	0	Reserved
D[3]	TS_CRIT_LOW_STATUS	RO	0	Temperature Sensor Critical Low 0 = Temperature is above the limit set in MR34 and MR35 1 = Temperature is below the limit set in MR34 and MR35
D[2]	TS_CRIT_HIGH_STATUS	RO	0	Temperature Sensor Critical High 0 = Temperature is below the limit set in MR32 and MR33 1 = Temperature is above the limit set in MR32 and MR33
D[1]	TS_LOW_STATUS	RO	0	Temperature Sensor Low 0 = Temperature above limit set in registers MR30 and MR31 1 = Temperature below limit set in registers MR30 and MR31
D[0]	TS_HIGH_STATUS	RO	0	Temperature Sensor High 0 = Temperature is below the limit set in registers MR28 and MR29 1 = Temperature is above the limit set in registers MR28 and MR29

1. This entire register is only applicable if MR1[7:0] programmed value is 0x18.

REG0x34: MR52 Register: Hub and Thermal Sensor Error Status

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	BUSY_ERROR_STATUS	RO	0	Write or Read Attempt while SPD5 Hub Device was Busy (Write Recovery Time Violation) (1) (2) 0 = No write or read attempt while SPD Hub device was busy 1 = Write or Read attempt while SPD5 Hub device was busy
D[6]	WR_NVM_BLK_ERROR_STATUS	RO	0	Write Attempt to Protected NVM Block 0 = No write attempt 1 = Write attempt to protected NVM Block
D[5]	WR_NVM_PRO_REG_ERROR_STATUS	RO	0	Write Attempt to NVM Protection Registers 0 = No attempt to modify write protect registers 1 = Write attempt to modify write protect registers
D[4:2]	Reserved	RO	0	Reserved
D[1]	PEC_ERROR_STATUS	RO	0	Packet Error (3) (4) 0 = No PEC Error 1 = PEC Error in one or more packets
D[0]	PAR_ERROR_STATUS	RO	0	Parity Check Error (4) (5) 0 = No Parity Error 1 = Parity Error in one or more bytes

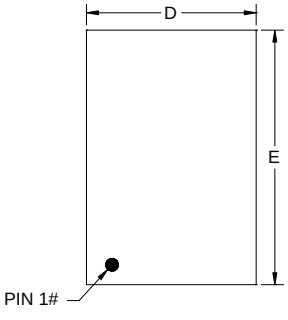
1. SPD5 Hub device busy status is only for accessing EEPROM memory. For any access to volatile register space, this bit definition does not apply.
2. When SPD5 Hub device is busy with EEPROM write/read, it sends NACK to the Host requests within write recovery time.
3. Only applicable MR18[5] = '1' and if PEC function is enabled.
4. This register is updated when SPD5 Hub device goes through bus reset as described in ***Bus Reset***.
5. Only applicable in MR18[5] = '1' and if Parity function is not disabled or for supported CCC in I^2C mode.

REVISION HISTORY

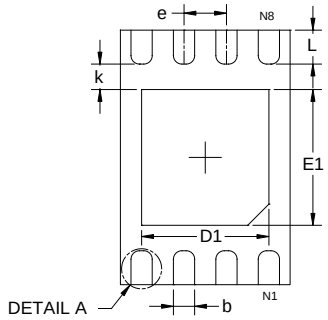
REVISION	DATE	COMMENTS
REV.A	Feb. 2024	Initial version release Updated: — UDFN package top marking — MR2[3:1]: DEV_REV_MINOR in *REG0x02: MR2 Register: Device Revision*
REV.A.1	Oct. 2026	Updated: — AC Measurement Conditions — Table 86. Register Attribute Modifier — Package Outline Dimensions Added: — Tape and Reel Information

PACKAGE OUTLINE DIMENSIONS

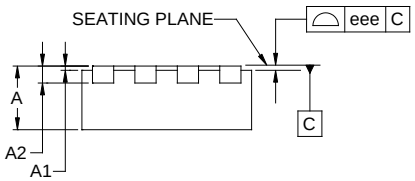
TDFN-2×3-8EL



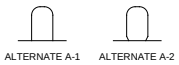
TOP VIEW



BOTTOM VIEW

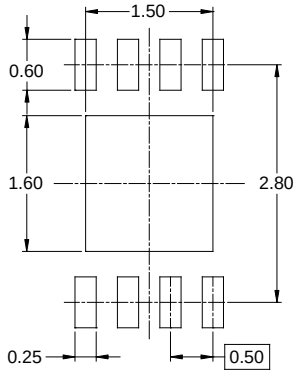


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



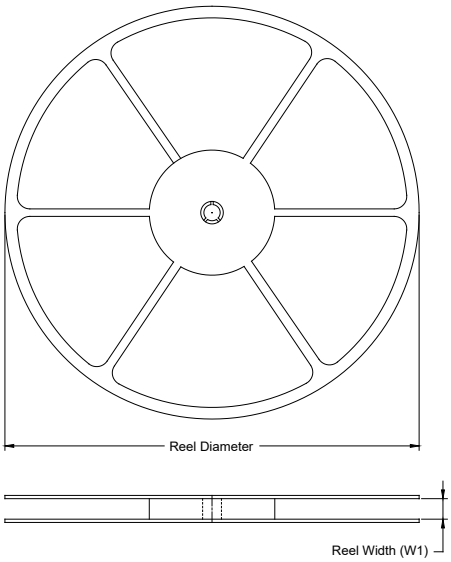
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	1.900	-	2.100
D1	1.400	-	1.600
E	2.900	-	3.100
E1	1.500	-	1.700
e	0.500 BSC		
k	0.300 REF		
L	0.300	-	0.500
eee	0.080		

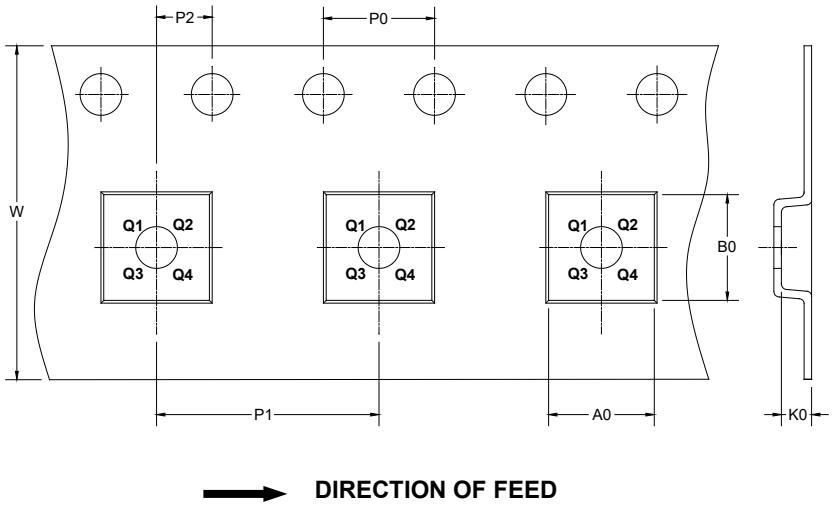
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



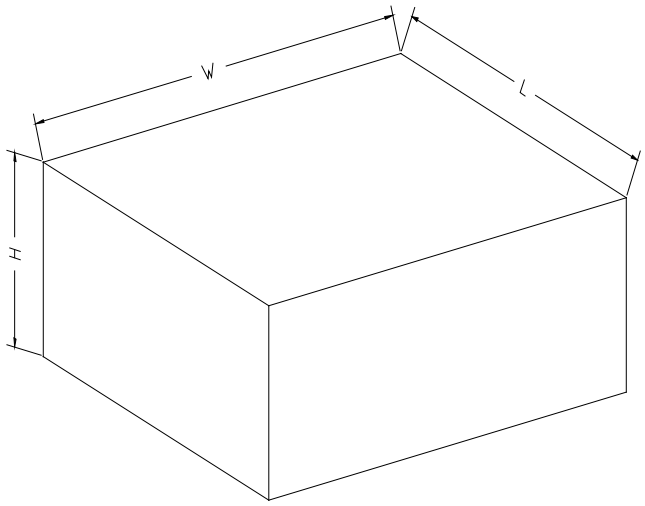
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×3-8EL	7"	8.6	2.30	3.30	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002