



SGM8609-1

3fA Input Bias Current, Rail-to-Rail Input and Output Precision Amplifier

GENERAL DESCRIPTION

The SGM8609-1 is a high precision, rail-to-rail input and output amplifier with an ultra-low input bias current at the 3fA level. The maximum limit of input bias current is $\pm 20\text{fA}$ at $+25^\circ\text{C}$ and $\pm 900\text{fA}$ at $+85^\circ\text{C}$. The device can keep this ultra-low input bias current within most of its input common mode voltage range.

The SGM8609-1 has a maximum low input offset voltage of $\pm 200\mu\text{V}$ and a low input offset voltage drift of $1.4\mu\text{V}/^\circ\text{C}$. The typical value of its input voltage noise density can be as low as $7\text{nV}/\sqrt{\text{Hz}}$. These combined characteristics make the device a good choice for high precision applications that require both accuracy and sensitivity in the system.

Additionally, the SGM8609-1 features a high gain-bandwidth product of 14MHz and a high open-loop voltage gain of 101dB. The device is suitable for use in signal conditioning, sensor interfaces and electrochemical cells.

The SGM8609-1 operates from 2.8V to 5.5V single supply or $\pm 1.4\text{V}$ to $\pm 2.75\text{V}$ dual supplies, and consumes only 3.4mA quiescent current at $V_S = 5.5\text{V}$. It is well-suited for portable and battery-powered equipment.

The SGM8609-1 is available in a Green SOIC-8 package. It features a unique pinout designed to isolate the input of the amplifier from the output and power supply pins. This special pin layout can help minimize system errors by reducing the leakage current between the input pins and the printed circuit board.

The SGM8609-1 operates over an ambient temperature range of -40°C to $+125^\circ\text{C}$.

FEATURES

- Ultra-Low Input Bias Current ($V_{CM} = [(+V_S) + (-V_S)]/2$)
 - ♦ $\pm 3\text{fA}$ (TYP) at $+25^\circ\text{C}$ when $(+V_S) - (-V_S) = 5\text{V}$
 - ♦ $\pm 10\text{fA}$ (TYP) at $+25^\circ\text{C}$ when $(+V_S) - (-V_S) = 2.8\text{V}$
 - ♦ $\pm 900\text{fA}$ (MAX) at $+85^\circ\text{C}$
- Low Input Offset Voltage: $\pm 30\mu\text{V}$ (TYP), $\pm 200\mu\text{V}$ (MAX)
- Low Input Offset Voltage Drift: $1.4\mu\text{V}/^\circ\text{C}$ (TYP)
- DC CMRR: 98dB (TYP)
- Open-Loop Voltage Gain: 101dB (TYP)
- Low Input Voltage Noise: $7\text{nV}/\sqrt{\text{Hz}}$ at 1kHz
- Low THD+N: 0.0007%
- Gain-Bandwidth Product: 14MHz
- Falling Edge Slew Rate: $8.5\text{V}/\mu\text{s}$
- Rail-to-Rail Input and Output
- Supply Voltage Range: 2.8V to 5.5V
- Quiescent Current: 3.4mA (TYP)
- -40°C to $+125^\circ\text{C}$ Operating Temperature Range
- Available in a Green SOIC-8 Package

APPLICATIONS

Transimpedance Amplifiers (TIAs) for Photodiodes
Buffers with High-Impedance Characteristic for Sensors
Picoammeters or Coulombmeters
Electrometers
Electrodes of pH Measurement

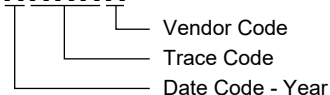
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8609-1	SOIC-8	-40°C to +125°C	SGM8609-1XS8G/TR	SGM 86091XS8 XXXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXXX = Date Code, Trace Code and Vendor Code.

XXXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V _S to -V _S ⁽¹⁾	-0.3V to 6V
Differential Input Voltage, V _{ID}	-0.3V to 0.3V
Input/Output Voltage Range	(+V _S) + 0.3V to (-V _S) - 0.3V
Package Thermal Resistance	
SOIC-8, θ _{JA}	119.7°C/W
SOIC-8, θ _{JB}	64.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(2) (3)}	
HBM	±8000V
CDM	±1000V

NOTES:

1. The voltage difference between any pair of pins should never exceed 6V.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, +V _S to -V _S	2.8V to 5.5V
Operating Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

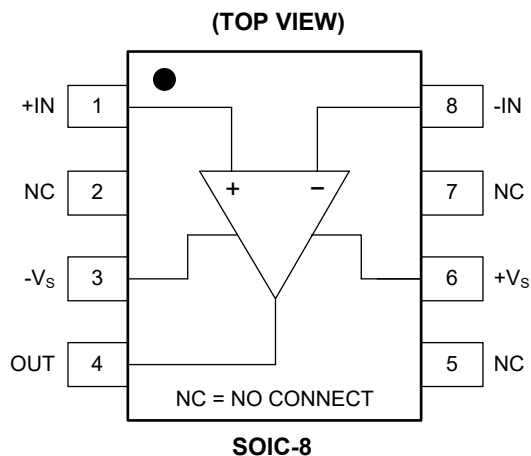
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
1	+IN	I	Non-Inverting Input.
2, 5, 7	NC	—	No Internal Connection.
3	-V _S	P	Negative Power Supply.
4	OUT	O	Output.
6	+V _S	P	Positive Power Supply.
8	-IN	I	Inverting Input.

NOTES:

1. I = input, O = output, P = power.

2. This SOIC-8 package does not adopt the standard pinout for single operational amplifiers. When using the SGM8609-1 as a replacement, a new printed circuit board layout will likely be needed.

ELECTRICAL CHARACTERISTICS

($+V_S = 5.5V$, $-V_S = 0V$, $V_{CM} = [(+V_S) + (-V_S)]/2$, Full = $-40^\circ C$ to $+125^\circ C$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V _{OS}		+25°C	-200	±30	200	μV
			Full	-850		850	
Input Offset Voltage Drift	ΔV _{OS} /ΔT		Full		1.4		μV/°C
Input Bias Current ^{(1) (2)}	I _B	V _S = 5V	+25°C	-20	±3	20	fA
			-40°C to +85°C	-900		900	
			Full	-5		5	pA
Input Offset Current ⁽²⁾	I _{OS}	V _S = 5V	+25°C	-40	±3	40	fA
Input Common Mode Voltage Range	V _{CM}	CMRR ≥ 80dB	+25°C	(-V _S) - 0.3		(+V _S) + 0.3	V
Common Mode Rejection Ratio	CMRR	V _{CM} = 0V to 5.5V	+25°C	78	98		dB
			Full	75			
Large-Signal Voltage Gain	A _{VOL}	V _S = 5V, V _{OUT} = 0.3V to 4.7V, R _L = 2kΩ to +V _S /2	+25°C	81	101		dB
			Full	68			
		V _S = 5V, V _{OUT} = 0.3V to 4.7V, R _L = 10kΩ to +V _S /2	+25°C	81	101		
			Full	68			
Output Characteristics							
Output Voltage Swing High	V _S - V _{OH}	R _L = 2kΩ to +V _S /2	+25°C		35	40	mV
			Full			60	
		R _L = 10kΩ to +V _S /2	+25°C		10	20	
			Full			30	
Output Voltage Swing Low	V _{OL}	R _L = 2kΩ to +V _S /2	+25°C		35	40	mV
			Full			60	
		R _L = 10kΩ to +V _S /2	+25°C		15	20	
			Full			30	
Output Short-Circuit Current	I _{SOURCE}	Sourcing to -V _S , V _{IN} = 200mV	+25°C	16	35		mA
			Full	10			
	I _{SINK}	Sinking to +V _S , V _{IN} = -200mV	+25°C	36	55		
			Full	32			
Power Supply							
Operating Voltage Range	V _S		Full	2.8		5.5	V
Power Supply Rejection Ratio	PSRR	+V _S = 2.8V to 5.5V, -V _S = 0V, V _{CM} = 0V	+25°C	88	106		dB
			Full	82			
Quiescent Current	I _Q		+25°C		3.4	4.2	mA
			Full			5	

NOTES:

1. A positive current denotes the flow of electricity entering the device.
2. Specified by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

($+V_S = 5V$, $-V_S = 0V$, $V_{CM} = [(+V_S) + (-V_S)]/2$, Full = $-40^\circ C$ to $+125^\circ C$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP		+25°C		14		MHz
Slew Rate	SR	G = +1, Rising (10% to 90%)	+25°C		6.5		V/μs
		G = +1, Falling (90% to 10%)	+25°C		8.5		
Total Harmonic Distortion + Noise	THD+N	V _{OUT} = 4V _{P-P} , G = +2, f = 1kHz, R _L = 100kΩ	+25°C		0.0007		%
		V _{OUT} = 4V _{P-P} , G = +2, f = 1kHz, R _L = 600Ω	+25°C		0.0007		
Noise, RTI ⁽³⁾							
Input Voltage Noise Density	e _n	f = 400Hz	+25°C		10		nV/√Hz
		f = 1kHz	+25°C		7		
Input Current Noise Density	i _n	f = 1kHz	+25°C		0.01		pA/√Hz

NOTE:

3. RTI stands for Referred-to-input.

ELECTRICAL CHARACTERISTICS (continued)

($+V_S = 2.8V$, $-V_S = 0V$, $V_{CM} = [(+V_S) + (-V_S)]/2$, Full = $-40^\circ C$ to $+125^\circ C$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V _{OS}		+25°C	-200	±30	200	μV
			Full	-750		750	
Input Offset Voltage Drift	ΔV _{OS} /ΔT		Full		1.5		μV/°C
Input Bias Current ^{(1) (2)}	I _B		+25°C	-20	±10	20	fA
			-40°C to +85°C	-900		900	
			Full	-5		5	pA
Input Offset Current ⁽²⁾	I _{OS}		+25°C	-40	±10	40	fA
Input Common Mode Voltage Range	V _{CM}	CMRR ≥ 75dB	+25°C	(-V _S) - 0.3		(+V _S) + 0.3	V
Common Mode Rejection Ratio	CMRR	V _{CM} = 0V to 2.8V	+25°C	76	91		dB
			Full	71			
Large-Signal Voltage Gain	A _{VOL}	V _{OUT} = 0.15V to 2.2V, R _L = 2kΩ to +V _S /2	+25°C	102	116		dB
			Full	94			
		V _{OUT} = 0.15V to 2.2V, R _L = 10kΩ to +V _S /2	+25°C	102	120		
			Full	98			
Output Characteristics							
Output Voltage Swing High	V _S - V _{OH}	R _L = 2kΩ to +V _S /2	+25°C		20	30	mV
			Full			35	
		R _L = 10kΩ to +V _S /2	+25°C		5	10	
			Full			20	
Output Voltage Swing Low	V _{OL}	R _L = 2kΩ to +V _S /2	+25°C		15	20	mV
			Full			30	
		R _L = 10kΩ to +V _S /2	+25°C		5	10	
			Full			20	
Output Short-Circuit Current	I _{SOURCE}	Sourcing to -V _S , V _{IN} = 200mV	+25°C	18	35		mA
			Full	10			
	I _{SINK}	Sinking to +V _S , V _{IN} = -200mV	+25°C	36	45		
			Full	32			
Power Supply							
Operating Voltage Range	V _S		Full	2.8		5.5	V
Power Supply Rejection Ratio	PSRR	+V _S = 2.8V to 5.5V, -V _S = 0V, V _{CM} = 0V	+25°C	88	106		dB
			Full	82			
Quiescent Current	I _Q		+25°C		3.1	3.9	mA
			Full			4.6	

NOTES:

1. A positive current denotes the flow of electricity entering the device.
2. Specified by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

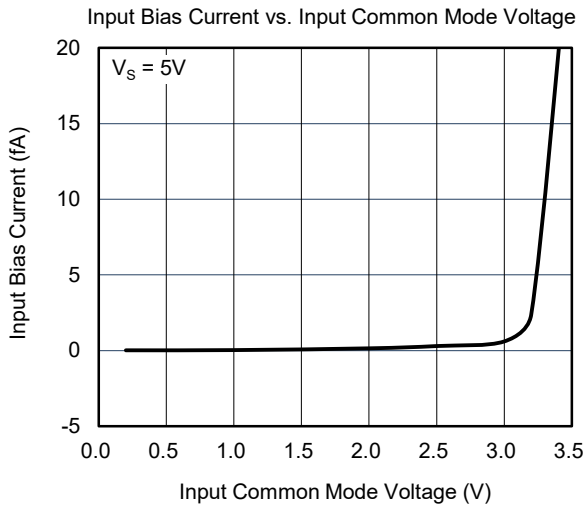
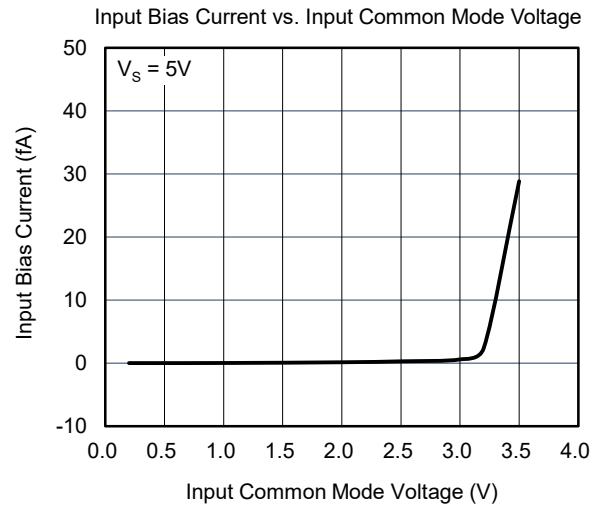
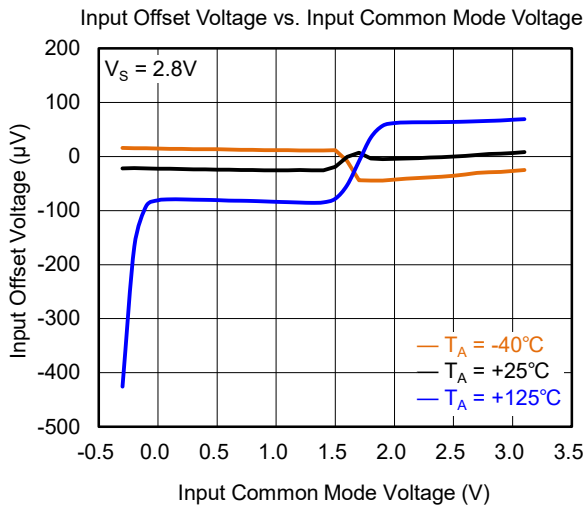
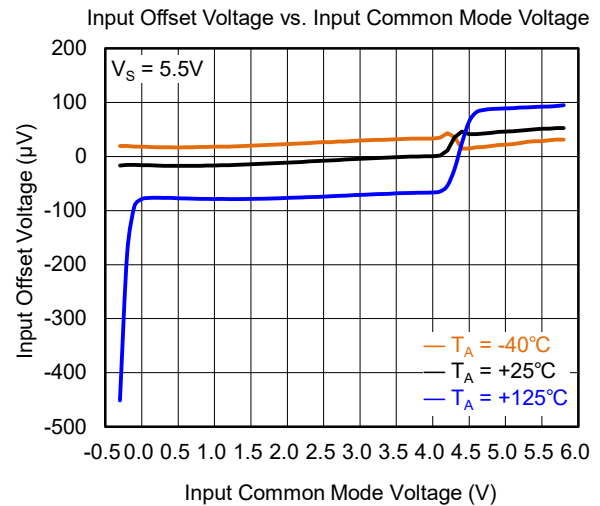
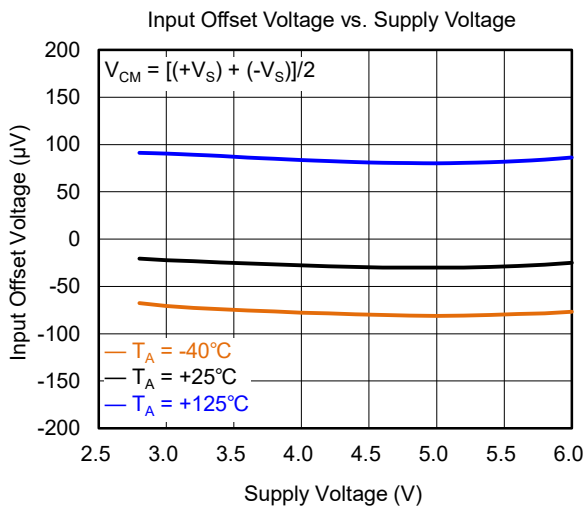
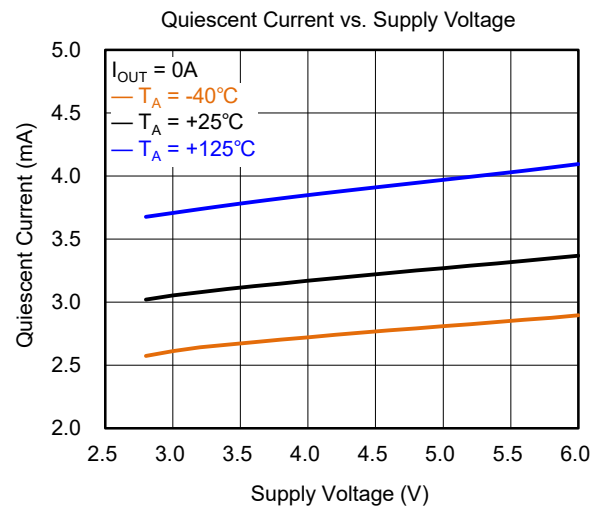
($+V_S = 2.8V$, $-V_S = 0V$, $V_{CM} = [(+V_S) + (-V_S)]/2$, Full = $-40^{\circ}C$ to $+125^{\circ}C$, typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP		+25°C		13		MHz
Slew Rate	SR	G = +1, Rising (10% to 90%)	+25°C		6.5		V/μs
		G = +1, Falling (90% to 10%)	+25°C		9.5		
Total Harmonic Distortion + Noise	THD+N	V _{CM} = 1.1V, V _{OUT} = 0.9V _{P-P} , G = +2, f = 1kHz, R _L = 100kΩ	+25°C		0.0015		%
		V _{CM} = 1.1V, V _{OUT} = 0.9V _{P-P} , G = +2, f = 1kHz, R _L = 600Ω	+25°C		0.0015		
Noise, RTI ⁽³⁾							
Input Voltage Noise Density	e _n	f = 400Hz	+25°C		9		nV/√Hz
		f = 1kHz	+25°C		7		
Input Current Noise Density	i _n	f = 1kHz	+25°C		0.03		pA/√Hz

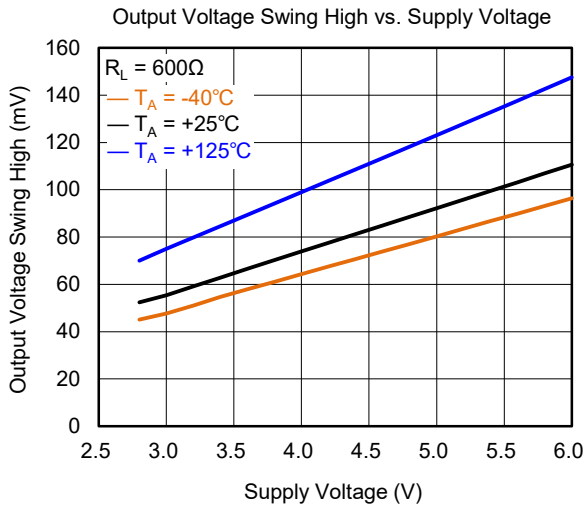
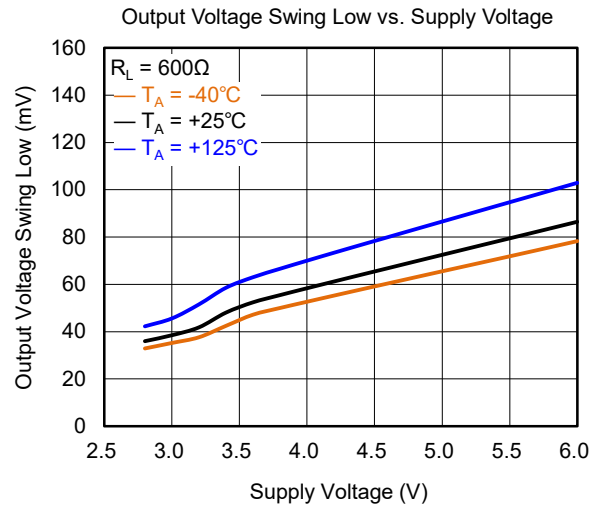
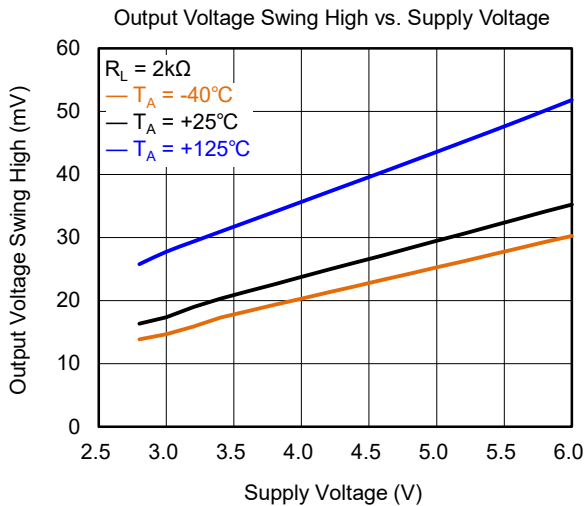
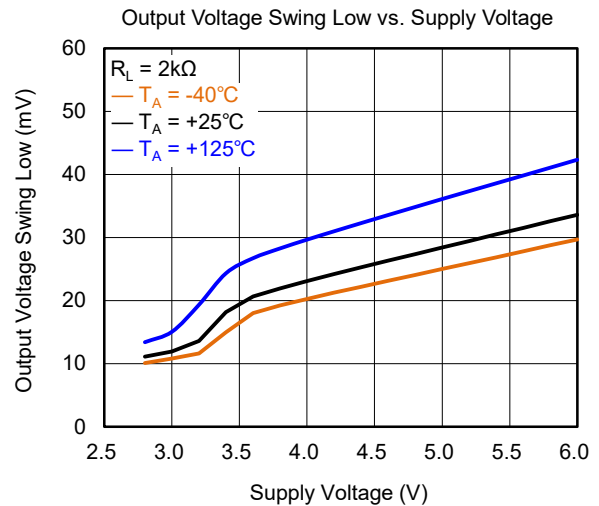
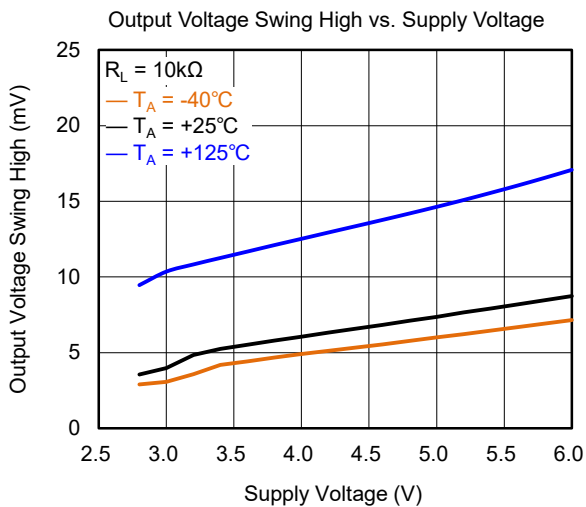
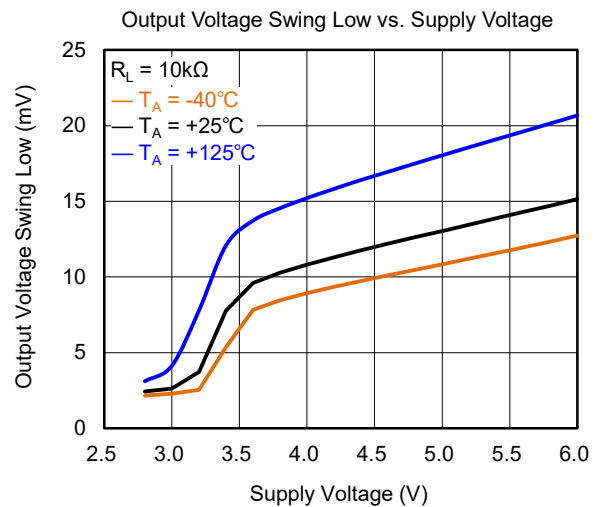
NOTE:

3. RTI stands for Referred-to-input.

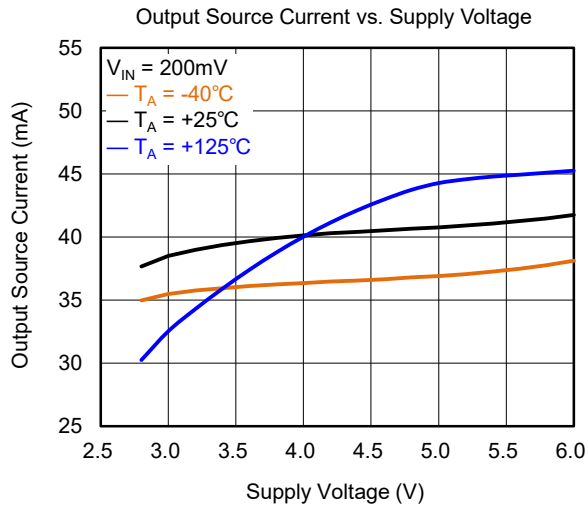
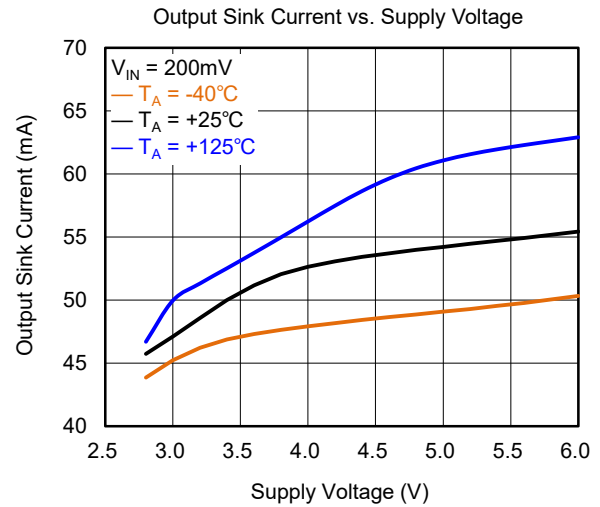
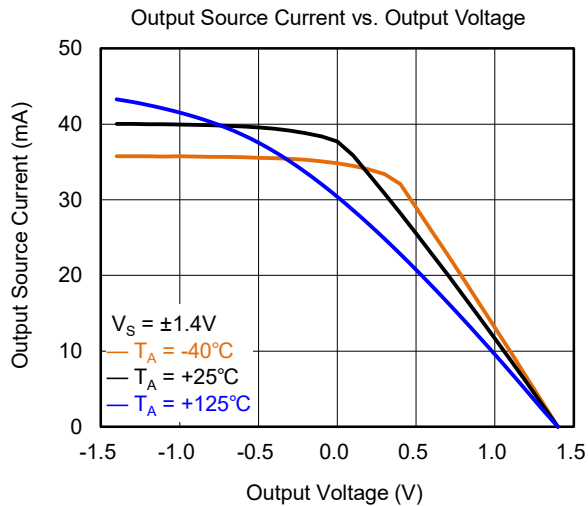
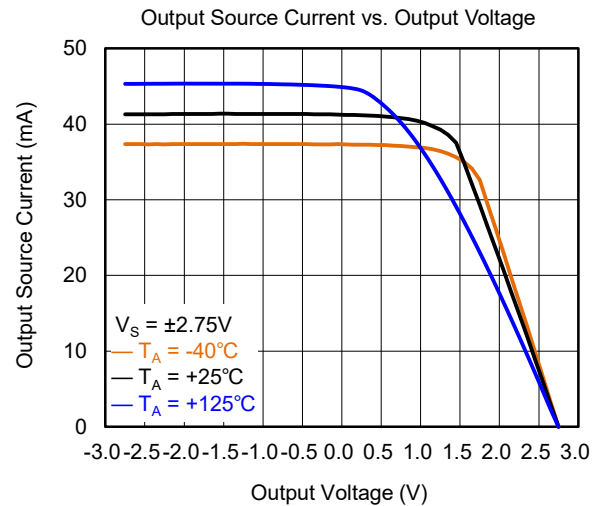
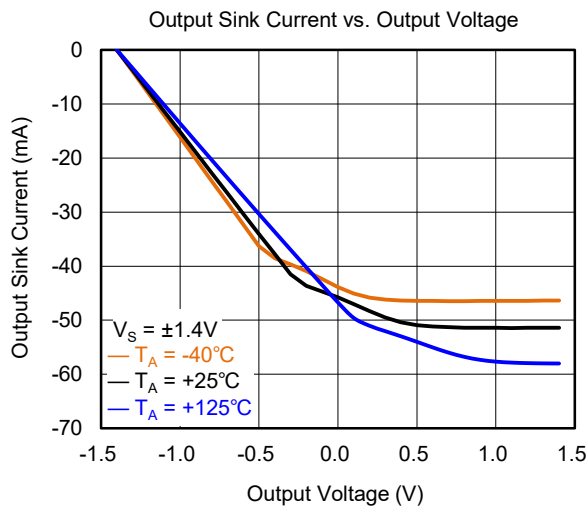
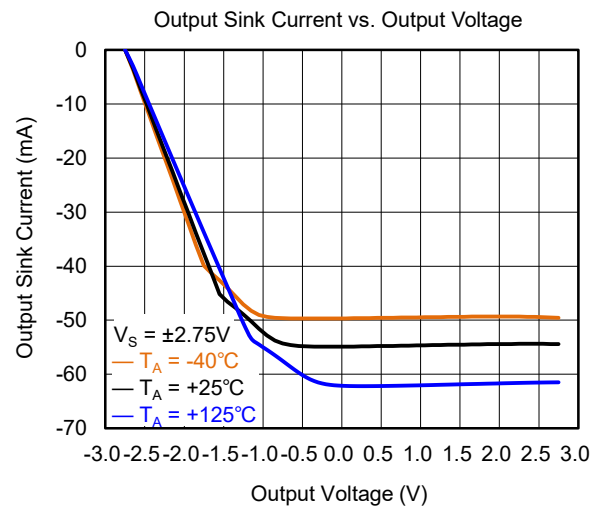
TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

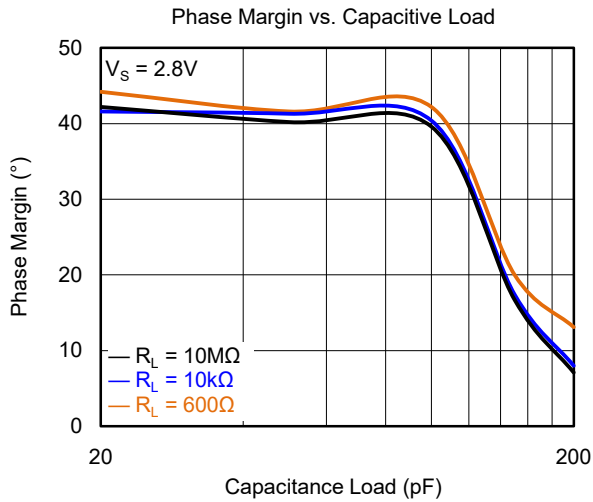
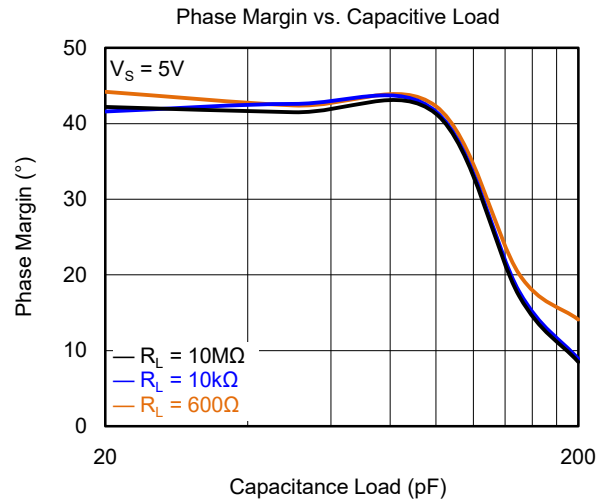
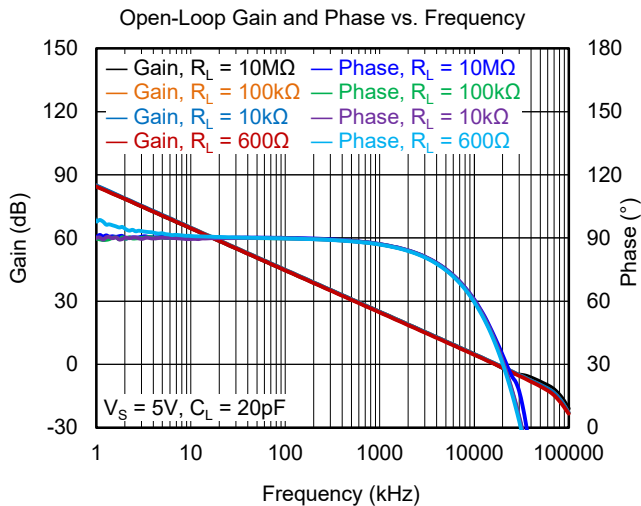
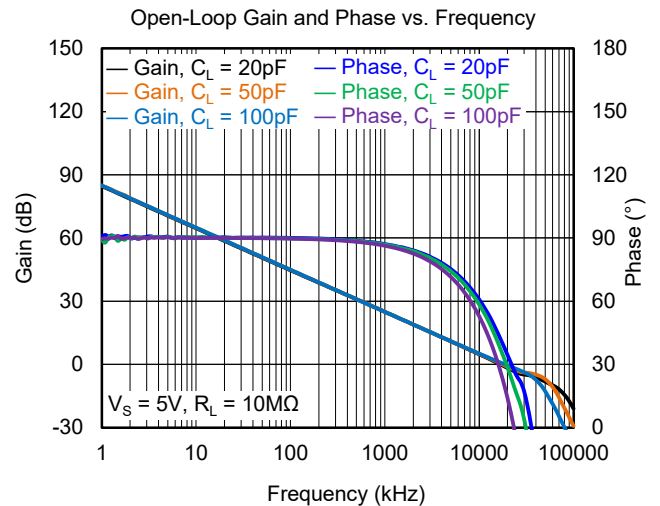
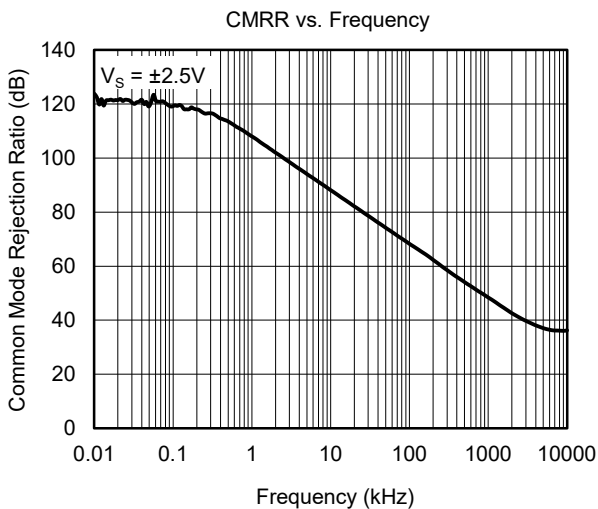
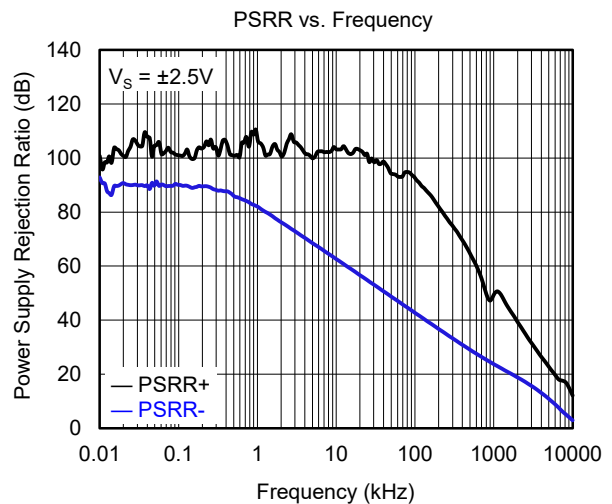
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At $T_A = +25^\circ\text{C}$, unless otherwise noted.

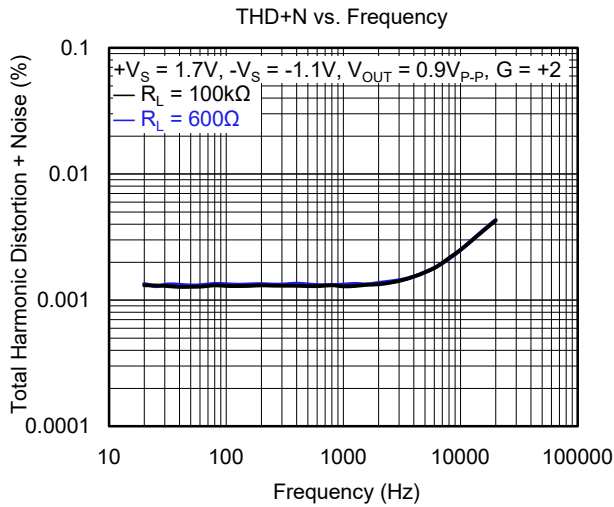
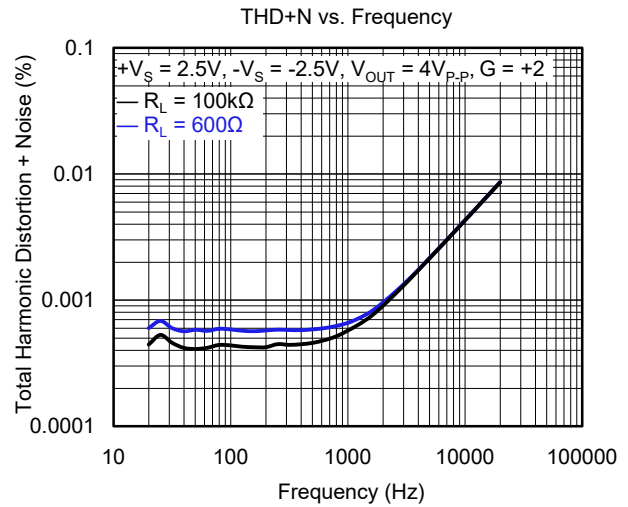
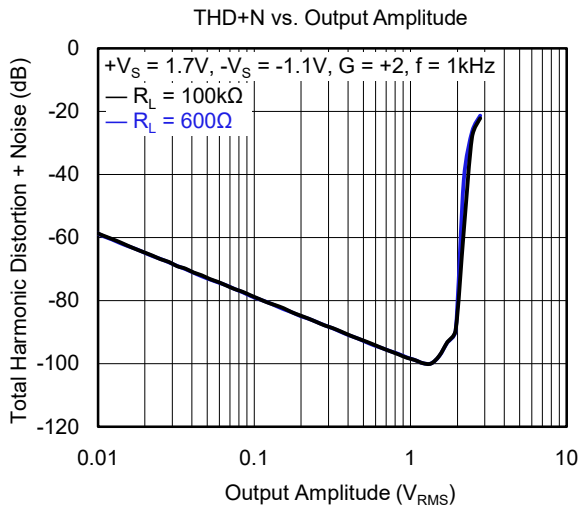
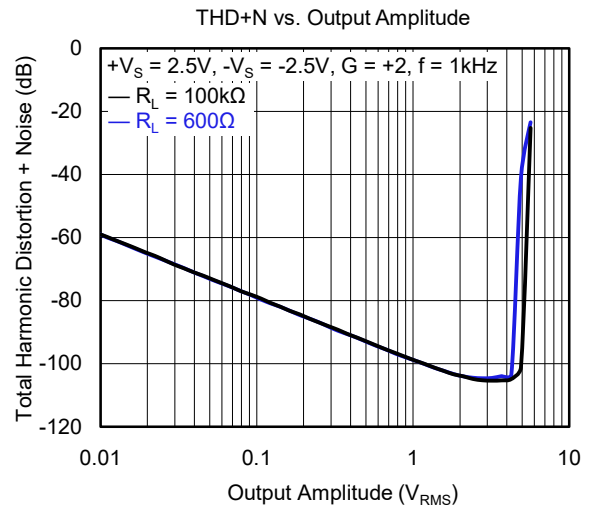
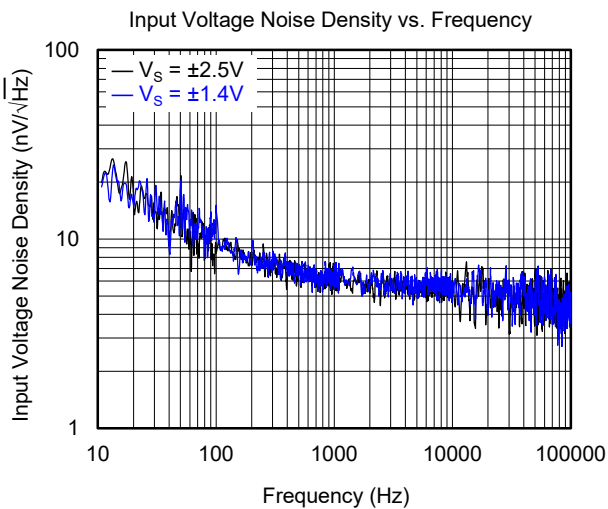
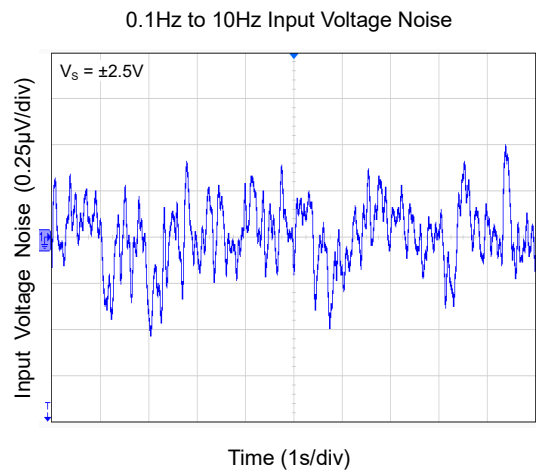
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

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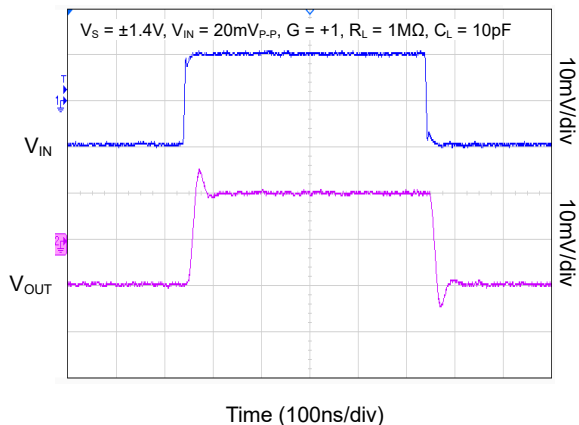
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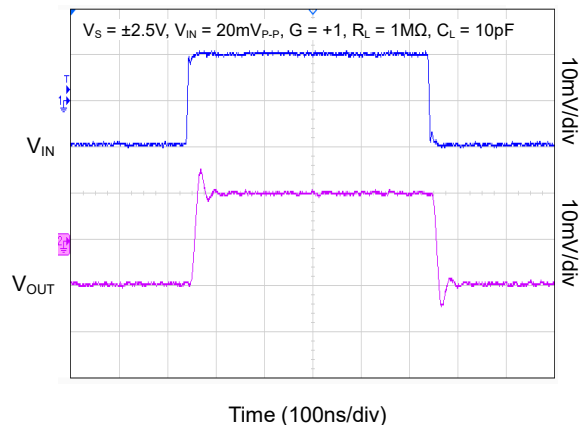
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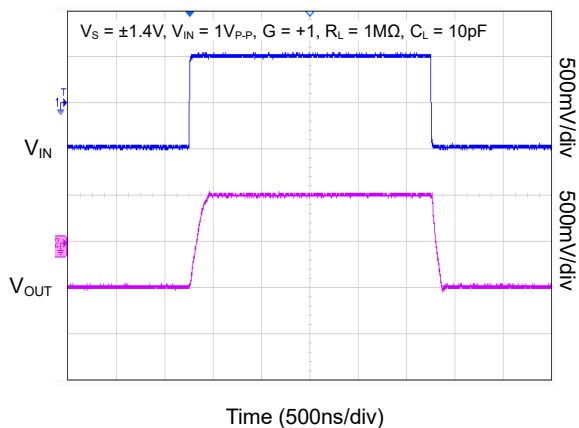
Small-Signal Step Response



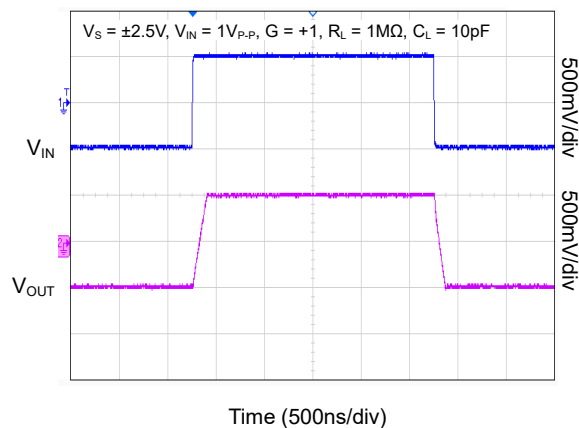
Small-Signal Step Response



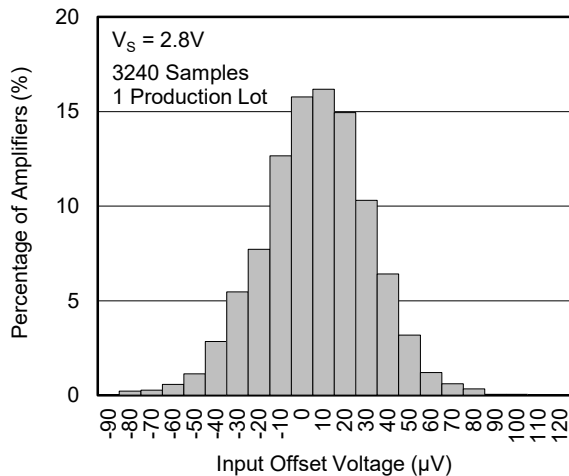
Large-Signal Step Response



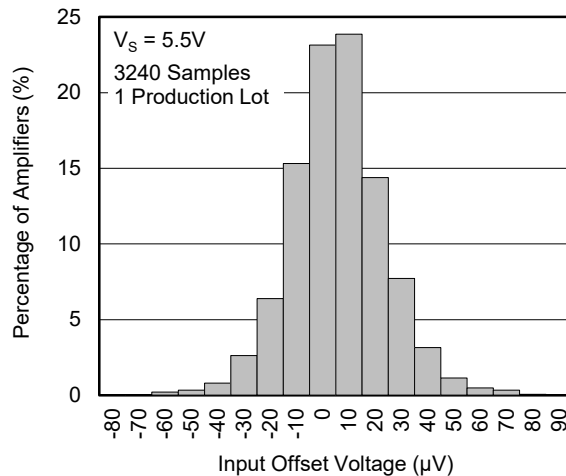
Large-Signal Step Response

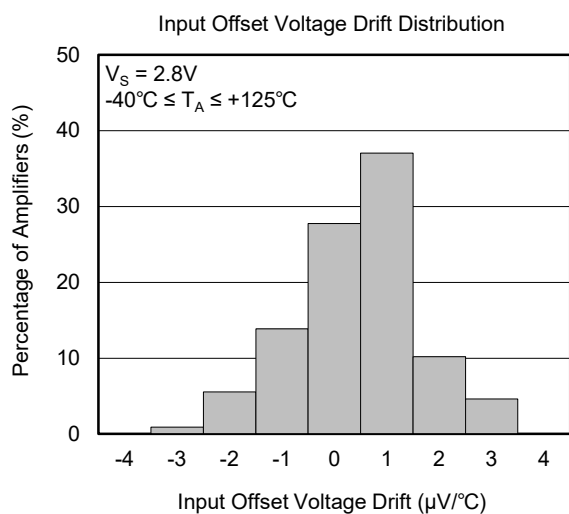
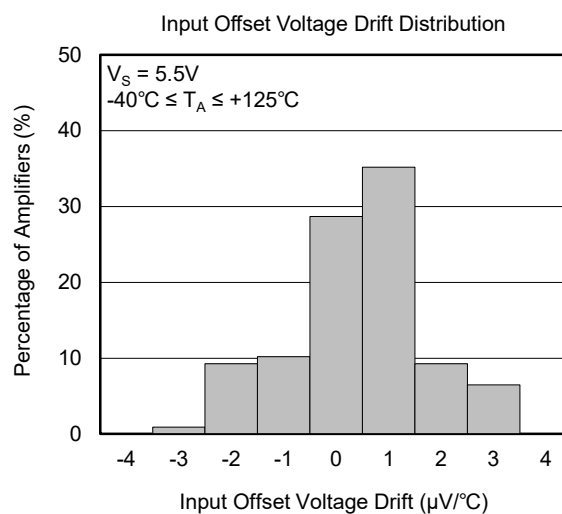


Input Offset Voltage Production Distribution



Input Offset Voltage Production Distribution



TYPICAL PERFORMANCE CHARACTERISTICS (continued)At $T_A = +25^\circ\text{C}$, unless otherwise noted.

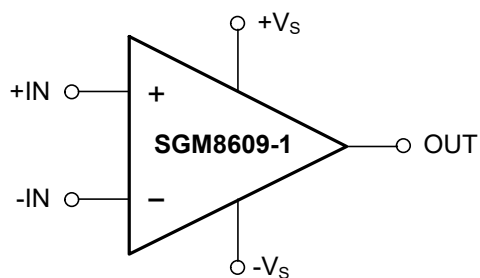
FUNCTIONAL BLOCK DIAGRAM

Figure 1. Block Diagram

APPLICATION INFORMATION

The operating supply voltage rail for the SGM8609-1 is from 2.8V to 5.5V, and the recommended operating temperature is from -40°C to +125°C. Where the electrical parameters vary with the supply voltage and temperature, this is indicated in the Electrical Characteristics and the Typical Performance Characteristics sections.

Rail-to-Rail Input

The SGM8609-1 supports rail-to-rail input, and the input common mode voltage range is from $(-V_S) - 0.3V$ to $(+V_S) + 0.3V$. This feature significantly increases dynamic range of the SGM8609-1 and allows the SGM8609-1 to be used in almost all single-supply and general purpose applications.

Input Protection

The input stage of the SGM8609-1 is shown in Figure 2. The ESD diodes between the inputs and the power supply rails will clamp the input voltage so that it does not exceed the rails.

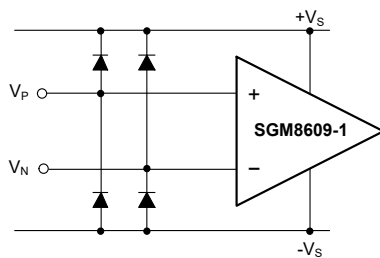


Figure 2. Input Stage

Rail-to-Rail Output

The SGM8609-1 supports rail-to-rail output operation. This feature gives it a larger output swing range which is especially useful when the supply voltage is low. Even when operating with a 2.8V supply, the output of the SGM8609-1 can source 35mA and sink 45mA.

Ultra-Low Input Bias Current

The SGM8609-1 has ultra-low input bias current. The typical value of the input bias current for SGM8609-1 is $\pm 3fA$. For the maximum value of I_B , the I_B for +25°C and +85°C are $\pm 20fA$ and $\pm 900fA$ respectively with a 5V or a 2.8V power supply and $V_{CM} = [(+V_S) + (-V_S)]/2$.

Wide Bandwidth

The SGM8609-1 is a high-performance amplifier with a 14MHz gain-bandwidth product and only draws 3.4mA of quiescent current. This provides a good choice for many applications that have higher requirements for operational amplifier bandwidth.

Low Input Noise

The input voltage noise density of SGM8609-1 at 1kHz is only $7nV/\sqrt{Hz}$, which combines with a very low input current noise density of just $0.01pA/\sqrt{Hz}$.

The low input voltage noise and ultra-low input bias current allow for a large dynamic range, which makes the amplifier ideally suited for use in sensor-based applications.

Stability Compensation

The SGM8609-1 is highly likely to be equipped with extremely large feedback resistors during application. However, when using a large feedback resistance, extra care has to be taken when designing the PCB layout. All amplifiers have input capacitance between the input terminals and AC ground. This input capacitance, together with the large feedback resistor, will cause a pole in the feedback path, which in turn may result in gain peaking and may even cause oscillation.

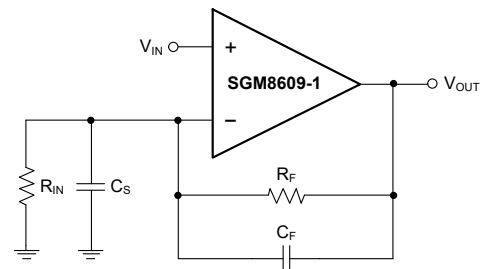


Figure 3. General Operational Amplifier Circuit

The frequency of the pole in Figure 3 is shown as below:

$$f_p = \frac{1}{2\pi C_S R_p} \quad (1)$$

where:

- R_p represents the parallel product of R_F and R_{IN} .
- C_S represents the total capacitance (parasitic, amplifier capacitance) at the terminal of the inverting input of the amplifier.

APPLICATION INFORMATION (continued)

The typical input capacitance of SGM8609-1 is approximately 7pF.

For instance, if the feedback resistive component is reduced to a few kΩ, the pole which is caused by the R_F and C_F will be much higher than the closed-loop bandwidth so that this pole can be negligible.

However, if the pole is 6 or 10 times smaller than the closed-loop bandwidth, the feedback capacitor C_F should also be placed in the feedback path to enhance the stability. To maintain the stability, the following equation should be taken into consideration.

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \leq \sqrt{6 \times 2\pi \times \text{GBP} \times R_F \times C_S} \quad (2)$$

where:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \quad (3)$$

is the low-frequency noise gain of the amplifier and the GBP is the gain-bandwidth product of the amplifier. The following equation represents the low-frequency noise gain of the operational amplifier:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \quad (4)$$

For both the inverting and non-inverting applications of the SGM8609-1, the feedback capacitor is always needed to avoid oscillation if the noise gain is low or feedback resistor is large.

For the above mentioned situations, if the noise gain of the circuit is:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \geq 2\sqrt{\text{GBP} \times R_F \times C_S} \quad (5)$$

the recommended feedback capacitor should be calculated as below:

$$C_F = \frac{C_S}{2 \left(\frac{R_F}{R_{IN}} + 1 \right)} \quad (6)$$

If

$$\left(\frac{R_F}{R_{IN}} + 1 \right) < 2\sqrt{\text{GBP} \times R_F \times C_S} \quad (7)$$

the recommended feedback capacitor should be calculated as below:

$$C_F = \sqrt{\frac{C_S}{\text{GBP} \times R_F}} \quad (8)$$

Note that the most conservative expression for the feedback capacitor to guarantee stability is shown as below:

$$C_F = \frac{C_S \times R_{IN}}{R_F} \quad (9)$$

Note that C_S is the summation of SGM8609-1's capacitance and the parasitic capacitance of the PCB. C_F can make the compensation of the feedback circuit so that the stability is improved.

A smaller feedback capacitor will provide more bandwidth. The stray capacitance of a PCB is strongly determined by its design and the material used, and will change from one design to the next. For this reason, it is recommended to directly measure the stray capacitance of the PCB before choosing the value of the feedback capacitance C_F . A somewhat larger value for C_F decreases the noise of the circuit, and also provides more stability, at the expense of a reduced bandwidth.

The SGM8609-1 is designed for driving the 200pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 4 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

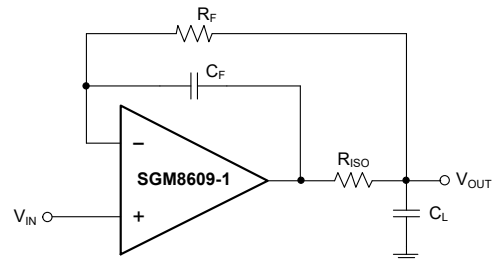


Figure 4. Circuit to Drive Heavy Capacitive Load

APPLICATION INFORMATION (continued)

Guard Ring Design

The SGM8609-1 is a device with ultra-low bias current. In order to maintain this advantage in application circuits, it is also necessary to design specialized guard ring in PCB design to avoid interference from other PCB traces and maintain ultra-low input bias current in the entire application.

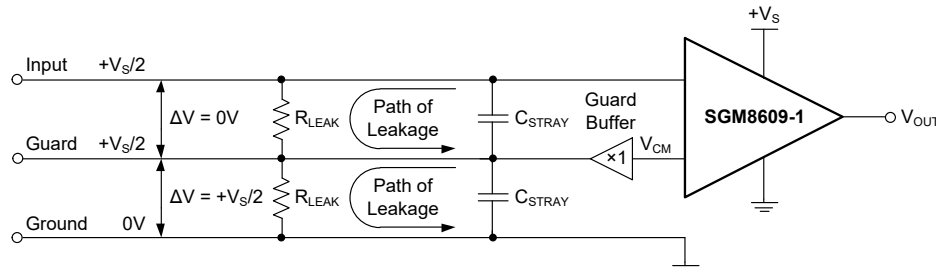


Figure 5. Guard Ring Schematic

The guard ring surrounds the input signal path of the circuit. It should be driven by the guard buffer so that it can make the average voltage of the guard equal to the voltage of the input signal and it can also decrease any leakage current from the input signal to ground. In addition, the guard ring can eliminate the effect of stray capacitance of the PCB because the voltage potential between the input signal path and guard ring is almost equal to zero.

For the non-inverting applications, the potential of guard should be taken from the inverting pin of the amplifier. Figure 6 illustrates the specific guard ring design for the non-inverting applications.

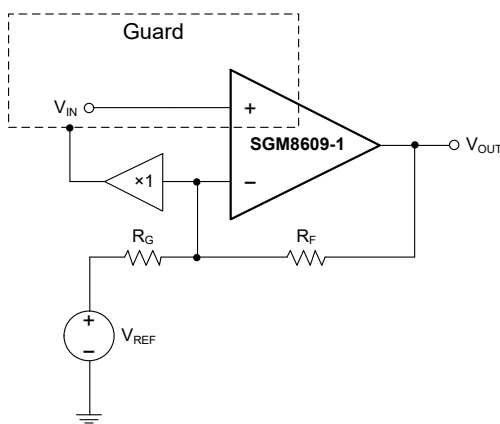


Figure 6. Guarding the Non-Inverting Configuration

Figure 7 illustrates that the guard trace surrounds the inverting signal path for the inverting applications.

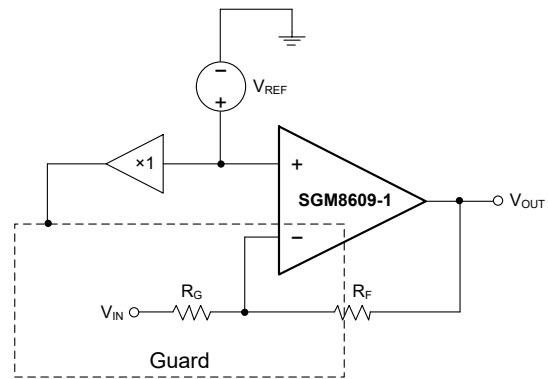


Figure 7. Guarding the Inverting or Transimpedance Configuration

To avoid stability problems of the guard buffer, it should be designed for a gain that is slightly smaller than one, and it should have a large phase margin. A 100Ω or 1kΩ resistor can be placed in series with the output of the guard buffer, to limit possible short-circuit currents and to improve the ability to drive large capacitive loads.

Also, the high-impedance node of the circuit should always be enclosed by the shield which is connected to the guard buffer to enhance the accuracy of the system.

The ground or shield plane should surround the guard ring to protect it from noise coupling, which can affect the input signal path of the circuit.

APPLICATION INFORMATION (continued)

Use Triaxial Cable

The structure of the triax is shown in Figure 8. The guard conductor is inserted between the outer ground and signal conductor to avoid the leakage current effect.

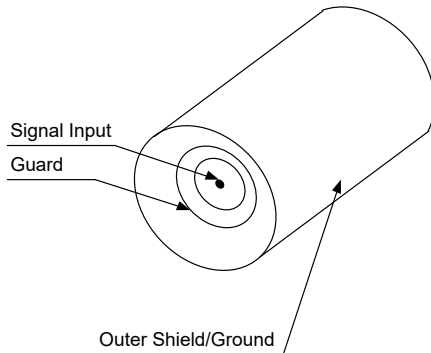


Figure 8. The Structure of a Triax

Properly Clean the Assembly

Properly cleaning the PCB is necessary when sub-picoamp currents are being measured. Leftover cleaning solvent, flux residue and moisture will cause extra leakage current, therefore reducing the accuracy of the circuit. Especially "water soluble" and "no clean" flux can leave a film on the PCB surface that will require that the board is washed with isopropyl alcohol or methanol and subsequently baked to make sure that the remaining moisture is sufficiently removed.

Typical Application

The ultra-low input bias current and the low input voltage noise of the SGM8609-1, in combination with its rail-to-rail input and output voltage ranges and a 14MHz gain-bandwidth product, allow for signal amplification at high gain and with a high bandwidth. The combination of these properties makes the SGM8609-1 very well suited for many applications where it is used as a transimpedance amplifier.

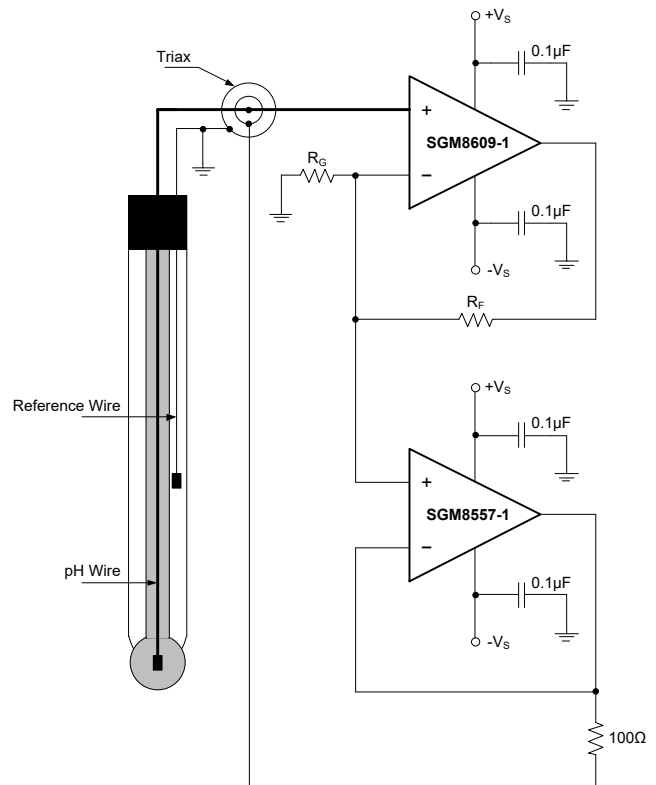


Figure 9. SGM8609-1 as pH Electrode Amplifier

Design Requirements

The ultra-low input bias current of SGM8609-1 results in a very small error caused by the high output impedance of pH electrodes (typically from 10MΩ to 1000MΩ). For instance, if a 10MΩ pH electrode is used, the SGM8609-1 generates an input error of only 30nV.

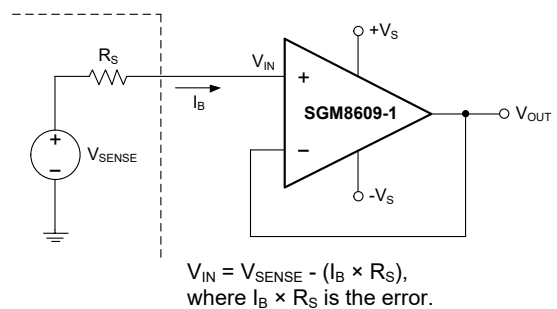


Figure 10. Error Caused by Amplifier's Input Bias Current and Sensor Source Impedance

APPLICATION INFORMATION (continued)

Detailed Design Procedure

To design the closed-loop gain of the circuit that can properly detect the pH within the output swing, the pH at +100°C should be taken into consideration and it contributes $\pm 518.3\text{mV}$ at the output of the pH electrode. For better performance, the output swing can be limited to 4V and the gain choice should be $4\text{V}/1.0366\text{V} = 3.8\text{V/V}$.

With $R_F = 2.8\text{k}\Omega$ and $R_G = 1\text{k}\Omega$, the gain will be 3.8V/V .

Figure 9 indicates an example of the pH electrode application. A triax should be used in this application to reduce the leakage current. The output voltage of the pH electrode is connected to the signal conductor of the triax and to the non-inverting pin of the SGM8609-1. The guard ring is driven by the guard buffer, and the input to the guard buffer is connected to the inverting pin of the SGM8609-1, such that the voltage of the guard follows that of the non-inverting pin. In addition, a 50Ω or 100Ω resistor can be inserted between the output of the guard buffer and the triax guard to enhance the stability and limit a possible short-circuit current.

Power Supply Recommendations

For precision applications, a clean and low noise power supply is very important in amplifier circuits. Although the SGM8609-1 exhibits excellent PSRR over a wide frequency range, residual noise on the power rail may still couple to the input stage through the inherent parasitic capacitance (approximately 0.5pF) of the integrated ESD protection network. Although such effects are not the main focus of most applications, charge-sensitive or high gain, high-impedance applications may still be affected.

Therefore, it is strongly recommended that an LDO is used for powering the power supply rails to reduce noise effects. However, if the power source is not clean enough, an RC (100Ω and $100\mu\text{F}$) network can be added between the source and the power supply pins. If the switching noise exists on the power rail, a series inductor should be taken into consideration to absorb the high-frequency component at the supply pins.

For the power supply pins of SGM8609-1, the power supply bypassing is an effective method to clear up the

noise at power supply, and the low-impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, $10\mu\text{F}$ ceramic capacitor paralleled with $0.1\mu\text{F}$ or $0.01\mu\text{F}$ ceramic capacitor is used in Figure 11. The ceramic capacitors should be placed as close as possible to the $+V_S$ and $-V_S$ power supply pins.

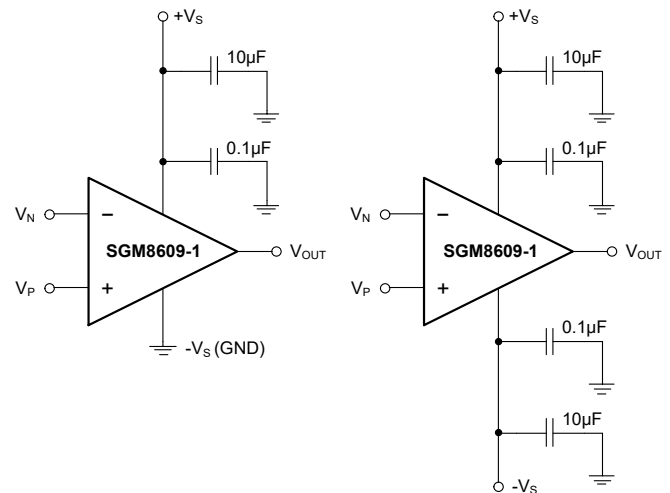


Figure 11. Amplifier Power Supply Bypassing

Layout

Layout Guidelines

To avoid excessive input current leakage, the layout and assembly of the PCB for the SGM8609-1 should be conducted with care. A guard ring should always surround the input pin to avoid leakage current and isolate the high-impedance pin from interference. The advantage of the guard ring is low-impedance, which allows it to protect the high-impedance nodes. The input pins should be surrounded by the guard rings as shown in the layout in Figure 12, as well as placing the guard ring at both sides of the PCB. The two NC pins should be connected to the guard ring, as shown in Figure 12.

Be aware that the solder mask must not cover the guard ring on both sides of the PCB, and that noisy or switching power supply source must be routed far away from the guarded input area.

APPLICATION INFORMATION (continued)

Layout Example

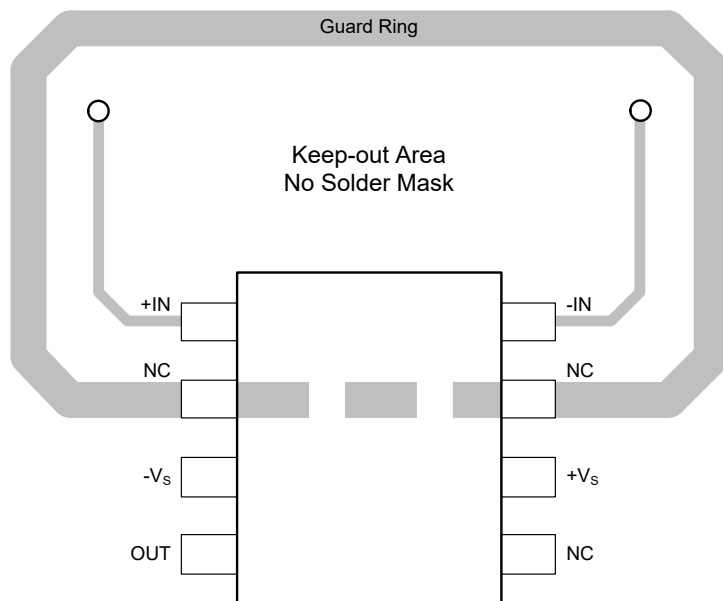


Figure 12. Layout Example Showing Guard Trace

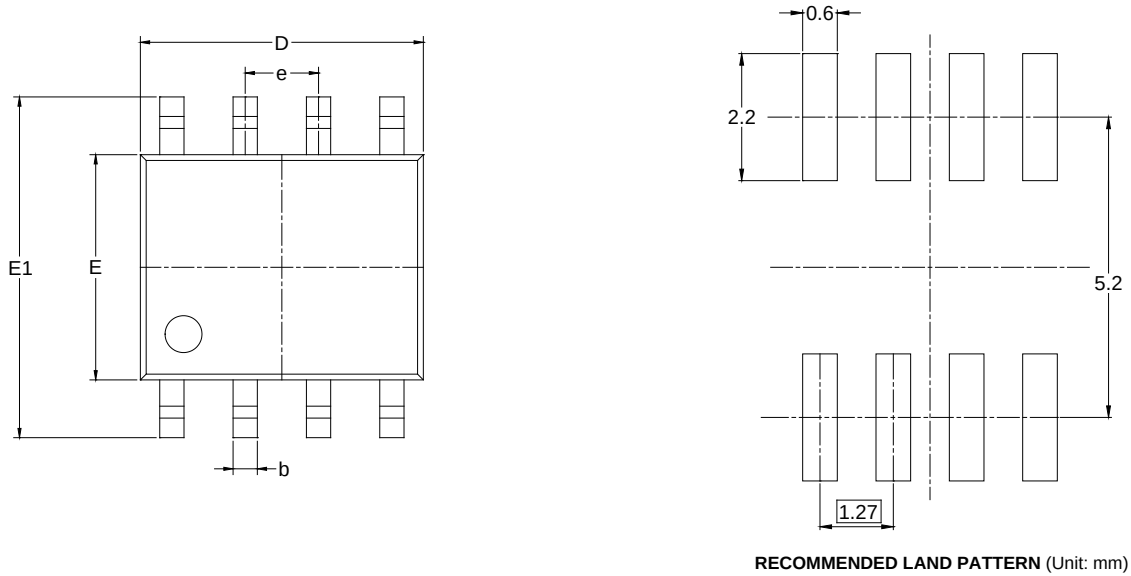
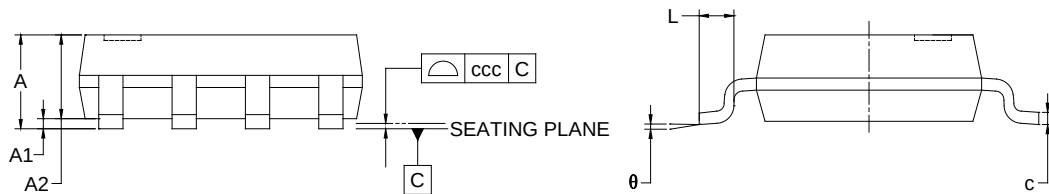
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

SOIC-8



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.350	-	1.550
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

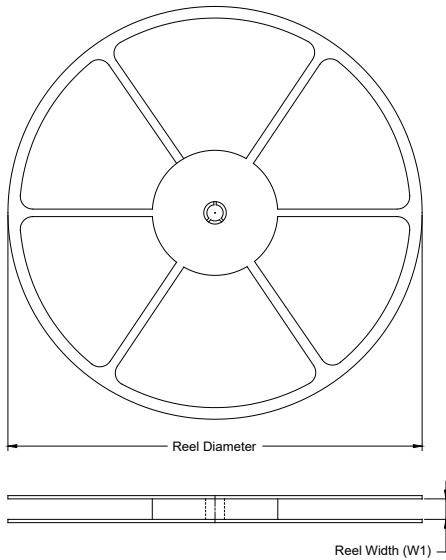
NOTES:

1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Reference JEDEC MS-012.

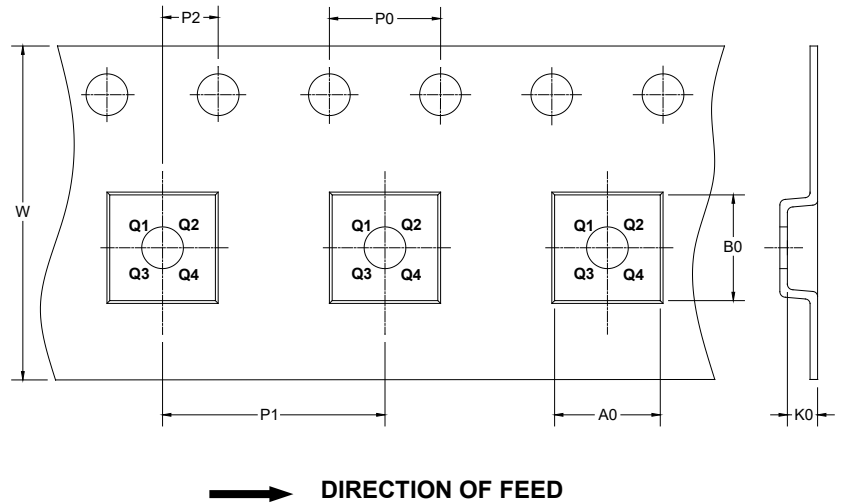
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

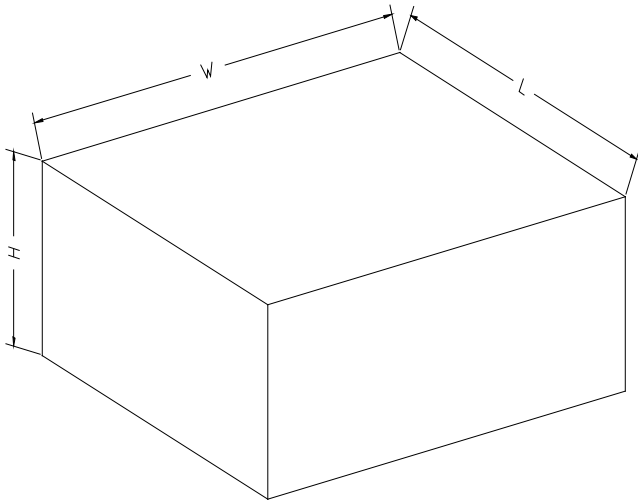
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002