SGM8257-1
High Voltage, High Current, Unity-Gain Stable, Operational Amplifier

GENERAL DESCRIPTION

The SGM8257-1 is a single, high voltage operational amplifier with high output drive capability. It can operate from 10V to 80V single supply or from ±5V to ±40V dual power supplies. The high voltage SGM8257-1 provides a wide input common mode voltage range and output voltage swing without phase inversion. The device is also capable of delivering a relatively high output current of ±50mA. It offers a gain-bandwidth product of 2.8MHz and can keep unity-gain stable in applications.

The SGM8257-1 includes built-in over-current and over-temperature protections. These conditions are monitored via the Status Flag pin, which is an open-drain output. When either condition occurs, the Status Flag pin goes active, alerting the system to take protective measures.

Additionally, the SGM8257-1 features a disable function. The E/D pin can enable or disable the output stage independently without affecting input signal transmission. The E/D COM pin serves as a common return, simplifying the connection of the E/D pin to low-voltage logic circuits. The disable function helps reduce power consumption and protects the load when the amplifier output is not needed.

The SGM8257-1 is available in a Green SOIC-8 (Exposed Pad) package. It is specified from 0℃ to +70℃ temperature range.

FEATURES

- **Support Single or Dual Power Supplies: 10V to 80V or ±5V to ±40V**
- **High Output Current: ±50mA**
- **Wide Output Voltage Swing: $(-V_S) + 1V$ to $(+V_S) - 1V$**
- **Independent Disable Function**
- **Over-Current Protection**
- **Over-Temperature Protection**
- **0℃ to +70℃ Operating Temperature Range**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Test Equipment
Medical Equipment
Current Sensing
Drivers of Piezoelectric Cells
Transducer Drivers
Servo Applications

SIMPLIFIED SCHEMATIC

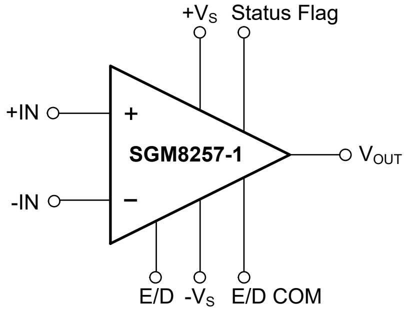


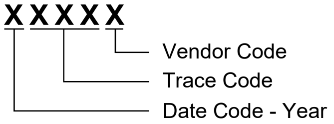
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8257-1	SOIC-8 (Exposed Pad)	0℃ to +70℃	SGM8257-1ZPS8G/TR	SGM 82571ZPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 100V

Signal Input Voltage Terminals

.... $(-V_S) - 0.3V$ to $(+V_S) + 0.3V$

Voltage, E/D to E/D COM 5.5V

Signal Input Current Terminals .... ±10mA

Output Short-Circuit Current (1) .... Continuous

Package Thermal Resistance

SOIC-8 (Exposed Pad), θ_{JA} .... 34.2℃/W

SOIC-8 (Exposed Pad), θ_{JB} .... 11.4℃/W

SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ .... 45.4℃/W

SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ .... 2.5℃/W

Package Thermal Characterization Parameter

SOIC-8 (Exposed Pad), ψ_{JT} .... 2.3℃/W

SOIC-8 (Exposed Pad), ψ_{JB} .... 11℃/W

Junction Temperature .... +150℃

Storage Temperature Range .... -65℃ to +150℃

Lead Temperature (Soldering, 10s) .... +260℃

ESD Susceptibility (2) (3)

HBM .... ±4000V

CDM .... ±1000V

NOTES:

1. Short-circuit to ground.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, $+V_S$ to $-V_S$ ....

.... 10V to 80V or ±5V to ±40V

Operating Temperature Range .... 0℃ to +70℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

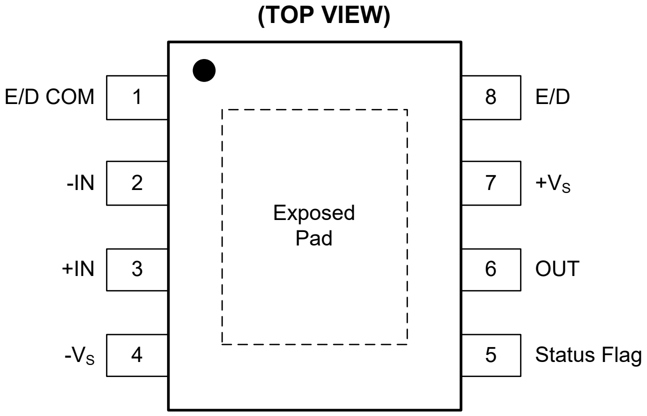
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	E/D COM	Enable/Disable Common. This pin is typically connected to a reference voltage or ground and serves as the reference level for the E/D pin.
2	-IN	Inverting Input.
3	+IN	Non-Inverting Input.
4	$-V_S$	Negative Power Supply.
5	Status Flag	Active-Low Open-Drain Output Referenced to the E/D COM. When either over-temperature or over-current condition occurs, the Status Flag pin goes active, alerting the system to take protective measures.
6	OUT	Output.
7	$+V_S$	Positive Power Supply.
8	E/D	Enable/Disable. When the E/D pin is left floating, the operational amplifier is enabled by default. To disable the operational amplifier, connect the E/D pin to a low logic level.
Exposed Pad	$-V_S$	Connect the exposed pad to $-V_S$. The exposed pad must always be soldered to the PCB, even in applications with minimal power dissipation.

ELECTRICAL CHARACTERISTICS

(V_S = ±40V, V_{CM} = V_{OUT} = mid-supply, R_L = 4.8kΩ to mid-supply, maximum and minimum values are at T_A = 0℃ to +70℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage		V_{OS}	I_{OUT} = 0mA		±0.1	±1.2	mV
Input Offset Voltage Drift (1)		$\Delta V_{OS}/\Delta T$	T_A = 0℃ to +70℃		±2	±5	μV/℃
Input Offset Voltage vs. Power Supply		PSRR	V_S = ±5V to ±40V, V_{CM} = 0V		±3	±20	μV/V
Input Bias Current		I_B	T_A = +25℃		±100	±600	pA
Input Offset Current		I_{OS}	T_A = +25℃		±100	±650	pA
Input Common Mode Voltage Range		V_{CM}	Linear operation	$(-V_S) + 2.5$		$(+V_S) - 2.5$	V
Common Mode Rejection Ratio		CMRR	$-15V \le V_{CM} \le 15V$	100	140		dB
			$-35V \le V_{CM} \le 35V$	100	146		
Open-Loop Voltage Gain		A_{OL}	$(-V_S) + 1V < V_{OUT} < (+V_S) - 1V$, R_L = 49kΩ, I_{OUT} = ±0.8mA	100	140		dB
			$(-V_S) + 1V < V_{OUT} < (+V_S) - 2V$, R_L = 4.8kΩ, I_{OUT} = ±8mA	90	113		
			$(-V_S) + 2V < V_{OUT} < (+V_S) - 3V$, R_L = 1880Ω, I_{OUT} = ±20mA	86	113		
Input Impedance	Differential				10^{11} || 6		Ω || pF
	Common Mode				10^{11} || 5		
Output Characteristics							
Output Voltage Swing from Rail		V_{OUT}	R_L = 49kΩ, $A_{OL} \ge$ 100dB, I_{OUT} = 0.8mA	$(-V_S) + 1$		$(+V_S) - 1$	V
			R_L = 4.8kΩ, $A_{OL} \ge$ 90dB, I_{OUT} = 8mA	$(-V_S) + 1$		$(+V_S) - 2$	
			R_L = 1880Ω, $A_{OL} \ge$ 86dB, I_{OUT} = 20mA	$(-V_S) + 2$		$(+V_S) - 3$	
Maximum Peak Current Output, Current Limit		I_{OUT}	Source		94		mA
			Sink		100		
Open-Loop Output Impedance		R_{OUT}	f = 1kHz		100		Ω
Capacitive Load Drive		C_L			200		pF
Output Disabled			Output capacitance		25		pF
Dynamic Performance							
Gain-Bandwidth Product		GBP	Small-signal		2.8		MHz
Slew Rate		SR	G = ±1, V_{OUT} = 60V step, R_L = 3.27kΩ		13		V/μs
Full-Power Bandwidth					55		kHz
Settling Time (2)	To ±0.1%	t_S	G = ±1, V_{OUT} = 20V step		3.5		μs
	To ±0.01%		G = ±5 or ±10, V_{OUT} = 60V step		10		
Total Harmonic Distortion + Noise (3)		THD+N	V_S = +40.6V/-39.6V, G = ±1, f = 1kHz, V_{OUT} = 37.7V_{P-P}		0.0005		%
Noise							
Input Voltage Noise			f = 0.01Hz to 10Hz		10		μV_{P-P}
Input Voltage Noise Density		e_n	f = 10Hz		250		$nV/\sqrt{Hz}$
			f = 10kHz		30		
Input Current Noise Density		i_n	f = 1kHz		160		$fA/\sqrt{Hz}$

NOTES:

1. Refer to simulation and characterization tests, mass production not tested.
2. See Settling Time section for more information.
3. The supplies are decreased to permit a closer swing to rails, constrained by the limitations of the test equipment.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±40V, V_{CM} = V_{OUT} = mid-supply, R_L = 4.8kΩ to mid-supply, maximum and minimum values are at T_A = 0℃ to +70℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Status Flag Pin (Referenced to E/D COM)						
Output Voltage		Normal operation			E/D COM + 2	V
		R_L = 10Ω during thermal overdrive, alarm	$(+V_S) - 2.5$			
Junction Temperature	T_J	Alarm (Status Flag high)		150		℃
		Return to normal operation (Status Flag low)		122		
Status Flag Delay		Enable → Disable		9		μs
		Disable → Enable		5		
		Over-current delay		25		
		Over-current recovery delay		12		
E/D (Enable/Disable) Pin (Referenced to E/D COM) (4)						
High (Output Enabled)	V_{SD}	Pin open or forced high	E/D COM + 2.5		E/D COM + 5	V
Low (Output Disabled)		Pin forced low	E/D COM		E/D COM + 0.65	V
Output Disable Time				4.5		μs
Output Enable Time				4.5		μs
E/D COM Pin						
Voltage Range			$(-V_S)$		$(+V_S) - 5$	V
Power Supply						
Operating Voltage Range	V_S		±5		±40	V
Quiescent Current	I_Q	I_{OUT} = 0mA		4.3	7	mA
Quiescent Current in Shutdown Mode	I_{SD}	I_{OUT} = 0mA, $V_{E/D}$ = 0.65V		220	300	μA
Temperature Range						
Operating Range	T_A		0		70	℃

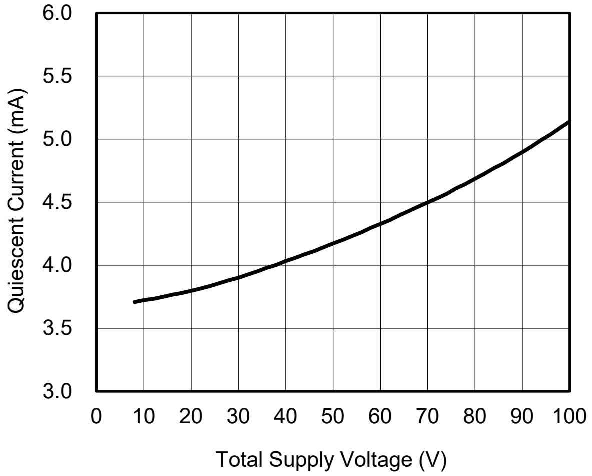
NOTE:

4. To enable the operational amplifier, connect the E/D pin to a high logic level.

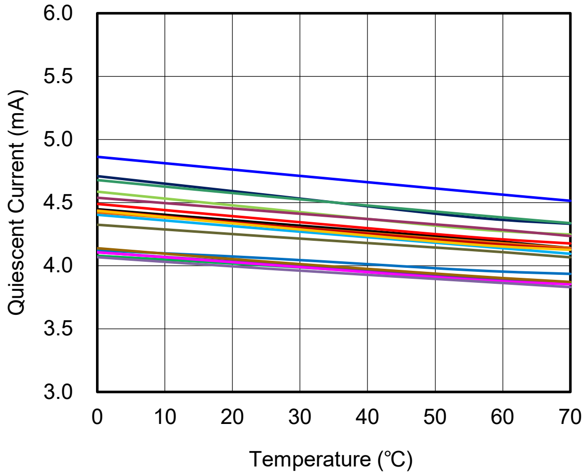
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

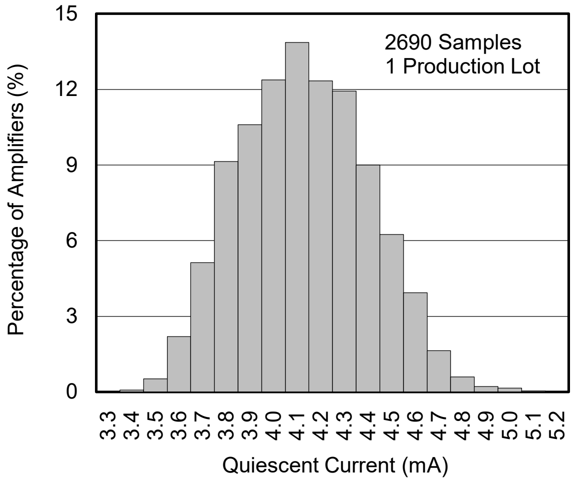
Quiescent Current vs. Total Supply Voltage



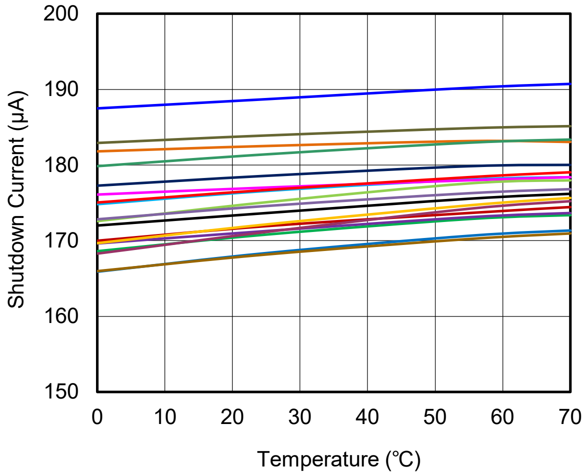
Quiescent Current vs. Temperature



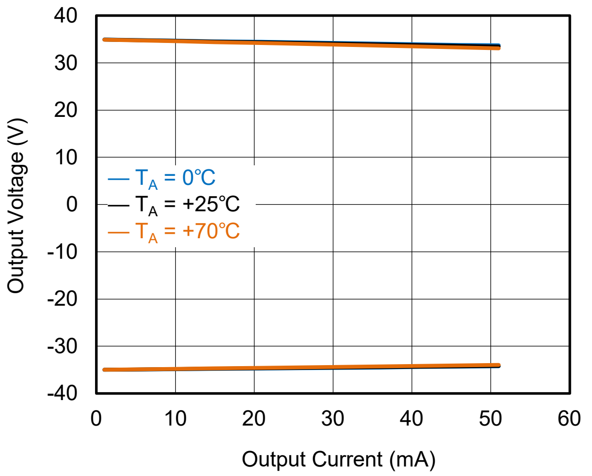
Quiescent Current Production Distribution



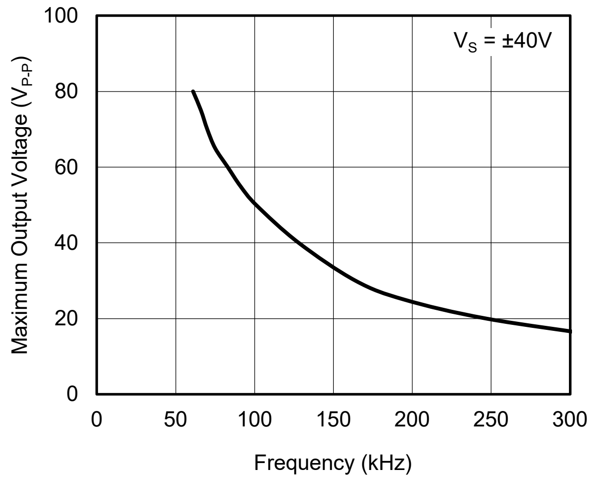
Shutdown Current vs. Temperature



Output Voltage vs. Output Current

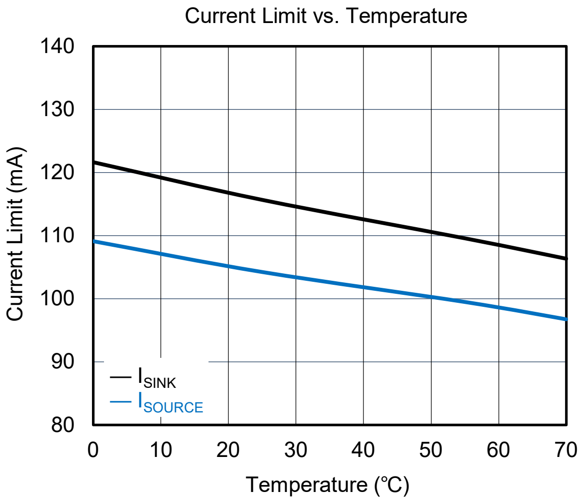


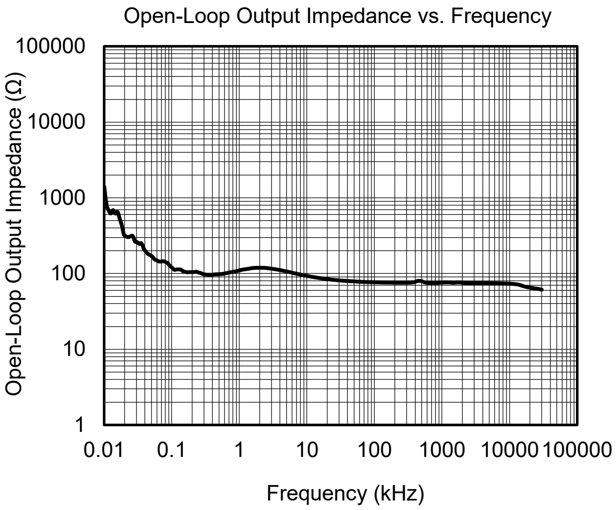
Maximum Output Voltage vs. Frequency

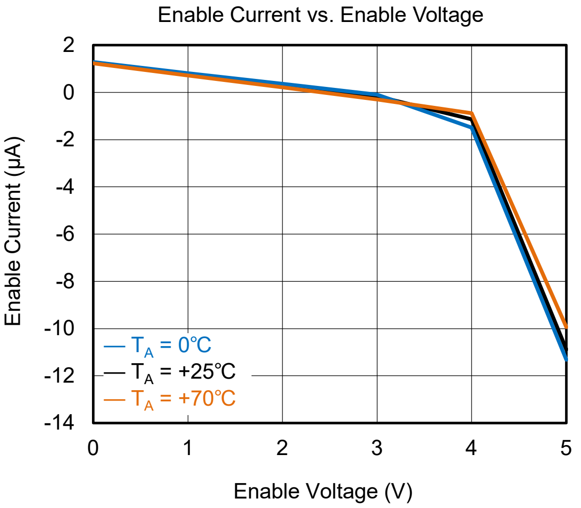


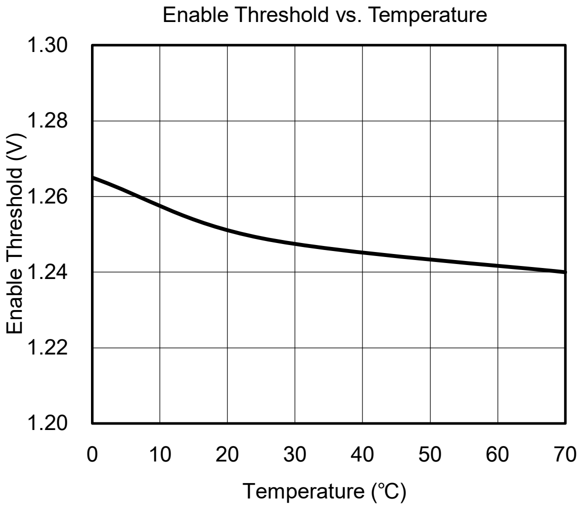
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

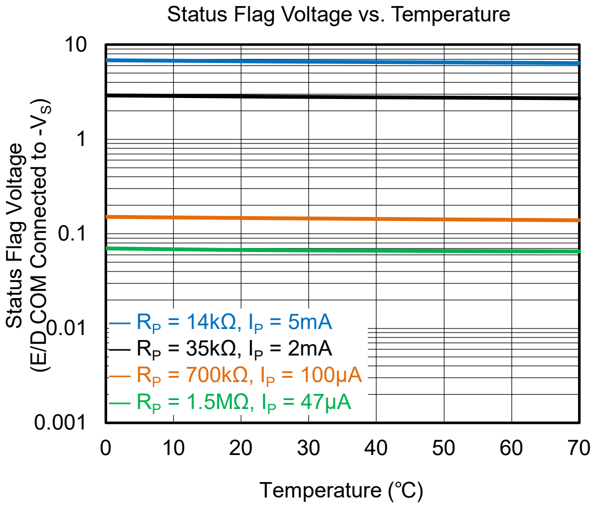
At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

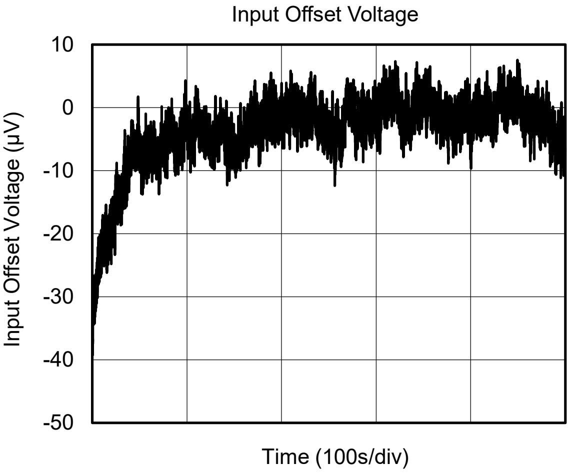






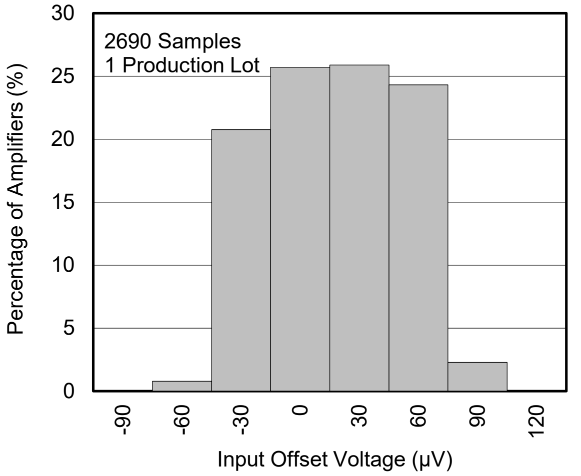


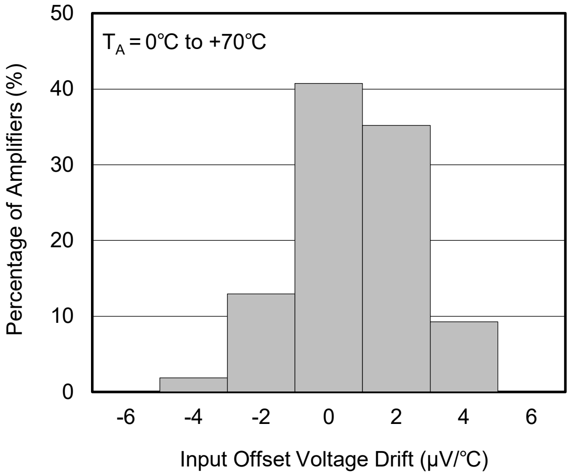


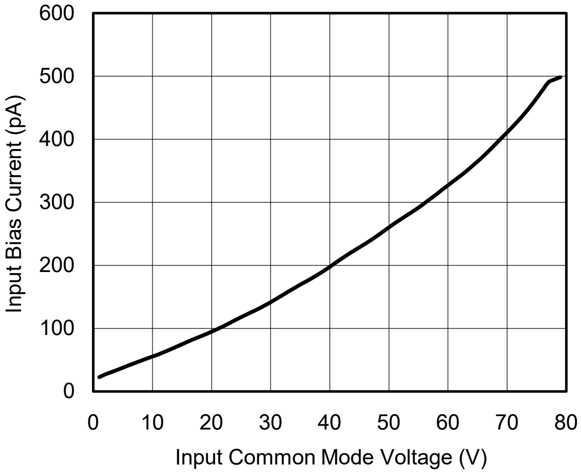


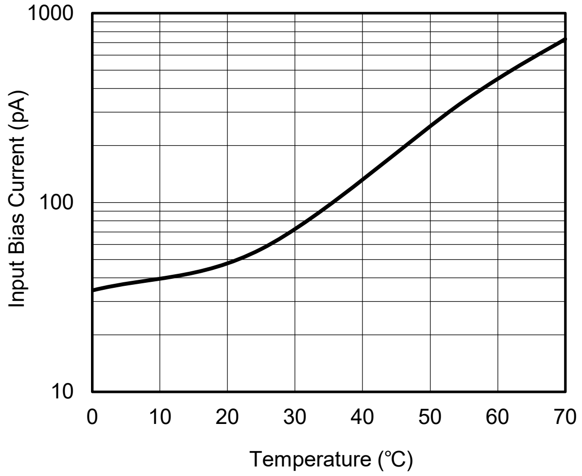
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

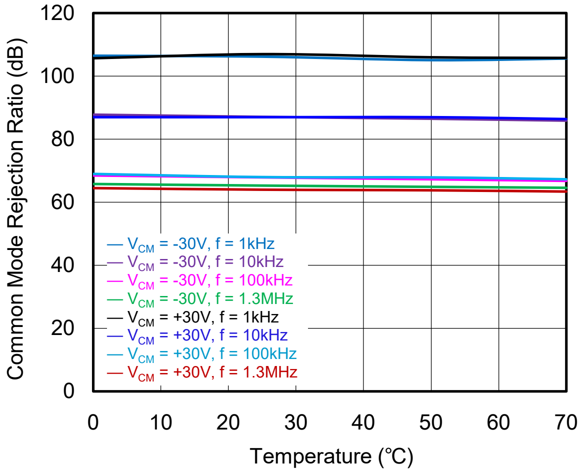
At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

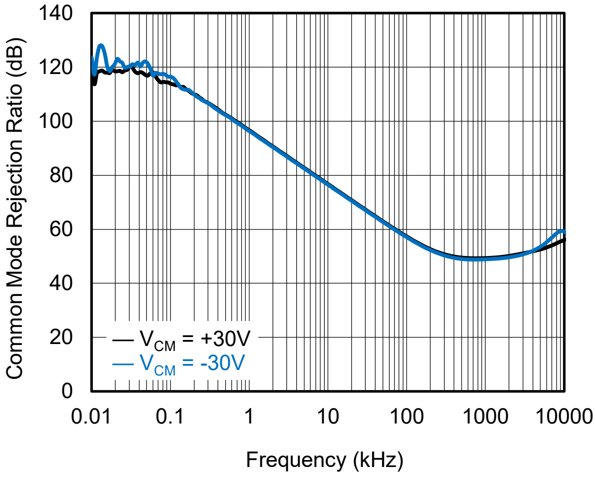

Input Offset Voltage Production Distribution


Input Offset Voltage Drift Distribution


Input Bias Current vs. Input Common Mode Voltage

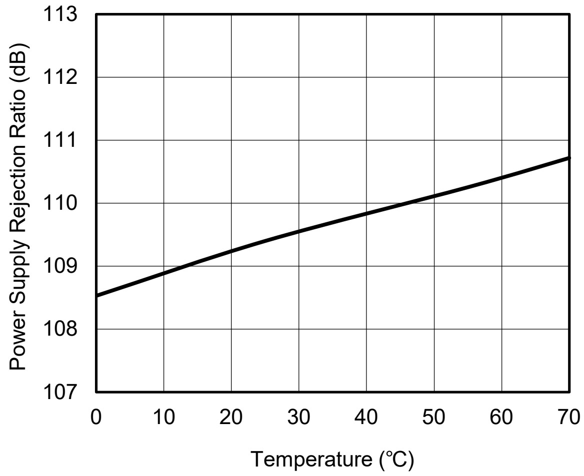

Input Bias Current vs. Temperature

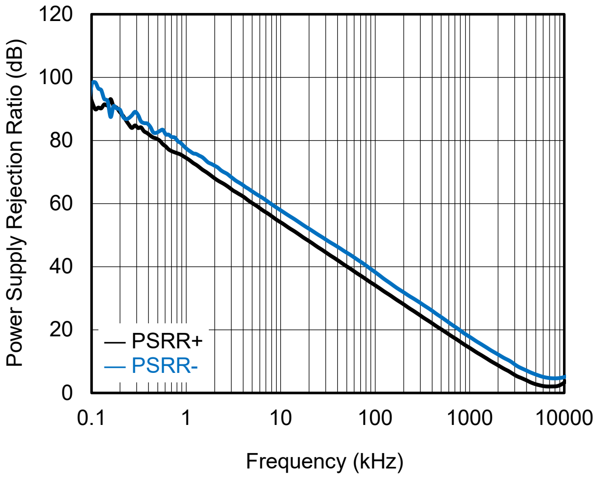

CMRR vs. Temperature

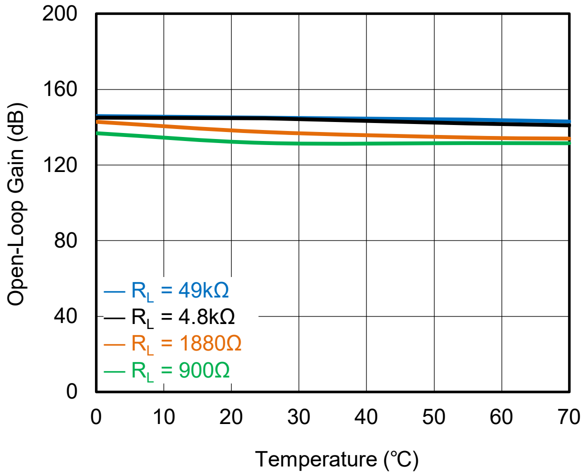

CMRR vs. Frequency

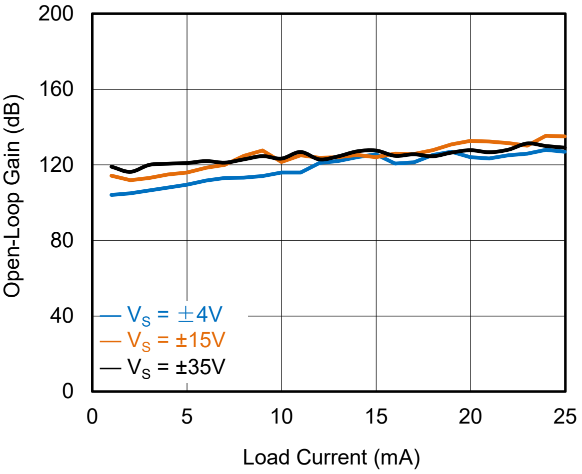
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

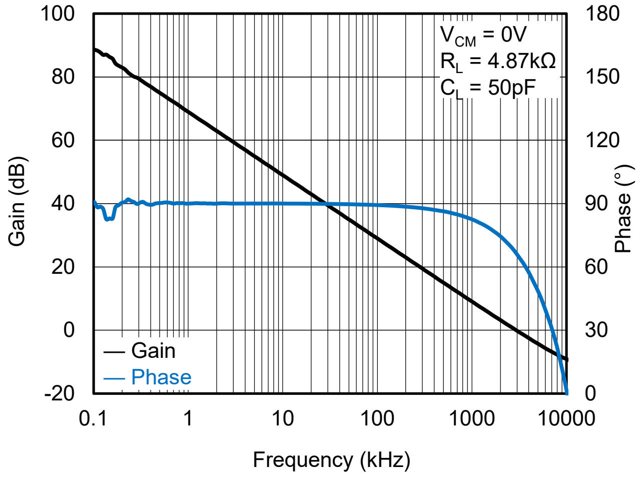
At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

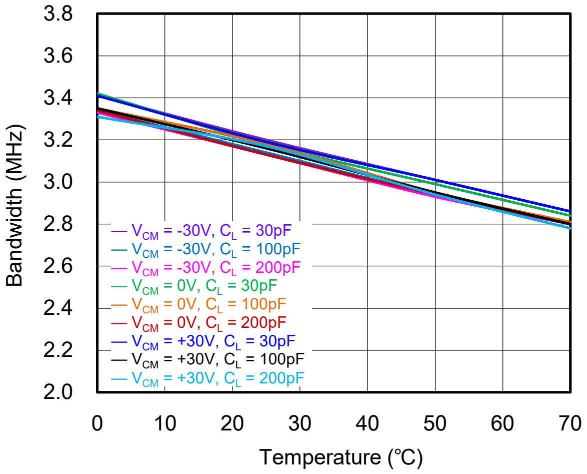

PSRR vs. Temperature


PSRR vs. Frequency


Open-Loop Gain vs. Temperature


Open-Loop Voltage Gain vs. Load Current

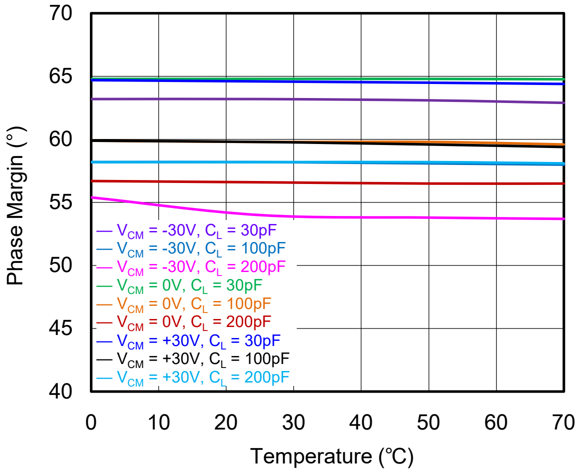

Open-Loop Gain and Phase vs. Frequency


Unity-Gain Bandwidth vs. Temperature

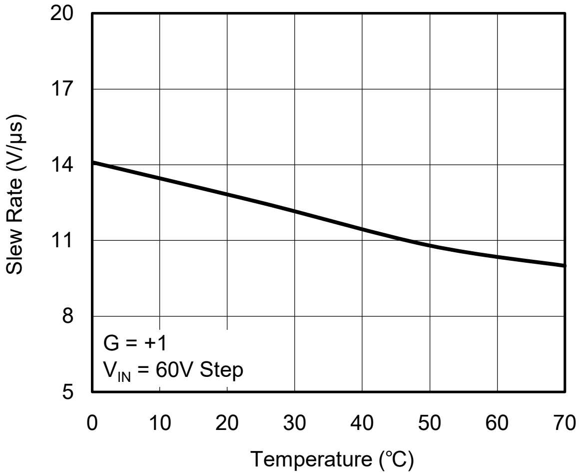
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

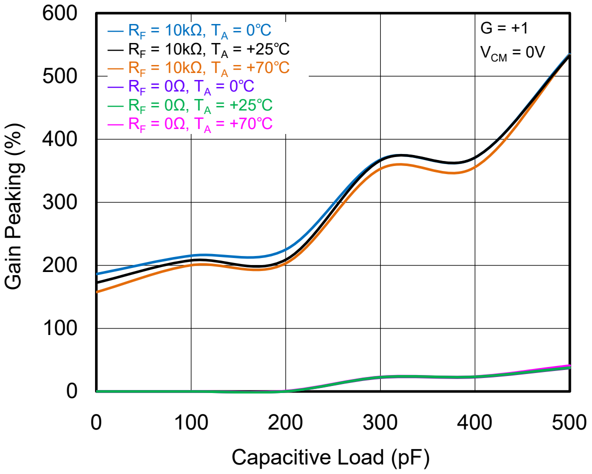
Phase Margin vs. Temperature



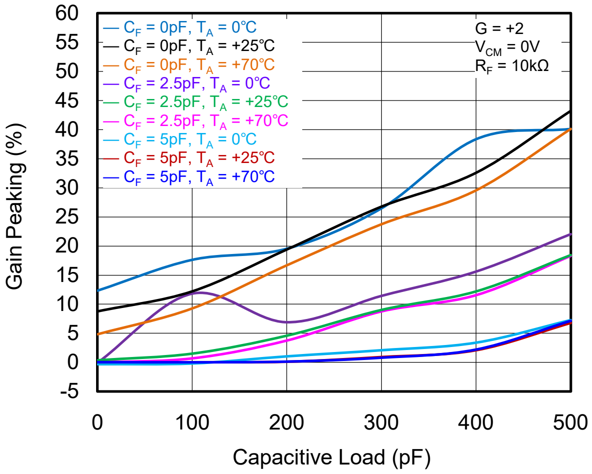
Slew Rate vs. Temperature



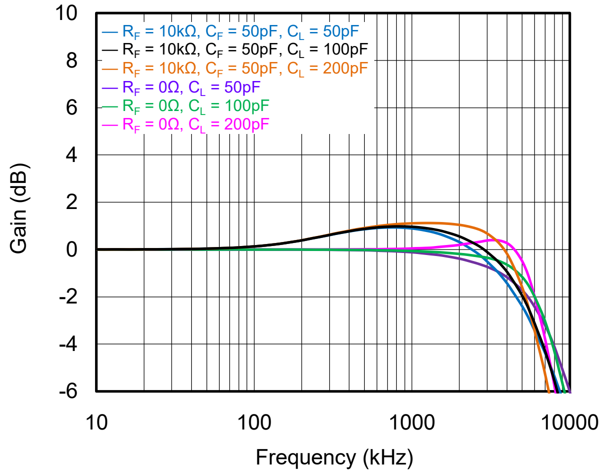
Gain Peaking vs. Capacitive Load



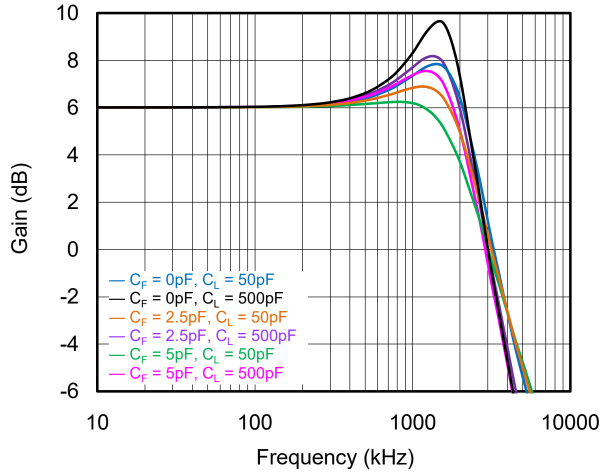
Gain Peaking vs. Capacitive Load



Gain of +1 vs. Frequency

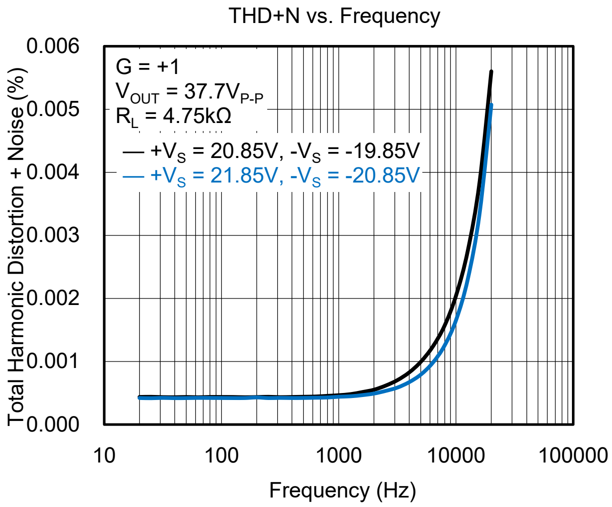


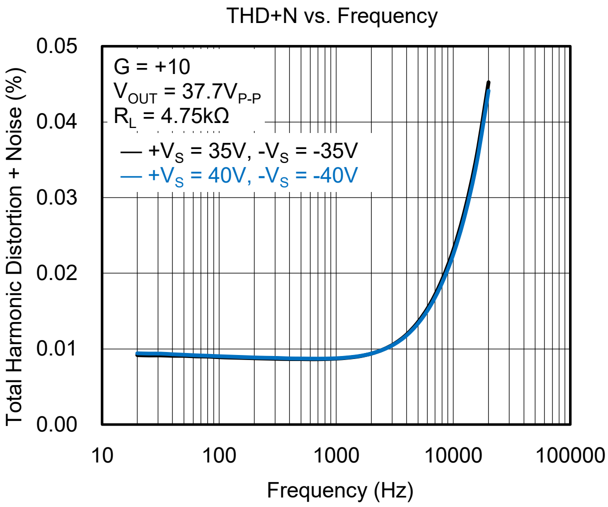
Gain of +2 vs. Frequency

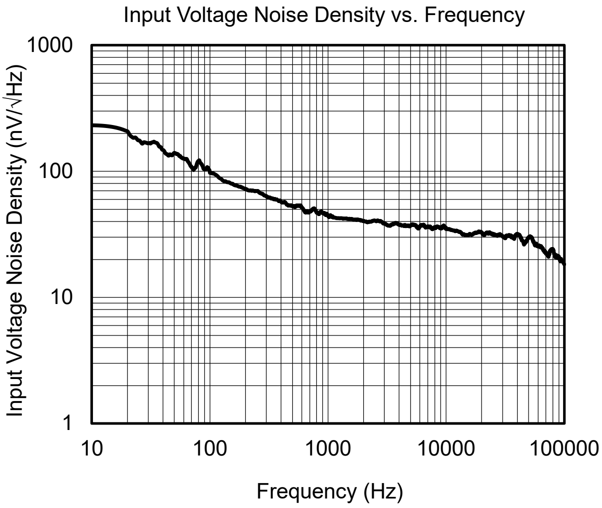


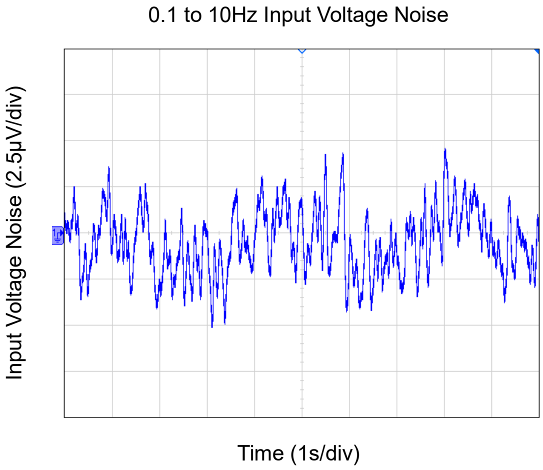
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

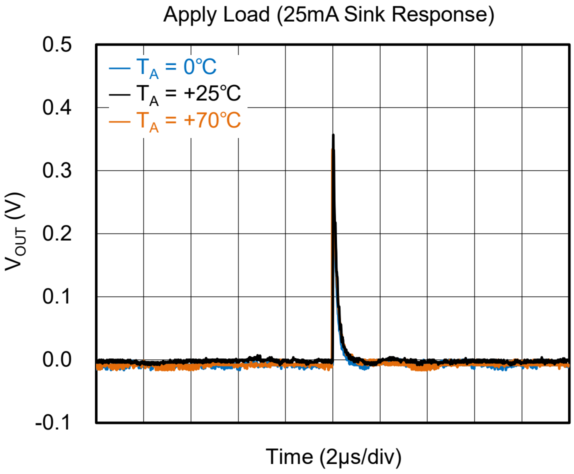
At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

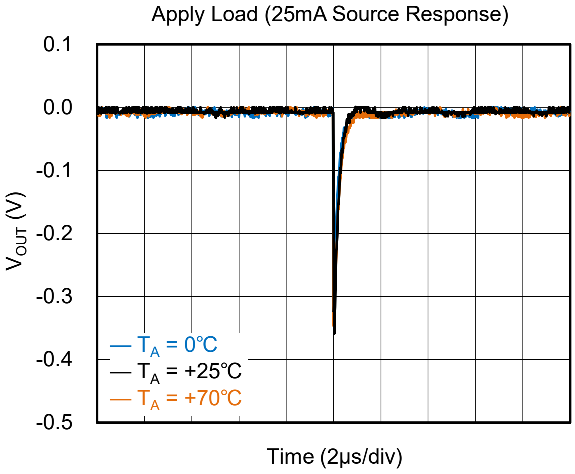

THD+N vs. Frequency


THD+N vs. Frequency


Input Voltage Noise Density vs. Frequency

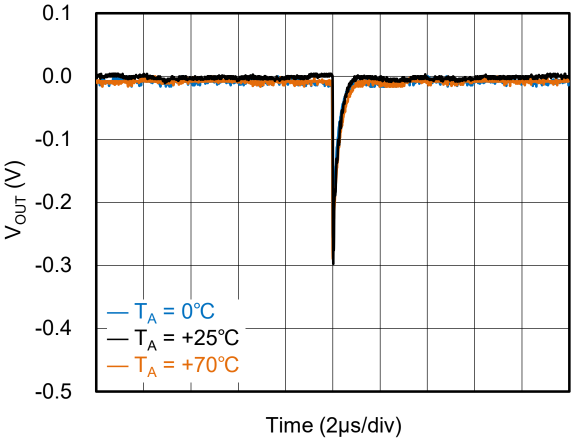

0.1 to 10Hz Input Voltage Noise


Apply Load (25mA Sink Response)


Apply Load (25mA Source Response)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.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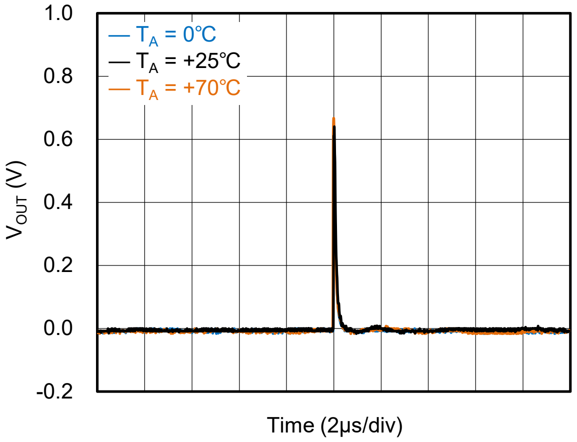
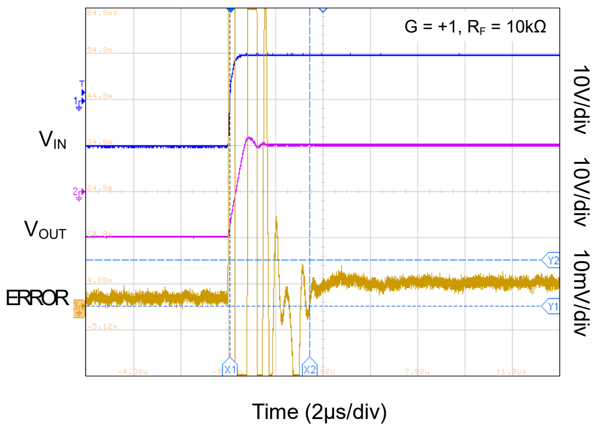
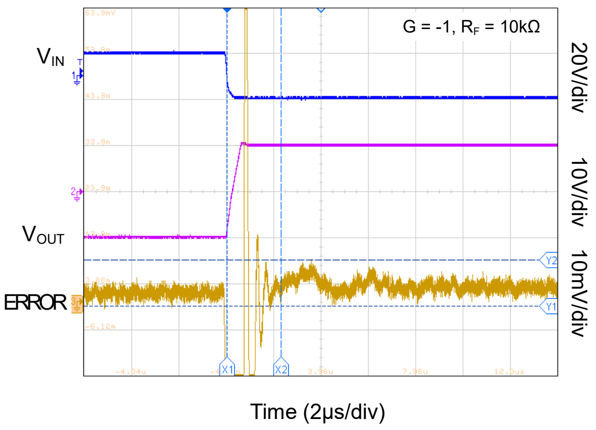
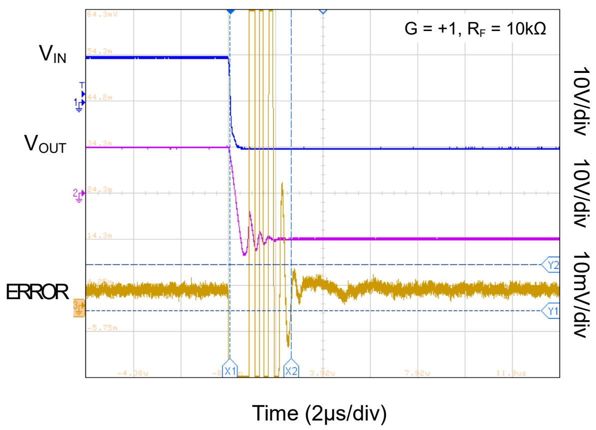
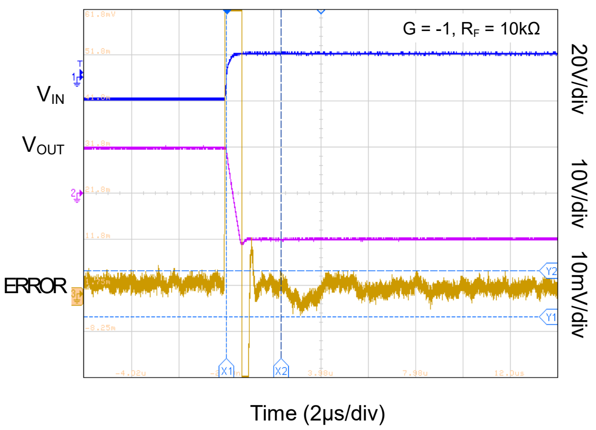

Remove Load (25mA Source Response)


Settling Time (Positive)


Settling Time (Positive)

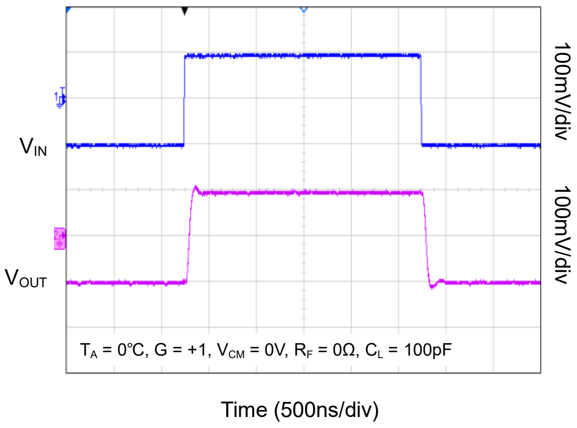

Settling Time (Negative)


Settling Time (Negative)

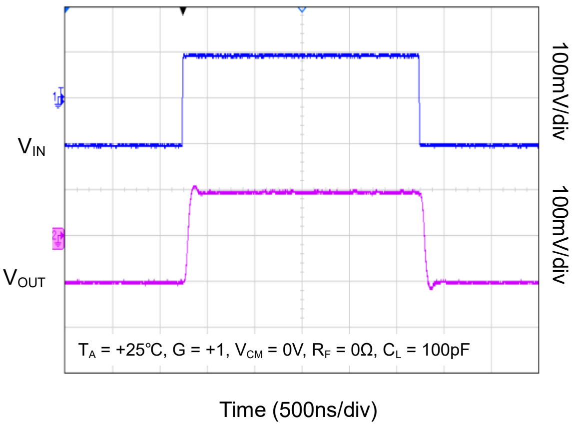
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

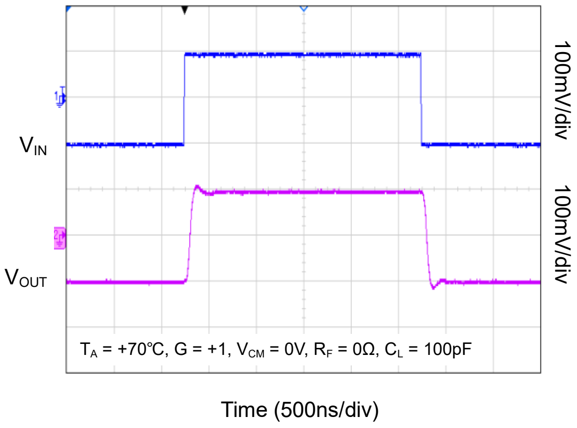
Small-Signal Step Response



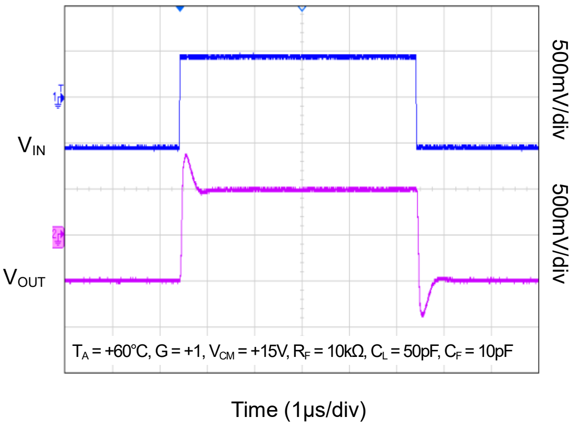
Small-Signal Step Response



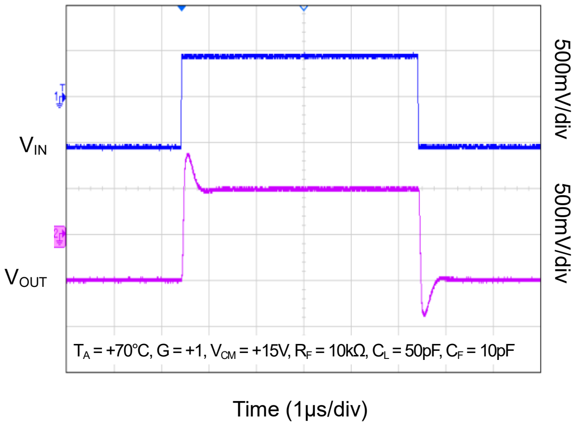
Small-Signal Step Response



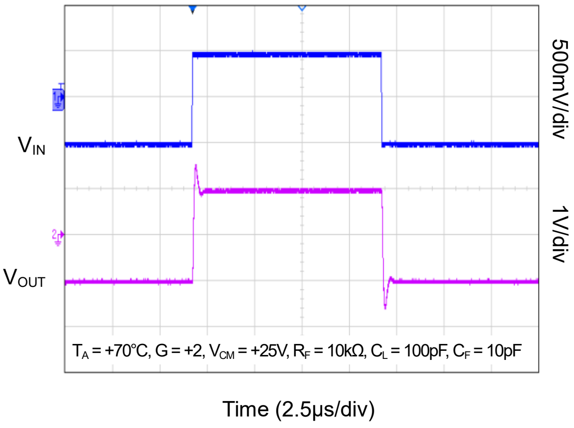
Large-Signal Step Response



Large-Signal Step Response



Large-Signal Step Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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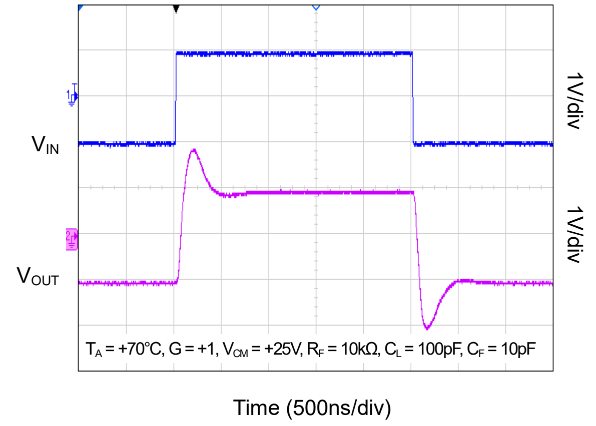
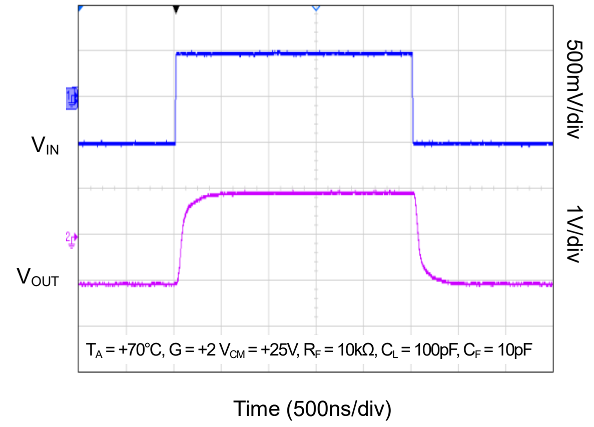
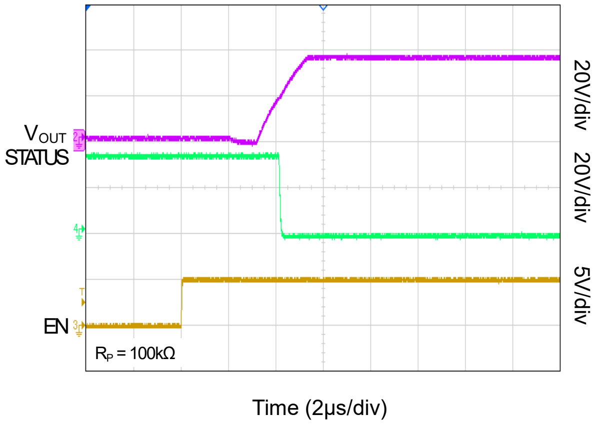
Step Response



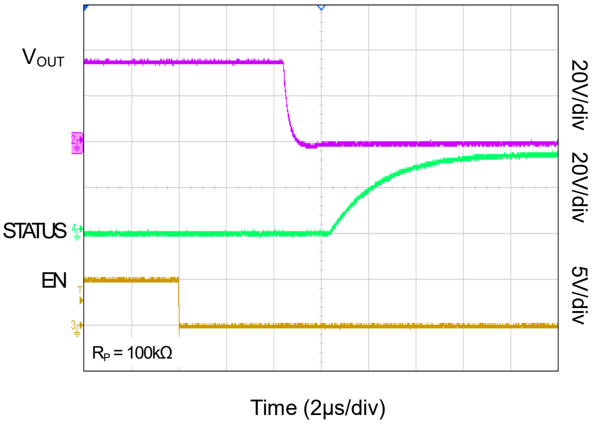
Step Response



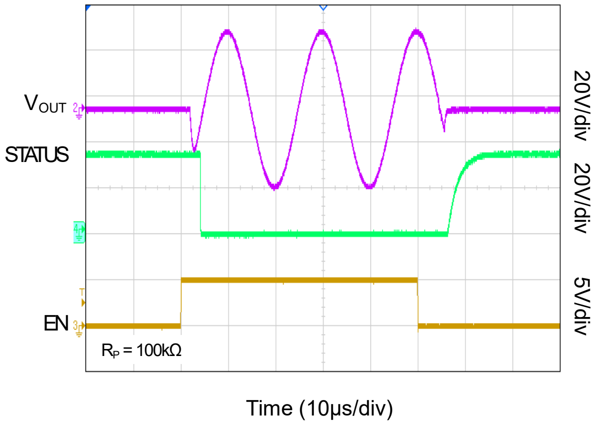
Enable Response Time



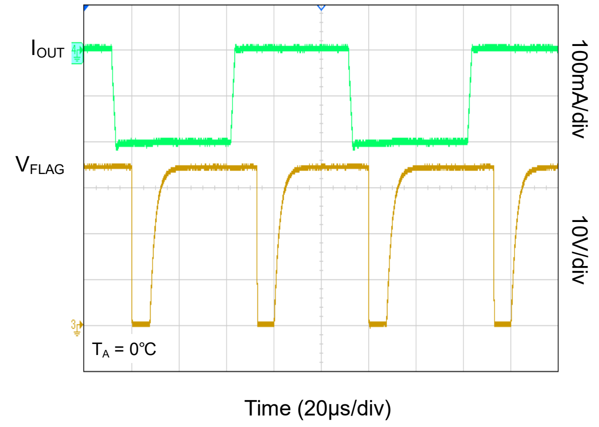
Disable Response Time



Enable Response Time



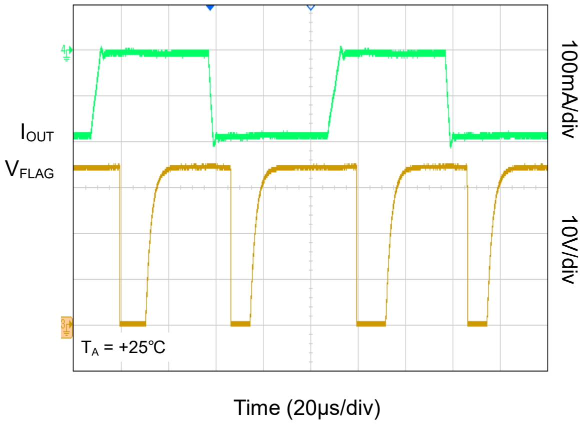
I_{LIMIT} Showing Flag Delay



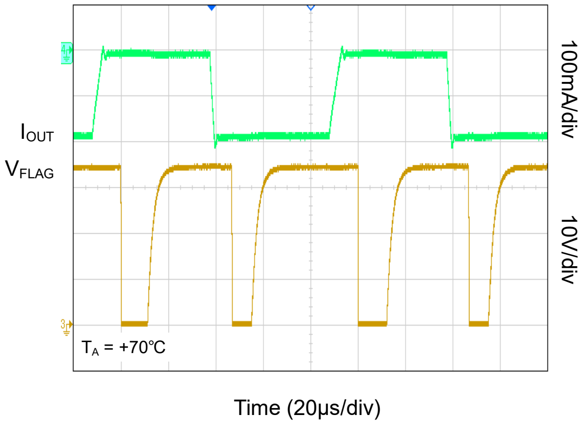
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±35V, and R_L = 4.8kΩ connected to GND, unless otherwise noted.

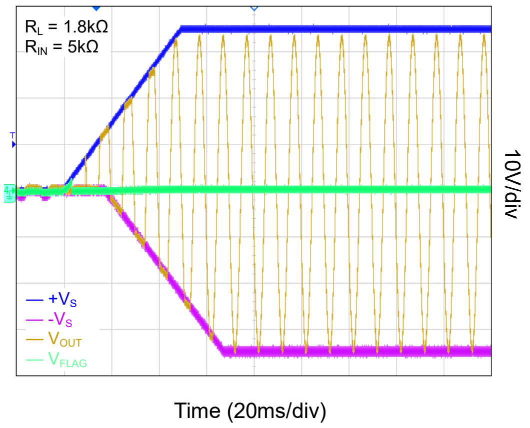
I_{LIMIT} Showing Flag Delay



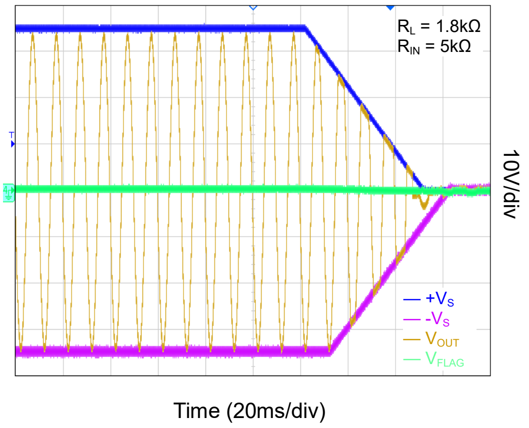
I_{LIMIT} Showing Flag Delay



Power On



Power Off



FUNCTIONAL BLOCK DIAGRAM

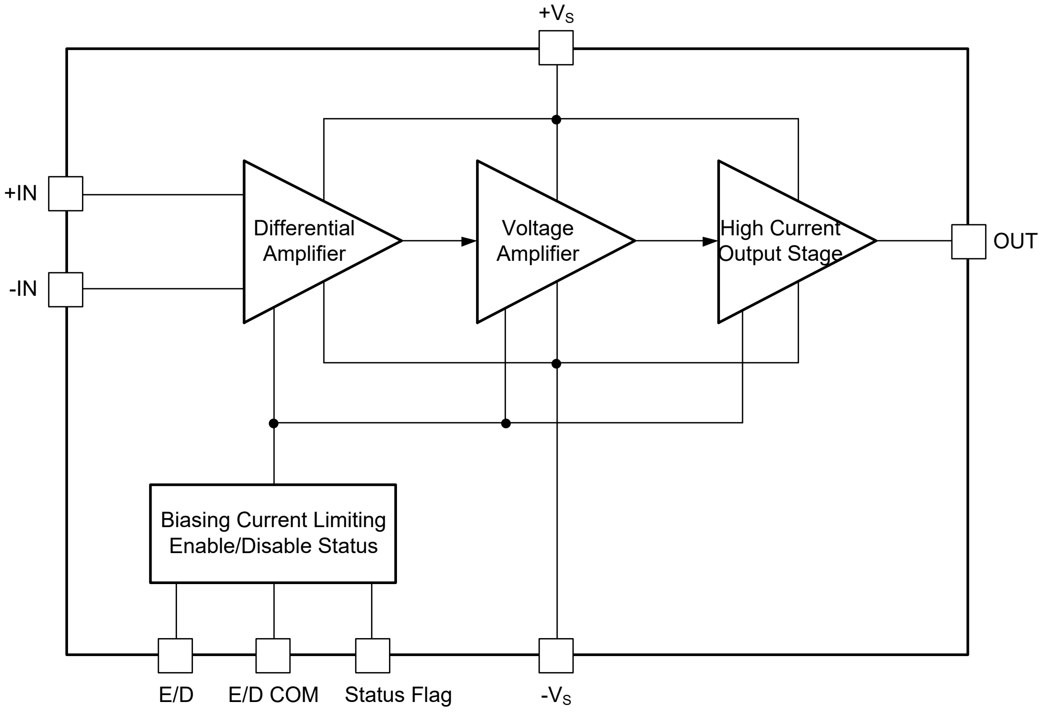


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM8257-1 features a maximum operating voltage of 80V and an output current capability of 50mA. The device offers stable unity-gain operation with a gain-bandwidth product of 2.8MHz. It provides wide input common mode voltage range and output voltage swing, and the output phase is not reversed within the specified input range. The accuracy performance of SGM8257-1 is excellent. Moreover, the SGM8257-1 is suitable for ±5V and ±40V applications, especially for those whose the power supply exceeds 36V.

The SGM8257-1 integrates internal protection mechanisms for both input and output stages. For the input stage, the operational amplifier's internal structure provides protection against multiple fault conditions. For the output stage, over-current and over-temperature events are detected and indicated by the Status Flag pin. Moreover, one of the advantages of SGM8257-1 is that the output swings within 1V with the output current equal to ±50mA. The power consumption can be automatically high or low when the E/D pin is controlled by an external device. The E/D pin and Status Flag pin are related, specifically, the Status Flag will indicate a fault condition and be pulled high when the E/D pin is applied low.

Input Protection

The internal protective mechanism can protect the SGM8257-1 from excessive differential input voltage or input terminals exceeding the power supply voltage, without any series resistors in front of the input terminals. The series JFET located at the input stage can limit the internal current to a non-damaging 10μA for excessive differential or common mode input voltage. Moreover, a dielectric material is inserted between the device and the substrate. On top of this, the IC fabrication process for the SGM8257-1 is also free from the traditional limitations of junction isolation.

Input Range

The SGM8257-1 operates at a linear operational range when the input voltage swings within the range of (-V_S) + 2.5V and (+V_S) - 2.5V. Commonly, the unity-gain configuration is the most general application. Figure 6 indicates the test circuit for Figure 3 and Figure 4, which illustrate the output behavior when the input reaches +V_S or -V_S. Figure 5 shows the output response when the input voltage reaches (-V_S) + 1V. The phase reversal effect caused by excessive input voltage can be mitigated by adding a series resistor at the input terminal.

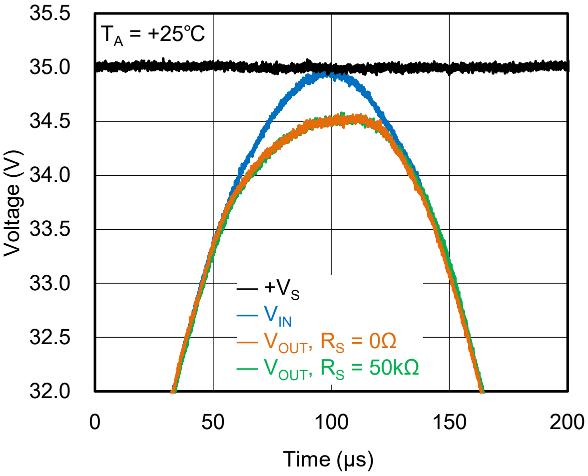


Figure 3. Output Response when Input Voltage Reaches +V_S

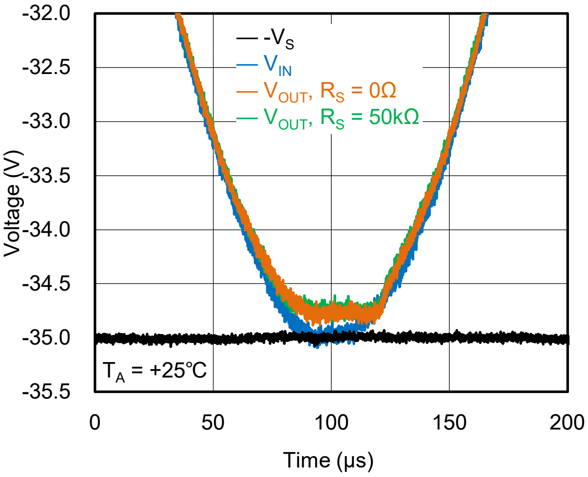


Figure 4. Output Response when Input Voltage Reaches -V_S

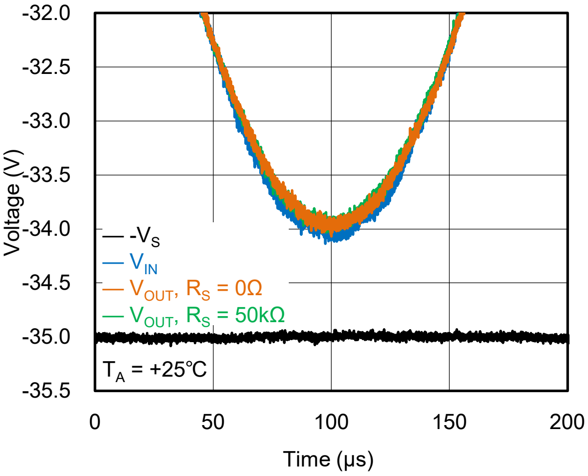


Figure 5. Output Response when Input Voltage Reaches (-V_S) + 1V

DETAILED DESCRIPTION (continued)

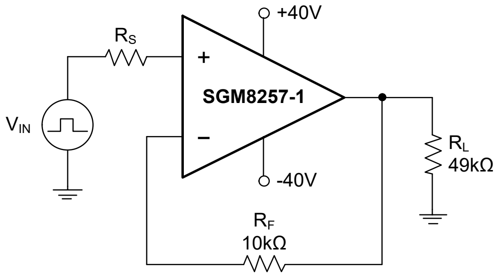


Figure 6. Input Range Test Circuit

Output Range

With a 49kΩ load, the SGM8257-1 achieves an output swing within 1V of the supply rails. Output swing decreases as the output current is increases. With a 1.88kΩ load, this device delivers an output swing within 2V of the ($-V_S$) and 3V of the ($+V_S$).

Settling Time

Settling time is measured using the circuit shown in Figure 7. The false-summing circuit at the top is utilized for both settling time and open-loop gain measurements. The two resistors R_1 and R_2 are used for isolating the summing junction from the probe and also provide a gain to the circuit, which will cause oscillation.

The combined output of the inverting and non-inverting circuits is applied by the circuit at the bottom, removing the large output response by the resistors R_5 and R_6. The summing point at V_2 illustrates the output settling time.

Settling time measurement for different gain configurations are listed in Table 1.

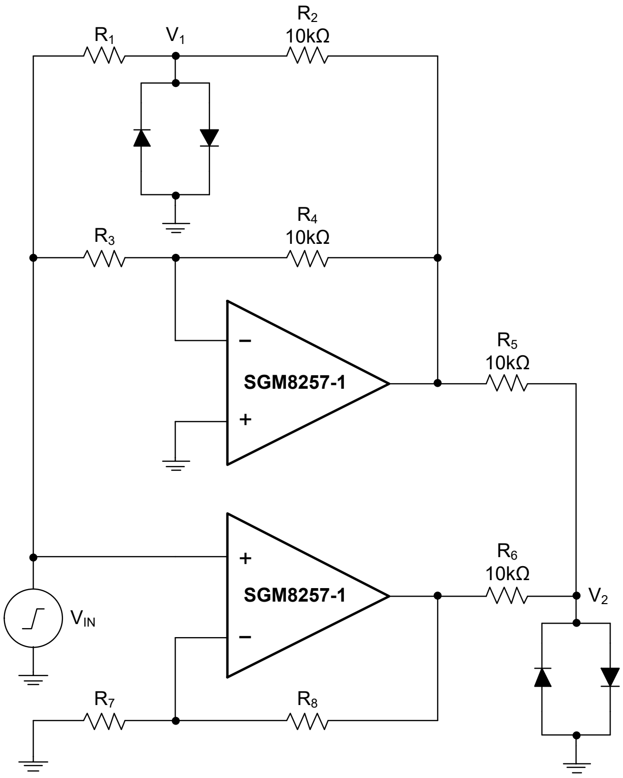


Figure 7. Settling Time Test Measurement Circuit

Table 1. Settling Time Measurement Configuration of Gain for Figure 7

Component	Gain		
	1	5	10
R_1	10kΩ	2kΩ	1kΩ
R_3	10kΩ	2kΩ	1kΩ
R_7	∞	1kΩ	1kΩ
R_8	10kΩ	4kΩ	9kΩ
V_{IN}	$20V_{P-P}$	$12V_{P-P}$	$6V_{P-P}$

DETAILED DESCRIPTION (continued)

E/D and E/D COM

If E/D COM is left floating, it will be driven to -V_S by a 15μA internal current source. If E/D is floating, it will be 2V higher than E/D COM, driven by a 1μA internal current source. Although the SGM8257-1 can still operate when both E/D and E/D COM are floating, a fast negative-coupled signal may cause the device to shut down by overpowering the 1μA current source. This phenomenon, which can be illustrated as an oscillation, occurs frequently at extremely low temperatures. If the enable function is not intended for use, the conservative method is to place a 30pF capacitor between the E/D pin and the low-impedance source. Moreover, an alternative way is to provide a sufficient current source from +V_S to keep E/D above the threshold of shutdown. The recommended connection for E/D is shown in Figure 8. The 1MΩ pull-up resistor R_P, connected between +V_S and E/D, can provide a 40μA current source to the E/D pin.

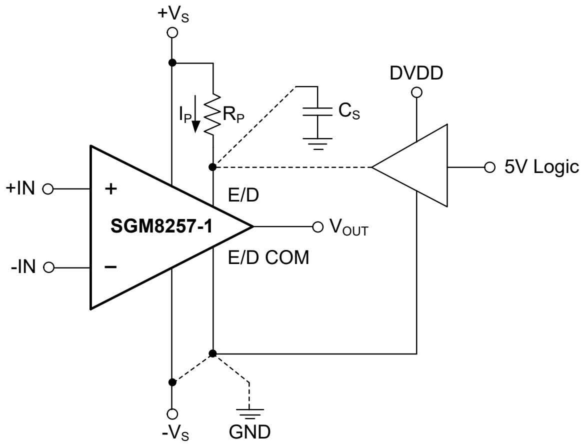


Figure 8. E/D and E/D COM

Current Limit

The internal limitation of the output transistors can limit the output current. Also, the output can continuously support the limited current when the operating temperature is below +70℃. However, if the SGM8257-1 is powered by the lowest specified supply voltages with sufficient heat-sinking, the device can continuously deliver the limited current without triggering thermal shutdown. For the consideration of reliability, users should avoid cyclical operation of the thermal shutdown mechanism, even though research has shown that the device can operate in this mode for 1000 hours with minimal parametric shifts. In addition, good heat-sinking (achieved either via airflow or a physical plate) is required to maintain the device's operating temperature below the threshold of shutdown. For the operating life considerations, the junction temperature should always be below +150℃.

Device Functional Modes

The output disable function of SGM8257-1 conserves power (I_{SD} = 220μA). Also, this function protects the load without disturbing the input signal path. For shutdown loop control, this achievement is also useful.

APPLICATION INFORMATION

The SGM8257-1 has the capability of high voltage and output current and can be applied under the power supply conditions of ±5V and ±40V. This design enables the SGM8257-1 to operate in high supply voltage and high output swing situations that other traditional operational amplifiers cannot reach. Also, the output swing can be one volt or several volts within the supply rails, which is determined by the output current. Moreover, the SGM8257-1 incorporates multiple protection mechanisms such as input over-voltage protection, output current-limit protection, thermal shutdown protection, and the E/D function.

Lowering Offset Voltage and Drift

Figure 9 illustrates that the SGM8257-1 and SGM8253-1 (zero-drift series) can be combined to provide ultra-low input offset temperature drift while supporting high supply rails.

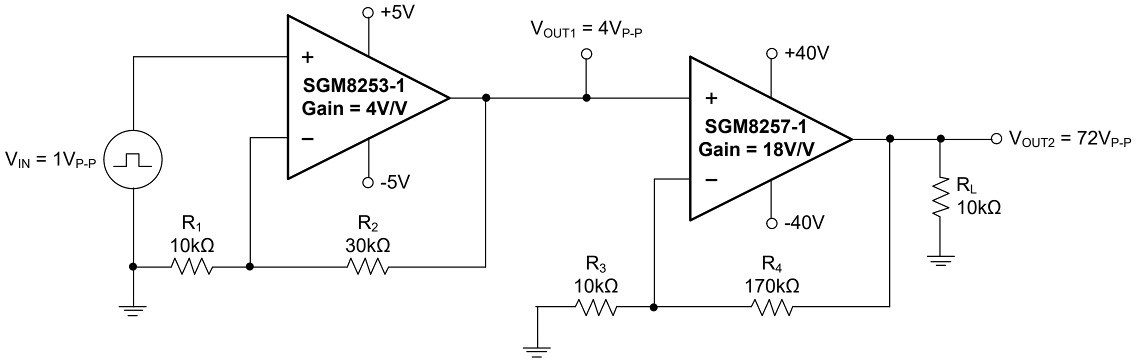
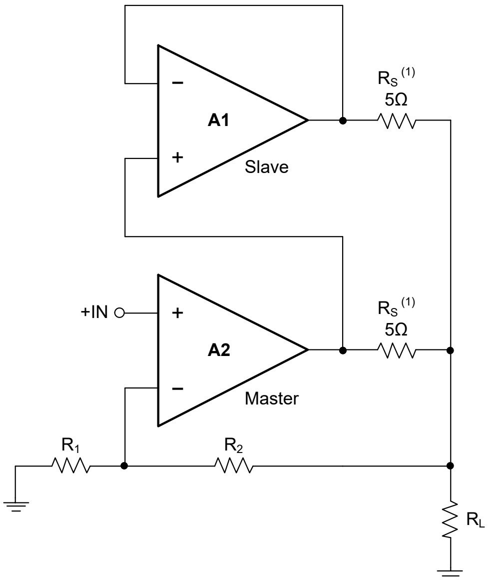


Figure 9. Two-Stage, High Voltage Operational Amplifier Circuit with Ultra-Low Input Offset Temperature Drift

APPLICATION INFORMATION (continued)

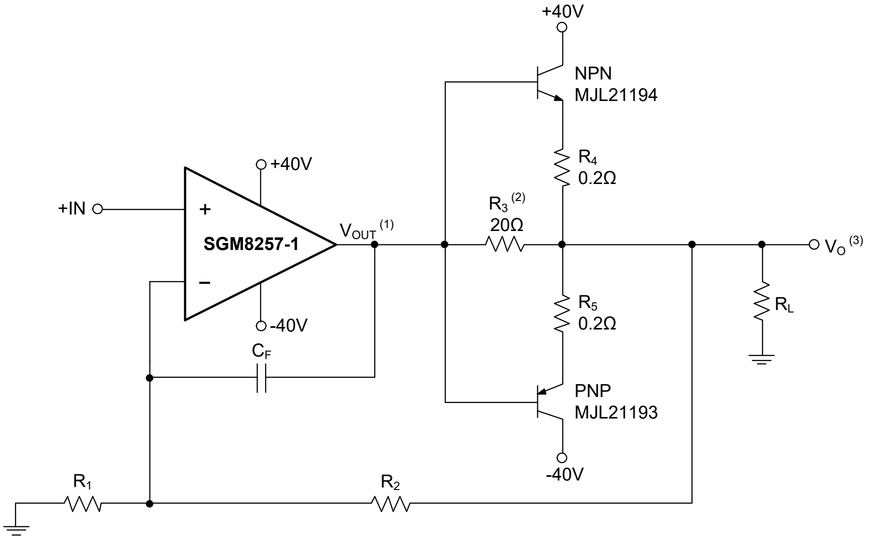
Increasing Output Current

Two or more SGM8257-1 units can be paralleled to enhance the driving capability of the output current for better performance. The master operational amplifier (A2) can be configured in nearly all amplifier circuits. The slave operational amplifier (A1) should be configured as a buffer circuit without feedback resistor. In addition, external output transistors may be added if higher output current capability is required. In Figure 10, the circuit with SGM8257-1 or external transistor can achieve an output current of 1A.



NOTE: 1. The R_S should always be placed to prevent any external current from flowing caused by the input offset voltage errors between the two operational amplifiers.

Figure 10. Parallel Amplifiers Increase Output Current Capability



NOTES:

1. The output of the SGM8257-1 can swing from +37V to -38V with suitable output loading.

2. Current limits consideration for SGM8257-1 and also allows the operation of the circuit if the output voltage is within ±0.7V (avoiding crossover distortion).

3. For 1A loading, the V_{OUT} of SGM8257-1 can swing from +34.1V to -35.1V.

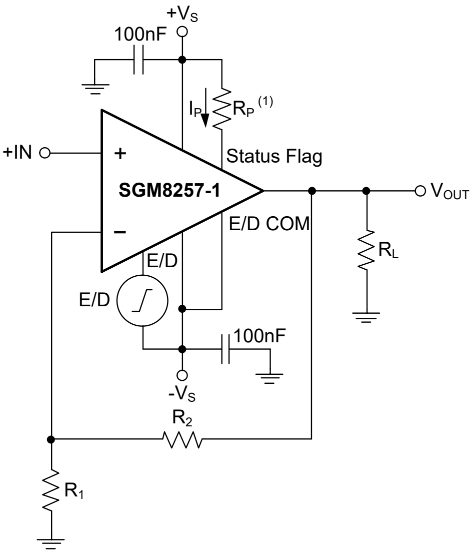
Figure 11. 1A Loading Application Achieved by SGM8257-1 and External Transistors

APPLICATION INFORMATION (continued)

Basic Non-Inverting Amplifier

The non-inverting circuit is shown in Figure 12. The SGM8257-1 can be operated with the power supplies of ±5V to ±40V with excellent linearity, which is acceptable for the applications with power supplies exceeding 36V.

The 100nF bypass capacitors should be connected to the terminals of the two supply pins as close as possible. Also, the voltage rating of the capacitors should be much larger than the corresponding operating supply voltage.



NOTE: 1. Pull-up resistor with at least 15μA (choose R_P = 1MΩ with $+V_S$ = 40V for I_P = 40μA).

Figure 12. Configuring the SGM8257-1 as a Non-inverting Circuit

Programmable Voltage Source

Figure 13 illustrates the SGM8257-1 in a programmable voltage source.

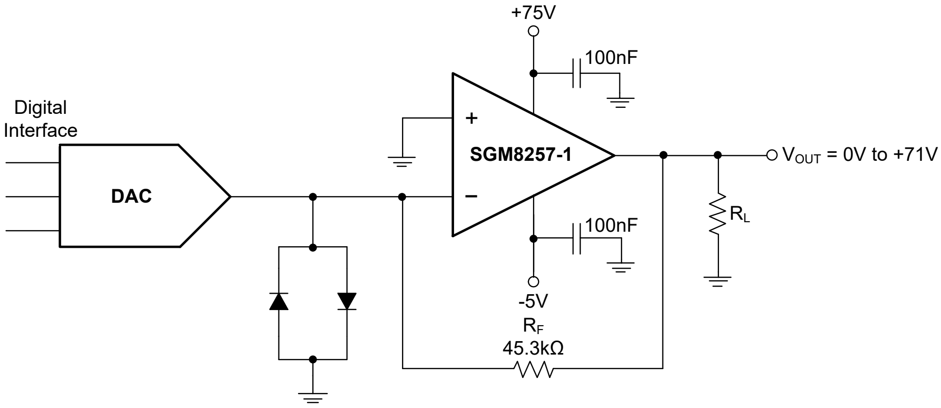


Figure 13. Programmable Voltage Source

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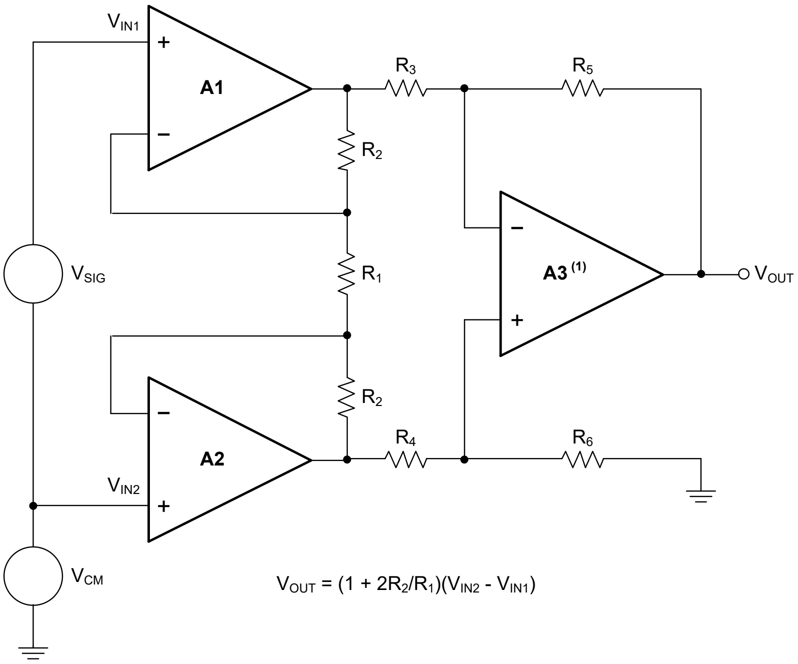
APPLICATION INFORMATION (continued)

High Voltage Instrumentation Amplifier

The high voltage instrumentation circuit application is shown in Figure 14. The voltage of V_{CM} + V_{SIG} should be always within the input range between (-V_S) + 2.5V and (+V_S) - 2.5V. The supply rails should also be limited to the range of ±40V or 80V.

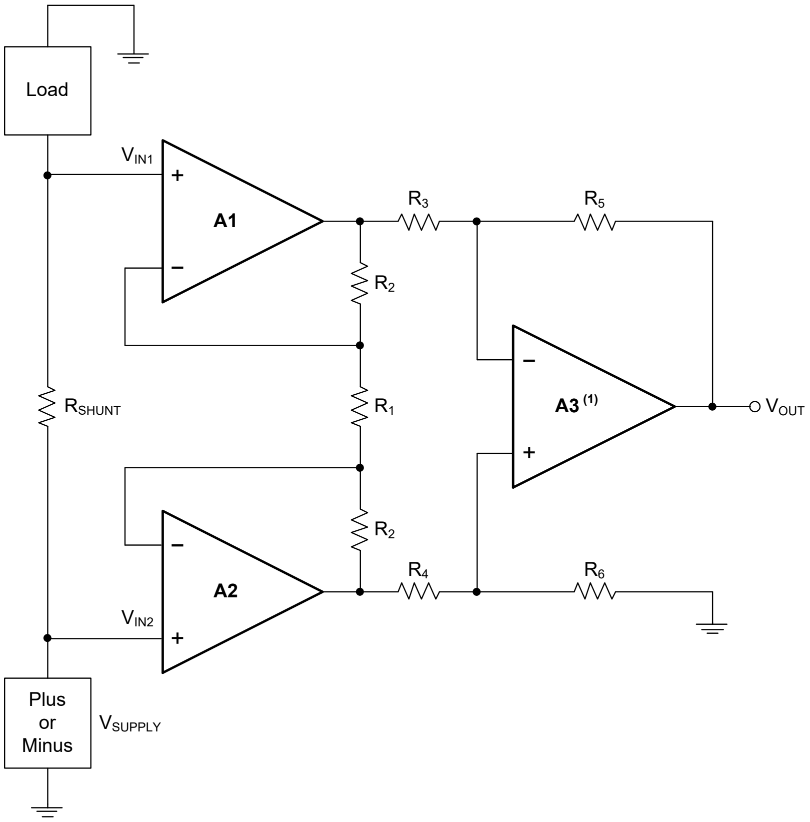


NOTE: 1. The linear input range is determined by the two operational amplifiers, which are A1 and A2.

Figure 14. High Voltage Instrumentation Amplifier

APPLICATION INFORMATION (continued)

The high-side current measurement is illustrated in Figure 15. The V_{SUPPLY} should be always within the linear input range between ($-V_S$) + 2.5V and ($+V_S$) - 2.5V. The supply rails should also be limited to the range of ±40V or 80V.



NOTES:

1. A_1 and A_2 should be applied as buffer circuits to increase the input voltage range of the current-sense circuit.
2. The maximum output swing of A_1 and A_2 limits the linear range of the circuit.

Figure 15. Current-Sense Monitor with Instrumentation Circuitry

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The supply rails should also be limited to the range of ±40V or 80V for the linearity of SGM8257-1. Most of the parameters remain unchanged for the full power supply ranges. The Electrical Characteristics section illustrates which parameters change with different power supply rails.

Most of the applications do not need equalized absolute values of the output swing so that the two supply rails do not need to be absolutely equal. The difference voltage of the maximum supply rails can be acceptable from 10V to 80V. For instance, the two supply rails can be 70V and -10V respectively (it is essential for operation to make sure that the voltage difference between the two supply rails is equal to or less than 80V).

Layout

Thermally-Enhanced Exposed Pad Package

A low-resistance (θ_{JC}) thermal path is achieved by the exposed pad package of SGM8257-1, which has a direct thermal path from the internal die to the exposed pad. In addition, for better performance, providing a good thermal path is essential.

The exposed pad construction is shown in Figure 16. On the bottom-side of the SOIC-8 (Exposed Pad) package, the lead frame is completely exposed as a thermal pad. The heat-sinking area of the PCB is tied together with the exposed pad of SGM8257-1. Moreover, the vias should also be placed on the PCB to conduct the heat to the bottom of the PCB. This kind of heat-sinking structure provides a convenient way for conducting heat and is also simple for the operator to mount.

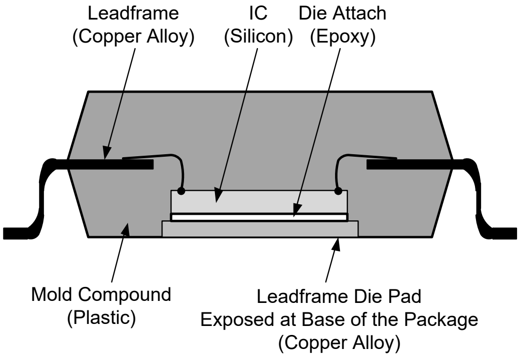


Figure 16. Cross-Section View of an Exposed Pad Package

Exposed Pad Layout Guidelines

The thermal pad of the package should always be mounted on the surface of the exposed copper of the PCB. This copper area has the ability to provide a thermal path and conduct the heat away from the package to any other heat-dissipating devices. Although the power consumption of the application is ultra-low, the exposed pad is also required to be mounted to the copper area of the PCB. The following steps illustrate the details of connecting the package to the PCB:

- Both thermal pads and leads should be etched, which means that the PCB with a top-side etch is required.
- The exposed pad should always be connected to the $-V_S$ of SGM8257-1.
- In the thermal pad of the PCB, placing the recommended amount of holes is significant. The size of the area on the PCB should always comply with the mechanical drawing which is shown in the appendix. The diameter of these holes should be 13mils (.013in, or 0.3302mm) so that solder wicking through the holes will not cause a problem for reflow. The recommended amount of holes for the exposed pad of the package is five.
- Providing vias on the PCB is recommended for better heat dissipation, but it is not required. The exposed copper area of the PCB should always be equal to the exposed pad if there are no vias, and connecting this area to $-V_S$ is required.
- Outside the area of thermal pad, the additional vias can be placed along the thermal plane, which is essential for the IC itself to conduct and dissipate the internal heat. In addition, the diameter of these holes should be larger than that of the holes in the thermal pad area (13mil). The reason is that they are not located at the area that needs to be soldered, which means that wicking will never be affected.
- All of the vias connected to the thermal pad area should be connected to $-V_S$ for better thermal dissipation.

APPLICATION INFORMATION (continued)

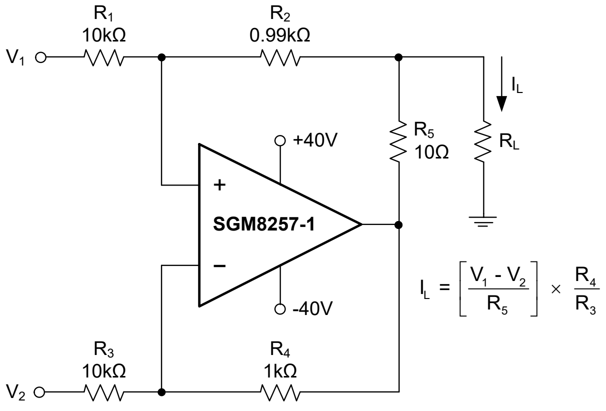
- The area of the thermal pad for the SGM8257-1 should always be left exposed for the consideration of thermal dissipation. The holes which are located on the bottom side of the PCB should be covered all the time for preventing the solder from being pulled away during the process of reflow.
- The traditional technology such as typical web or the connection of spoke via is not recommended when connecting the holes to the plane. The thermal resistance is extremely high for the web connection so that it can slow the heat transfer for soldering. However, for the SGM8257-1 applications, low thermal resistance is desired and required for the efficiency of the heat transfer. Therefore, for reducing the thermal resistance, the operator should make the vias which are located on the exposed pad connect completely to the internal plane of the PCB.
- The solder should be applied to the exposed power pad area and all the terminals of the SGM8257-1.
- After finishing the preparation of the above steps, the SGM8257-1 can be connected to the specific locations of the PCB through the reflow process.

Power Dissipation

The power dissipation is strongly related to the input signal levels, voltage of the power supply rails and the loading. If a DC signal is applied to the input of the SGM8257-1, the mathematical relationship between the power dissipation and the load current is: $P_D = I_L \times (V_S - V_{OUT})$. According to the output voltage level, the voltage of the power supply rails should be reduced to minimize the power dissipation of the amplifier.

The maximum power dissipation occurs when the output voltage is equal to one-half of the voltage of the power supply rails for the resistive loads. However, the power dissipation of an AC signal is much lower, since the root-mean-square (RMS) value of power dissipation (P_D) should be taken into account. Figure 17 illustrates a constant current source circuit in which the maximum P_D occurs at the minimum output voltage.

For normal operations, the SGM8257-1 can supply 25mA or more output current. If the supply power is equal to ±15V, this amount of current can be supplied without any problem. However, the power dissipation will increase dramatically with the rise of the power supply rails. Moreover, unbalanced power supply rails will apply a larger voltage across the output transistor so that power dissipation is increased. A heat spreader is required for high power dissipation applications.



NOTE: $R_1 = R_3$ and $R_4 = R_2 + R_5$.

Figure 17. Precision Voltage-to-Current Converter with Differential Inputs

Heat-Sinking

The junction temperature (limited to +150℃) rises accordingly with the increase of power dissipation. Most of the applications need a heatsink to reduce the effect of power dissipation for better operation stability, so that the junction temperature is not exceeded. Equation 1 illustrates the mathematical expression of the junction temperature:

$$T_J = T_A + P_D \times \theta_{JA} \tag{1}$$

θ_{JA}, the thermal resistance of the package, is strongly related to the environment. The thermal resistance is increased dramatically for socketing and poor air circulation. In addition, most of the applications have one or more channels that require many amplifiers, and these amplifiers will be placed close together, so that the surrounding temperature will increase accordingly. One of the methods to improve the thermal performance is using wide PCB trace to connect the SGM8257-1.

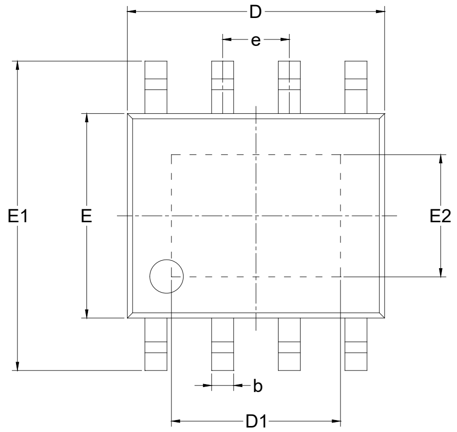
REVISION HISTORY

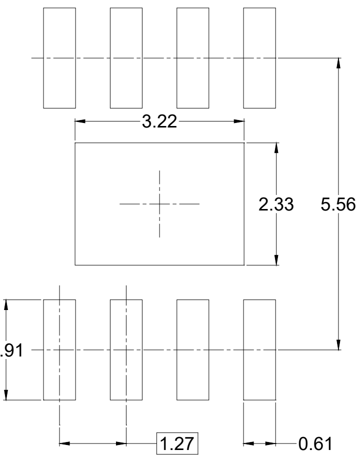
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (APRIL 2026)	Page
Changed from product preview to production data	All

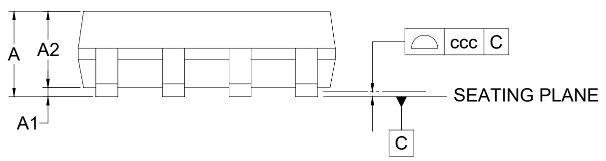
PACKAGE OUTLINE DIMENSIONS

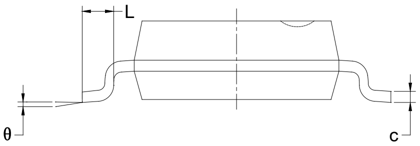
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



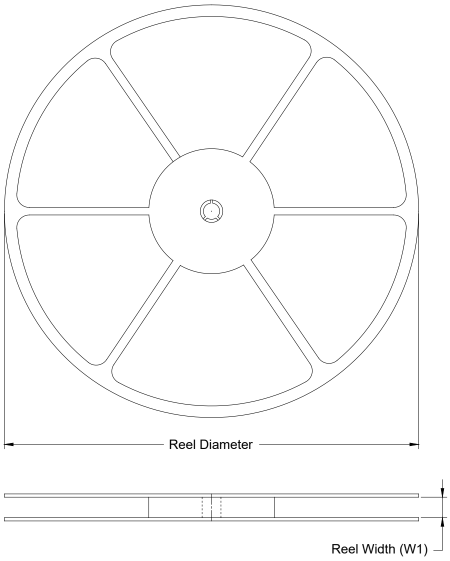


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

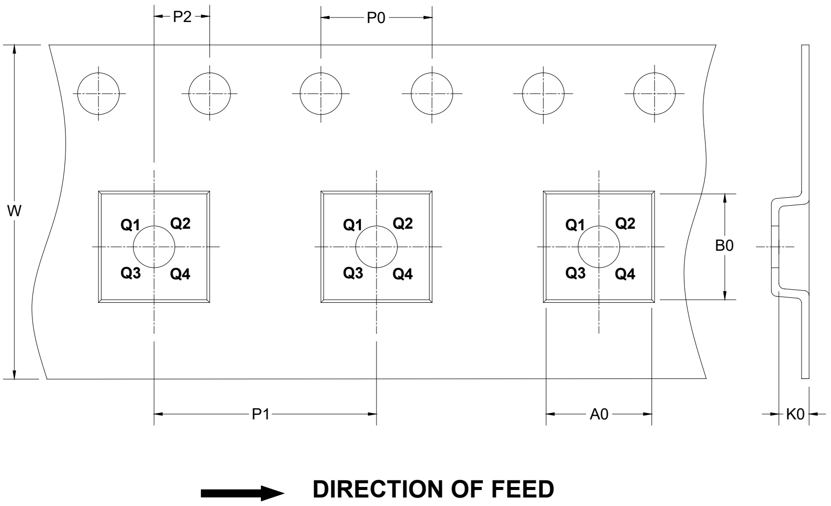
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



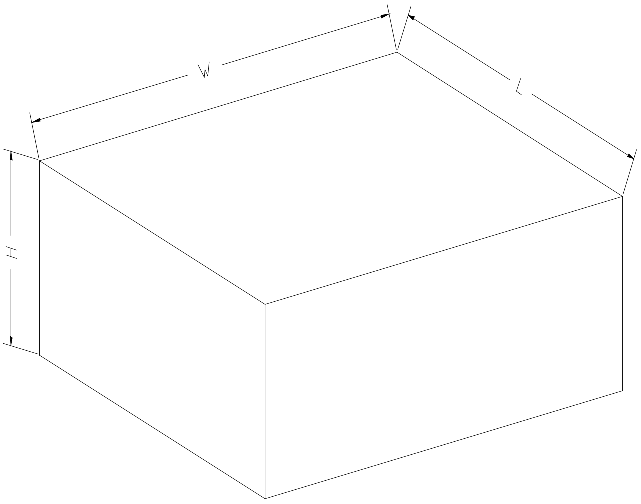
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002