SGM612A12
High Efficiency 24V Input, 12A Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM612A12 is a wide 4.5V to 24V input voltage, 0.6V to 5.5V output voltage, 12A continues output current, synchronous Buck converter with integrated power MOSFETs. This device uses constant on-time (COT) control topology to get fast transient response.

The SGM612A12 has four selectable switching frequencies 500kHz, 800kHz, 1MHz and 1.2MHz by FS pin. The device has adjustable cycle-by-cycle valley over-current protection by CLM pin to meet various applications.

The SGM612A12 has a MODE pin to select power saving mode (PSM) or ultrasonic mode (USM) during light loading. In PSM, it could get high light loading efficiency by skip pulse. In USM, it could avoid acoustic noise.

The SGM612A12 provides OV (over-voltage), UV (under-voltage), OT (over-temperature) and UVLO (under-voltage lockout) protections combined with power-good indicator and build-in output discharge function.

The SGM612A12 is available in a Green TQFN-3×4-19L package.

FEATURES

- **4.5V to 24V Wide Input Voltage Range**
- **0.6V to 5.5V Output Voltage Range**
- **Supports 12A Continues Output Current**
- **Low R_{DSON} MOSFET Switches (12mΩ/5mΩ)**
- **0.6V Reference Voltage and ±1% Accuracy at +25℃**
- **56μA (TYP) Low Quiescent Current**
- **500kHz, 800kHz, 1MHz and 1.2MHz (TYP) Switching Frequency Selection via FS Pin**
- **Selectable 20A, 26A, 33A (TYP) Cycle-by-Cycle Valley Over-Current Protection via CLM Pin**
- **Optional PSM and USM for Light-load Operation via MODE Pin**
- **Adjustable Soft Start Time**
- **Constant On-Time (COT) Control for Fast Transient Response**
- **Support All Low ESR MLCC Output Capacitor**
- **Power Good Indicator**
- **Integrated Output Discharge Function**
- **Latch-off Protection for UV and OV**
- **Non-Latch Protection for OT and UVLO**
- **Built-In Output Discharge Function**
- **Available in a Green TQFN-3×4-19L Package**

APPLICATIONS

Laptops and Notebook Computers
Industrial Low Power Systems

SIMPLIFIED SCHEMATIC

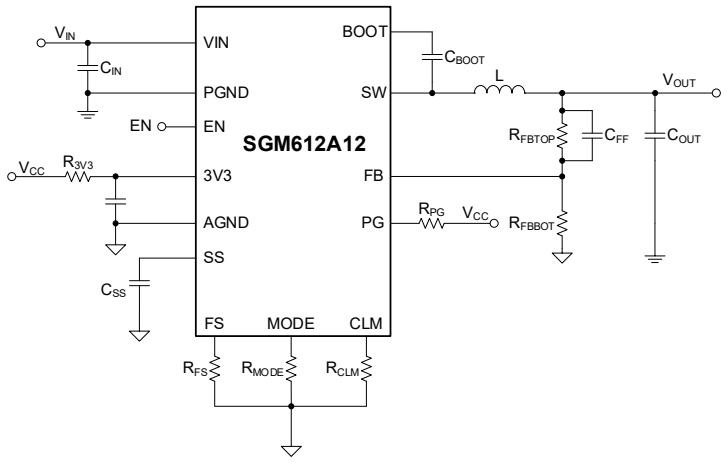


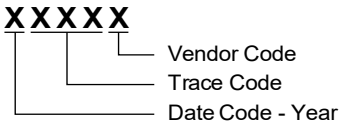
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM612A12	TQFN-3×4-19L	-40℃ to +125℃	SGM612A12XTXQ19G/TR	SGM 2NDTXQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... -0.3V to 28V
3V3 Voltage ..... -0.3V to 4.5V
Switch Voltage
SW ..... -1V to 28V
SW (Less than 30ns) ..... -5V to 30V
BOOT-SW Voltage, V_{BOOT} ..... -0.3V to 4.5V
PGND, AGND ..... -0.3V to 0.3V
Other I/O Pin Voltage ..... -0.3V to 4.5V
Package Thermal Resistance
TQFN-3×4-19L, θ_{JA} ..... 38.8℃/W
TQFN-3×4-19L, θ_{JB} ..... 3.5℃/W
TQFN-3×4-19L, θ_{JC} ..... 33.4℃/W
Junction Temperature ..... -40℃ to +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 4.5V to 24V
3V3 Voltage ..... 3.15V to 3.5V
Switch Voltage, SW ..... -0.5V to 24V
BOOT-SW Voltage, V_{BOOT} ..... -0.3V to 3.5V
PGND, AGND ..... -0.1V to 0.1V
Other I/O Pin Voltage ..... -0.1V to 3.5V
Operating Junction Temperature ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

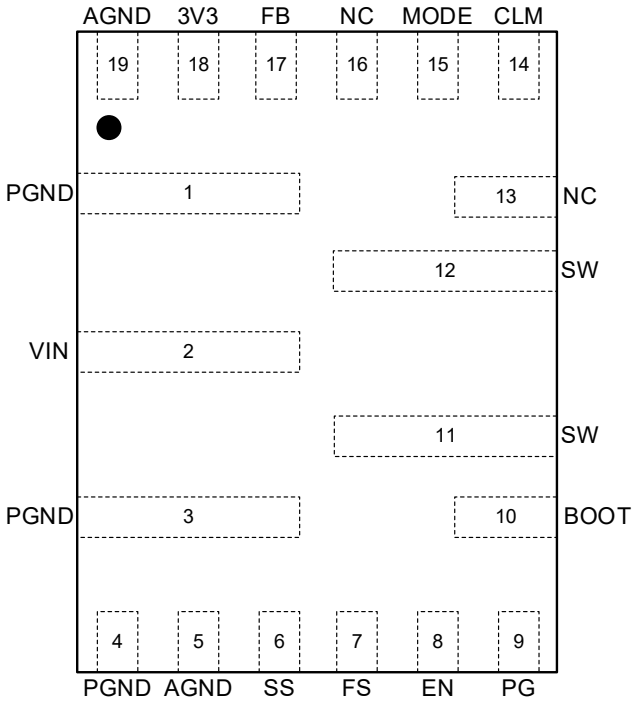
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×4-19L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1, 3, 4	PGND	G	Power Ground.
2	VIN	I	Input Supply Pin. Decouple this pin to PGND with at least 20μF and 0.1uF ceramic capacitor as close as possible to these two pins.
5, 19	AGND	G	Analog Ground.
6	SS	O	Soft-Start Time Program Pin. Connect a capacitor to AGND to program the soft-start time.
7	FS	I	FS Pin to choose the switching frequency, connect a resistor to AGND.
8	EN	I	Enable Input. Applying a logic high voltage to EN pin enables the device and a logic low shut it down. Default status is low.
9	PG	O	Open-Drain Power Good Indicator. Pull it up with a resistor (like 100kΩ), this output will go high when the VOUT gets nominal value.
10	BOOT	I	Upper Gate Driver Supply Bootstrap Input. Place a ceramic capacitor C_{BOOT} between BOOT and SW pins as close as possible to the IC.
11, 12	SW	O	Switching Node Output of the Internal Switches. These pins connect to one terminal of the output inductor and the bootstrap circuit. Keep this trace short with minimal copper area to minimize noise coupling, but it should be enough to carry inductor current.
13	NC	NC	NC Pin. Connect a ceramic capacitor C_{BOOT} to SW or leave it floating.
14	CLM	O	Current Limit Adjustable Pin. Connect a resistor to AGND to choose different current limit.
15	MODE	O	USM Mode and PSM Mode Selection Pin. Connect a resistor to AGND to choose different operation mode under light loading.
16	NC	NC	NC Pin. Connect to VOUT plane or leave it floating.
17	FB	I	Feedback Input Pin. Connect the output voltage with an RC network for closed loop control. Keep this line away from noise sources such as SW node.
18	3V3	I	External 3.3V Input for Control and Driver. It is recommended to place a 5.1Ω (TYP) and 1μF capacitor to form an RC filter.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, V_{3V3} = 3.3V, typical values are at V_{IN} = 12V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Input Voltage Range	V_{IN}		4.5		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising		4.1	4.4	V
UVLO Hysteresis	V_{HYS}			0.4		V
3V3 UVLO Rising	V_{3V3_VTH}		2.8	2.95	3.1	V
3V3 UVLO Hysteresis	V_{3V3_HYS}			0.2		V
Quiescent Current on 3V3	I_Q	V_{EN} = 2V, I_{OUT} = 0A, V_{OUT} = V_{OUT_TARGET} × 103%		56	95	μA
Shutdown Current on 3V3	I_{SHDN}	EN = 0V, T_J = +25℃			2	μA
Feedback						
Feedback Reference Voltage	V_{REF}	T_J = +25℃	0.594	0.6	0.606	V
Feedback Reference Voltage	V_{REF}	T_J = -40°C to +125℃	0.591	0.6	0.609	V
MOSFET						
Top FET R_{DSON}	R_{DSON}	T_J = +25℃		12		mΩ
Bottom FET R_{DSON}	R_{DSON}	T_J = +25℃		5		mΩ
Current Limit						
Bottom FET Current Limit	I_{LMT_BOT}	CLM resistor = 0Ω		20		A
		CLM resistor = 91kΩ		26		
		CLM resistor ≥ 150kΩ or float		33		
Bottom FET Reverse Current Limit	I_{LMT_RVS}	USM, T_J = +25℃	3.7	5.8		A
Soft-Start						
Soft-Start Source Current	I_{SS}			1.6		μA
Enable Logic						
EN Input Voltage High	V_{EN_H}		1.1	1.2	1.3	V
EN Hysteresis	V_{EN_HYS}			125		mV
EN Input Resistor	R_{EN}			1.2		MΩ
Switching Frequency						
Switching Frequency	f_{SW}	CCM, FS resistor = 91kΩ		800		kHz
Minimum On-Time (1)	t_{ON_MIN}			60		ns
Minimum Off-Time (1)	t_{OFF_MIN}			200		ns
USM Frequency	f_{SW_USM}	Mode resistor = 91kΩ		30		kHz
Output Voltage						
Output Over-Voltage Protection Threshold	V_{OVP}	V_{FB} rising	120	125	130	%V_{REF}
Output Over-Voltage Protection Hysteresis	V_{OVP_HYS}			5		%V_{REF}
Output OVP Deglitch	t_{OVP_Deg}			60		μs
Output Under-Voltage Protection Threshold	V_{UVP}		55	60	65	%V_{REF}
Output UVP Deglitch	t_{UVP_Deg}			125		μs
Output Discharge Resistor	R_{DIS}	V_{EN} = 0V, T_J = +25℃		50		Ω

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, V_{3V3} = 3.3V, typical values are at V_{IN} = 12V and T_J = +25℃, unless otherwise noted.)

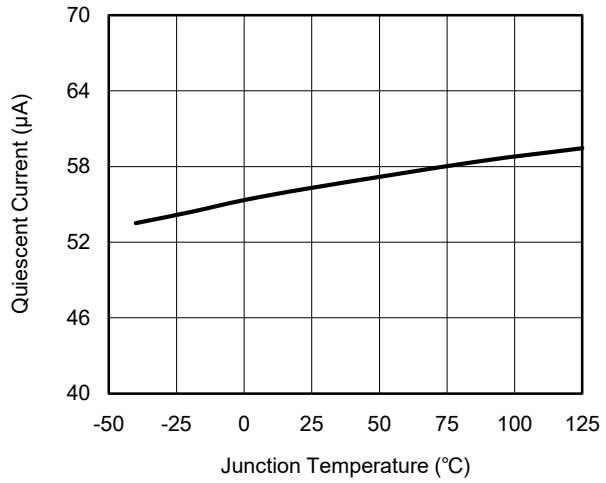
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Good						
Power Good Threshold	V_{PG}	V_{FB} rising (good)		95		%V_{REF}
		V_{FB} falling (fault)		85		
		V_{FB} rising (fault)		115		
		V_{FB} falling (good)		105		
Power Good Deglitch	t_{PG_R}	Low to high		125		μs
	t_{PG_F}	High to low		60		
Power Good Low Voltage	V_{PG_LOW}	I_{PG} = 5mA, V_{FB} = 0V			0.4	V
Power Good Leakage Current	I_{PGLK}	V_{PGOOD} = 3.3V			1	μA
Thermal Shutdown (1)						
Thermal Shutdown Temperature	T_{OTP}	T_J rising		165		℃
Thermal Shutdown Hysteresis	T_{OTP_HYS}			25		℃

NOTE: 1. Specified by design. Not production tested.

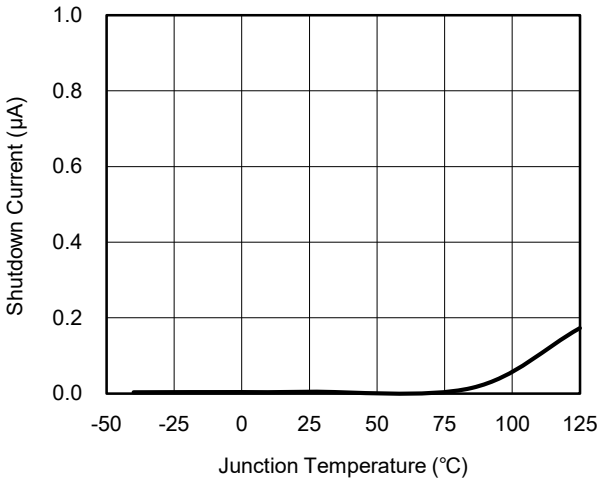
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 0.77V and f_{SW} = 800kHz, unless otherwise noted.

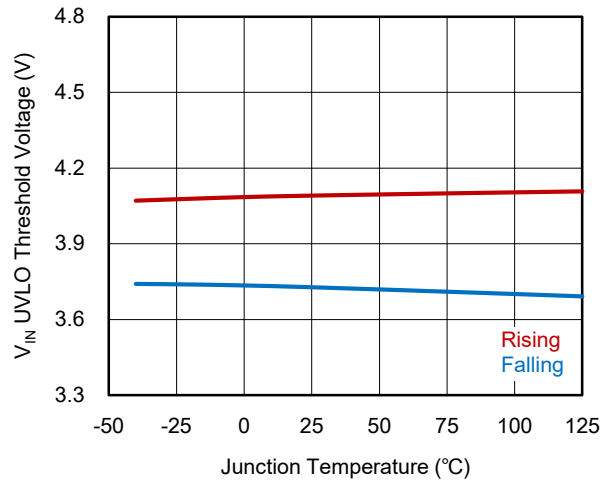
Quiescent Current vs. Junction Temperature



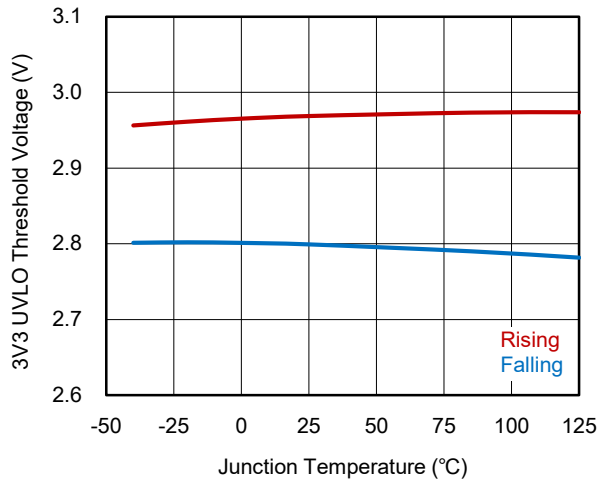
Shutdown Current vs. Junction Temperature



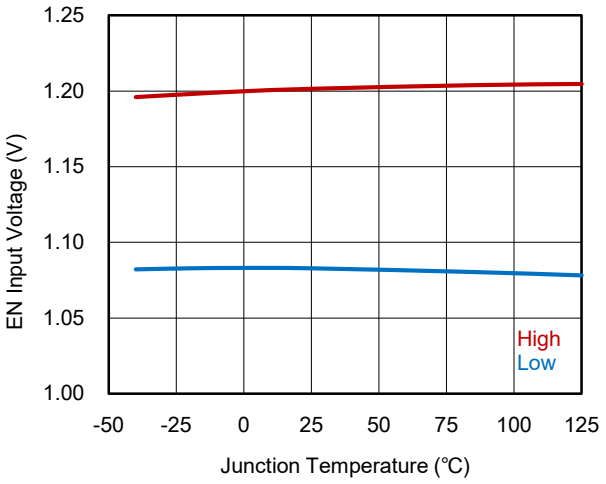
V_{IN} UVLO Threshold Voltage vs. Junction Temperature



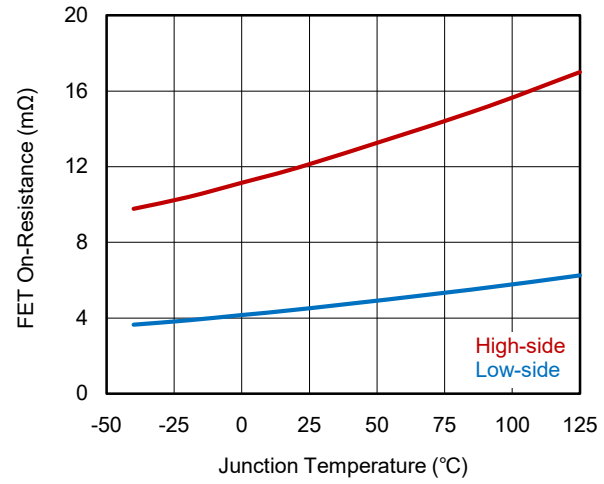
3V3 UVLO Threshold Voltage vs. Junction Temperature



EN Input Voltage vs. Junction Temperature



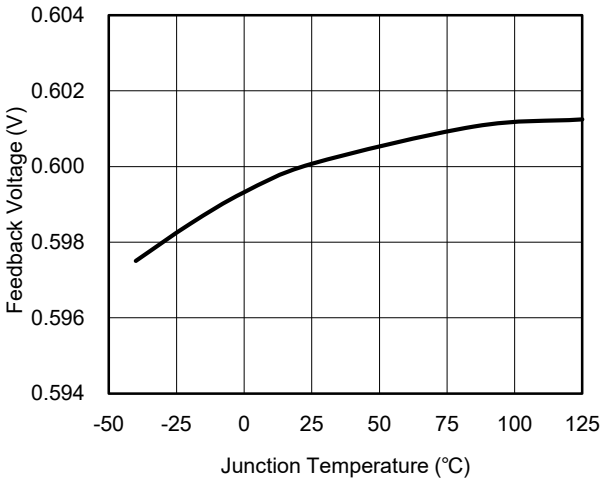
FET On-Resistance vs. Junction Temperature



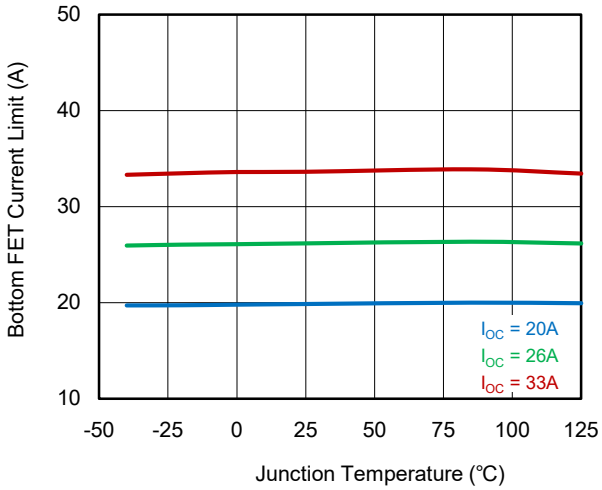
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 0.77V and f_{SW} = 800kHz, unless otherwise noted.

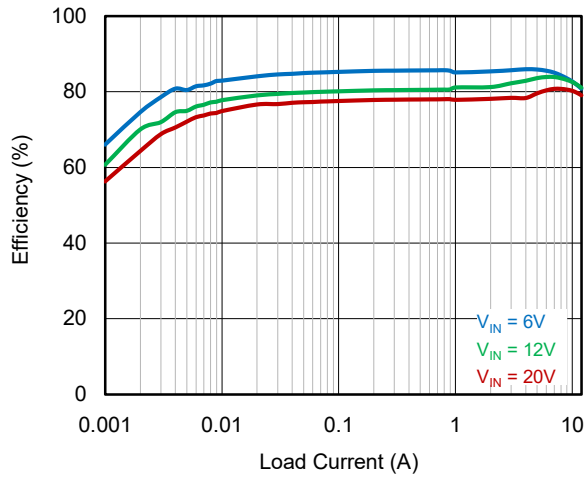
Feedback Voltage vs. Junction Temperature



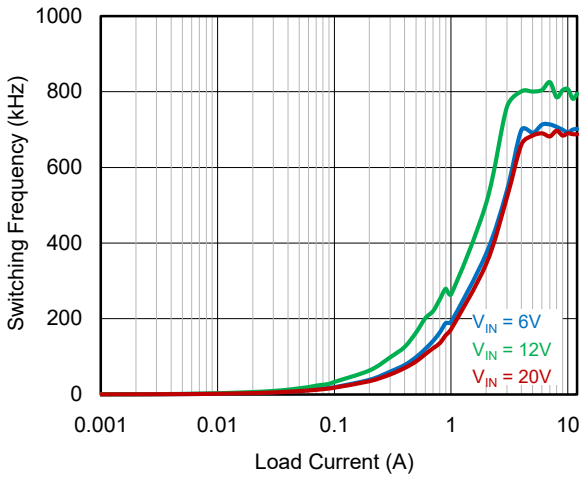
Bottom FET Current Limit vs. Junction Temperature



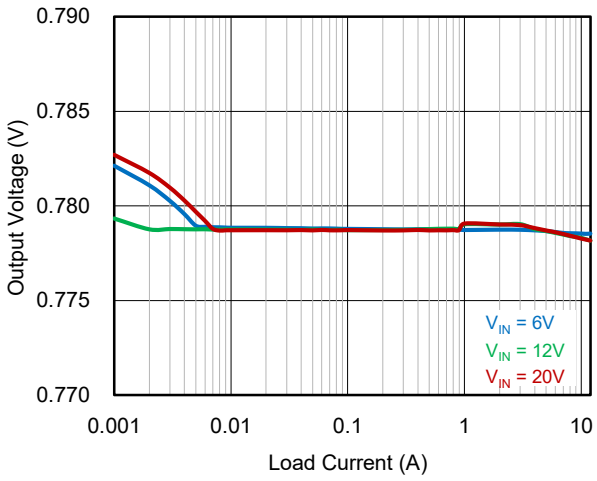
Efficiency



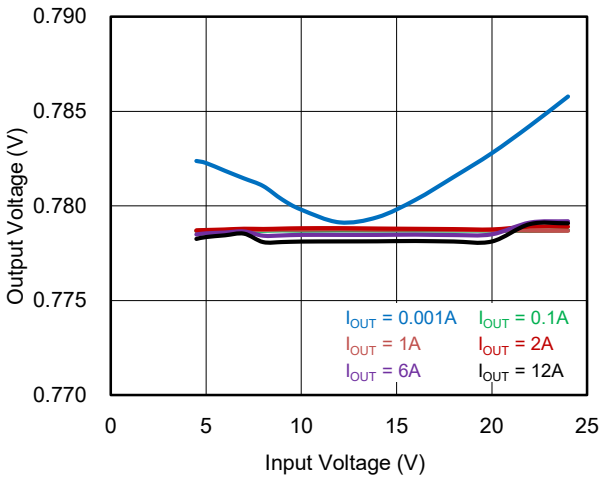
Switching Frequency vs. Load Current



Load Regulation



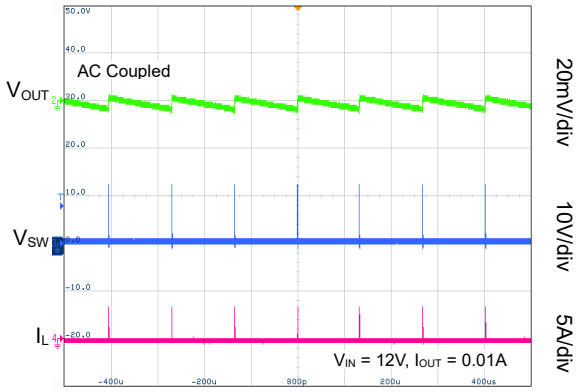
Line Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

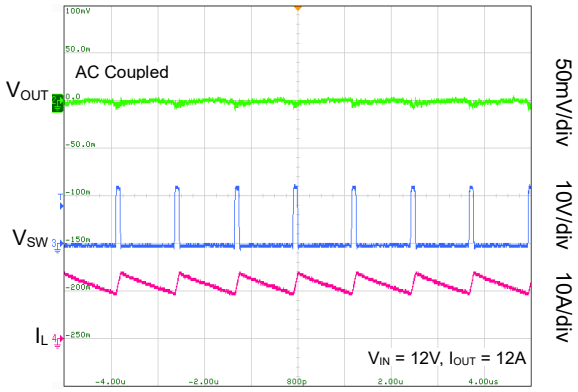
V_{IN} = 12V, V_{OUT} = 0.77V and f_{SW} = 800kHz, unless otherwise noted.

Output Voltage Ripple



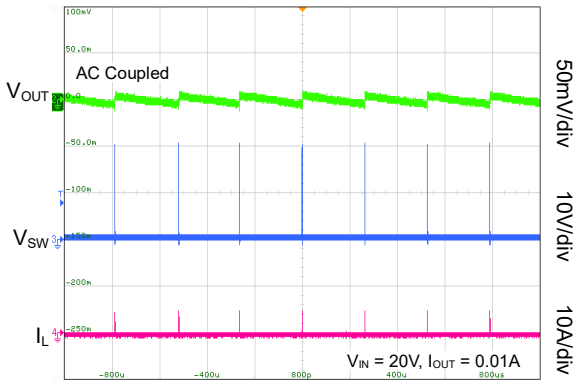
Time (100μs/div)

Output Voltage Ripple



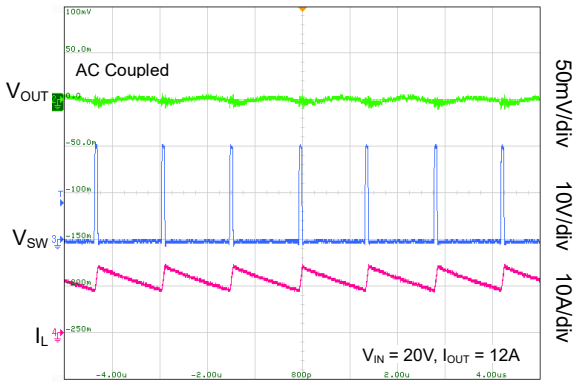
Time (1μs/div)

Output Voltage Ripple



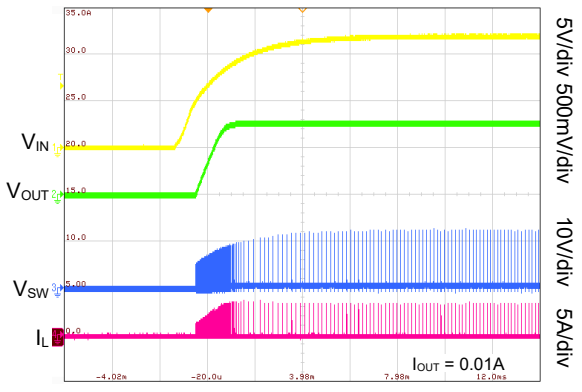
Time (200μs/div)

Output Voltage Ripple



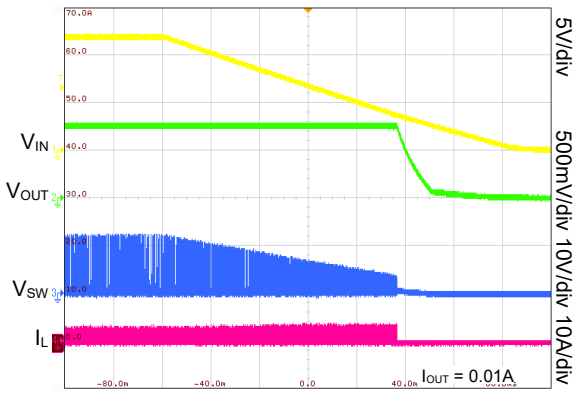
Time (1μs/div)

Power On



Time (2ms/div)

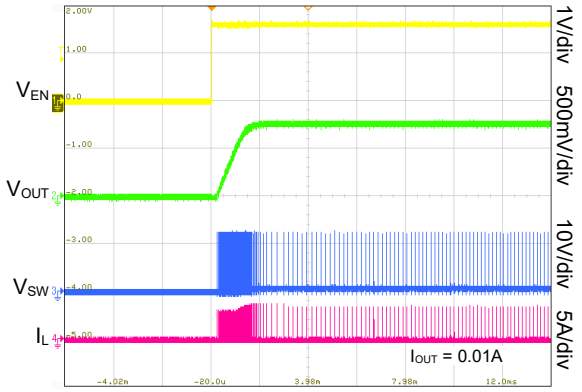
Power Off



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

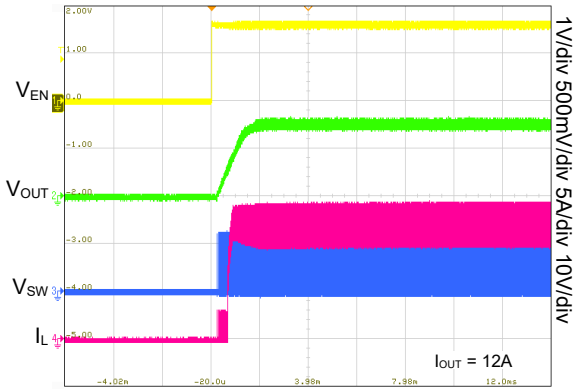
V_{IN} = 12V, V_{OUT} = 0.77V and f_{SW} = 800kHz, unless otherwise noted.

EN On



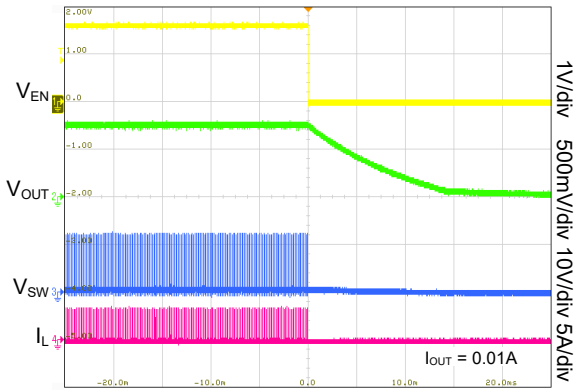
Time (2ms/div)

EN On



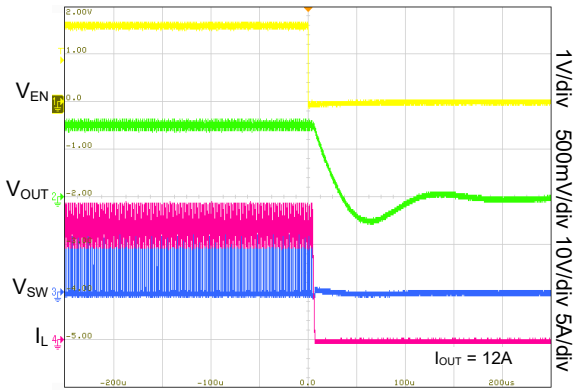
Time (2ms/div)

EN Off



Time (5ms/div)

EN Off



Time (50μs/div)

Load Transient Response

Time (1ms/div)

FUNCTIONAL BLOCK DIAGRAM

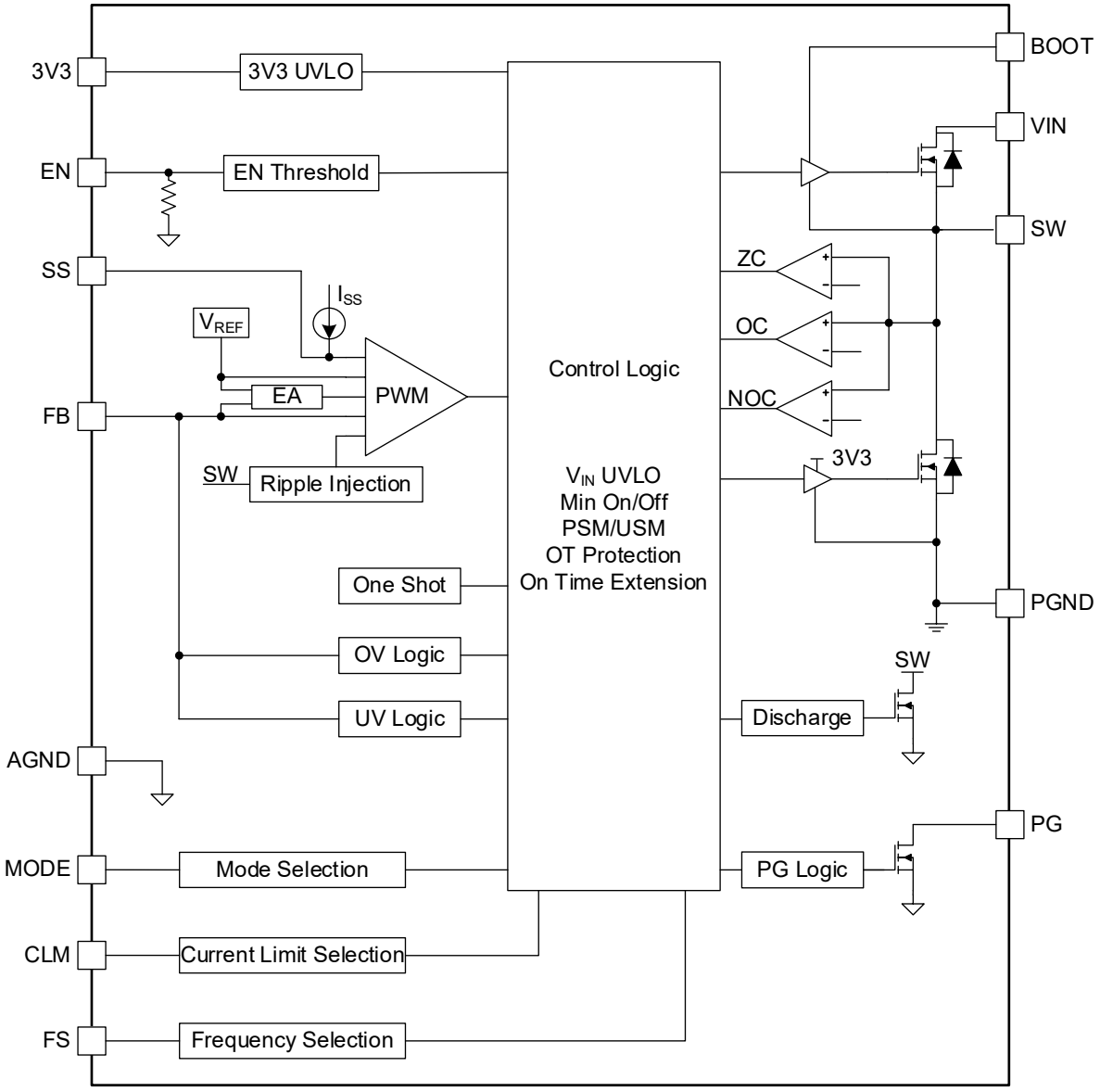


Figure 2. Block Diagram

OPERATION DESCRIPTION

The SGM612A12 is a wide input voltage synchronous Buck converter with constant on-time (COT) control and integrated low R_{DSON} power MOSFETs. The COT control loop allows stable operation and fast transient response even with low ESR output ceramic capacitors and no complicated external compensation. It can deliver 12A output current due to its integrated low R_{DSON} switches. The V_{IN} input range is from 4.5V to 24V.

The proprietary technology used the COT control for this device, provides excellent load and line regulation and very fast transient response along with high flexibility.

Transient response is almost instantaneous because the COT is not clock-based unlike other methods using clocked PWM where the loop reacts to the events in the next clock cycles. Therefore, the inductor current reacts to deviations immediately to keep the output in regulation.

This device can employ both low ESR (like POSCAP or SP-CAP) and ultra-low ESR ceramic capacitors for output capacitance.

Under-Voltage Lockout (UVLO)

The input voltage (V_{IN}) is continuously monitored and if it falls below the UVLO threshold, the device shuts down. The UVLO is necessary to avoid device malfunction.

If V_{IN} and V_{3V3} exceeds V_{UVLO}, and EN is logic high, device starts switching. The V_{IN} UVLO is non-latching.

3V3 Voltage

SGM612A12 needs external voltage to supply the IC control and driver circuits from 3V3 pin. It should be decoupled with one at least 1μF ceramic capacitor close to the device. It is suggested to place a resistor (5.1Ω TYP) to form an RC filter.

3V3 regulator has UVLO protection and it is non-latching.

Enable Input (EN)

The EN input pin can be used to enable or shutdown the device. If EN is a logic low, device will shut down. EN default status is low by internal pull-down resistor.

Bootstrap Circuit (C_{BOOT})

The high-side (HS) switch gate driver needs a voltage higher than V_{IN} to turn on the gate of the high-side NMOSFET switch. The external bootstrap capacitor (C_{BOOT}) is used to provide this higher voltage for supplying the HS gate driver. C_{BOOT} is charged through the internal bootstrap switch from 3V3 when the low-side (LS) switch turns on and SW node is at around 0V. When the LS switch turns off and HS switch turns on, the SW voltage will rise to the V_{IN} rail voltage. The C_{BOOT} voltage is charged to V_{IN} + 3V3 voltage to supply the HS driver. Refer to Figure 3 for C_{BOOT} selection.

Soft-Start

SGM612A12 employs a flexible soft-start (SS) mechanism to ensure smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft-start finishes, and the part enters steady-state operation. The minimum soft-start time is 0.4ms (TYP) even if there is no SS cap.

The SS time is calculated through below equation; typical I_{SS} is 1.6μA.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (1)$$

Power Good Indicator Output (PG)

The SGM612A12 has a built-in PG function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pull up resistor (10kΩ to 100kΩ) to any voltage below 3.5V.

After the FB pin voltage (V_{FB}) is between 95% and 105% of the internal reference voltage (V_{REF}) and after a deglitch time of 125μs (TYP), the PG turns to high. The PG pin is pulled low after a deglitch time of 60μs (TYP) when V_{FB} is lower than 85% of the internal reference voltage or greater than 115% of the V_{REF}, or in events of thermal shutdown, UVLO or EN shutdown conditions.

Large Duty Operation

The SGM612A12 can support large duty operation by the internal on time extension function. When V_{IN}/V_{OUT} < 1.2 and the output voltage is lower than target value, the switching frequency is allowed to smoothly drop to make on time extended to implement the large duty operation and also improve the performance of the load transient performance.

OPERATION DESCRIPTION (continued)

Power Saving Mode (PSM) and Ultrasonic Mode (USM)

In light loading, the SGM612A12 can enter the PSM mode to keep the efficiency high. In PSM, upon detection of zero inductor current, the LS switch turns off and the output capacitor will take longer time to discharge until the V_{OUT} (or V_{FB}) drops to the level needed to begin a new cycle.

This device also has USM mode to avoid acoustic noise when the PSM frequency drops below audible range (20kHz). In this mode, a special discharge circuit will be activated to keep the minimum switching frequency to be 30kHz (TYP), which is called ultrasonic mode. This mode can keep the switching frequency above the hearing range even in no load condition.

For USM mode, the inductor current is allowed to go negative. When this current exceeds the LS negative current limit I_{LMT_RVS}, the LS switch is turned off and HS switch is turned on immediately, which is used to protect the LS switch from excessive negative current. The I_{LMT_RVS} limitation should be considered when doing inductor selection for USM mode.

The Mode pin is used to select PSM or USM. Mode selection is in Table 1.

Table 1. Mode vs. Mode Resistor to GND

Mode	Mode Resistor to GND
PSM	0Ω or ≥ 230kΩ or floating
USM	91kΩ

Frequency selection is in Table 2.

Table 2. Frequency vs. FS Resistor to GND

Frequency	FS Resistor to GND
500kHz	0Ω
800kHz	91kΩ
1MHz	150kΩ
1.2MHz	≥ 230kΩ or floating

Output Current Limit (OCP)

A cycle-by-cycle valley current detection is implemented to limit the output current. During LS on, the current of the LS switch is monitored by measuring its drain-to-source voltage that is proportional to its current. This measurement is temperature compensated for better accuracy. If the current is higher than the valley current limit, the converter maintains LS on and HS off, even the feedback loop requires one, until the current drops below the valley current limit. During current limiting, the output voltage will drop because the required load current is not supplied by the inductor. If the output voltage drops below the output UVP level (see Output Over/Under-Voltage Protection), the device will shut down and turn on discharge to avoid over-temperature.

The device has CLM pin to select different OC limit value to meet various application.

Table 3. OC Limit vs. CLM Resistor to GND

OC Limit	CLM Resistor to GND
20A	0kΩ
26A	91kΩ
33A	≥ 150kΩ or floating

Output Over/Under-Voltage Protection

An over-voltage protection (OVP) is triggered if the V_{OUT} exceeds the over-voltage threshold. Upon OVP trigger, the HS and LS switch both turn off and the discharge is turned on to discharge output voltage.

Output voltage is also protected by under-voltage protection (UVP). If the output voltage falls and remains below the under-voltage threshold, the device shuts down and the discharge is turned on.

After OVP or UVP, the device will shut down in latch mode and will not restart automatically. An EN toggle, V_{IN} or 3V3 power cycling is needed to restart the device.

Discharge Function

The SGM612A12 has a 50Ω (TYP) discharge switch that discharges the output during any event of fault like output over-voltage, output under-voltage, thermal shutdown, UVLO or when the EN is pulled down.

Thermal Shutdown

The junction temperature (T_J) is constantly monitored for over-temperature protection (OTP). If T_J exceeds the T_{OTP} threshold (+165°C, TYP), the device shuts down and the discharge path is turned on to avoid damage.

OTP is a non-latch protection and once the junction temperature decreases below the hysteresis amount of +25ºC, it initiates a new soft-start.

APPLICATION INFORMATION

The design method and component selection for the SGM612A12 Buck converter are explained in this section. A typical application circuit for the SGM612A12 is shown in Figure 3. It is used for converting a 4.5V to 24V supply voltage to a lower 0.77V output voltage with a maximum output current of 12A.

Typical Application

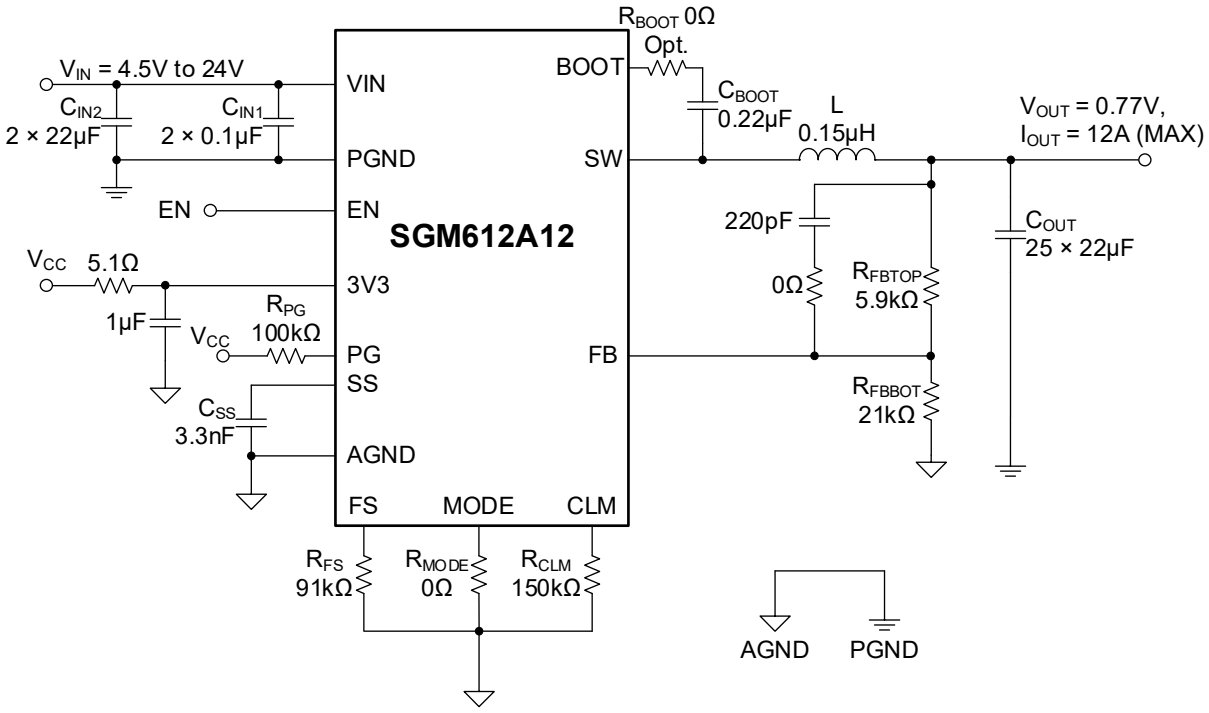


Figure 3. Typical Application

Output Voltage Set

The output voltage is set by a resistor divider between VOUT and AGND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use below Equation to calculate the output voltage. Lower divider resistor values increase loss and reduce light load efficiency. Larger resistor values improve efficiency at light load. Note that if divider resistor is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = 0.6 \times \frac{R_{FBTOP} + R_{FBBOT}}{R_{FBBOT}} \quad (2)$$

Input Capacitor Selection

For the input capacitor selection, SGM612A12 requires high-quality ceramic decoupling capacitors, such as X5R or X7R or similar. These types of capacitors are commonly used for power regulator capacitors due to their stable dielectric material, which results in less capacitance variation and greater temperature stability. When choosing the input capacitors, the voltage rating of capacitor should have a safe margin from maximum input voltage. Choosing an input capacitor with a voltage rating 1.5 times higher than the maximum input voltage is a safe design practice. The input RMS current can be calculated by Equation 3:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[\left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times {I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12} \right]} \quad (3)$$

To select a suitable capacitor for the RMS current rating, it is recommended to use multiple capacitors with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. Therefore, two 22μF low ESR capacitors are suggested at the input. The input ripple voltage can be calculated by Equation 4:

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{C_{IN} \times f_{SW} \times V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (4)$$

Two additional 0.1μF capacitor are suggested to add to filter high frequency ring voltage. The capacitor voltage rating must be greater than the maximum input voltage.

APPLICATION INFORMATION (continued)

Inductor Selection

When selecting an inductor, it is important to specify both the inductance and the peak current required. Inductor selection is usually flexible, and depending on the tradeoff between size, cost, and circuit efficiency. Lower inductor values can reduce size and cost, and improve transient response. However, the inductor ripple current and output voltage ripple are increased, and the efficiency is also reduced due to the higher peak current. In contrast, higher inductance values result in higher efficiency, but at the cost of increased physical size. In addition, the transient response will be slower due to the additional time it takes to change the current in the inductor. The approximate inductor value can be calculated by using Equation 5, which the ripple current (ΔI_L) is normally 0.3 times of maximum output current (I_{OUT_MAX}):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L} \quad (5)$$

With the selected inductor value, the corresponding peak inductor current I_{L_PEAK} can be calculated using Equation 6:

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{\Delta I_L}{2} \quad (6)$$

To ensure the full load range requirement, the saturation current rating (I_{SAT}) must be larger than the I_{L_PEAK}. To achieve optimal efficiency, select an inductor with low DC resistance that meets size and cost requirements. An inductor with a shielded ferrite core is the best choice for the application, which minimizes the core losses and causes fewer EMI and noise issues. In Table 4, the inductor uses Wurth 744355215 for 0.15μH and Wurth 744373965015 for 1.5μH.

Output Capacitor Selection

It is suggested to use below BOM to get better performance. In below table, the output capacitor uses 0603 footprint and 6.3V rated voltage.

Table 4. Suggested Component Selections

V_{OUT}	R_{FBTOP}	R_{FBBOT}	L	C_{OUT}	C_{FF}	Frequency Set
0.77V	5.9kΩ	21kΩ	0.15μH	25 × 22μF (MLCC) 330μF (PosCap Optional)	220pF	1MHz /800kHz
3.3V	91kΩ	20kΩ	1.5μH	6 × 22μF	68pF	800kHz
5V	110kΩ	15kΩ	1.5μH	7 × 22μF	68pF	800kHz

PCB LAYOUT INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for optimal IC performance. A 4-layer layout is strongly recommended to improve thermal performance.

For the best results, refer to Figure 4 and follow the guidelines below:

• Route the high-current loops (PGND, VIN, and SW) as close to the IC as possible, using short and wide traces.

• Place the input capacitors as close to VIN and PGND as possible, and on the same layer as the IC.

• Connect the VIN and PGND pads using a large copper plane with several vias to improve thermal performance.

• Connect a decoupling capacitor to 3V3 and AGND pins as close as possible.

• Single point connection of AGND to PGND with inner ground layer.

• Place a capacitor to SS pin and AGND with short connection.

• Keep the SW and BOOT trace with minimal copper area to minimize noise, but it should be enough to carry inductor current.

• Place the FB network far away from switching trace.

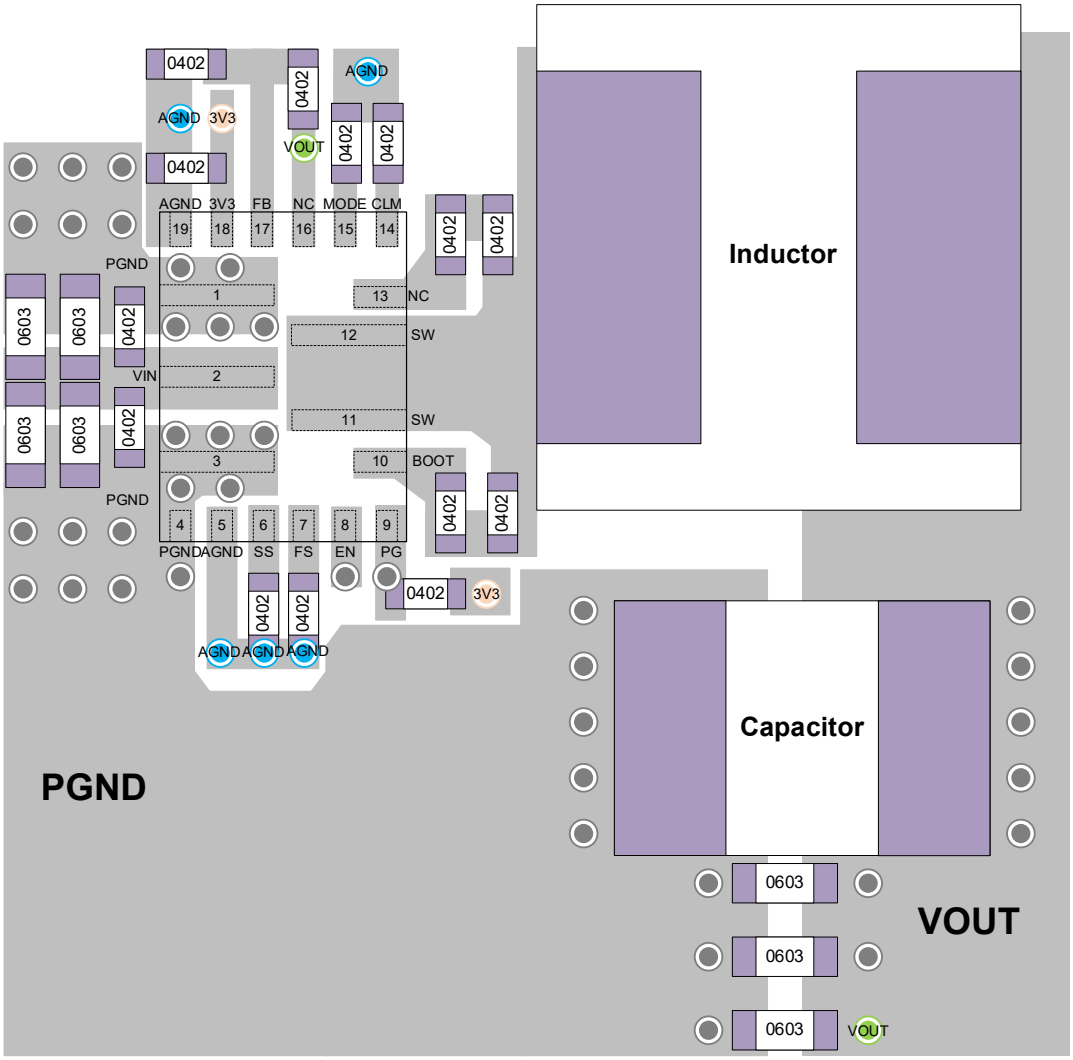


Figure 4. PCB Layout Example

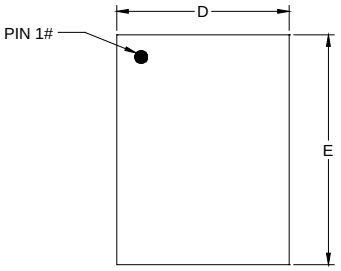
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

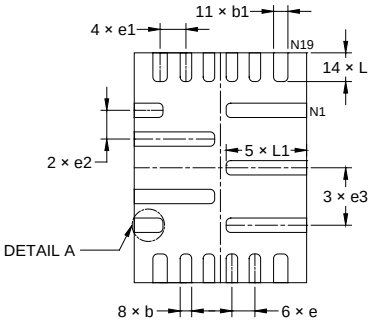
Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

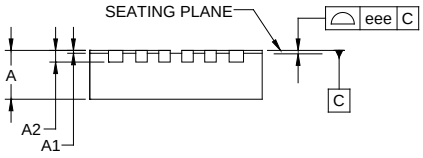
TQFN-3×4-19L



TOP VIEW



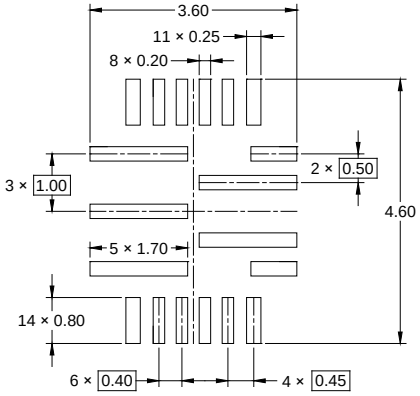
BOTTOM VIEW



SIDE VIEW

ALTERNATE A-1 ALTERNATE A-2

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



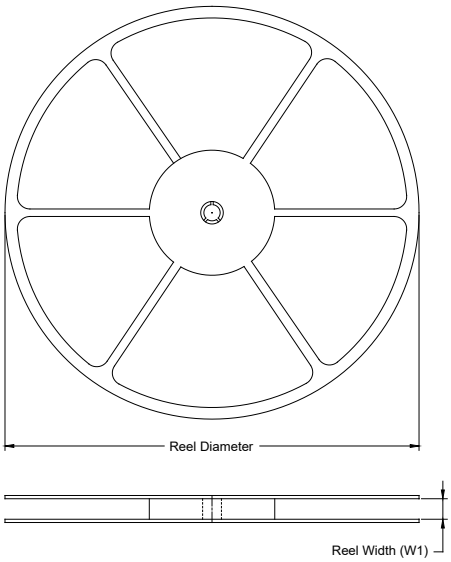
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
b1	0.200	-	0.300
D	2.900	-	3.100
E	3.900	-	4.100
e		0.400 BSC	
e1		0.450 BSC	
e2		0.500 BSC	
e3		1.000 BSC	
L	0.400	-	0.600
L1	1.300	-	1.500
eee		0.080	

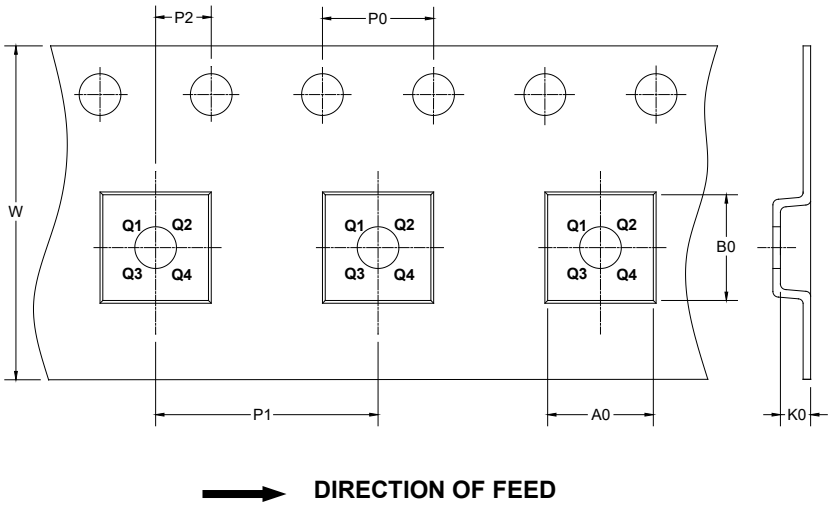
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



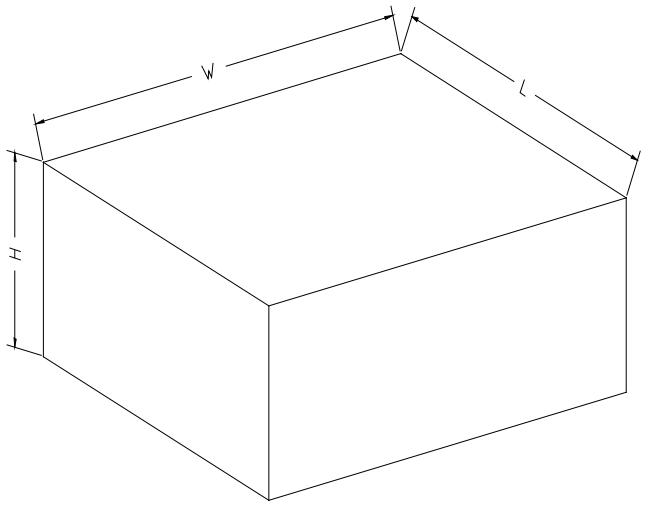
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-19L	13"	12.4	3.30	4.30	1.00	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002