SGM6618/SGM6618A
23V V_{IN}, 25V V_{OUT}, 6A, High-Efficiency, Synchronous Boost Converter with Programmable Peak Current Limit

GENERAL DESCRIPTION

The SGM6618 family is a high-voltage synchronous Boost converter that offers high efficiency and a small size with its integrated 41mΩ low-side and 33mΩ high-side power switches. The SGM6618 family has a wide input voltage range of 2.9V to 23V and provides an adjustable output voltage between 4.5V and 25V, with a switching current capability up to 6A.

The SGM6618 family utilizes the constant off-time peak current control topology for output voltage regulation，which provides enhanced dynamic performance. The device operates in PWM mode under heavy load conditions and automatically switches to PFM mode at light load, maintaining high conversion efficiency across the entire load range. The SGM6618 family operates in pulse width modulation (PWM) mode under moderate to heavy load conditions. For light load condition, the device provides a choice between two operating modes, selected by the MODE pin. One is pulse frequency modulation (PFM) mode, which is used to achieve high light load efficiency. The other is forced PWM mode, which keeps the switching frequency constant to avoid audible noise and other application problems caused by low switching frequency.

The SGM6618 family integrates a programmable peak switching current limit function and a soft-start function. The SGM6618 family also implements various protection features, such as output over-voltage protection (OVP), cycle-by-cycle over-current protection (OCP), and thermal shutdown to improve device robustness.

The SGM6618 family is available in a Green TQFN-2.5×2-13L package.

FEATURES

- **Wide Input Voltage Range: 2.9V to 23V, 3V for Start-up**
- **Wide Output Voltage Range: 4.5V to 25V**
- **1.5A to 6A Programmable Peak Current Limit**
- **Switching Frequency**
  - **SGM6618: 650kHz**
  - **SGM6618A: 1.2MHz**
- **6A (TYP) Peak Switching Current Limit**
- **Integrated MOSFETs**
  - **High-side MOSFET: 33mΩ (TYP)**
  - **Low-side MOSFET: 41mΩ (TYP)**
- **66μA (TYP) Quiescent Current**
- **2μA (MAX) Shutdown Current**
- **Up to 96% Efficiency (V_{IN} = 9V, V_{OUT} = 16V, and I_{OUT} = 2.0A)**
- **Up to 96.7% Efficiency (V_{IN} = 12V, V_{OUT} = 24V, and I_{OUT} = 1.5A)**
- **Selectable Auto PFM Mode and Forced PWM Mode**
- **Precise EN/UVLO Threshold**
- **External Loop Compensation**
- **Output Over-Voltage Protection (OVP)**
- **Cycle-by-Cycle Over-Current Protection (OCP)**
- **Thermal Shutdown**
- **Available in a Green TQFN-2.5×2-13L Package**

APPLICATIONS

3.3V V_{IN}, 5V V_{IN} to 12V V_{OUT}, 24V V_{OUT} Power Conversion

Industrial Power Systems

Appliances

SIMPLIFIED SCHEMATIC

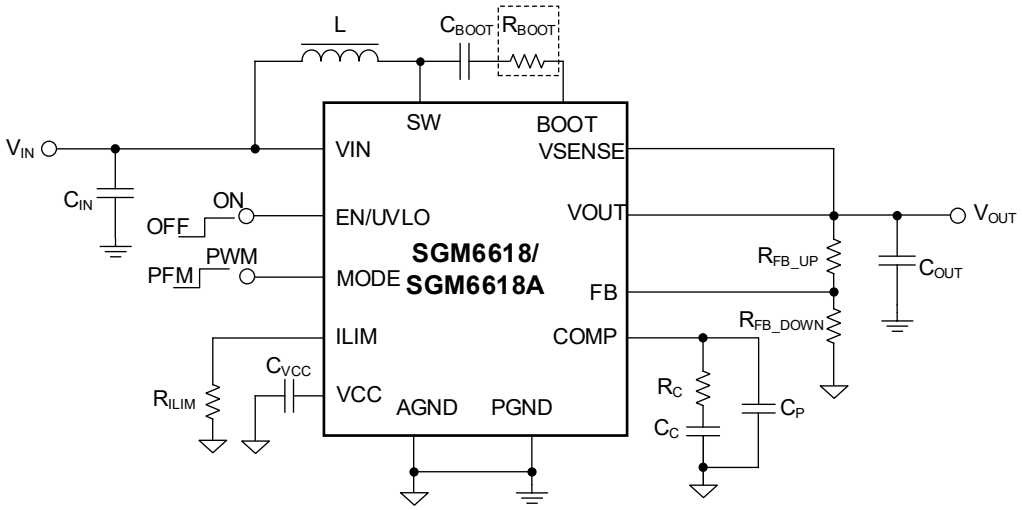


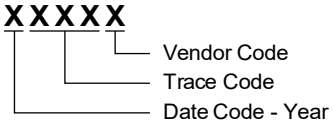
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6618	TQFN-2.5×2-13L	-40℃ to +125℃	SGM6618XTXG13G/TR	6618 XXXXX	Tape and Reel, 3000
SGM6618A	TQFN-2.5×2-13L	-40℃ to +125℃	SGM6618AXTXG13G/TR	6618A XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltage (1)
VIN, EN/UVLO ..... -0.3V to 25V
SW, VOUT, VSENSE ..... -0.3V to 30V
BOOT ..... -0.3V to V_{SW} + 6V
MODE, FB, ILIM, VCC, COMP ..... -0.3V to 6V
Package Thermal Resistance
TQFN-2.5×2-13L, θ_{JA} ..... 59.8℃/W
TQFN-2.5×2-13L, θ_{JB} ..... 4.8℃/W
TQFN-2.5×2-13L, θ_{JC} ..... 52.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. All voltage values are relative to network ground terminal.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN} ..... 2.9V to 23V
Output Voltage, V_{OUT} ..... 4.5V to 25V
Inductance, Effective Value, L .. 2.2μH to 10μH, 4.7μH (TYP)
Input Capacitance, Effective Value, C_I ..... 22μF (TYP)
Output Capacitance, Effective Value, C_O ..... 10μF to 2000μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

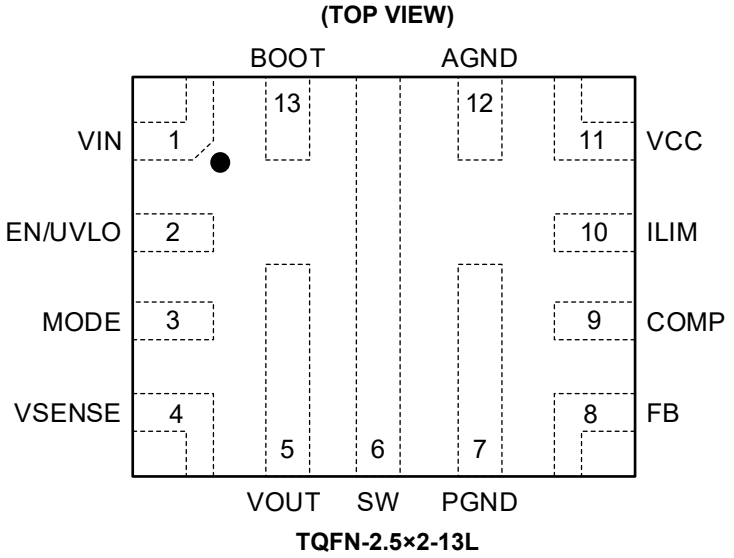
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-2.5×2-13L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VIN	I	Power Supply Input of the IC.
2	EN/UVLO	I	Enable Input and Under-Voltage Lockout (UVLO) Pin. Logic high enables the device. Logic low shuts down the device. Connecting this pin to VIN through a resistor divider can program the start-up and shutdown levels of the device. This pin must not be left floating.
3	MODE	I	Operating Mode Selection Pin in Light Load Condition. When sets it logic high, the device operates in forced PWM mode. When sets it logic low, the device operates in auto PFM mode.
4	VSENSE	I	Output Voltage Sense Pin. This pin must be connected to the VOUT pin. The connection must be either direct or through a 0Ω resistor; it must not be left floating or connected through any resistor of non-zero value.
5	VOUT	P	Output of the Boost Converter.
6	SW	P	Switching Node Pin. Connect to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
7	PGND	P	Power Ground.
8	FB	I	Voltage Feedback Pin. Connect to the resistor divider to program the output voltage.
9	COMP	O	Output of the Internal Error Amplifier. Put the loop compensation network between this pin and the AGND pin.
10	ILIM	I	Programmable Switch Peak Current Limit Setting Pin. A resistor is placed between ILIM and AGND to program the switch peak current limit.
11	VCC	O	Output of the Internal Regulator. Connect this pin to AGND with a capacitor more than 1.0μF effective.
12	AGND	P	Analog Signal Ground.
13	BOOT	O	Gate Driver Supply of High-side MOSFET. Connect this pin to SW pin through a 5Ω resistor necessarily in series with a 0.22μF to 0.47μF ceramic capacitor.

NOTE: I = input, O = output, I/O = input/output, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, L = 4.7μH, V_{IN} = 5V and V_{OUT} = 12V, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Input Voltage Range	V_{IN}		2.9		23	V
VIN Under Voltage Lockout Threshold	V_{IN_UVLO}	V_{IN} rising		2.8	3.0	V
		V_{IN} falling		2.65	2.9	
VIN UVLO Hysteresis	V_{IN_HYS}			188		mV
Quiescent Current into VOUT Pin	I_Q	IC enabled, no load, no switching, V_{IN} = 2 .9V to 5.25V, V_{OUT} = 25V, V_{FB} = V_{REF} + 0.1V		66	100	μA
		IC enabled, no load, no switching, V_{IN} = 5.5V to 23V, V_{OUT} = 25V, V_{FB} = V_{REF} + 0.1V		27	40	
Quiescent Current into VIN Pin	I_Q	IC enabled, no load, no switching, V_{IN} =2.9V to 5.25V, V_{FB} = V_{REF} + 0.1V		0.26	0.80	μA
		IC enabled, no load, no switching, V_{IN} = 5.5V to 23V, V_{FB} = V_{REF} + 0.1V		38	65	
VCC UVLO Threshold	V_{CC_UVLO}	V_{CC} rising		2.75		V
VCC UVLO Hysteresis	V_{CC_HYS}	V_{CC} hysteresis		156		mV
VCC Regulation	V_{CC}	I_{VCC} = 4mA, V_{OUT} = 12V		4.9		V
Shutdown Current into VIN Pin	I_{SD}	T_J = -40℃ to +85℃, IC disabled, V_{IN} = 23V, EN = GND			2	μA
Leakage Current into SW	I_{SW_LKG}	IC disabled, V_{OUT} = V_{SW} = 25V			2	μA
Leakage Current into VOUT	I_{VOUT_LKG}	IC disabled, V_{OUT} = 25V, SW floating			2	μA
Leakage Current into FB	I_{FB_LKG}	IC disabled, V_{FB} = 1V			100	nA
Output Voltage						
Output Over-Voltage Protection Threshold	V_{OVP}	V_{OUT} rising	26.4	27.4	28.6	V
Output Over-Voltage Protection Hysteresis	V_{OVP_HYS}	OVP threshold		1		V
Reference Voltage						
Reference Voltage at FB Pin	V_{REF}		0.98	1	1.02	V
Power Switch						
Low-side MOSFET On-Resistance	R_{DSON}	V_{CC} = 5V		41		mΩ
High-side MOSFET On-Resistance	R_{DSON}	V_{CC} = 5V		33		mΩ
Current Limit						
Peak Switching Current Limit FPWM	I_{LIM_SW}	R_{LIM} = 14.3kΩ	5	6	7	A
Peak Switching Current Limit Auto PFM	I_{LIM_SW}	R_{LIM} = 14.3kΩ	5	6	7	A
Peak Switching Current Limit FPWM	I_{LIM_SW}	R_{LIM} = 57.6kΩ	1.25	1.50	1.75	A
Peak Switching Current Limit Auto PFM	I_{LIM_SW}	R_{LIM} = 57.6kΩ	1.25	1.50	1.75	A

ELECTRICAL CHARACTERISTICS (continued)

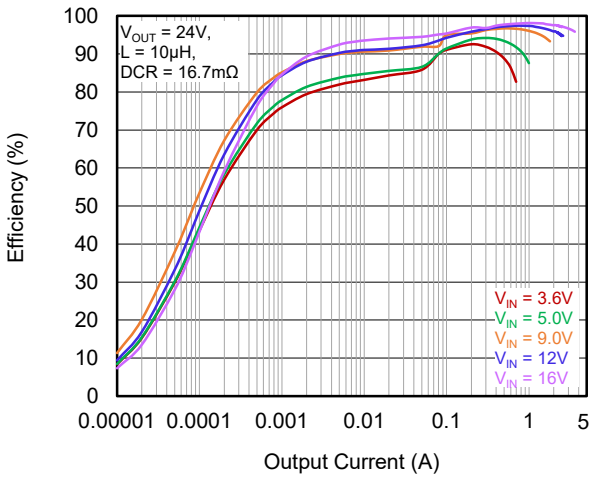
(T_J = -40℃ to +125℃, L = 4.7μH, V_{IN} = 5V and V_{OUT} = 12V, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency						
Switching Frequency	f_{SW}	SGM6618	500	650	800	kHz
		SGM6618A	1000	1200	1400	
Soft-Start Time	t_{SS}			4		ms
Minimum Off-Time	t_{OFF_MIN}			120		ns
Minimum On-Time	t_{ON_MIN}			75		ns
Error Amplifier						
COMP Pin Sink Current	I_{SINK}			20		μA
COMP Pin Source Current	I_{SOURCE}			20		μA
COMP Pin High Clamp Voltage	V_{CCLPH}			1.98		V
COMP Pin Low Clamp Voltage	V_{CCLPL}			0.7		V
Error Amplifier Trans-Conductance	G_{EA}			257		μS
Logic Interface						
EN Logic High Threshold	V_{EN_H}				0.812	V
EN Logic Low Threshold	V_{EN_L}		0.33			V
EN Threshold Hysteresis	V_{EN_HYS}			38		mV
UVLO Rising Threshold	V_{UVLO}		0.75	0.813	0.88	V
Sourcing Current at the EN/UVLO Pin	I_{UVLO_HYS}		1.55	2.00	2.35	μA
MODE Pins Logic High Threshold	V_{MODE_H}				0.8	V
MODE Pins Logic Low Threshold	V_{MODE_L}		0.4			V
MODE Pins Internal Pull-Down Resistor	R_{DOWN}			800		kΩ
Thermal Shutdown						
Thermal Shutdown Rising Threshold	T_{SD_R}	T_J rising		150		℃
Thermal Shutdown Falling Threshold	T_{SD_F}	T_J falling		130		℃

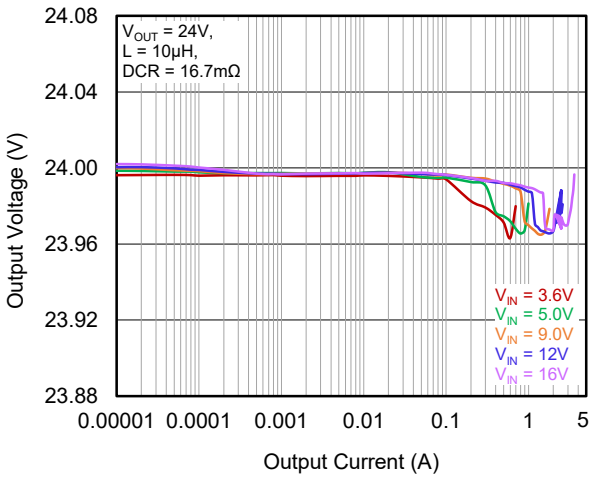
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, f_{SW}= 650kHz, unless otherwise noted.

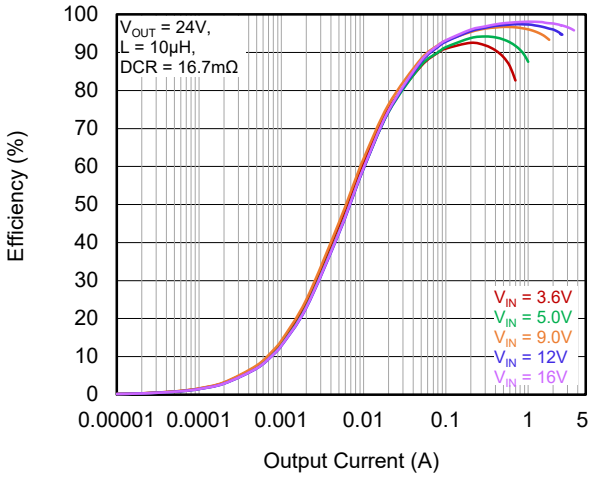
Efficiency vs. Output Current (PFM)



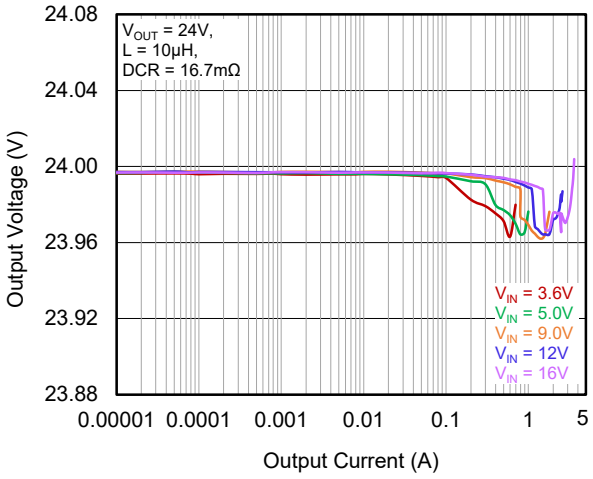
Output Voltage vs. Output Current (PFM)



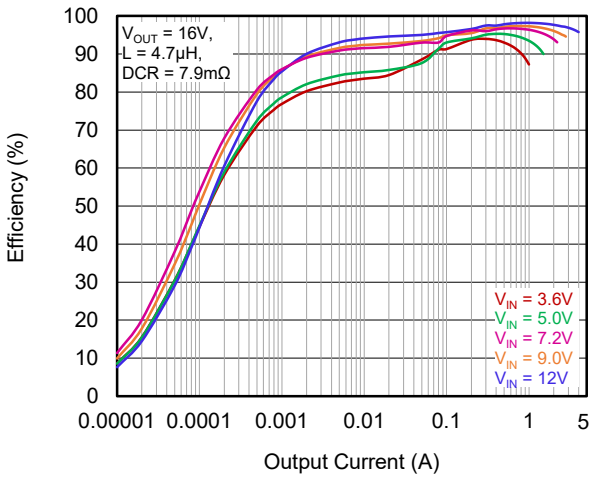
Efficiency vs. Output Current (FPWM)



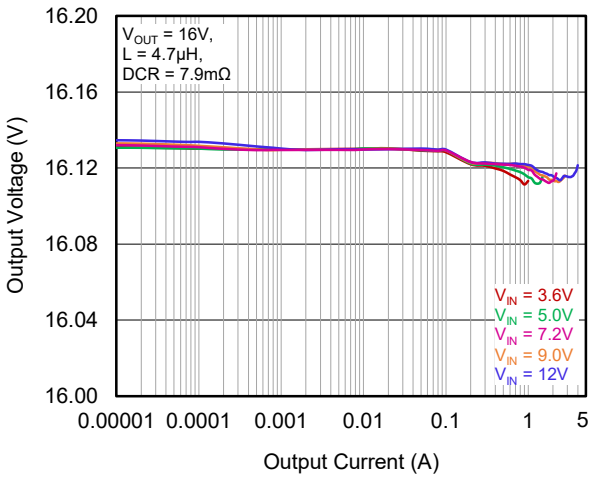
Output Voltage vs. Output Current (FPWM)



Efficiency vs. Output Current (PFM)



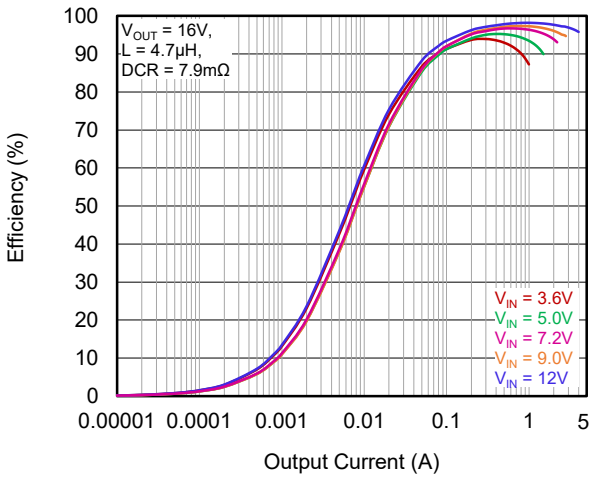
Output Voltage vs. Output Current (PFM)



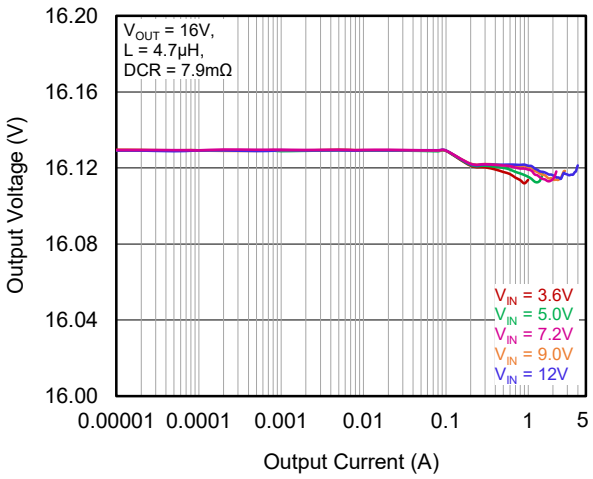
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f_{SW}= 650kHz, unless otherwise noted.

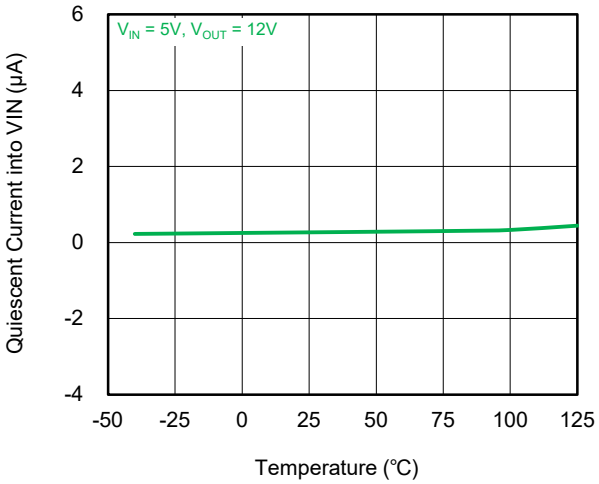
Efficiency vs. Output Current (FPWM)



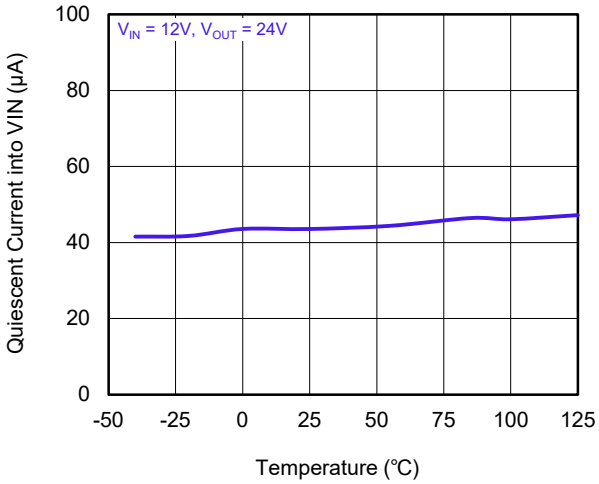
Output Voltage vs. Output Current (FPWM)



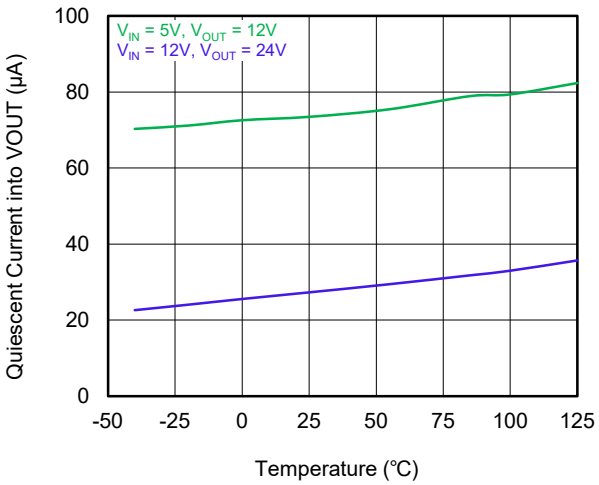
Quiescent Current into VIN vs. Temperature



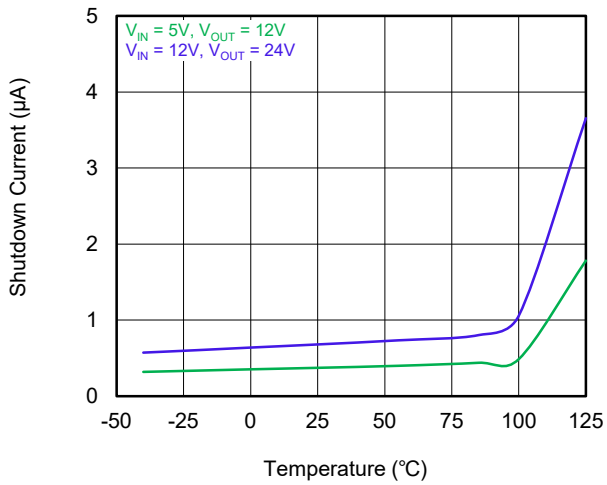
Quiescent Current into VIN vs. Temperature



Quiescent Current into VOUT vs. Temperature



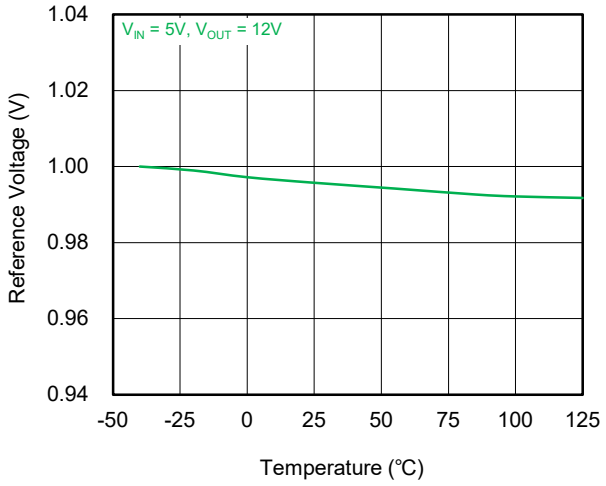
Shutdown Current vs. Temperature



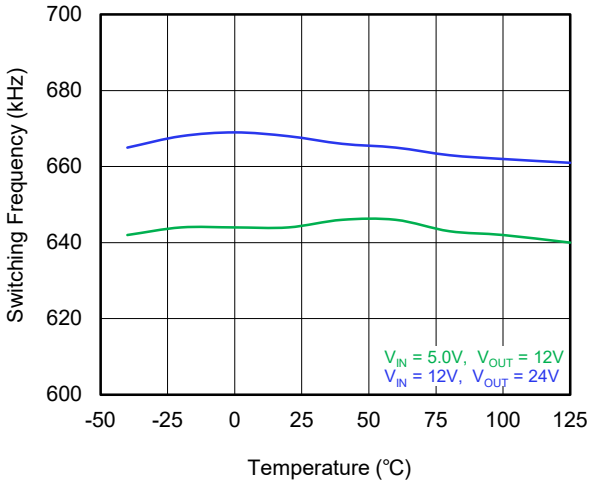
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f_{SW}= 650kHz, unless otherwise noted.

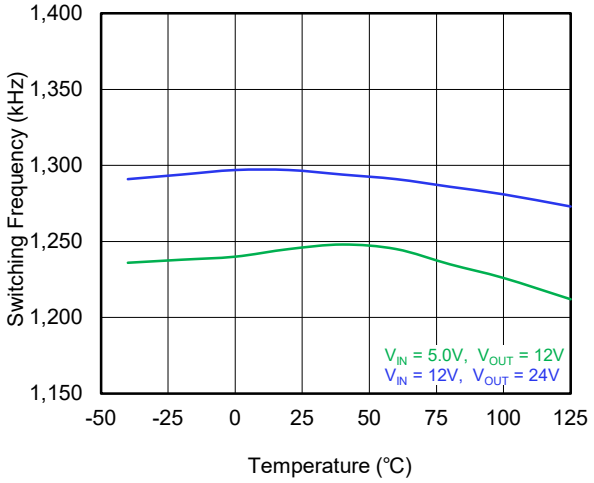
Reference Voltage vs. Temperature



Switching Frequency vs. Temperature



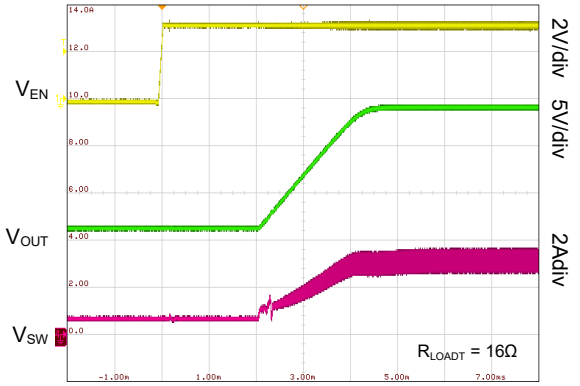
Switching Frequency vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

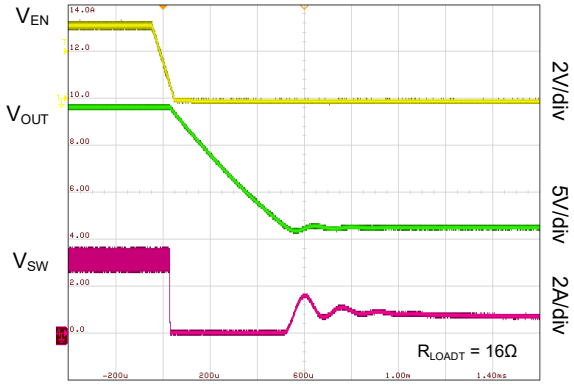
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 24V, C_{OUT} = 78μF, L = 10μH, EVM-based, unless otherwise noted.

Start-up by EN Waveforms



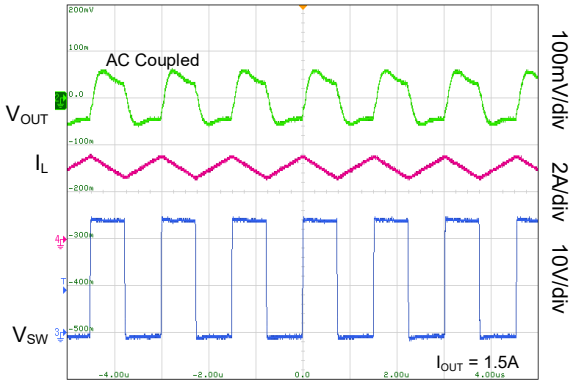
Time (1ms/div)

Shutdown By EN Waveforms



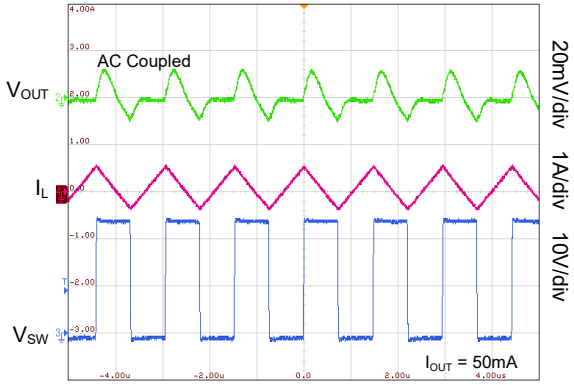
Time (200μs/div)

Switching Waveforms (CCM)



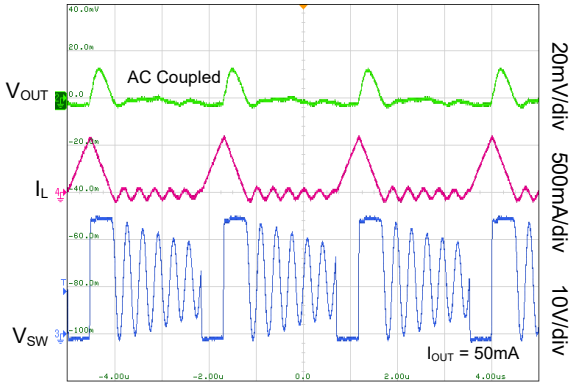
Time (1μs /div)

Switching Waveforms (FPWM)



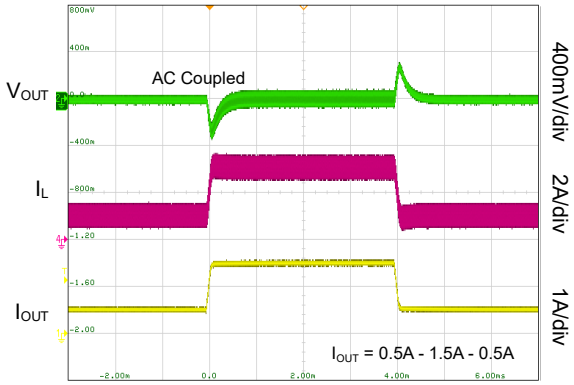
Time (1μs /div)

Switching Waveforms (PFM)



Time (1μs /div)

Load Transient

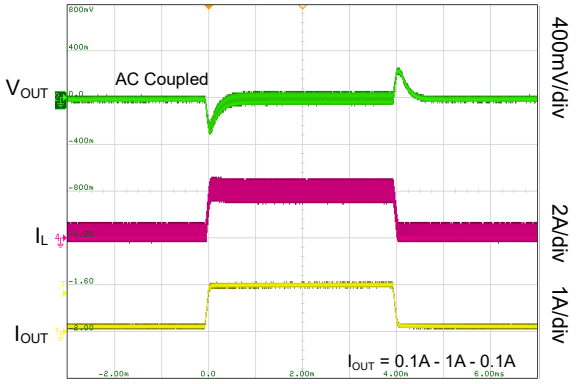


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

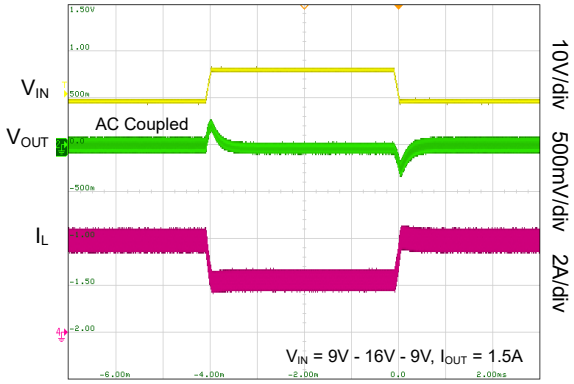
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 24V, C_{OUT} = 78μF, L = 10μH, EVM-based, unless otherwise noted.

Load Transient



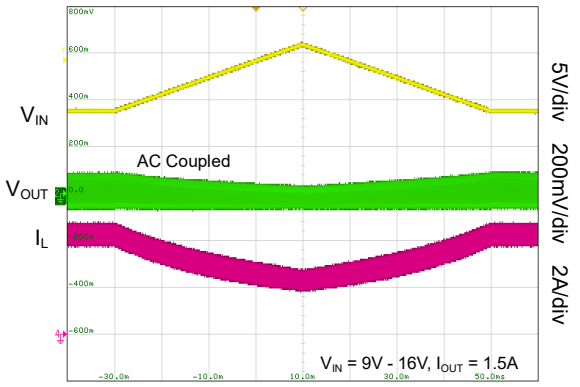
Time (1ms/div)

Line Transient



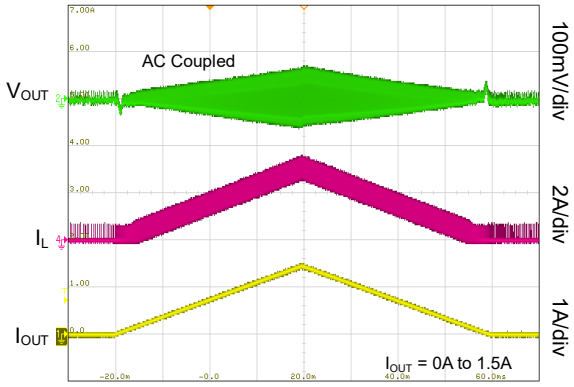
Time (1ms/div)

Line Sweep



Time (10ms/div)

Load Sweep



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

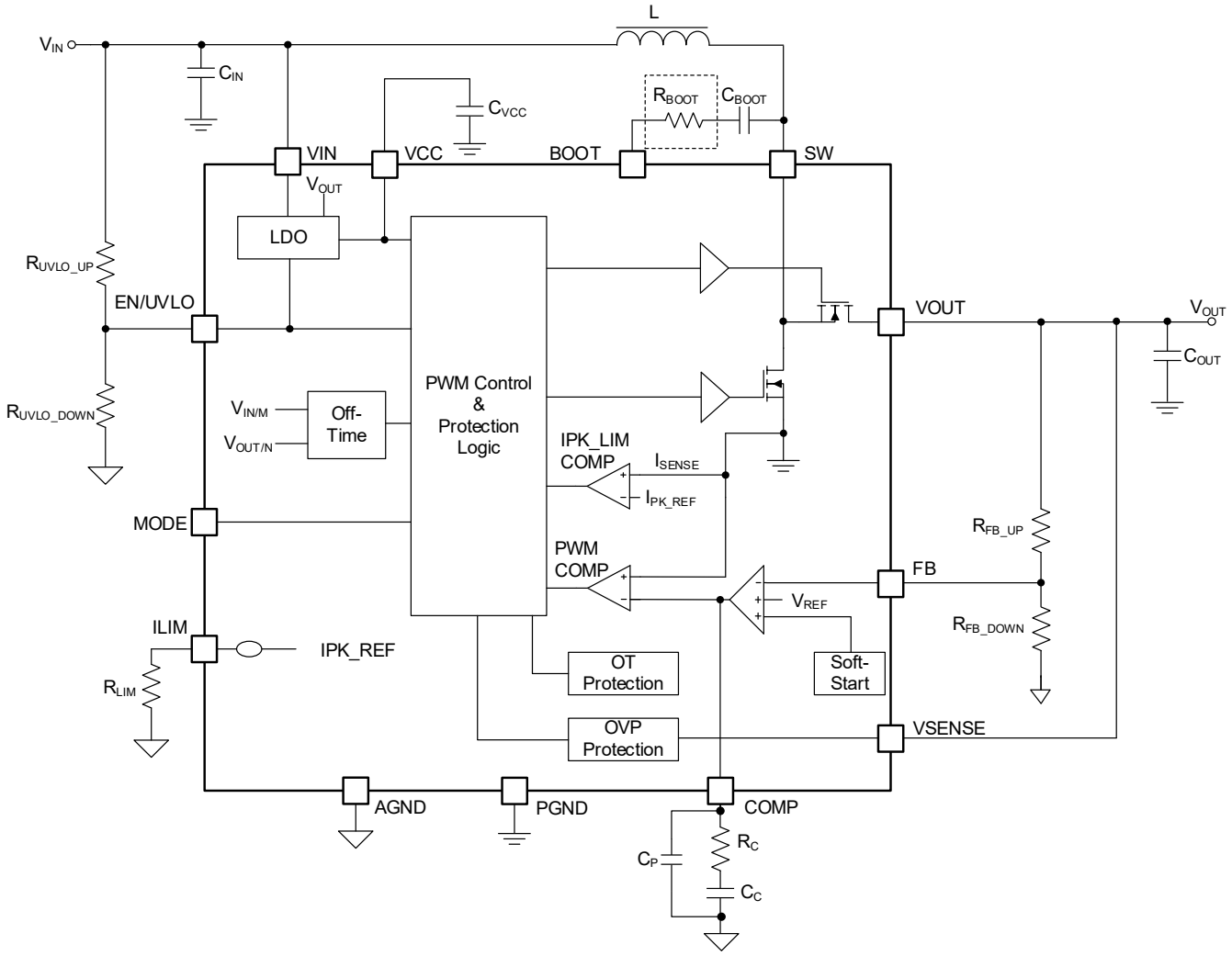


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6618 family is a fully-integrated high-voltage synchronous Boost converter that offers high efficiency and a small size solution with its integrated 41mΩ (TYP) low-side and 33mΩ (TYP) high-side power switches. The SGM6618 family has a wide input voltage range of 2.9V to 23V and provides an adjustable output voltage between 4.5V and 25V, with a switching current capability up to 6A (TYP). The peak switching current is programmable by a resistor connected between the ILIM pin and GND.

The SGM6618 family utilizes the constant off-time peak current control topology for output voltage regulation, which provides enhanced dynamic performance. The device operates in pulse width modulation (PWM) mode under moderate to heavy load conditions. As with conventional adaptive off-time converters, the device modulates its off-time based on the input and output voltages to maintain a quasi-constant switching frequency. For light load conditions, the device provides a choice between two operating modes, selected by the MODE pin. When the MODE pin is logic low, the device operates in auto pulse frequency modulation (PFM) mode, which is used to achieve high light load efficiency. When the MODE pin is logic high, the device operates in forced PWM mode, which keeps the switching frequency quasi-constant to avoid audible noise and other application problems caused by low switching frequency. The SGM6618 family employs external loop compensation, providing flexibility in the selection of inductors and output capacitors. Additionally, the device implements a soft-start function to limit inrush current during start-up. The device also implements various protection features, such as output over-voltage protection (OVP), cycle-by-cycle over-current protection (OCP), and thermal shutdown to improve device robustness.

Feature Description

VCC Power Supply

The internal LDO of SGM6618 family generates a regulated 4.9V output with a 10mA current capability. When the VIN pin voltage is below 5.25V, the LDO is powered from the VOUT pin; when V_{IN} exceeds 5.5V, it switches to the VIN pin for power. A ceramic capacitor of at least 1μF effective must be connected between the VCC and AGND pins to stabilize and decouple the VCC voltage. A capacitor with an X7R or X5R dielectric and a voltage rating of 10V or higher is recommended.

Enable and Programmable UVLO

The SGM6618 family features a combined enable and under-voltage lockout (UVLO) circuit. The device is enabled and begins switching when the VIN voltage exceeds its UVLO rising threshold of 2.8V (TYP) and the EN/UVLO pin is pulled above its own rising threshold. The EN/UVLO pin incorporates an accurate internal voltage reference and sources a hysteresis current (I_{UVLO_HYS}) to implement a programmable input UVLO with hysteresis, thereby preventing on/off chattering from input noise. By using resistor divider as shown in Figure 3, the turn-on threshold can be calculated by Equation 1.

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where, V_{UVLO} is the UVLO threshold of 0.813V (TYP) at the EN/UVLO pin.

The hysteresis voltage is determined by the value of the upper resistor (R_1) in the EN/UVLO divider, thus setting the difference between the turn-on and turn-off thresholds, as given by Equation 2.

$$V_{IN(UVLO)} = I_{UVLO\_HYS} \times R_1 \quad (2)$$

where, I_{UVLO} is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above V_{UVLO}.

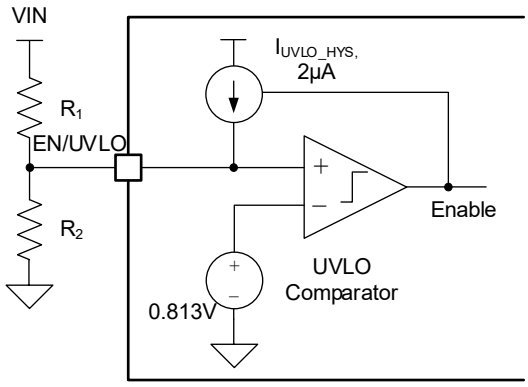


Figure 3. Programmable UVLO with Resistor Divider at EN/UVLO Pin

DETAILED DESCRIPTION (continued)

Soft-Start

The SGM6618 family features a 4ms (TYP) internal soft-start function to prevent excessive inrush current.

When the EN/UVLO pin is pulled high, a constant-current source charges an internal soft-start capacitor. The rising capacitor voltage is compared with a 1V (TYP) internal reference, and the lower voltage is fed to the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the soft-start capacitor voltage charges. The soft-start phase is completed when this capacitor voltage exceeds the 1V internal reference, with a typical rise time of 4ms from 0V to 1V. When the EN/UVLO pin is pulled low, the internal soft-start capacitor is actively discharged to ground.

Switching Frequency

The SGM6618 family regulates the output voltage using an adaptive constant off-time peak current control topology. It operates in pulse width modulation (PWM) mode at moderate to heavy loads, with a quasi-constant switching frequency of 650kHz (1.2MHz for SGM6618A). Under light load conditions, the SGM6618 can be configured via the MODE pin to operate in either auto PFM mode or forced PWM mode.

Programmable Inductor Peak Current Limit

The SGM6618 family integrates an internal, cycle-by-cycle peak switching current limit that is programmable from 1.5A to 6A. Once the switch current reaches the programmed limit threshold, the control circuit immediately turns off the low-side power switch to prevent over-current conditions. This peak current limit is set by a resistor connected from the ILIM pin to ground, with the relationship given by Equation 3.

$$I_{PEAK} = 0.54V \times \frac{160k\Omega}{R_{LIM}} \quad (3)$$

where,

- R_{LIM} is the resistance between the ILIM pin and the AGND pin.
- I_{PEAK} is the typical peak switching current limit.

Based on Equation 3, the resistor between the ILIM pin and AGND should be within the range of 14.4kΩ to 57.6kΩ. For instance, a typical peak switching current of 5.4A is achieved with an R_{LIM} of 16kΩ. The ILIM pin must not be left floating or connected to VCC.

Shutdown

When the input voltage falls below the UVLO threshold or the EN/UVLO pin is pulled low, the SGM6618 family enters shutdown mode, disabling all internal functions.

Over-Voltage Protection

The SGM6618 family provides an output over-voltage protection (OVP). When the voltage at the VSENSE pin is detected above 27.4V (TYP), the device immediately stops switching to prevent output over-voltage and protect downstream circuits. Switching remains disabled until the voltage at the VSENSE pin falls below the OVP threshold by the hysteresis value.

Thermal Shutdown

A thermal shutdown circuit is provided to prevent damage from excessive heat and power dissipation. The protection is typically triggered at a junction temperature of 150℃ (TYP), which stops the device from switching. It recovers automatically and resumes operation once the junction temperature falls below 130℃ (TYP).

DETAILED DESCRIPTION (continued)

Device Functional Modes

Operation

The SGM6618 family operates in quasi-constant frequency pulse-width modulation (PWM) under moderate to heavy loads. For each cycle, a circuit predicts the required off-time based on the VIN-to-VOUT ratio. The cycle begins by turning on the low-side N-MOSFET switch (as shown in Figure 2), and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. Once this peak current is detected by the current comparator, the low-side N-MOSFET switch is turned off. The inductor current then commutates to the body diode of the high-side N-MOSFET during the dead time. After the dead time, the high-side switch is turned on for synchronous rectification. Since V_{OUT} is higher than V_{IN}, the inductor current ramps down during this phase. The high-side switch remains on until the off-time is reached. Following another brief dead time, the low-side switch turns on again to begin the next switching cycle.

At light load conditions, the device provides a choice between two operating modes, PFM mode and forced PWM mode, to meet different application requirements. When the MODE pin is logic high, the device operates in forced PWM mode. When the MODE pin is logic low, the device operates in PFM mode.

Forced PWM Mode

In forced PWM mode, the SGM6618 family maintains a constant switching frequency even under light loads. As the load current decreases, the internal error amplifier reduces its output to lower the inductor peak current, thereby delivering less power. When the output current further reduces, the inductor current may decay to zero before the end of the off-time. It should be noted that the high-side switch remains on, causing the inductor current to reverse direction and creating a reverse power flow from output to input. While this mode leads to reduced efficiency, it effectively prevents audible noise and other issues associated with variable, low switching frequencies.

Auto PFM Mode

In auto PFM mode, the SGM6618 family seamlessly transits between PWM and PFM operations via its smooth on/off-time and automatic pulse-skipping modes, achieving high efficiency across a wide load range. As the load current decreases or VIN increases, the output of the internal error amplifier drops, thereby reducing the inductor peak current and the power delivered to the load. Once this error amplifier output falls to a level corresponding to a peak current of approximately 500mA, the peak current is clamped at this threshold and stops decreasing. To further regulate the output voltage, the device then extends the switching off-time, thereby reducing the energy per cycle delivered to the output. In addition, the output voltage ripple is also small at light load due to low peak current. See Figure 4.

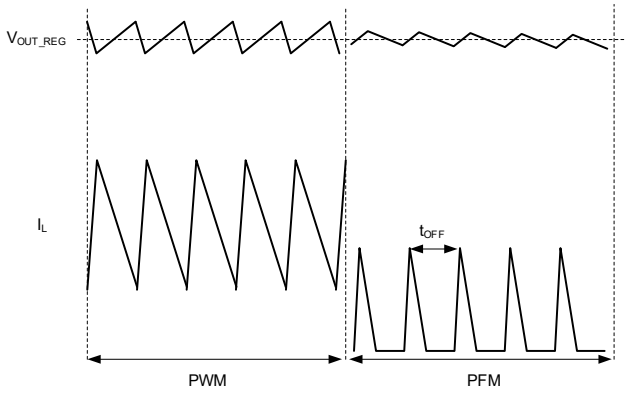


Figure 4. Auto PFM Mode Diagram

APPLICATION INFORMATION

The SGM6618 family is a Boost converter supporting output voltages up to 25V and peak switching current limit up to 6A. It features quasi-constant frequency PWM operation for medium/heavy load conditions. Under light load conditions, the converter can operate in either PFM mode or forced PWM mode, depending on the mode selected. The PFM mode provides higher light load efficiency, while the forced PWM mode can avoid the acoustic noise by maintaining a relatively fixed switching frequency. The adaptive constant off-time peak current control architecture ensures excellent line and load transient response with minimal output capacitance. The SGM6618 family also offers design flexibility, allowing the use of various inductor and output capacitor combinations through external compensation.

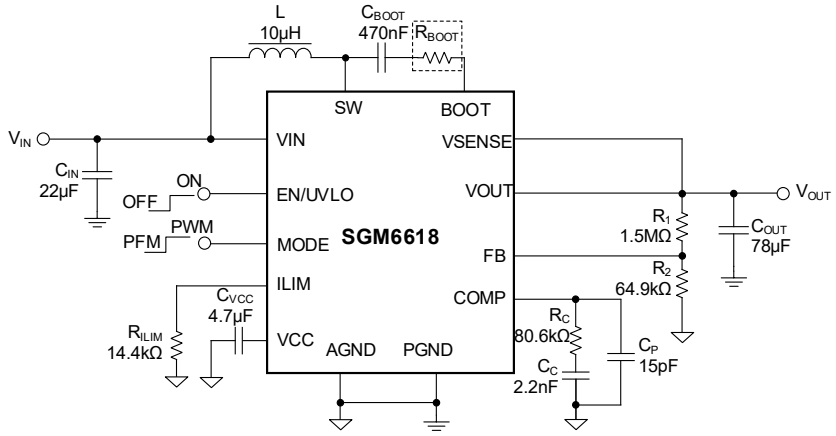


Figure 5. SGM6618 Typical Application Circuit

Design Requirements

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	9V to 16V
Output Voltage	24V
Output Voltage Ripple	100mV Peak-to-Peak
Output Current Rating	1.5A
Operating Frequency	650kHz

Detailed Design Procedure

Setting Output Voltage

The output voltage is set by an external resistor divider (R_1, R_2 in Figure 5). For optimal accuracy, R_2 should be less than 500kΩ to ensure the divider current is at least 100 times greater than the FB pin leakage current. While a lower value for R_2 improves noise immunity, a higher value reduces the quiescent current, thereby increasing light load efficiency.

Once R_2 is selected, the value of R_1 can be calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (4)$$

Inductor Selection

The inductor is the most critical component in a DC/DC switching converter design. Its selection defines the key performance of the converter, including steady-state operation, transient responses, loop stability, and overall efficiency. The three most important inductor specifications are inductance value, DC resistance (DCR), and saturation current.

The SGM6618 family is designed to operate with inductor values ranging from 2.2μH to 10μH. A 2.2μH inductor offers a size advantage, while a 10μH inductor provides lower current ripple, presenting a size/performance trade-off. Furthermore, if the converter's output current is limited by the internal peak current protection, selecting a higher inductance value within this range can help maximize the output current capability.

Consider both the initial tolerance (±20% to ±30% at 0A) and the drop in inductance (20% to 35%) that occurs as the current approaches the saturation point. Consequently, the selected inductor must have a rated saturation current that is higher than the converter's peak inductor current in all cases.

APPLICATION INFORMATION (continued)

For maximum output current, it is recommended to limit the inductor peak-to-peak ripple current to less than 40% of the average inductor current. The worst-case condition's peak-to-peak inductor current can be calculated with Equation 6 to 8: minimum V_{IN}, maximum V_{OUT}, and maximum load current.

To ensure sufficient design margin, perform this calculation using the minimum switching frequency, the inductor's minimum value (accounting for -30% tolerance), and a conservative estimate for power conversion efficiency.

In a Boost converter, calculate the inductor DC current as in Equation 5.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (5)$$

where,

- V_{OUT} is the output voltage of the Boost converter.
- I_{OUT} is the output current of the Boost converter.
- V_{IN} is the input voltage of the Boost converter.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 6.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (6)$$

where,

- I_{PP} is peak-to-peak ripple current of the inductor.
- L is the inductance.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the inductor peak current (I_{LPEAK}) can be calculated using Equation 7.

$$I_{L\_PEAK} = I_{DC} + \frac{I_{PP}}{2} \quad (7)$$

It is important that the peak inductor current must always remain below the inductor saturation current.

It should be noted that higher current ripple increases both DC and AC losses. For higher efficiency, an inductor with lower DCR is generally recommended. However, this often trades off against a larger component footprint. A list of recommended inductors is provided in the table below.

Table 2. Recommended Inductors

Part Number	L (μH)	DCR TYP (mΩ)	Saturation Current (A)	Size (L × W × H, mm)	Vendor
74437356022	2.2	20.3	19.6	9.2×8.5×3.0	WURTH
7443320330	3.3	5.7	24.7	12.1×11.4×9.5	WURTH
7443320470	4.7	7.9	17.1	12.1×11.4×9.5	WURTH
7443320680	6.8	11.0	14.2	12.1×11.4×9.5	WURTH
7443321000	10	16.7	11.3	12.1×11.4×9.5	WURTH

Bootstrap Capacitor Selection

The bootstrap capacitor (connected between BOOT and SW) provides the gate drive current for the high-side FET during the turn-on of each cycle. Therefore, a ceramic capacitor with a value between 0.22μF and 0.47μF is recommended. In addition, a 5Ω resistor in series with C_{BOOT} is necessary.

Input Capacitor Selection

Multilayer ceramic capacitors (MLCCs) are excellent choices for input decoupling due to their very low ESR and compact size. They must be placed as close as possible to the device. While a 22μF capacitor is typically sufficient, a larger value can be used to further reduce input current ripple.

When using only ceramic capacitors at the input with a power source connected via long leads (e.g., a wall adapter), a load step can cause ringing at the VIN pin due to interaction with the lead inductance. This ringing may couple to the output and could be misinterpreted as loop instability or potentially damage the device. To suppress this ringing, place additional bulk capacitance (electrolytic/tantalum) between the power source leads and the local ceramic input capacitor (C_{IN}).

APPLICATION INFORMATION (continued)

Output Capacitor Selection

The output capacitor is selected to meet both steady-state and load-transient requirements, with its value influencing the compensation design. The output voltage ripple is primarily determined by the capacitor's equivalent series resistance (ESR) and its capacitance. For a theoretical capacitor with zero ESR, the minimum required capacitance for a target ripple can be calculated using Equation 8.

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (8)$$

where,

- C_{OUT} is the output capacitor.
- I_{OUT} is the output current.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- ΔV is the output voltage ripple required.
- f_{SW} is the switching frequency.

The additional output voltage ripple component due to the capacitor's ESR is given by Equation 9:

$$\Delta V_{ESR} = I_{L\_PEAK} \times R_{ESR} \quad (9)$$

where,

- ΔV_{ESR} is the output voltage ripple caused by ESR.
- R_{ESR} is the equivalent series resistance of the output capacitor.

While the ESR of ceramic capacitors is not negligible, the ESR of tantalum or electrolytic capacitors must be considered in ripple calculations.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 10:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (10)$$

where,

- ΔI_{STEP} is the transient load current step.
- ΔV_{TRAN} is the allowed voltage dip for the load current step.
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero).

The DC bias derating characteristic of ceramic capacitors must be carefully considered in design. Capacitance can decrease by as much as 70% at its rated voltage. Therefore, enough margins on the voltage rating must be considered to guarantee that sufficient capacitance is maintained at the actual output voltage.

Loop Stability

The SGM6618 family features external compensation for customizable loop optimization. The COMP pin serves as the output of the internal error amplifier. An external compensation network - comprising resistor R_C and ceramic capacitors C_C and C_P - is connected to this pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by Equation 11.

$$G_{PS}(S) = K_{COMP} \times \frac{R_O \times (1-D)}{2} \times \frac{\left(1 + \frac{S}{2\pi f_{ESRZ}}\right) \times \left(1 - \frac{S}{2\pi f_{RHPZ}}\right)}{1 + \frac{S}{2\pi f_P}} \quad (11)$$

where,

- D is the switching duty cycle.
- R_O is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current/comp voltage), which is 6.5A/V.

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (12)$$

where, C_O is effective output capacitance.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (13)$$

where, R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (14)$$

APPLICATION INFORMATION (continued)

The COMP pin is the output of the internal transconductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2\pi f_{COMZ}}\right)}{\left(1 + \frac{S}{2\pi f_{COMP1}}\right) \times \left(1 + \frac{S}{2\pi f_{COMP2}}\right)} \quad (15)$$

where,

- G_{EA} is the trans-conductance of the amplifier, which is 257μS (TYP).
- R_{EA} is the output resistance of the amplifier, which is 16MΩ.
- V_{REF} is the reference voltage at the FB pin.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. A higher crossover frequency generally yields a faster transient response. As a general guideline, f_C should not exceed the lower of either one-tenth of the switching frequency (f_{SW}/10) or one-fifth of the right-half-plane zero frequency (f_{RHPZ}/5).

Then set the value of R_C, C_C, and C_P (in Figure 5) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1-D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (16)$$

where, f_C is the selected crossover frequency. The value of C_C can be calculated by Equation 17.

$$C_C = \frac{R_O \times C_O}{2R_C} \quad (17)$$

The value of C_P can be calculated by Equation 18.

$$C_P = \frac{R_{ESR} \times C_O}{R_C} \quad (18)$$

If the calculated value of C_P is less than 10pF, it can be left open.

Designing the control loop for a phase margin greater than 45° and a gain margin greater than 10dB ensures stable operation by preventing output voltage ringing during line and load transients.

Power Supply Recommendations

The device is designed for an input voltage supply range of 2.9V to 23V, which must be well-regulated. If the supply is located far away from the converter, additional bulk capacitance may be required. A typical solution is to add a 47μF electrolytic or tantalum capacitor.

The internal body diode of the high-side MOSFET creates an always-on path from VIN to VOUT, an external Schottky diode connected SW to VOUT is necessary in VIN plug-in applications. Furthermore, the Schottky diode is also required in high V_{IN} applications when the device is in shutdown mode but a heavy load continues to draw current from VOUT to VIN via the high-side MOSFET's body diode.

APPLICATION INFORMATION (continued)

Layout Guidelines

PCB layout is vital for stability and noise performance, especially in high-frequency, high-current designs like this switching power supplies. Consequently, to maximize efficiency, the switch node rise and fall times are minimized, which requires careful management of the high-frequency switching path to prevent unwanted radiation (for example, EMI). Therefore, minimize the length and area of all SW pin traces and employ a ground plane beneath the regulator to reduce interplane coupling.

Place the input capacitor as close as possible to the VIN and PGND pins to minimize input supply ripple.

Additionally, keep all high-current power paths - including VOUT, the output capacitor, and PGND - as short and wide as possible to reduce parasitic inductance.

Thermal management must be carefully considered in the layout due to the SGM6618/A's high power density. To enhance thermal performance, connect the high-current pins (SW, VOUT, and PGND) to large copper polygons. Additionally, placing thermal vias underneath the SW pin further improves heat dissipation.

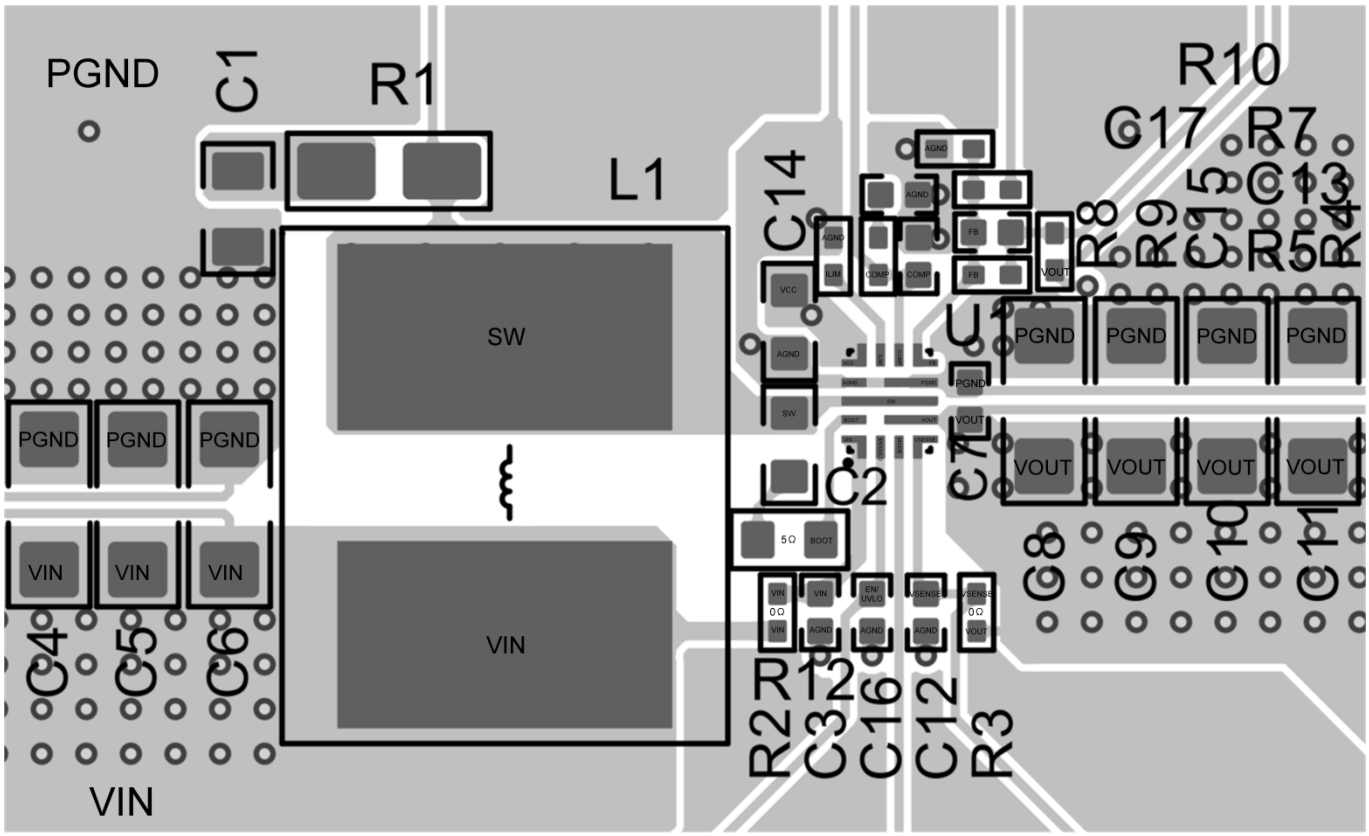


Figure 6. Layout Example

REVISION HISTORY

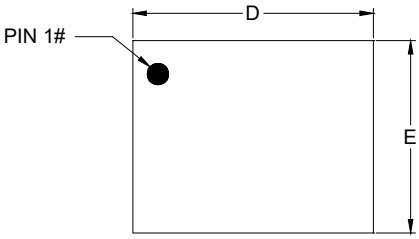
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2026 – REV.A to REV.A.1	Page
Updated Figure 6 Layout Example	20

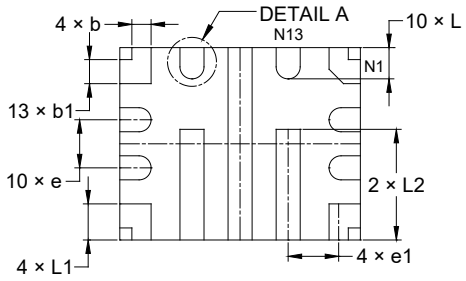
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

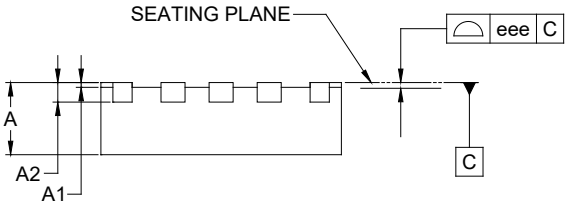
TQFN-2.5×2-13L



TOP VIEW



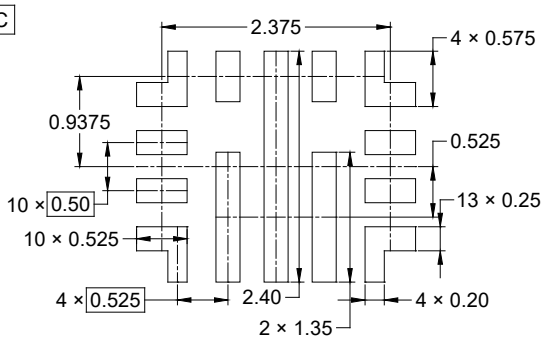
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



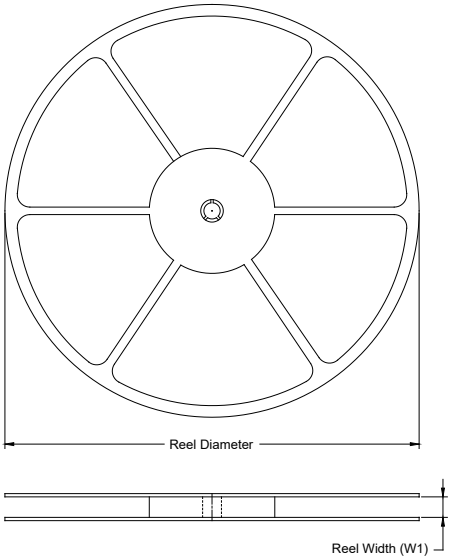
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
b1	0.200	-	0.300
D	2.400	-	2.600
E	1.900	-	2.100
e		0.500 BSC	
e1		0.525 BSC	
L	0.225	-	0.425
L1	0.275	-	0.475
L2	1.050	-	1.250
eee		0.080	

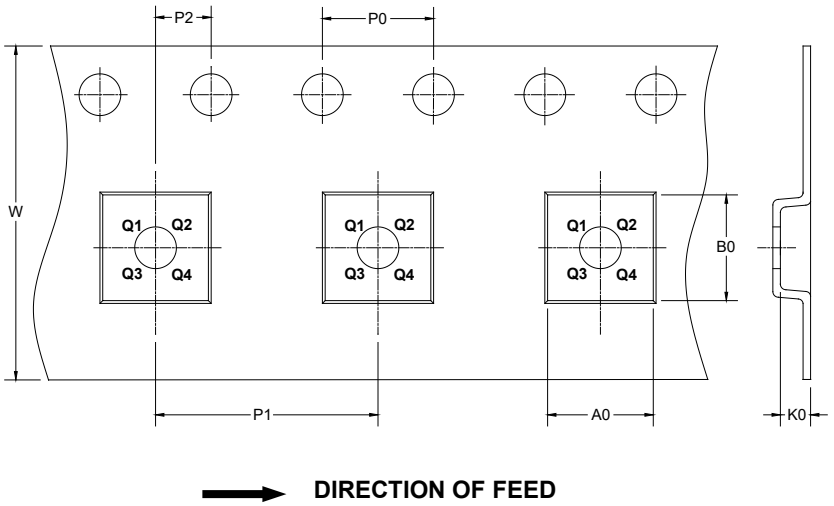
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



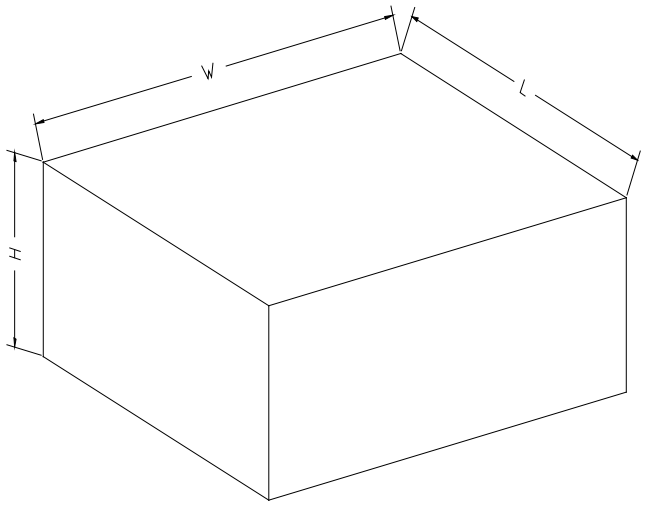
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.5×2-13L	7"	9.5	2.25	2.80	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002