SGM851
Low-Power, Push-Button Controller with Configurable Delay

GENERAL DESCRIPTION

The SGM851 family is a push-button controller with configurable delay, which has the advantages of low supply current and ultra-small package size. The device has a long timing delay to reset the system as required, and enter the low-power mode after the timing delay ends. It can not only avoid the reset caused by the button closing or pressing for a short time, but also distinguish hard system reset and software interruption.

The input pins of SGM851A/BC/BG are PB1 and PB2, while the input pin of SGM851CG is PB1. The output pin of all devices is an active-low, open-drain output (nRST). For SGM851A, nRST goes low when both PB1 and PB2 remain low for the set timing delay, and nRST goes high when either a PBx input goes high. For SGM851BC/BG, nRST goes low when both PB1 and PB2 remain low for the set timing delay, and nRST goes high after a fixed time reset pulse. For SGM851CG, nRST goes low when PB1 remain low for the set timing delay, and nRST goes high after a fixed time reset pulse.

The nRST pin is an active-low, open-drain output and can be wire-ORed with other open-drain devices. All devices have the advantages of accurate reset, low supply current and ultra-small size in applications.

The SGM851 family is available in a Green UTDFN-1.45×1-6AL package. They specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Operating Voltage Range: 1.6V to 6.5V**
- **Single (SGM851CG) or Dual (SGM851A/BC/BG) Push-Button Inputs**
- **Low Supply Current:**
  - **SGM851A: 100nA (TYP)**
  - **SGM851BC/BG/CG: 50nA (TYP)**
- **Two-State Logic, User-Selectable Input Delay:**
  - **SGM851A: 7.5s and 12.5s**
  - **SGM851BC/BG/CG: 0s and 7.5s**
- **Fixed Time Reset Pulse at nRST:**
  - **SGM851BC: 80ms (TYP)**
  - **SGM851BG/CG: 400ms (TYP)**
- **Active-Low, Open-Drain Output**
- **Available in a Green UTDFN-1.45×1-6AL Package**

APPLICATIONS

Computers
Gaming Consoles
Portable Equipment
Navigation Devices
Consumer Medical

TYPICAL APPLICATION

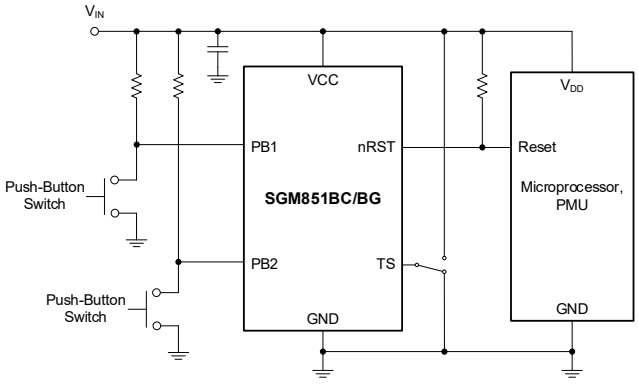


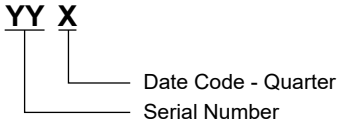
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM851A	UTDFN-1.45×1-6AL	-40℃ to +125℃	SGM851AXUDL6G/TR	01X	Tape and Reel, 5000
SGM851BC	UTDFN-1.45×1-6AL	-40℃ to +125℃	SGM851BCXUDL6G/TR	02X	Tape and Reel, 5000
SGM851BG	UTDFN-1.45×1-6AL	-40℃ to +125℃	SGM851BGXUDL6G/TR	03X	Tape and Reel, 5000
SGM851CG	UTDFN-1.45×1-6AL	-40℃ to +125℃	SGM851CGXUDL6G/TR	04X	Tape and Reel, 5000

MARKING INFORMATION

NOTE: X = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MODEL	Push-Button Inputs	Push-Button Timer, t_{TIMER} (s)		Reset Pulse Duration t_{nRST} (ms)
		TS = VCC	TS = GND	
SGM851A	Dual	12.5	7.5	—
SGM851BC	Dual	0	7.5	80
SGM851BG	Dual	0	7.5	400
SGM851CG	Single	0	7.5	400

ABSOLUTE MAXIMUM RATINGS

VCC, nRST, PB1, PB2, TS Pins Voltage ..... -0.3V to 7V
nRST Pin Current 20mA
Package Thermal Resistance
UTDFN-1.45×1-6AL, θ_{JA} ..... 262.2℃/W
UTDFN-1.45×1-6AL, θ_{JB} ..... 83.7℃/W
UTDFN-1.45×1-6AL, θ_{JC} ..... 161.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... ±4000V
CDM ..... ±1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage, V_{CC} ..... 1.6V to 6.5V
PB1,PB2, TS Pins Voltage ..... 0V to 6.5V
nRST Pin Voltage, V_{nRST} ..... 0V to 6.5V
nRST Pin Current, I_{nRST} ..... 0.35μA to 8mA

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

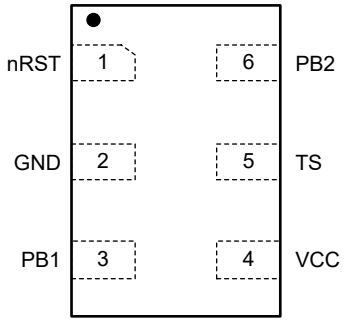
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

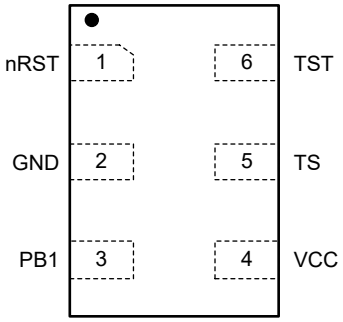
PIN CONFIGURATIONS

SGM851A/BC/BG (TOP VIEW)



UTDFN-1.45×1-6AL

SGM851CG (TOP VIEW)



UTDFN-1.45×1-6AL

PIN DESCRIPTION

NAME	PIN NUMBER		FUNCTION
	SGM851A/BC/BG	SGM851CG	
nRST	1	1	Active-Low Open-Drain Reset Output Pin. When the output is in a high-impedance state, a pull-up resistor is needed.
GND	2	2	Ground.
PB1	3	3	Push-Button Input Pin. The nRST goes low when PB1 and PB2 remain low for the set timing delay.
VCC	4	4	Supply Voltage Pin. The VCC pin requires a power supply of 1.6V to 6.5V to power the device. A 0.1μF bypass capacitor is recommended to connected to VCC pin.
TS	5	5	Push-Button Timer Selection Pin. It can be connected to VCC or GND to set different delay time. The status of TS can not be changed under normal operating conditions. The TS pin status can be changed only when the device is powered off or a PBx input is high.
PB2	6	—	Push-Button Input Pin. The nRST goes low when PB1 and PB2 remain low for the set timing delay.
TST	—	6	This pin needs to be connected to GND or VCC under normal operating conditions.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.6V to 6.5V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, V_{CC} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		1.6		6.5	V
Supply Current (Standby)	I_{CC}	SGM851A, V_{CC} = 3.3V		100		nA
		SGM851A, V_{CC} = 6.5V			400	
		SGM851BC/BG/CG, V_{CC} = 3.3V		50		
		SGM851BC/BG/CG, V_{CC} = 6.5V			330	
Supply Current (Active Timer) (1)	I_{CC}	SGM851A/BC/BG, V_{CC} = 6.5V		0.49	1.5	μA
		SGM851CG, V_{CC} = 6.5V		86	136	
High-Level Input Voltage	V_{IH}	SGM851A	0.85			V
		SGM851BC/BG/CG	0.7 × V_{CC}			
Low-Level Input Voltage	V_{IL}	SGM851A			0.35	V
		SGM851BC/BG/CG			0.3 × V_{CC}	
PB1 Internal Pull-Up Resistance	R_{PB1}	SGM851CG		76		kΩ
Input Current (PB1, PB2)	I_{PB}	PBx = V_{CC}	-200		200	nA
		SGM851A/BC/BG, PBx = 0V	-50		50	
Low-Level Output Voltage	V_{OL}	V_{CC} = 4.5V, I_{SINK} = 8mA			0.4	V
		V_{CC} = 3.3V, I_{SINK} = 5mA			0.3	
		V_{CC} = 1.6V, I_{SINK} = 3mA			0.3	
Open-Drain Output Leakage Current	I_{LKG}	V_{nRST} = 6.5V	-0.35		0.35	μA

NOTE:

1. For SGM851CG, the supply current (active timer) includes the current through the internal pull-up resistor between PB1 and VCC.

TIMING REQUIREMENTS

(V_{CC} = 1.6V to 6.5V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, V_{CC} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Push-Button Timer (1)	t_{TIMER}		-24.0		17.5	%
		SGM851A, TS = GND	5.7	7.5	8.9	s
		SGM851A, TS = VCC	9.5	12.5	14.7	
		SGM851BC/BG/CG, TS = GND	5.7	7.5	8.9	
		SGM851BC/BG/CG, TS = VCC		620		μs
Reset Pulse Duration	t_{nRST}	SGM851BC	60	80	94	ms
		SGM851BG/CG	304	400	470	
Detection Delay (From Input to nRST) (2)	t_{DD}	For 0s t_{TIMER} condition		620		μs
Start-up Delay (2)	t_{SD}	VCC rising		710		μs

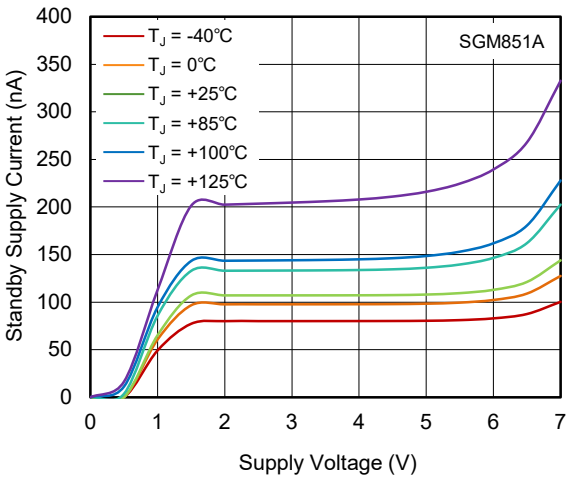
NOTES:

1. The TS pin is recommended to connect to GND under normal operating conditions. For factory testing or debugging, the TS pin can be connected to VCC with a 0s timer.

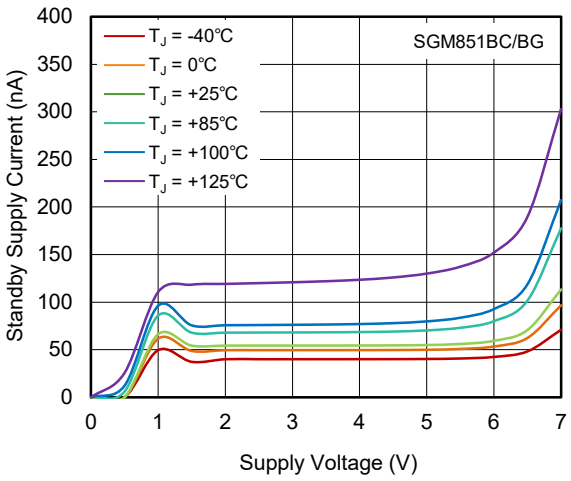
2. If the TS pin is connected to VCC with a 0s timer, reset is active after a detection delay when both PB inputs are low. If TS = VCC with a 0s timer, reset is active after a start-up delay when both PB inputs are low during power-on. This value is specified by design.

TYPICAL PERFORMANCE CHARACTERISTICS

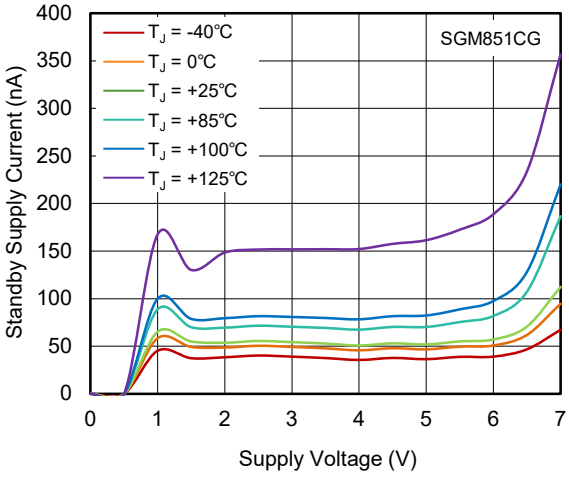
Standby Supply Current vs. Supply Voltage



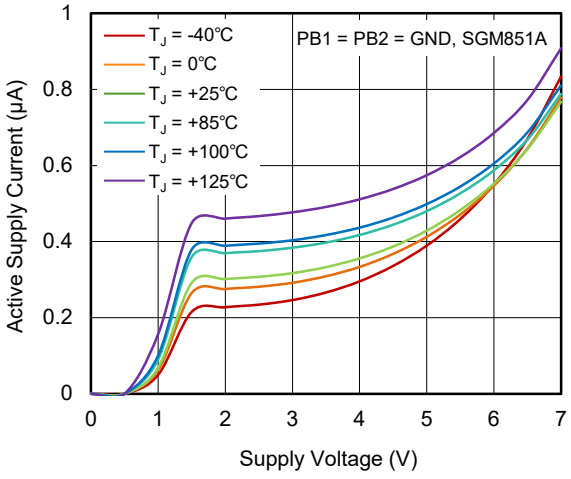
Standby Supply Current vs. Supply Voltage



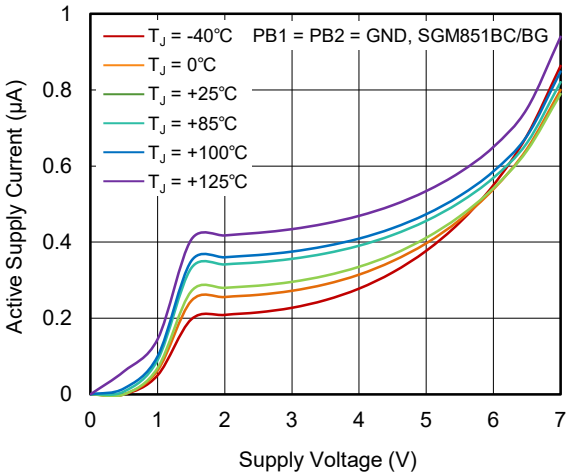
Standby Supply Current vs. Supply Voltage



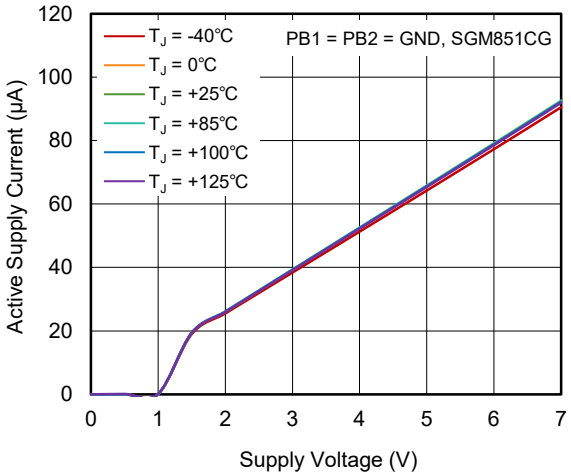
Active Supply Current vs. Supply Voltage



Active Supply Current vs. Supply Voltage

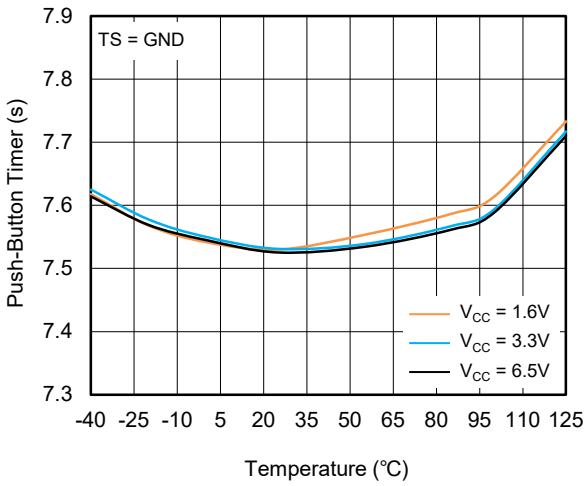


Active Supply Current vs. Supply Voltage

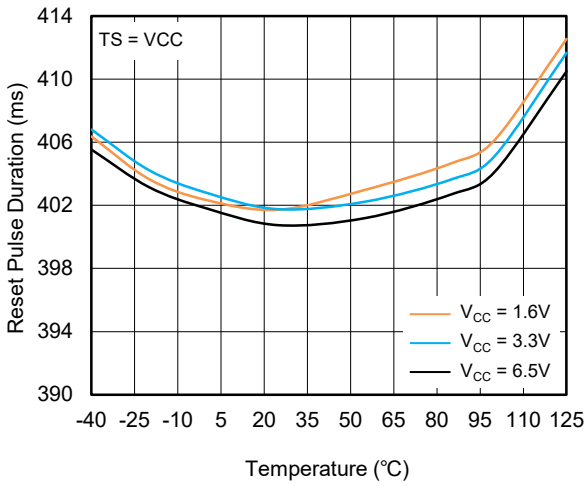


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

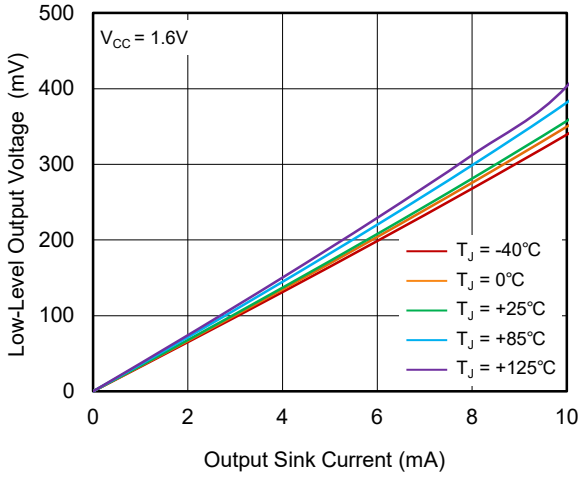
Push-Button Timer vs. Temperature



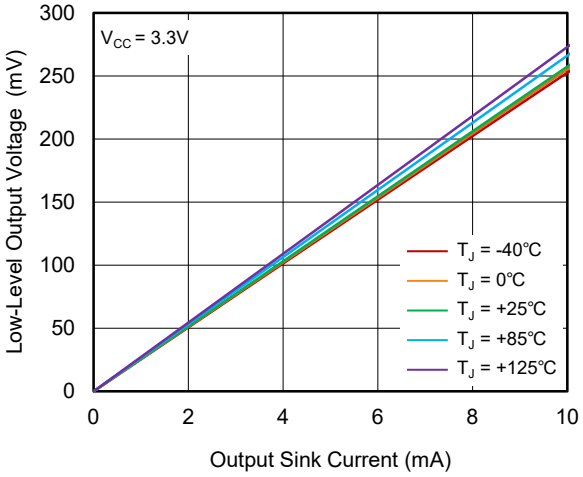
Reset Pulse Duration vs. Temperature



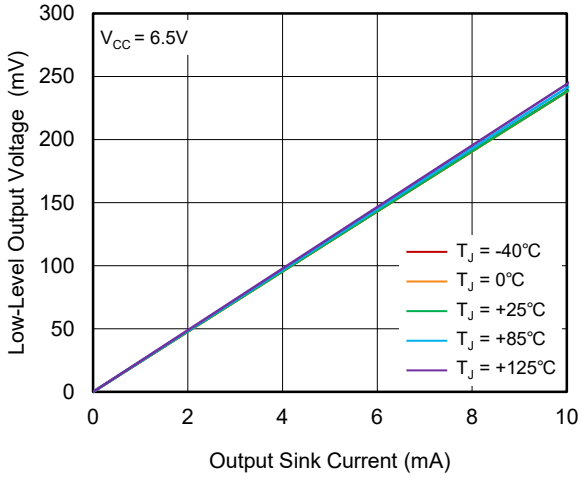
Low-Level Output Voltage vs. Output Sink Current



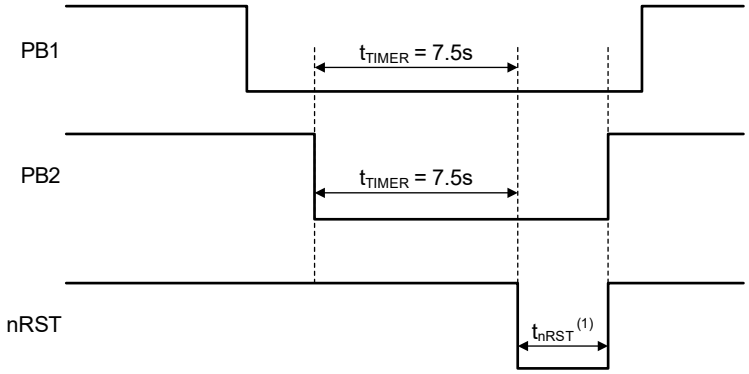
Low-Level Output Voltage vs. Output Sink Current



Low-Level Output Voltage vs. Output Sink Current



TIMING DIAGRAMS



NOTE: 1. t_{nRST} is not a fixed time for SGM851A, but depends on one of the PBx pins going high.

Figure 2. SGM851A Timing Diagram

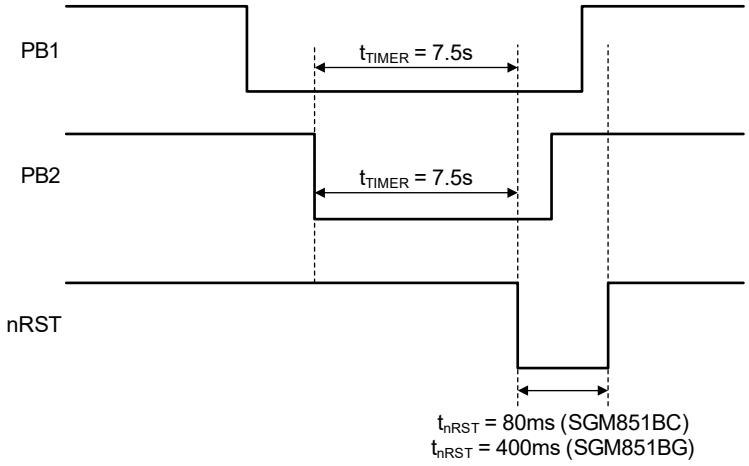


Figure 3. SGM851BC/BG Timing Diagram

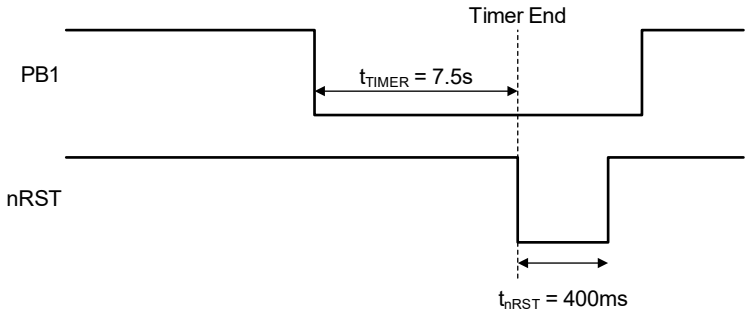


Figure 4. SGM851CG Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

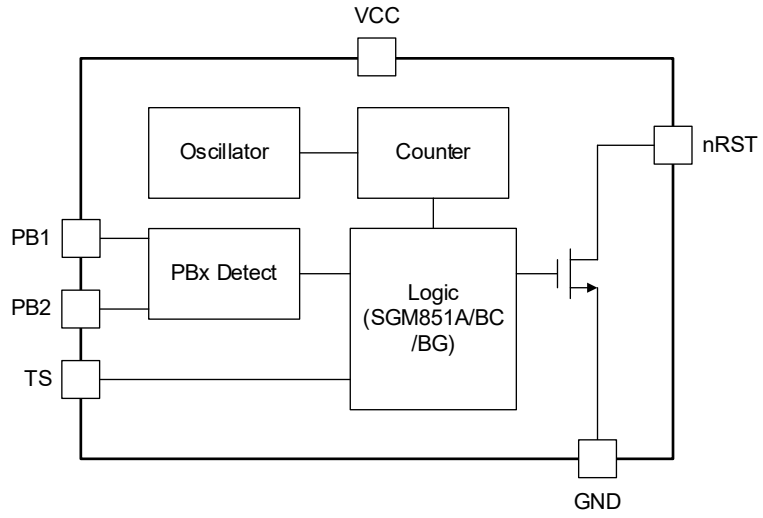


Figure 5. SGM851A/BC/BG Block Diagram

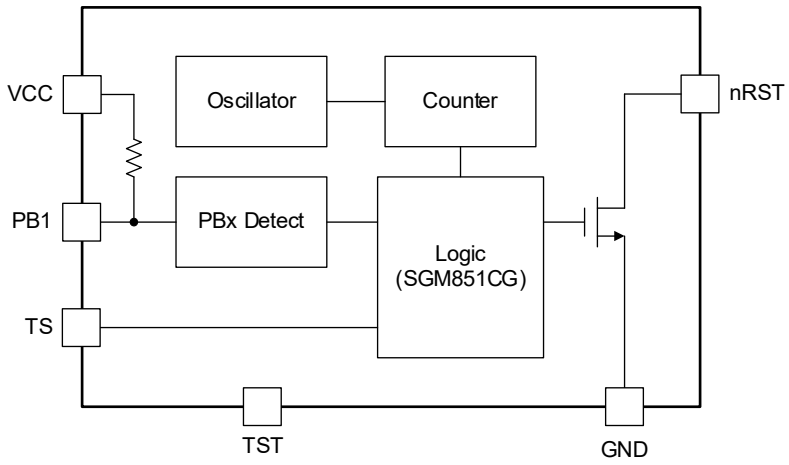


Figure 6. SGM851CG Block Diagram

DETAILED DESCRIPTION

The SGM851 family is a push-button controller with an selectable long setting period to prevent resets from a short switch closures. See Table 1 for more details.

The SGM851A is a device with two input channels. The output signal nRST resets to be low when both input channels (PB1 and PB2) remain low for the duration of push-button timer, and it becomes high if either input (PBx) is released.

The SGM851BC/BG also has two input channels. The output signal nRST resets to be low when both input channels (PB1 and PB2) remain low for the duration of push-button timer, and it becomes high after a preset time-out duration.

The SGM851CG is a device with single input-channel. The reset signal becomes activated (low level) when the input signal remains low for the duration of push-button timer, and it becomes high after a preset time-out duration.

The SGM851 series has TS pins which are used to adjust two different push-button timers of the device. The different timers can be selected by connecting the TS pin to VCC or to GND.

Feature Description

Push-Button Timer Selection (TS)

The push-button timer of SGM851 series has two different options and can be selected by changing the connection of TS pin to VCC or GND. The different timings are shown in Table 2 below.

During the power-up of VCC, the state of the TS pin is checked and confirmed. To avoid incorrect operation, the connection of TS pin cannot be changed if both input channels (PB1 and PB2) are detected as low. The state of the TS pin can only be altered when either input signal (PB1 or PB2) goes high or when VCC is powered off.

Inputs

The two input channels (PB1 and PB2) of the SGM851A are NMOS-based threshold inputs. And when both inputs are detected as low for the duration of the button timer (t_{TIMER}), the output will be reset. For each valid input condition as described previously, the device sends the reset state only once. If either of the two inputs goes high, the reset state is stopped and a new reset pulse can be activated when a new input condition occurs for t_{TIMER}. The block diagram is shown in Figure 5.

The SGM851BC/BG has two digital logic input channels. And when both inputs are detected as low for t_{TIMER}, the output will be reset low and the reset-state holds for a fixed reset pulse duration (t_{nRST}). For each valid input condition as described previously, the device sends the reset state only once. Only if either of the two inputs goes high, a new reset pulse can be activated when a new input condition occurs for t_{TIMER}. The block diagram is shown in Figure 5.

Table 1. Device Family Options

Device	Channels	Input	Reset Behavior (Deassertion)
SGM851A	2	NMOS-based threshold	Input (PBx) dependent
SGM851BC/BG	2	External pull up to VCC	Fixed pulse
SGM851CG	1	Internal pull up	Fixed pulse

Table 2. Push-Button Timer Option Examples

MODEL	Push-Button Inputs	Push-Button Timer, t_{TIMER} (s)		Reset Pulse Duration t_{nRST} (ms)
		TS = VCC	TS = GND	
SGM851A	Dual	12.5	7.5	—
SGM851BC	Dual	0	7.5	80
SGM851BG	Dual	0	7.5	400
SGM851CG	Single	0	7.5	400

DETAILED DESCRIPTION (Continued)

The SGM851CG has a single digital logic input channel with an internal pull-up resistor. When the input is detected low for t_{TIMER}, the output is reset (pulled low). The reset-state holds for a fixed t_{nRST} and is independent of the input state. The output resets only one time when the input condition is met. The reset is only triggered again when the input pin is released and turns low again. The block diagram is shown in Figure 6.

Output (nRST)

The output of the SGM851 series is an open-drain structure. The output needs a pull-up resistor to maintain a high level when it is in a high-impedance state (not in reset state). Through the pull-up resistor, the output can be connected to another power rail which is independent on the input rail of the device. The output voltage can be pulled up to maximum 6.5V. The value of the pull-up resistor should be correctly determined to ensure the proper output voltage. The resistor is dependent on the V_{OL}, sink current capability, and the leakage current of the output. The specifications of the resistors are shown in Electrical Characteristics.

The Inputs (PB1, PB2) describes how the output is asserted or deasserted. See Figure 2 (SGM851A), Figure 3 (SGM851BC/BG), or Figure 4 (SGM851CG) for a timing diagram that describes the relationship between the PB1 and PB2 inputs and the output.

Figure 7 shows the timing diagram of SGM851BC/BG output with the relationship of PB1 and PB2.

From the above diagram, if either input pulses change (From low to high and then to low) during the reset period of the output, the SGM851BC/BG is unable to recognize this shift in pulses. If either PB1 or PB2 turns high, the reset state is removed and the device can detect a new cycle of valid input conditions as stated previously.

Device Functional Modes

Normal Operation (V_{CC} > 1.6V)

Once V_{CC} is higher than 1.6V (V_{CC_MIN}) for nearly 710μs (t_{SD}), the reset signal (nRST) responds to the status of the input pins PBx and the device starts to work normally. Details can be found in Table 1.

Below V_{CC_MIN} (1.3V < V_{CC} < 1.6V)

If V_{CC} is below V_{CC_MIN} but within the range of 1.3V to 1.6V, the output nRST works normally but the electrical specifications in Electrical Characteristics and Timing Requirements may not be met any more.

Power-On Reset (V_{CC} < 1.3V)

When V_{CC} is lower than 1.3V, the nRST pin ought to turn into high-impedance state. However, this may not be always satisfied under all conditions.

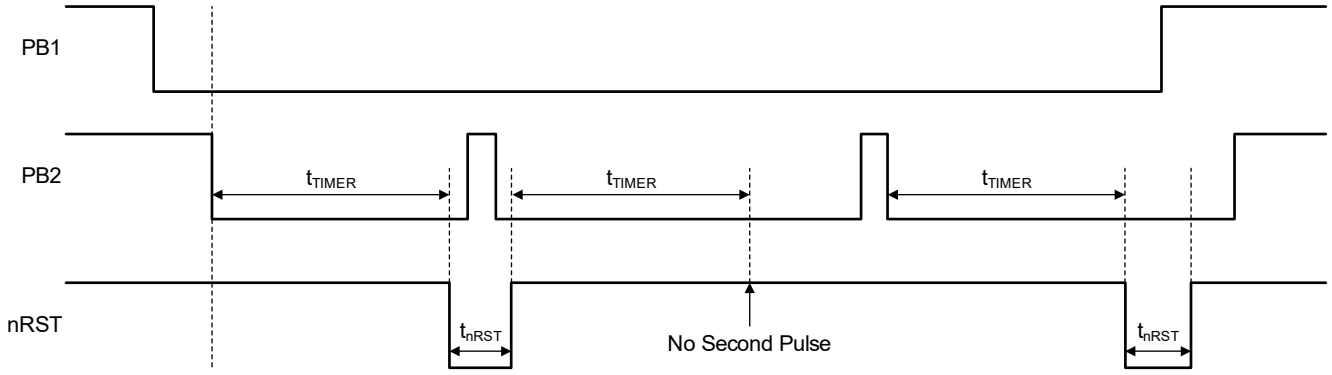


Figure 7. SGM851BC/BG Reset Timing Diagram

APPLICATION INFORMATION

The SGM851 family is a push-button controller with configurable delay, which has the advantages of low supply current and ultra-small package size. To prevent undesired resets due to short jitters of push-button, a long timing delay is adopted to provide the reset signals for the system. This method helps distinguish the user input from the hardware resets. The SGM851 has an open-drain output, with the input range of 1.6V to 6.5V and the temperature range of -40℃ to +125℃.

If two inputs need to be monitored, the SGM851A and SGM851BC/BG are preferred. However, for the cases of only one input in need, the SGM851CG is more suitable.

Typical Applications

Single Input with Fixed Reset Pulse Duration

It is suitable to use the SGM851CG when only one input pin is desired to determine the state of the logic pin (nRST). For example, the input pin PB1 of the SGM851CG can be used to assert a load switch. Once a reset signal is detected, the nRST is active low for a fixed amount of time (t_{nRST}) whatever the status of PB1 changes.

Figure 8 shows an application diagram for SGM851CG. Please connect TS to VCC or ground to obtain different PB time delays. Table 3 lists the design requirements for Figure 8.

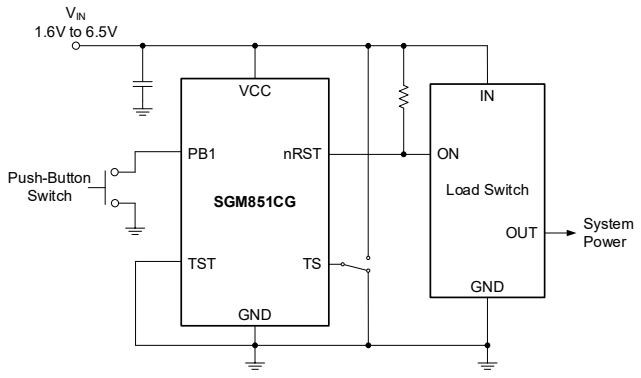


Figure 8. SGM851CG Application Diagram

Table 3. Design Requirements and Results

Design Requirements	Design Result
Single input	PB1
Do not react to input signal less than 5s	6s (MIN)
Reset pulse greater than 240ms	320ms (MIN)
I_{CC} < 5μA	3.3μA (MAX)

The nRST pin will rise up to the high level if the output pin turns into high-impedance status, where the rising time is related to the pull-up resistance and capacitance on that pin. How to choose the pull-up resistors needs to consider two aspects. The one is to meet the falling time demands while the other is to satisfy the sink current requirements to obtain a low enough V_{OL} for the application. For example, please choose resistors from 1kΩ to 1MΩ under low-capacitive load condition.

Dual Input Applications

It is suitable to choose SGM851A/BC/BG when two pins of input are needed to determine the reset pin status. To be more detailed, choose which device depends on its actual function for the system. Choose SGM851A if you need nRST to be always low unless one of the PBx pin becomes high. Besides, you may need to choose SGM851BC/BG if you want the nRST pin holds low for a constant period without the influence of the PBx pin.

Table 4 lists the design requirements for Figure 9. Please connect TS to VCC or ground to obtain different PB time delays. It can be used as a single channel if users short the PB pin to ground.

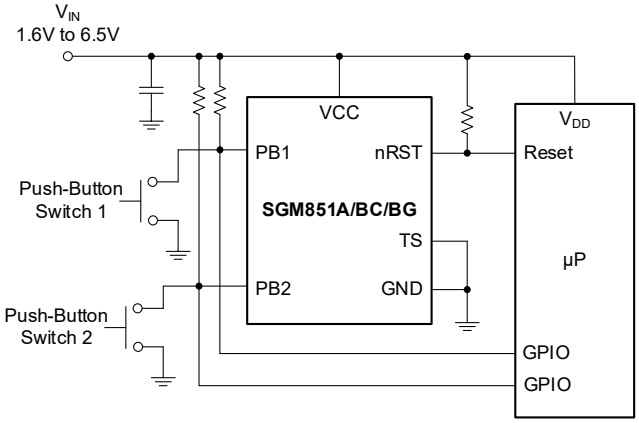


Figure 9. SGM851A/BC/BG Application Diagram

APPLICATION INFORMATION (Continued)

Table 4. Design Requirements and Results

Design Requirements	Design Result	
	SGM851A	SGM851BC/BG
Dual input	PB1 and PB2	PB1 and PB2
Do not react to input signal less than 5s	6s (MIN)	6s (MIN)
Reset pulse greater than 140ms	Depend on PBx timing	320ms (MIN)
Reset pulse ends after at least one input goes high	True	Do not depend on PBx timing

The nRST pin will rise up if the output pin turns into the high-impedance status, where the rising time is related to the pull-up resistance and capacitance on that pin. How to choose the pull-up resistors needs to consider two aspects. The one is to meet the falling time demands while the other is to satisfy the sink current requirements to obtain a low enough V_{OL} for the application. For example, please choose resistors from 1kΩ to 1MΩ under low-capacitive load condition.

Latched Reset Signal

In some applications, the reset signal (nRST) should be latched and the status will not be altered until another low signal is detected. In order to achieve this goal, a D flip-flop is adopted and its output (Q) is used as the reset signal.

Figure 10 shows an example how to construct a latched reset signal. Table 5 summarizes the design requirements for Figure 10.

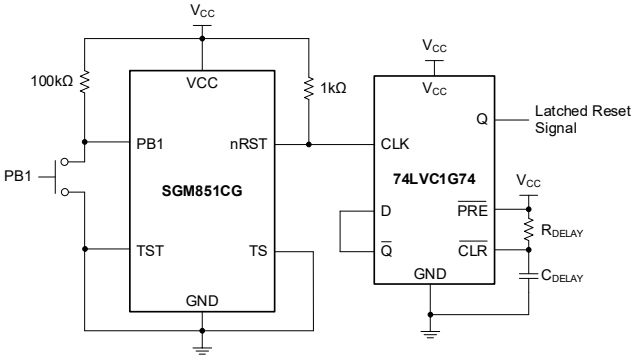


Figure 10. Latched Reset Schematic

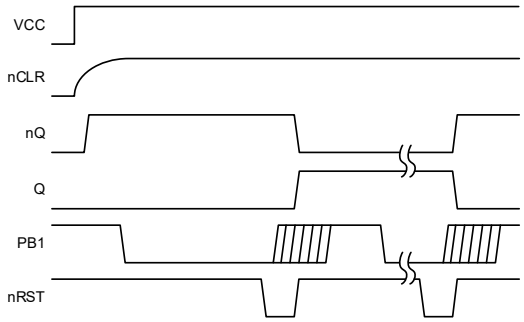


Figure 11. Timing Diagram

Table 5. Design Requirements and Results

Design Requirements	Design Result
Single input	PB1
Latched output	Q
Do not react to input signal less than 5s	6s (MIN)
Reset pulse greater than 200ms	320ms (MIN)
I_{CC} < 20μA	13.3μA (MAX)

Ensure the reset signal (nRST) has a fast slew rate to assert the flip-flop once a positive-edge triggered D flip-flop is taken. For the 74LVC1G74 in Figure 10, a resistor of 1kΩ is recommended. To initialize the D flip-flop to a known status, make sure that the RC time constant of the delay capacitor (C_{DELAY}) and delay resistor (R_{DELAY}) is 10 times of the rising time of the input voltage to VCC. As the consequence, a clear signal can be obtained and sent to the D flip-flop.

Power Supply Recommendations

A well-regulated power supply range from 1.6V to 6.5V is recommended as the input. Besides, a 0.1μF ceramic capacitor, though not mandatory, should be placed near the VCC pin as a good design practice.

Layout Guidelines

Some design guidelines are provided below for the SGM851 to lay out the printed circuit board (PCB).

1. Place the decoupling capacitor as close as possible to the VCC pin of the device.

2. Use short traces for the VCC node. An LC tank can be created by the VCC capacitor (C_{VDD}) and its parasitic inductance between the supply and the capacitor. As a result, ringing waveforms can be observed with peak voltage higher than the maximum value at VCC pin.

REVISION HISTORY

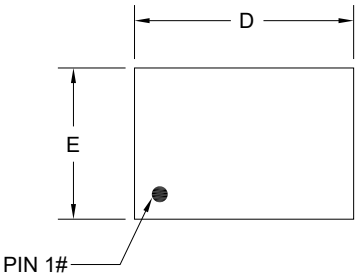
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2026 – REV.A to REV.A.1	Page
Updated Absolute Maximum Ratings section	2
Updated Electrical Characteristics section	4

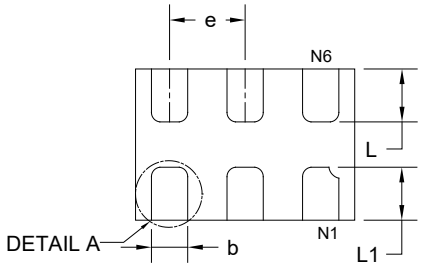
Changes from Original (MAY 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

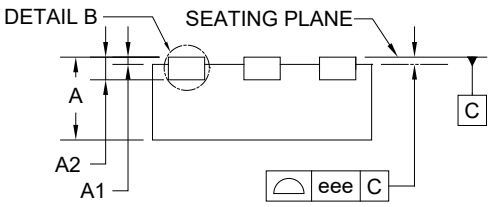
UTDFN-1.45×1-6AL



TOP VIEW



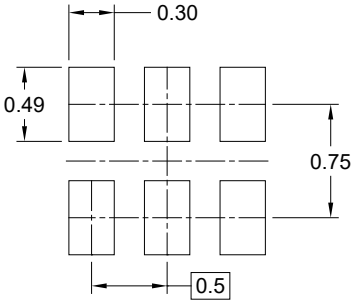
BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

DETAIL B
ALTERNATE CONSTRUCTION



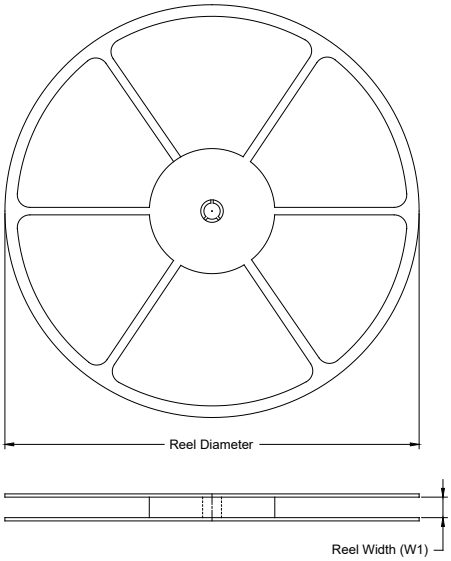
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.450	-	0.600
A1	-0.004	-	0.050
A2	0.150 REF		
b	0.150	-	0.300
D	1.374	-	1.526
E	0.924	-	1.076
e	0.500 BSC		
L	0.250	-	0.450
L1	0.250	-	0.500
L2	0.000	-	0.100
eee	0.050		

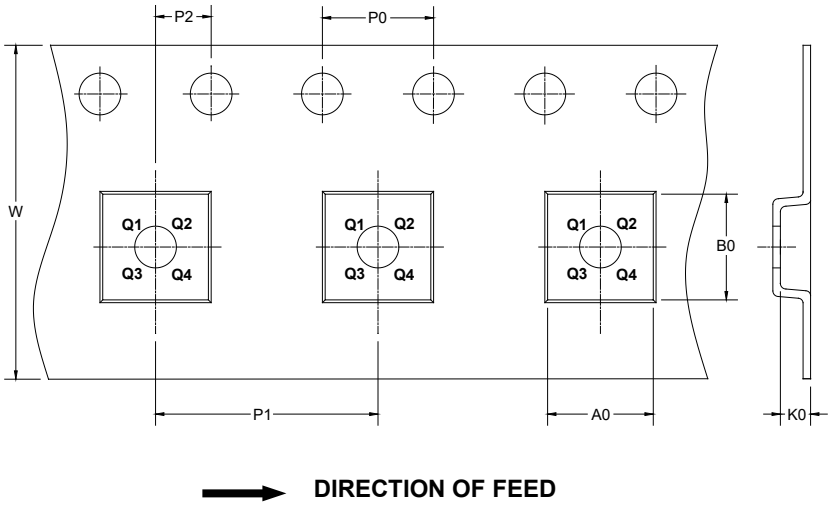
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



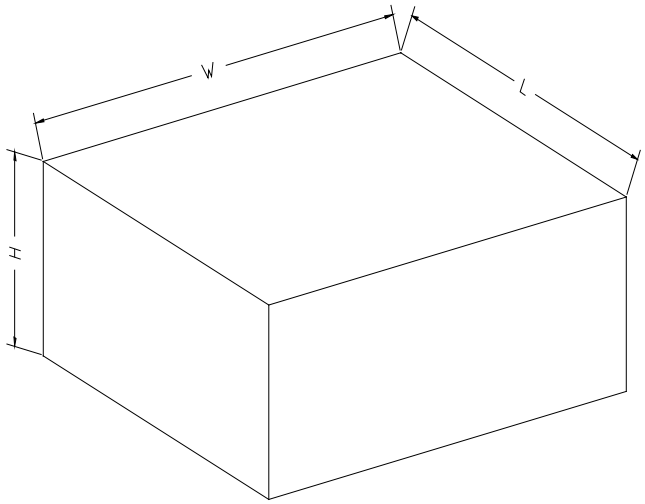
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.45×1-6AL	7"	9.5	1.15	1.60	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002