



SGM41608

I²C Controlled, Single-Cell 8A Switched Cap Parallel Battery Charger with Bypass Mode

GENERAL DESCRIPTION

The SGM41608 is an efficient 8A switched-capacitor battery charging device with I²C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.3V to 12V input voltage range (VBUS) from smart wall adapters or power banks. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

The SGM41608 is equipped with the capability to facilitate a 5A bypass mode charge, formerly known as battery switch charge, via its built-in MOSFETs. The R_{DS(ON)} value for the charging path in bypass mode is kept under 15mΩ to accommodate high current operations. This integrated bypass mode ensures that a 5V fast charging adapter can be used to charge a single-cell battery, thereby maintaining backward compatibility.

The SGM41608 is available in a Green WLCSP-2.38×2.38-35B package.

APPLICATIONS

Smartphone, Tablet

FEATURES

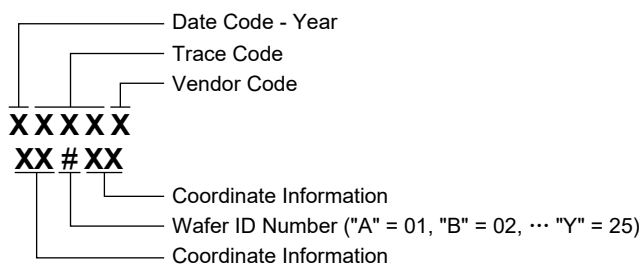
- Supports Reverse 1:2 Mode and Reverse 1:1 Mode
- Efficiency Optimized Switched-Capacitor Architecture
 - ◆ Up to 8A Output Current
 - ◆ 3.3V to 12V Input Voltage Range
 - ◆ 125kHz to 2MHz Switching Frequency Setting
 - ◆ Above 97.2% Voltage Divider Mode Efficiency (when V_{BAT} = 4.4V, I_{BAT} = 6A)
- Integrated Programmable Protection Features for Safe Operation
 - ◆ Input Over-Voltage Protection (VBUS_OVP)
 - ◆ Battery Over-Voltage Protection (VBAT_OVP)
 - ◆ Input Over-Current Protection (IBUS_OCP)
 - ◆ Battery Over-Current Protection (IBAT_OCP)
 - ◆ Input Under-Current Protection (IBUS_UCP)
 - ◆ Input Short-Circuit Protection (VBUS_SCP)
 - ◆ Output Over-Voltage Protection (VOUT_OVP)
 - ◆ Input Over-Voltage Protection (VAC_OVP)
 - ◆ Battery Temperature Monitoring (TSBAT_FLT)
 - ◆ Die Over-Temperature Protection (TDIE_OTP)
- Up to 13A Charging Current with Synchronized Dual SGM41608 for Parallel Charging
- 8-Channel 12-Bit (Effective) ADC Converter
 - ◆ VAC, VBUS, IBUS, VOUT, VBAT, IBAT, TSBAT, TDIE for Monitoring
- Available in a Green WLCSP-2.38×2.38-35B Package

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41608	WLCSP-2.38x2.38-35B	-40°C to +85°C	SGM41608YG/TR	SGM21E XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)	
VAC (Converter not Switching)	-0.3V to 35V
VBUS (Converter not Switching).....	-0.3V to 20V
PMID (Converter not Switching)	-0.3V to 20V
BST1-CFH1, BST2-CFH2.....	-0.3V to 6V
ACDRV to VBUS	-22V to 6V
PMID to VBUS	-0.3V to 6V
CFL1, CFL2	-0.3V to 6V
CFH1 to VOUT, CFH2 to VOUT.....	-0.3V to 6V
VOUT	-0.3V to 6V
BATP, REGN, nINT, SDA, SCL, SRN_SYNCIN, TSBAT_SYNCOUT	
BATN_SRP_ADDR.....	-0.3V to 6V
Package Thermal Resistance	
WLCSP-2.38x2.38-35B, θ_{JA}	38.9°C/W
WLCSP-2.38x2.38-35B, θ_{JB}	4.1°C/W
WLCSP-2.38x2.38-35B, θ_{JC}	12.2°C/W
Junction Temperature	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ⁽¹⁾⁽²⁾	
HBM.....	±4000V
CDM	±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage at VAC	12V (MAX)
Input Voltage at VBUS.....	12V (MAX)
Input Voltage at PMID	12V (MAX)
Voltage across Q _{CH1} , Q _{CH2}	
PMID-CFH1, PMID-CFH2	5V (MAX)
Voltage across Q _{DH1} , Q _{DH2}	
CFH1-VOUT, CFH2-VOUT.....	5V (MAX)
Voltage across Q _{CL1} , Q _{CL2}	
VOUT-CFL1, VOUT-CFL2.....	5V (MAX)
Voltage across Q _{DL1} , Q _{DL2}	
CFL1, CFL2.....	5V (MAX)
Charging Current, I _{CHG}	8A (MAX)
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

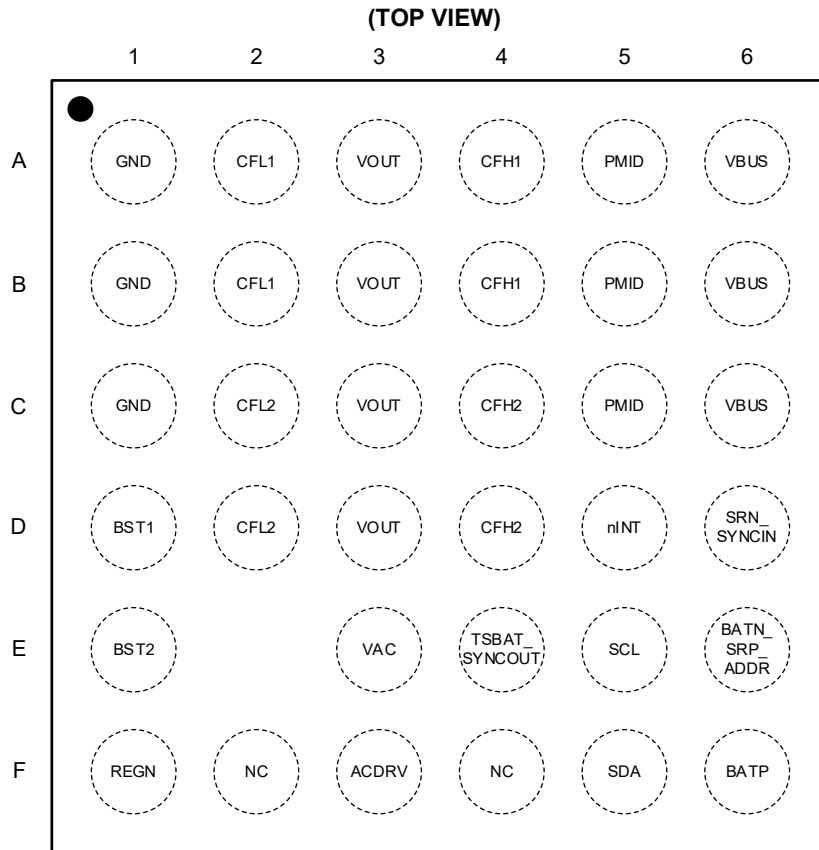
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



WLCSP-2.38x2.38-35B

PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
A1, B1, C1	GND	P	Power Ground Pins.
A2, B2	CFL1	P	Channel-1 Flying Capacitor Negative Pins. Connect 1~3 22μF parallel capacitors between CFH1 and CFL1 as close as possible to the device.
A3, B3, C3, D3	VOUT	P	Device Output Pins. Connect it to the battery pack positive terminal. A 22μF capacitor between VOUT and GND pins is recommended.
A4, B4	CFH1	P	Channel-1 Flying Capacitor Positive Pins. Connect 1~3 22μF parallel capacitors between CFH1 and CFL1 as close as possible to the device.
A5, B5, C5	PMID	P	Power Stage Supply Input Pins. Bypass them with at least a 10μF ceramic capacitor to GND.
A6, B6, C6	VBUS	P	Device Power Input Pins. Use a 1μF or larger ceramic capacitor between VBUS and GND pins close to the device.
C2, D2	CFL2	P	Channel-2 Flying Capacitor Negative Pins. Connect 1~3 22μF parallel capacitors between CFH2 and CFL2 as close as possible to the device.
C4, D4	CFH2	P	Channel-2 Flying Capacitor Positive Pins. Connect 1~3 22μF parallel capacitors between CFH2 and CFL2 as close as possible to the device.
D1	BST1	O	Bootstrap Capacitor for Channel1. Connect a 100nF ceramic capacitor from BST1 to CFH1.
D5	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. It is normally high but generates a low 256μs pulse when a charge status or fault occurs to inform the host.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
D6	SRN_SYNCIN	AI	Battery Current Sensing Negative Input and SYNCIN for Secondary Configuration. Place a 2mΩ or 5mΩ (R _{SNS}) shunt resistor between SRP and SRN_SYNCIN pins. Short SRP and SRN_SYNCIN together to GND if not used. If configured as a secondary IC for parallel charging, this pin functions as SYNCIN, and connect it to TSBAT_SYNCOUT of the primary IC.
E1	BST2	O	Bootstrap Capacitor for Channel2. Connect a 100nF ceramic capacitor from BST2 to CFH2.
E3	VAC	AI	VAC Voltage Sense Input Pin. Connect it to VBUS if ACFET and RBFET are not used.
E4	TSBAT_SYNCOUT	AI	Battery Temperature Sense Input and SYNCOUT for Primary Configuration. See the TSBAT section for choosing the resistor divider values. If configured as a primary IC for parallel charging, this pin functions as SYNCOUT, and is connected to SRN_SYNCIN of the secondary IC.
E5	SCL	DI	I ² C Interface Clock Input Line. The device I ² C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
E6	BATN_SRP_ADDR	AI	Battery Voltage Sensing Negative Input or Battery Current Sensing Positive Input. Connect a 100Ω resistor between this pin and negative terminal of the battery pack. Place a 2mΩ or 5mΩ (R _{SNS}) shunt resistor between this pin and SRN_SYNCIN pin. This pin can be used to set the I ² C address.
F1	REGN	AO	Internal 5V LDO Output. Connect a 4.7μF MLCC capacitor between this pin and GND. Do not use this pin for any other function.
F2, F4	NC	—	No Connection.
F3	ACDRV	P	External Dual N-MOSFET Gate Control Pin. Connect it to the gate of the external back-to-back N-MOSFET in the charging path, or connect it to ground if the back-to-back N-MOSFET is not used.
F5	SDA	DIO	I ² C Interface Data Line. The SDA line is forced to release when the 25ms I ² C timeout fault occurs.
F6	BATP	AI	Battery Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP and positive terminal of the battery pack.

NOTE:

1. P = Power, AIO = Analog Input/Output, AI = Analog Input, DO = Digital Output, AO = Analog Output, DIO = Digital Input/Output.

ELECTRICAL CHARACTERISTICS(T_J = -40°C to +85°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
Battery Only Quiescent Current	I _{Q_BAT}	ADC disabled, charge disabled, VBUS, VAC not present, V _{BAT} = 4V		4	8	μA
		ADC enabled, charge disabled, VBUS, VAC not present, V _{BAT} = 4V		1300	2100	
VAC Quiescent Current	I _{Q_VAC}	ADC disabled, charge disabled, ACDRV disabled, HIZ_EN = 1, V _{VAC} = 8V		31		μA
		ADC disabled, charge disabled, ACDRV disabled, V _{VAC} = 8V		880		
		ADC disabled, charge disabled, ACDRV enabled, V _{VAC} = 8V		1030		
VAC UVLO Rising Threshold	V _{AC_UVLO_R}	V _{VAC} rising, for active I ² C		2.9	3.3	V
VAC UVLO Falling Threshold	V _{AC_UVLO_F}	V _{VAC} falling		2.7		V
VAC UVLO Hysteresis	V _{AC_UVLO_HYS}			200		mV
VBUS UVLO Rising Threshold	V _{BUS_UVLO_R}	V _{VBUS} rising, for active I ² C		2.9	3.3	V
VBUS UVLO Falling Threshold	V _{BUS_UVLO_F}	V _{VBUS} falling		2.7		V
VBUS UVLO Hysteresis	V _{BUS_UVLO_HYS}			200		mV
VBUS Present Rising Threshold	V _{BUS_PRESENT_R}	V _{VBUS} rising to allow user set CHG_EN = 1		2.9	3.3	V
VBUS Present Falling Threshold	V _{BUS_PRESENT_F}	V _{VBUS} falling		2.8		V
VBUS Present Hysteresis	V _{BUS_PRESENT_HYS}			100		mV
VOOUT UVLO Rising Threshold	V _{OUT_UVLO_R}	V _{VOOUT} rising, for active I ² C		2.5	2.9	V
VOOUT UVLO Falling Threshold	V _{OUT_UVLO_F}	V _{VOOUT} falling		2.3		V
VOOUT UVLO Hysteresis	V _{OUT_UVLO_HYS}			200		mV
VOOUT Present Rising Threshold	V _{OUT_PRESENT_R}	V _{VOOUT} rising to allow forward mode		2.6	3	V
	V _{OUT_PRESENT_R1}	V _{VOOUT} rising to allow reverse mode		2.9	3.3	V
VOOUT Present Falling Threshold	V _{OUT_PRESENT_F}	V _{VOOUT} falling (forward mode)		2.5		V
	V _{OUT_PRESENT_F1}	V _{VOOUT} falling (reverse mode)		2.8		V
VOOUT Present Hysteresis	V _{OUT_PRESENT_HYS}			100		mV
External OVP Control						
VAC Present Rising Threshold	V _{AC_PRESENT_R}	V _{VAC} rising to turn on ACFET- RBFET		2.9	3.3	V
VAC Present Falling Threshold	V _{AC_PRESENT_F}	V _{VAC} falling		2.8		V
VAC Present Hysteresis	V _{AC_PRESENT_HYS}			100		mV
VAC Present Rising Threshold Deglitch Time	t _{VAC_IN_DEG}	Deglitch between V _{VAC} rising above V _{AC_PRESENT_R} and starting external OVPFET turn-on		6		ms
VAC OVP Rising Threshold Range	V _{AC_OVP_R}	V _{VAC} rising	6.5		18	V
VAC OVP Threshold Accuracy	V _{AC_OVPR_ACC}	V _{AC_OVP_R} = 12V	-3		3	%
VAC Over-Voltage Hysteresis	V _{AC_OVP_HYS}	Falling hysteresis		2		%
VAC OVP Rising Deglitch Time	t _{VAC_OVPR_DEG}	Deglitch between V _{VAC} rising above V _{AC_OVP_R} and triggering the protection action		100		ns
VAC OVP Resume Time	t _{VAC_OVP_RSM}			100		μs

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40°C to +85°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
VAC Pull-Down Current	I _{PDN_VAC}	VAC_PD_EN = 1		35		mA	
VBUS Pull-Down Current	I _{PDN_VBUS}	VBUS_PD_EN = 1		20		mA	
REGN LDO							
REGN LDO Output Voltage	V _{REGN}	V _{VBUS} = 8V, I _{REGN} = 20mA		5		V	
REGN LDO Current Limit	I _{REGN}	V _{VBUS} = 8V, V _{REGN} = 4.5V	20			mA	
Switched Cap Chargers							
VBUS to VOUT Resistance	R _{DROPOUT}	Bypass mode		15		mΩ	
R _{DSON} of Reverse Blocking FET	R _{DS_QRB}	V _{VOUT} = 8V		6.5		mΩ	
R _{DSON} of Q _{CH1}	R _{DS_QCH1}	V _{PMID} = 8V		12		mΩ	
R _{DSON} of Q _{DH1}	R _{DS_QDH1}	V _{VOUT} = 4V		10		mΩ	
R _{DSON} of Q _{CL1}	R _{DS_QCL1}	V _{VOUT} = 4V		10		mΩ	
R _{DSON} of Q _{DL1}	R _{DS_QDL1}	V _{VOUT} = 4V		10		mΩ	
R _{DSON} of Q _{CH2}	R _{DS_QCH2}	V _{PMID} = 8V		12		mΩ	
R _{DSON} of Q _{DH2}	R _{DS_QDH2}	V _{VOUT} = 4V		10		mΩ	
R _{DSON} of Q _{CL2}	R _{DS_QCL2}	V _{VOUT} = 4V		10		mΩ	
R _{DSON} of Q _{DL2}	R _{DS_QDL2}	V _{VOUT} = 4V		10		mΩ	
PMID Pull-Down Current	I _{PDN_P MID}	PMID_PD_EN = 1		45		mA	
Protection							
nINT Low Pulse Duration when a Protection Occurs	t _{INT}			256		μs	
VBUS OVP Rising Threshold Range	V _{BUS_OVP_R}	Voltage divider mode	I ² C programmable, 500mV per step, 10.5V by default		10.5	14	V
		Bypass mode	I ² C programmable, 250mV per step, 5.25V by default		5.25	7	
VBUS OVP Accuracy	V _{BUS_OVPR_ACC}	V _{BUS_OVP_R} = 5.5V		-2.3	2.3	%	
		V _{BUS_OVP_R} = 11V		-2.5	2.5		
VBUS OVP Rising Deglitch Time	t _{VBUS_OVPR_DEG}	Deglitch between V _{VBUS} rising above V _{BUS_OVP_R} and triggering protection action, 1μs by default		1		μs	
				10		μs	
IBUS OCP Threshold Range	I _{BUS_OCP}	I ² C programmable, 50mA per step, 3.5A by default		1	6.35	A	
IBUS OCP Threshold Accuracy	I _{BUS_OCP_ACC}	I _{BUS_OCP} = 3A		-5	5	%	
IBUS OCP Deglitch Time	t _{IBUS_OCP_DEG}	Deglitch between I _{BUS} rising above I _{BUS_OCP} and trigger protection action, 320μs by default		80		μs	
				320		μs	
				640		μs	
				5		ms	
IBUS UCP Threshold	I _{BUS_UCP}	I _{BUS_UCP_R} = 300mA, BUSUCP = 1			300	mA	
		I _{BUS_UCP_R} = 500mA, BUSUCP = 0			500		
		I _{BUS_UCP_F} = 150mA, BUSUCP = 1			150		
		I _{BUS_UCP_F} = 250mA, BUSUCP = 0			250		

ELECTRICAL CHARACTERISTICS (continued)(T_J = -40°C to +85°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
IBUS UCP Deglitch Time	t _{IBUS_UCP_DEG}	Deglitch between I _{BUS} falling below I _{BUS_UCP} and trigger protection action. I ² C programmable, 5ms by default.		10		μs	
				5		ms	
				50		ms	
				150		ms	
IBUS OCP RVS Threshold Range	I _{BUS_OCP_RVS}	I ² C programmable, 50mA per step, 3.5A by default	1		6.35	A	
IBUS OCP RVS Threshold Accuracy	I _{BUS_OCP_RVS_ACC}	I _{BUS_OCP_RVS} = 3A, initial accuracy, T _J = +25°C	-5		5	%	
VBUS Short-Circuit Threshold	V _{BUS_SCP}	During BUS_INSERT interval or during OVPFET turn-on interval		2		V	
VOUT OVP Rising Threshold Range	V _{OUT_OVP_R}	I ² C programmable, 100mV per step, 5V by default	4.7		5	V	
VOUT OVP Threshold Accuracy	V _{OUT_OVP_ACC}	V _{OUT_OVP_R} = 5V	-1		1	%	
VOUT OVP Rising Deglitch Time	t _{VOUT_OVP_DEG}	Deglitch between V _{VOUT} rising above V _{OUT_OVP_R} and triggering protection action, 10μs by default		10		μs	
				5		ms	
VBAT OVP Rising Threshold Range	V _{BAT_OVP_R}	I ² C programmable, 10mV per step, 4.74V by default	4.04		5.11	V	
VBAT OVP Threshold Accuracy	V _{BAT_OVP_ACC}	V _{BAT_OVP_R} = 4.4V	-1		1	%	
VBAT OVP Deglitch Time	t _{VBAT_OVP_DEG}	Deglitch between V _{BAT} rising above V _{BAT_OVP} and triggering protection action, 1.28ms by default		8		μs	
				640		μs	
				1.28		ms	
				5		ms	
IBAT OCP Threshold Range	I _{BAT_OCP}	I ² C programmable, 100mA per step, 8.1A by default	0.5		12.7	A	
IBAT OCP Threshold Accuracy	I _{BAT_OCP_ACC}	I _{BAT_OCP} = 2A, R _{SNS} = 2mΩ, initial accuracy, T _J = +25°C		-4		4	%
				-1.2		1.2	
IBAT OCP Deglitch Time	t _{IBAT_OCP_DEG}	Deglitch between I _{BAT} rising above I _{BAT_OCP} and triggering protection action, 320μs by default		80		μs	
				320		μs	
				640		μs	
				5		ms	
PMID2VOUT_OVP Range	V _{PMID2VOUT_OVP}	Rising threshold over V _{PMID} /2 - V _{VOUT} (2:1 charger mode) or over V _{PMID} - V _{VOUT} (1:1 charger mode)	400	500	1100	mV	
PMID2VOUT_UVP Range	V _{PMID2VOUT_UVP}	Falling threshold Over V _{PMID} /2 - V _{VOUT} (2:1 charger mode) or over V _{PMID} - V _{VOUT} (1:1 charger mode)	-450	-150	-100	mV	
PMID2VOUT_OVP Deglitch Time	t _{PMID2VOUT_OVP_DEG}	In charging mode, I ² C programmable, 100ns by default		100		ns	
				1		μs	
PMID2VOUT_UVP Deglitch Time	t _{PMID2VOUT_UVP_DEG}	In charging mode, I ² C programmable, 100ns by default		100		ns	
				1		μs	
V _{ACDRV} - V _{BUS} Voltage	V _{ACDRV}	V _{VBUS} = 5V		4.8		V	

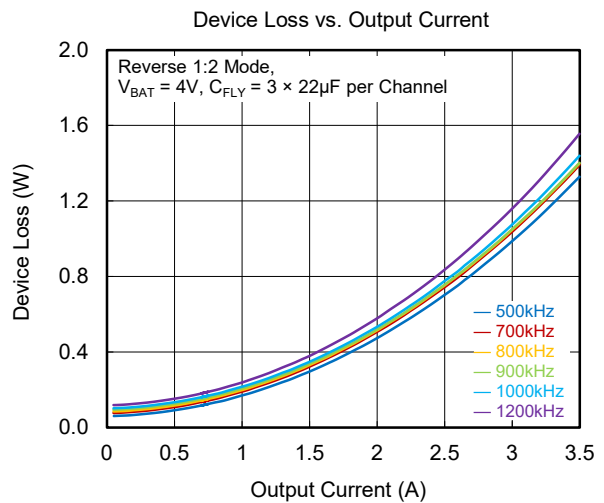
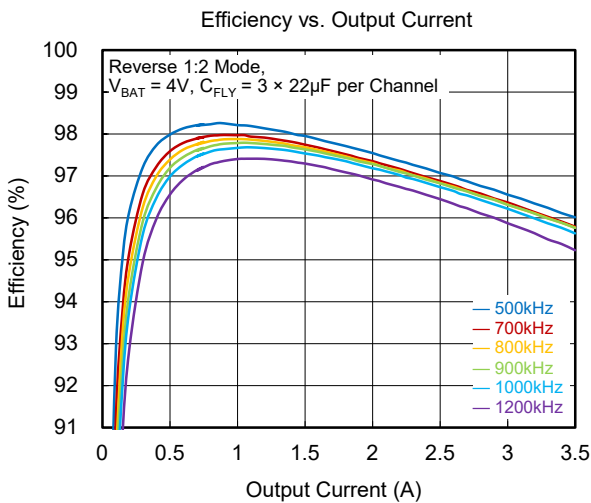
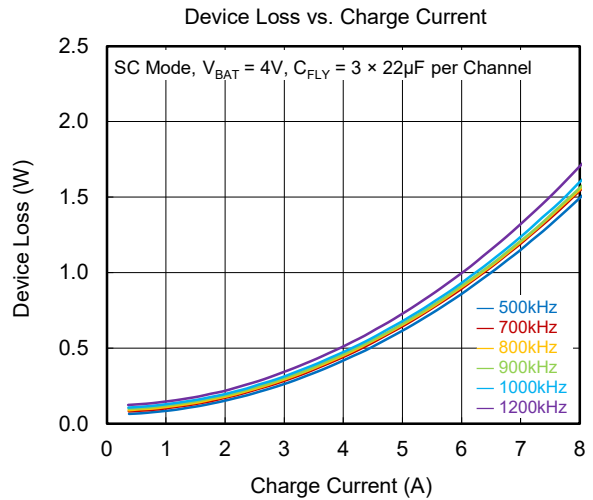
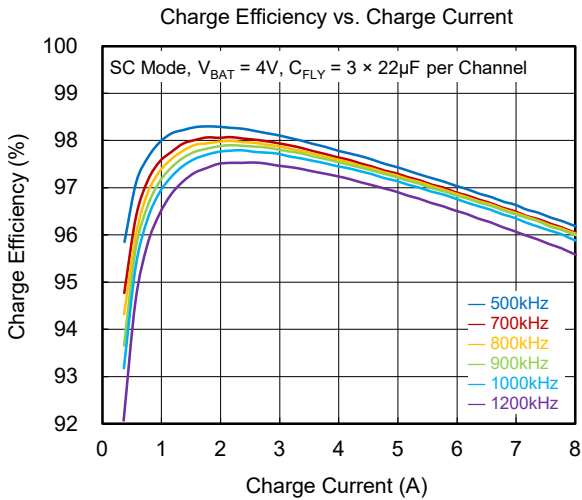
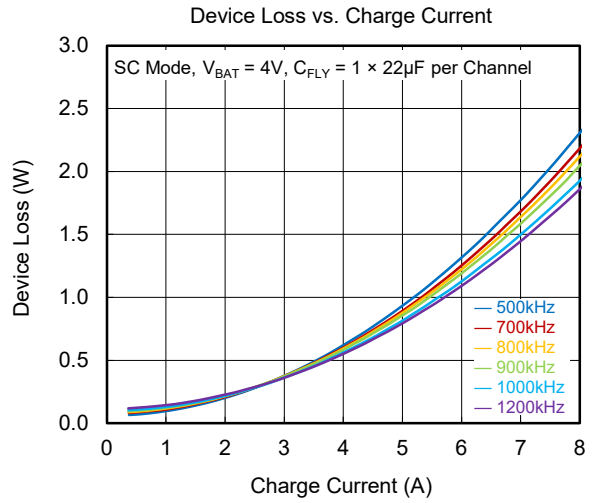
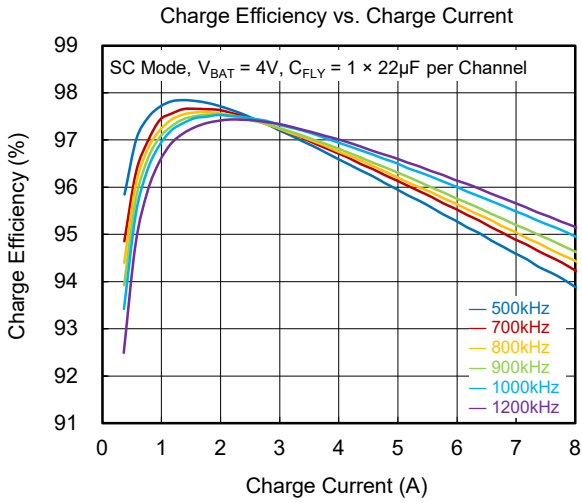
ELECTRICAL CHARACTERISTICS (continued)(T_J = -40°C to +85°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
VBUS High Threshold	V _{BUS_ERRHI_FALLING}	V _{BUS} /(2 × V _{VOU} T) in voltage divider mode, V _{BUS} /V _{VOU} T in bypass mode		1.175		V/V	
	V _{BUS_ERRHI_RISING}			1.2		V/V	
VBUS Low Threshold	V _{BUS_ERRLO_FALLING}				1		V/V
	V _{BUS_ERRLO_RISING}				1.0125		V/V
TSBAT Fault Threshold Range	TS _{BAT_FLT_RANGE}	I ² C programmable, 25mV per step, 0.6V by default	0		1.575	V	
TSBAT Fault Accuracy	TS _{BAT_FLT_ACC}		-3.5		3.5	%	
TDIE OTP Rising Threshold	T _{DIE_OTP_R}			140		°C	
ADC Specification							
ADC Conversion Time for Each Channel	t _{ADC_CONV}			3		ms	
ADC Resolution	ADC _{RES}			12		bit	
ADC IBUS Current Readable in REG0x1F and REG0x20	I _{BUS_ADC}	Effective Range	0		10.24	A	
		LSB		2.5		mA	
IBUS_ADC Accuracy	I _{BUS_ADC_ACC}	I _{BUS} = 2A, initial accuracy, T _J = +25°C	-3		3	%	
		I _{BUS} = 3A, initial accuracy, T _J = +25°C	-3		3	%	
ADC VBUS Voltage Readable in REG0x21 and REG0x22	V _{BUS_ADC}	Effective Range	0		14	V	
		LSB		3.75		mV	
VBUS_ADC Accuracy	V _{BUS_ADC_ACC}	V _{VBUS} = 4V, initial accuracy, T _J = +25°C	-1		1	%	
		V _{VBUS} = 8V, initial accuracy, T _J = +25°C	-1		1	%	
ADC VAC Voltage Readable in REG0x23 and REG0x24	V _{VAC_ADC}	Effective Range	0		14	V	
		LSB		5		mV	
VAC_ADC Accuracy	V _{VAC_ADC_ACC}	V _{VAC} = 4V, initial accuracy, T _J = +25°C	-1		1	%	
		V _{VAC} = 8V, initial accuracy, T _J = +25°C	-1		1	%	
ADC VOUT Voltage Readable in REG0x25 and REG0x26	V _{OUT_ADC}	Effective Range	0		5.12	V	
		LSB		1.25		mV	
VOUT_ADC Accuracy	V _{OUT_ADC_ACC}	V _{VOUT} = 4V, initial accuracy, T _J = +25°C	-0.3		0.3	%	
		V _{VOUT} = 4.4V, initial accuracy, T _J = +25°C	-0.3		0.3	%	
ADC VBAT Voltage Readable in REG0x27 and REG0x28	V _{BAT_ADC}	Effective Range	0		5.12	V	
		LSB		1.25		mV	
VBAT_ADC Accuracy	V _{BAT_ADC_ACC}	V _{BAT} = 4V, initial accuracy, T _J = +25°C	-0.3		0.3	%	
		V _{BAT} = 4.4V, initial accuracy, T _J = +25°C	-0.3		0.3	%	
ADC IBAT Current Readable in REG0x29 and REG0x2A	I _{BAT_ADC}	Effective Range	0		12.8	A	
		LSB		3.125		mA	
IBAT_ADC Accuracy	I _{BAT_ADC_ACC}	I _{BAT} = 2A, R _{SNS} = 2mΩ	-3.2		3.2	%	
		I _{BAT} = 8A, R _{SNS} = 2mΩ	-1.2		1.2	%	
ADC TSBAT Pin Percentage Readable in REG0x2B and REG0x2C	TS _{BAT_ADC}	Effective Range	0		1.8	V	
		LSB		0.44		mV	
TSBAT_ADC Accuracy	TS _{BAT_ADC_ACC}	TSBAT pin Voltage 1V	-2.4		2.4	%	
ADC DIE Temperature Readable in REG0x2D and REG0x2E		Effective Range	0		150	°C	
		LSB		0.5		°C	

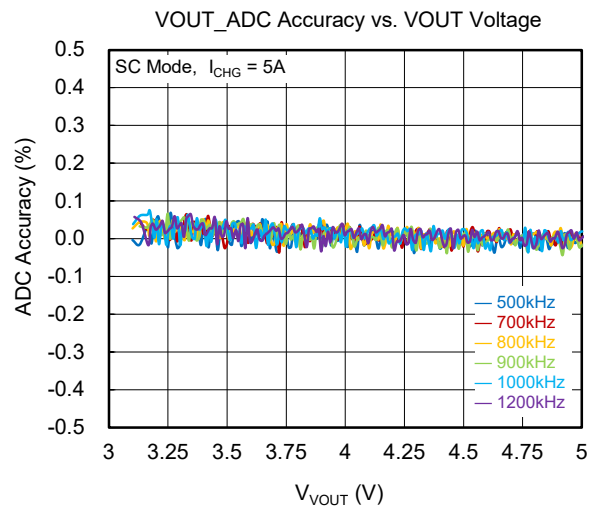
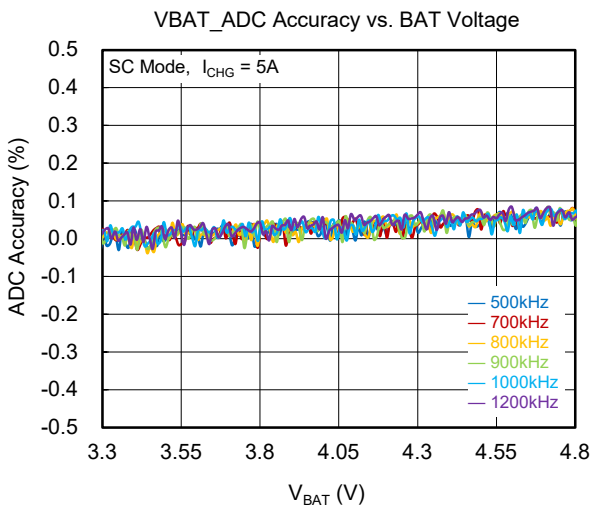
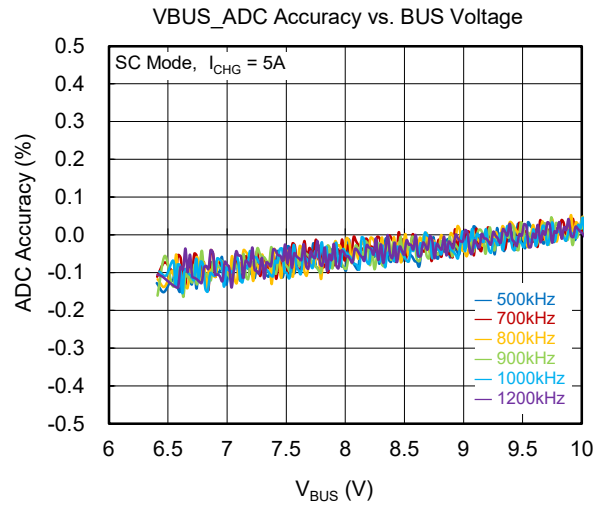
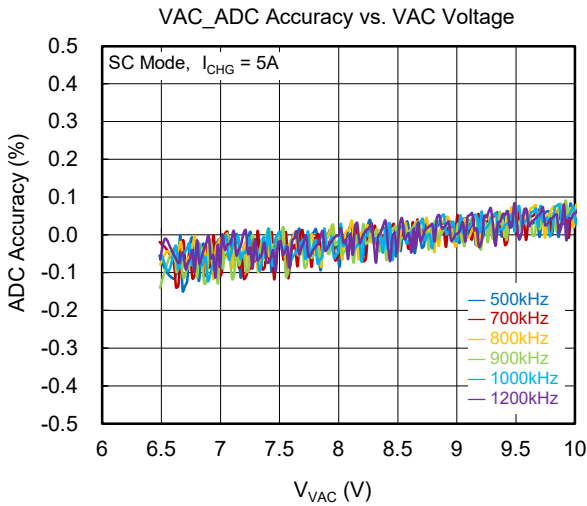
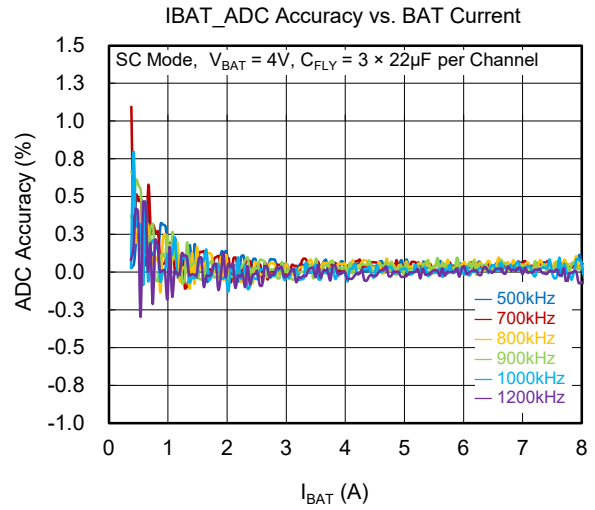
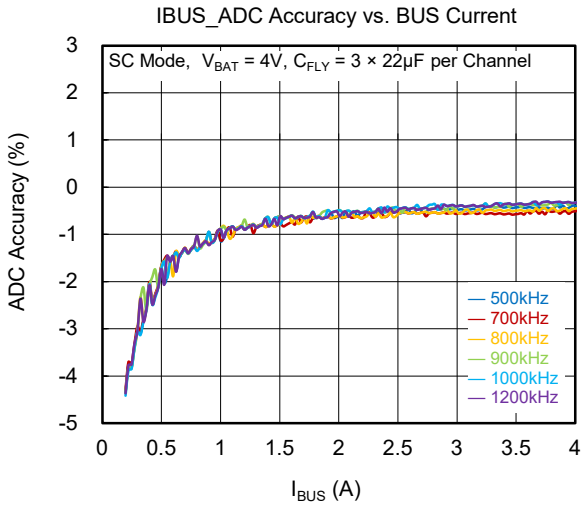
ELECTRICAL CHARACTERISTICS (continued)(T_J = -40°C to +85°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Interface (SCL and SDA Pins)						
High-Level Input Voltage	V _{IH_I2C}	SCL and SDA pins	0.825			V
Low-Level Input Voltage	V _{IL_I2C}	SCL and SDA pins			0.4	V
Low-Level Output Voltage	V _{OL_SDA}	Sink 5mA, SDA pin			0.4	V
High-Level Leakage Current	I _{LKG_I2C}	Connected to 1.2V			1	μA
SCL Clock Frequency	f _{CLK}				1000	kHz
Logic Output Pin (nINT, TSBAT_SYNCOUT)						
Low Level Output Voltage, nINT Pin	V _{OL_INT}	Sink 5mA			0.4	V
High-Level Leakage Current, nINT Pin	I _{LKG_nINT}	Connected to 1.2V			1	μA
Low Level Output Voltage, TSBAT_SYNCOUT Pin	V _{OL_TSBAT_SYNCOUT}	Sink 5mA			0.4	V
High-Level Leakage Current, TSBAT_SYNCOUT Pin	I _{LKG_TSBAT_SYNCOUT}	Connected to 1.2V			1	μA
Logic Input Pin (SRN_SYNCIN)						
High Level Input Voltage, SRN_SYNCIN Pin	V _{IH_SRN_SYNCIN}		0.825			V
Low Level Input Voltage, SRN_SYNCIN Pin	V _{IL_SRN_SYNCIN}				0.4	V
High-Level Leakage Current, SRN_SYNCIN Pin	I _{LKG_SRN_SYNCIN}	Connected to 1.8V			1	μA

TYPICAL PERFORMANCE CHARACTERISTICS

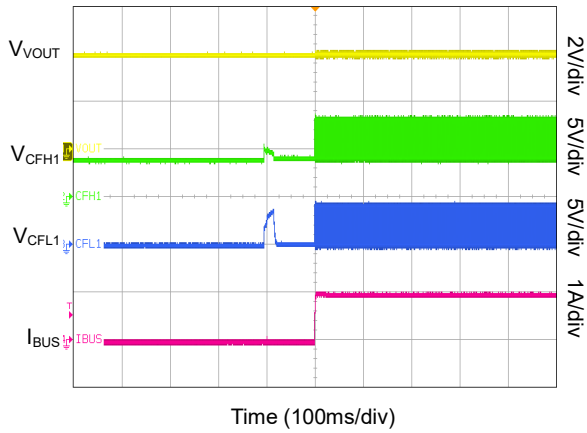


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

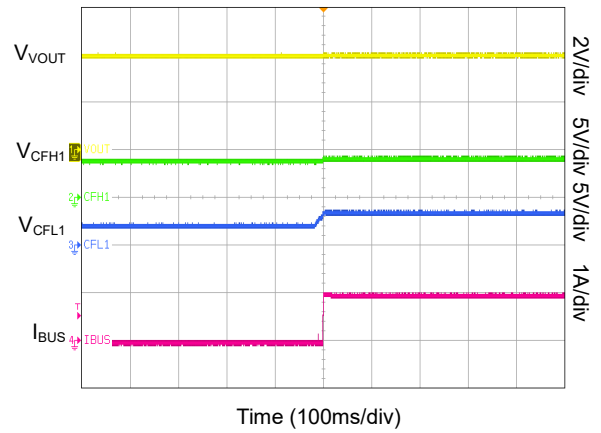


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

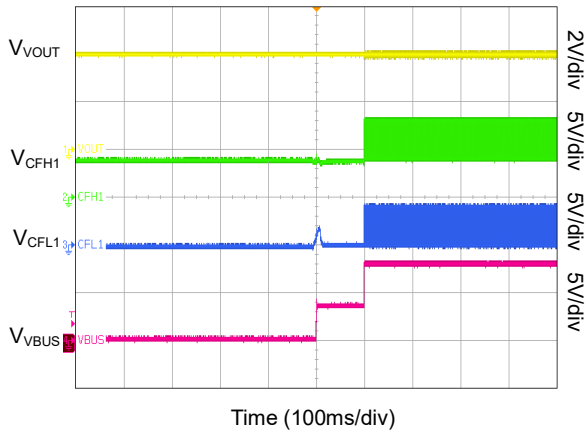
Switched Cap Forward Mode Power Up



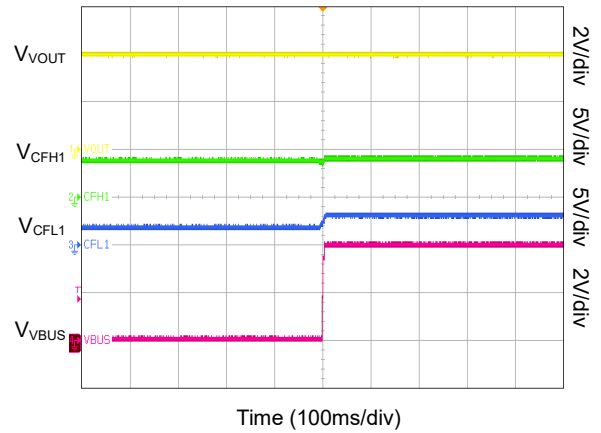
Bypass Forward Mode Power Up



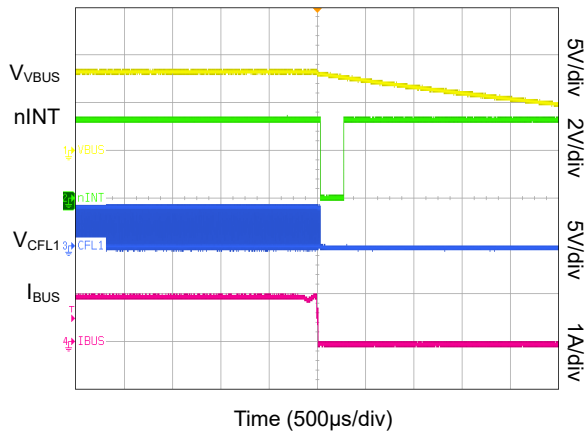
Switched Cap Reverse Mode Power Up



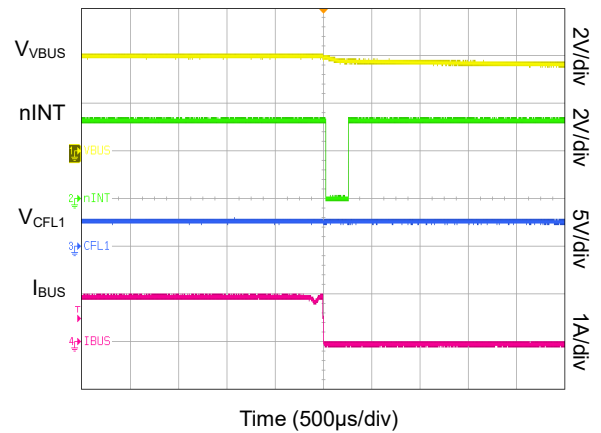
Bypass Reverse Mode Power Up



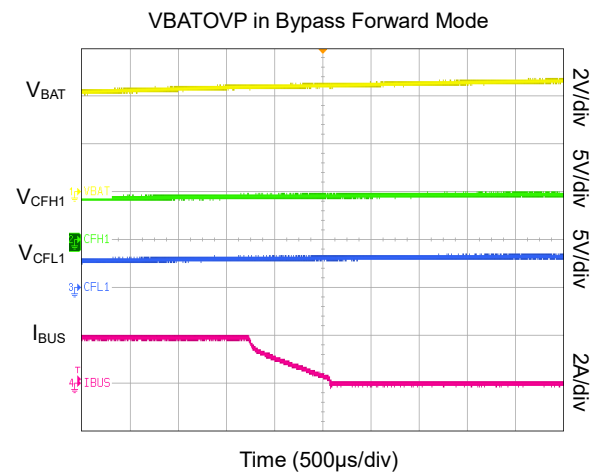
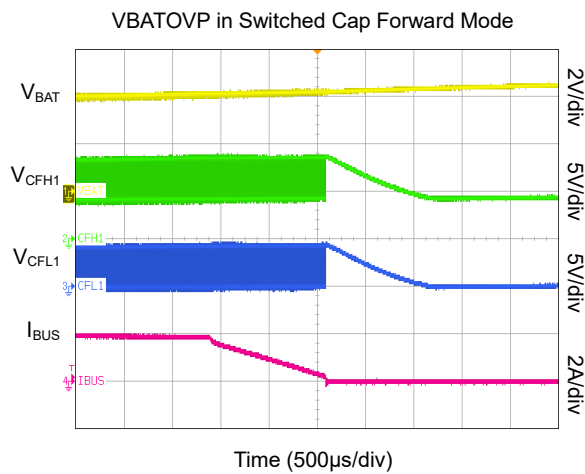
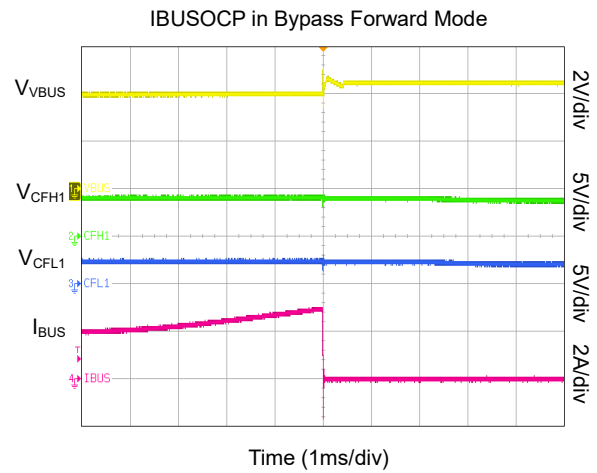
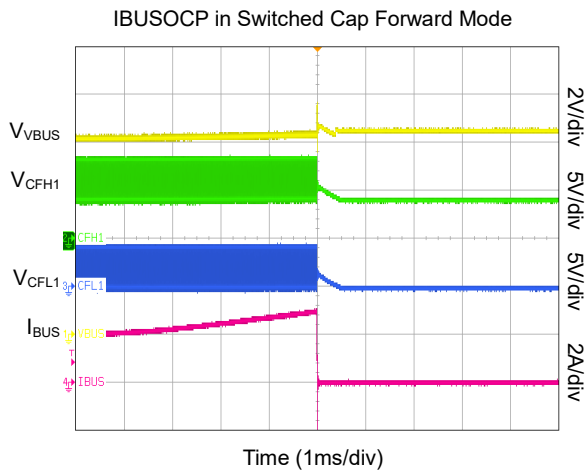
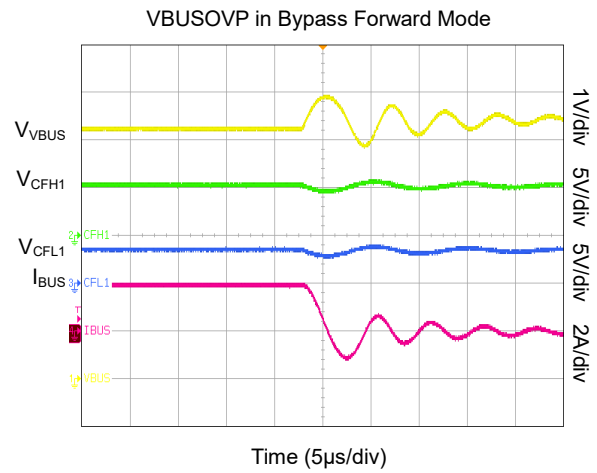
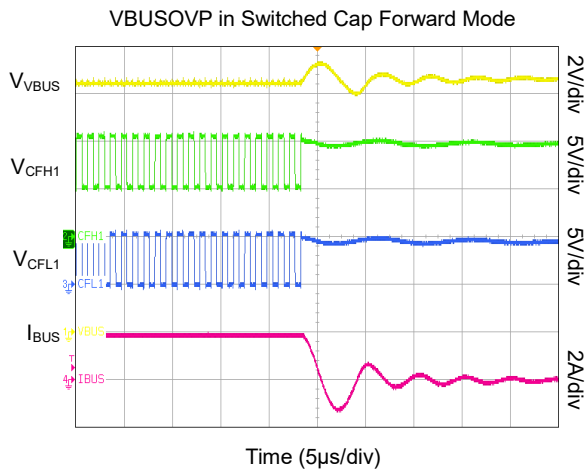
Adapter Unplug in Switched Cap Forward Mode



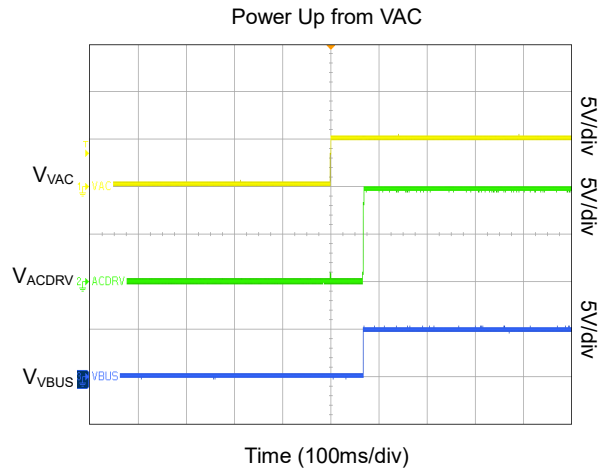
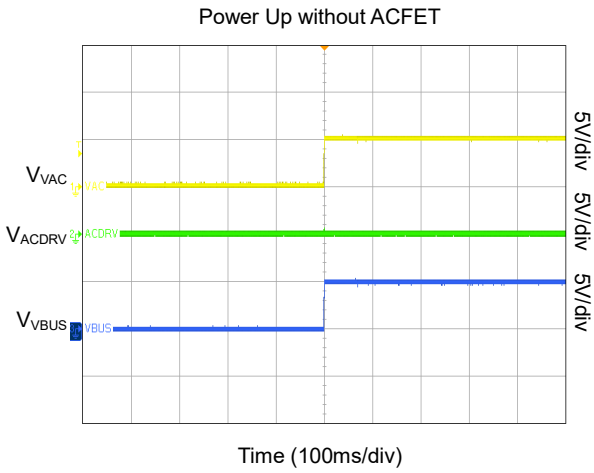
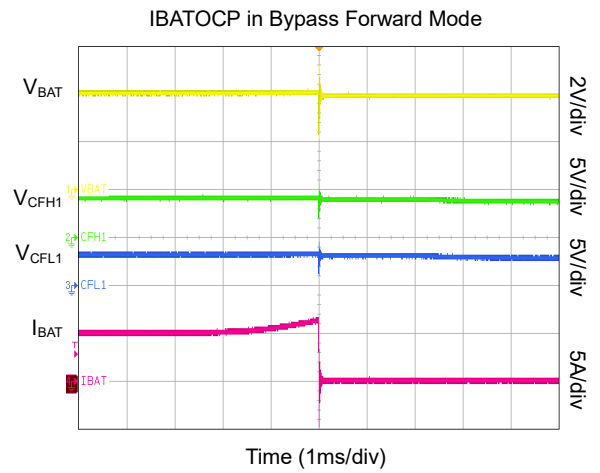
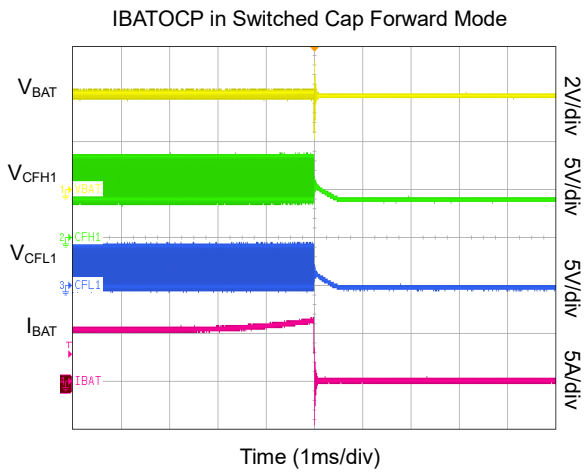
Adapter Unplug in Bypass Forward Mode



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TYPICAL APPLICATION CIRCUIT

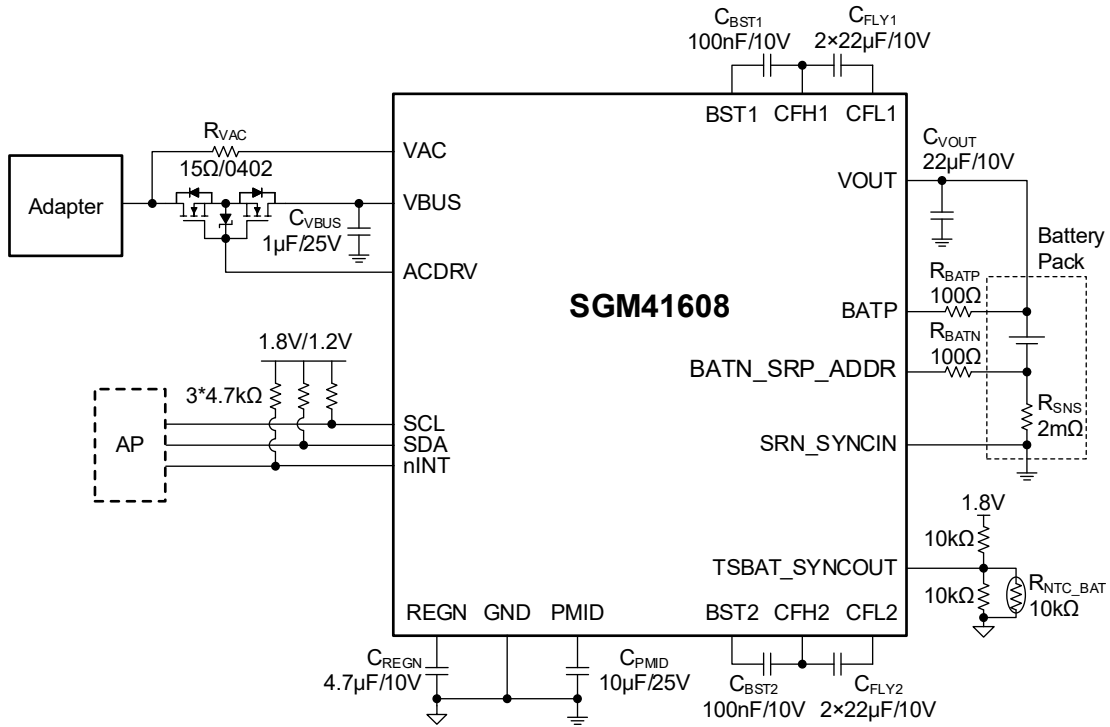


Figure 1. Single SGM41608 Typical Application Circuit

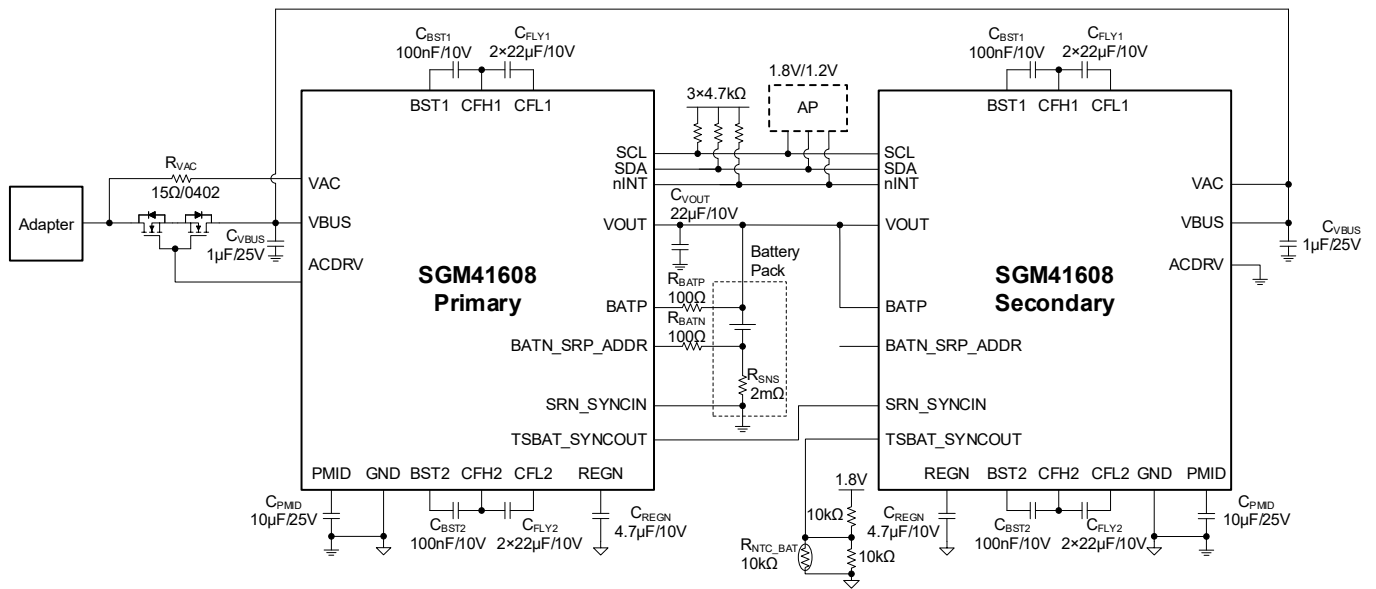


Figure 2. Dual SGM41608 Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

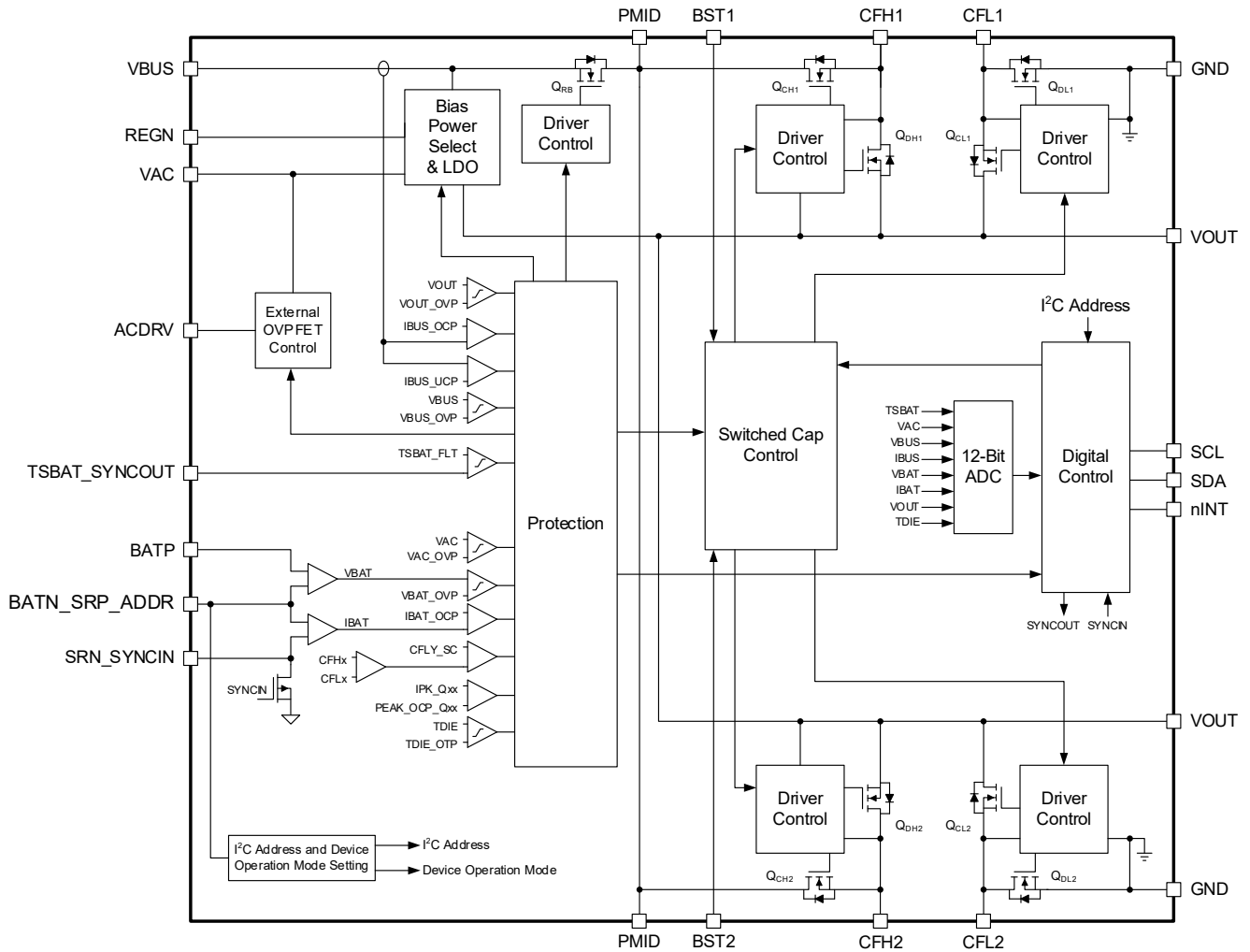


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

The SGM41608 is an efficient 8A switched-capacitor battery charging device with I²C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge 1-cell Li-Ion or Li-polymer battery in a wide 3.3V to 12V input voltage range (VBUS) from smart wall adapter. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. It also allows single input with no external OVPFET or single OVPFET. Moreover, it supports two devices in parallel for higher power systems.

A high speed 12-Bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, battery temperature, and die temperature information for the charge management host via I²C serial interface.

Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. Taking one of the two channels in the switched-capacitor as an example, the basic principle of operation is shown in Figure 4. In period 1, Q1 and Q3 are tuned on and V_{PMID} charges the C_{FLY} and the battery (in series) such that:

$$V_{CFLY} = V_{PMID} - V_{BAT} \tag{1}$$

In period 2, Q2 and Q4 are turned on and C_{FLY} appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \tag{2}$$

Ignoring the small fluctuation of the capacitor and battery voltages in period 1 and 2 in steady state operation, Equation 1 and 2 can be combined to calculate capacitor voltage:

$$V_{CFLY} = V_{BAT} = V_{PMID}/2 \tag{3}$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID} \times I_{BUS} = V_{BAT} \times I_{BAT} \tag{4}$$

or

$$I_{BUS} = I_{BAT}/2 \tag{5}$$

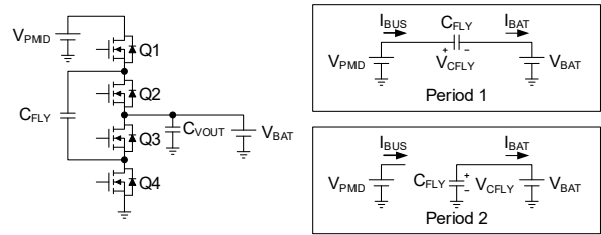


Figure 4. Voltage Divider Charger Operating Principle

Assuming no charge leakage path and considering R_{EFF} as the effective input to output resistance (due to the switch on-resistances and C_{FLY} losses), the divider can be modeled as shown in Figure 5. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The SGM41608 has two channels of such architecture operating at f_{sw} frequency with 180° phase difference. Each channel provides I_{VOUT}/2 at the V_{OUT} node, so:

$$V_{VOUT} = \frac{1}{2}V_{PMID} - \frac{1}{2}R_{EFF} \times I_{VOUT} \tag{6}$$

At low switching frequencies the capacitor charge sharing losses are dominant and R_{EFF} ≈ 1/(4f_{sw}C_{FLY}). As frequency increases, R_{EFF} finally approaches (R_{DS_QCH} + R_{DS_QDH} + R_{DS_QCL} + R_{DS_QDL})/2.

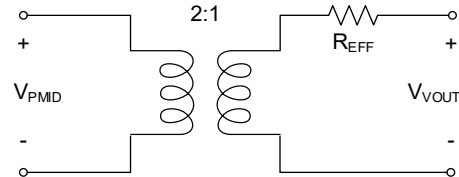


Figure 5. Model of Voltage Divider

The two-channel interleaved operation ensures a smooth input current and simplifies the noise filtering. The V_{OUT} ripple can be estimated by first order approximation of C_{FLY} voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time.

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

DETAILED DESCRIPTION (continued)

Bypass Mode

The SGM41608 is designed to operate in bypass mode when V_{VBUS} is close to the V_{VOUT}. When such valid voltage is present on VBUS, all switches between VBUS and VOUT are fully turned on while the other switches are kept off. When V_{VBUS} is near V_{VOUT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 5A. The bypass mode switched-capacitor charger is showed in Figure 6.

The output voltage is close to the V_{VBUS} minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two channels in parallel:

$$R_{EFF} \text{ (Bypass mode)} \approx R_{DS_QRB} + (R_{DS_QCH1} + R_{DS_QDH1}) \parallel (R_{DS_QCH2} + R_{DS_QDH2}) \quad (7)$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

Charging System

The SGM41608 is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41608. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 7 shows the block diagram of a charge system using the SGM41608 along with other devices. In this system, the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is inserted, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41608) that provides high current charging. The communication between those devices is through I²C interface.

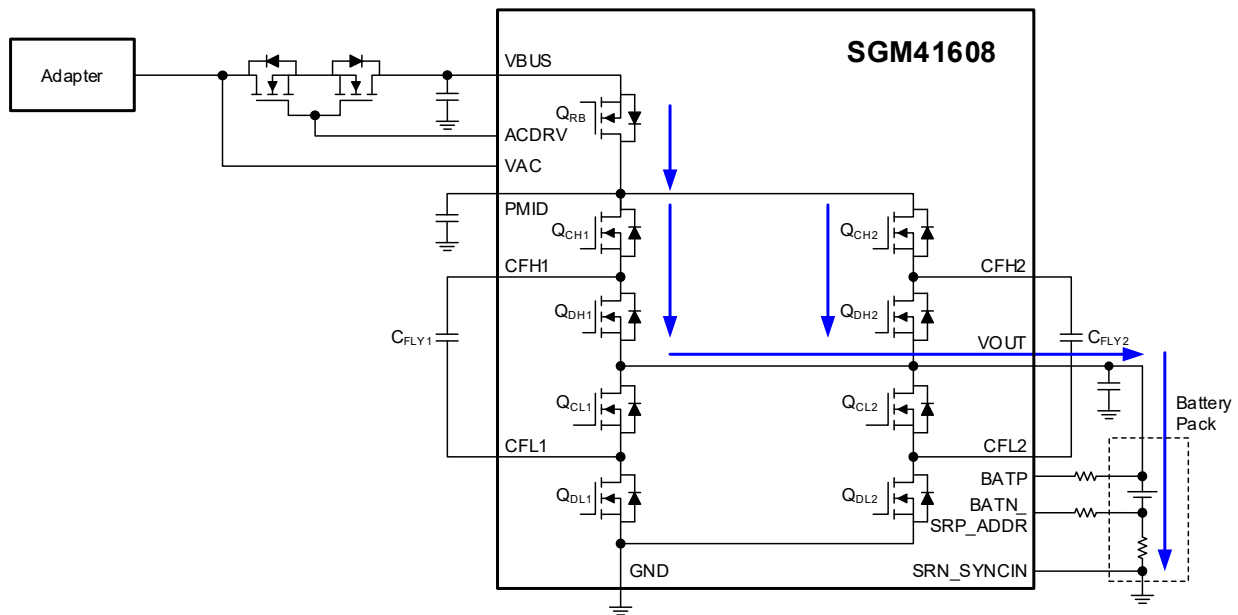


Figure 6. SGM41608 Bypass Mode

DETAILED DESCRIPTION (Continued)

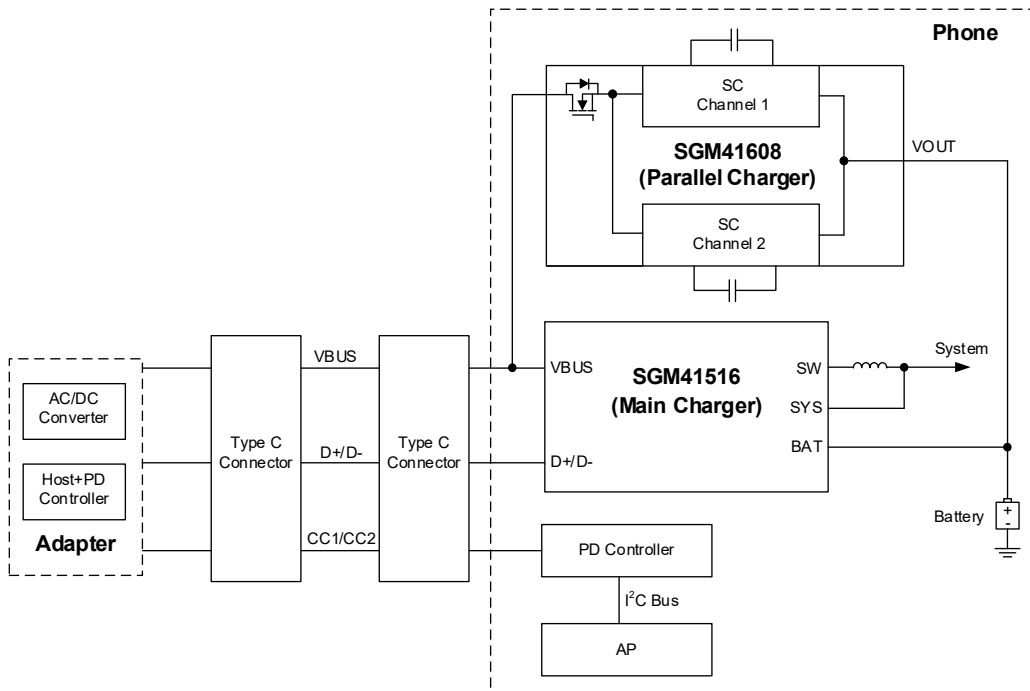


Figure 7. SGM41608 Charging System Diagram

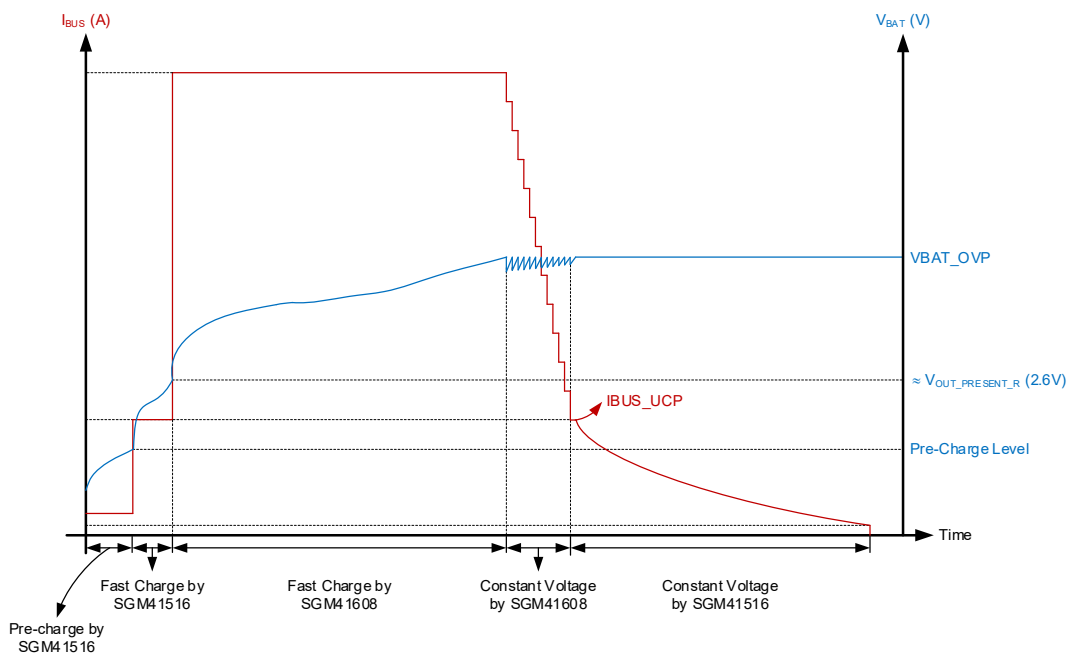


Figure 8. SGM41608 System Charging Profile

DETAILED DESCRIPTION (Continued)

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 8. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches $V_{OUT_PRESENT_R}$ (2.6V, TYP), the adapter can negotiate for a higher bus voltage and enable the SGM41608 for charging (bypass or voltage divider mode).

Startup Sequence

The SGM41608 is powered from the greater of VAC, VBUS or VOUT (VAC is used as a sense input for adapter voltage as well). When V_{VOUT} rises above $V_{OUT_UVLO_R}$, or V_{VAC} , or V_{VBUS} rises above their respective UVLO rising threshold, the I²C interface is ready for communication and all the registers are reset to default values.

The device does not start charging after powered up, because by default the charger is disabled but the ADC can be enabled and the AP can read the system parameters before enabling charge. The charge can be enabled only if $V_{VBUS} > V_{BUS_PRESENT_R}$ and $V_{VOUT} > V_{OUT_PRESENT_R}$.

Device Power up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, the REGN LDO and most of the sensing circuits are turned off, except VAC_PRESENT, VBUS_PRESENT and VOUT_PRESENT functions.

Device Power up from Input Source

When an input source is plugged-in and the conditions of $V_{VBUS} > V_{BUS_PRESENT_R}$ and $V_{VOUT} > V_{OUT_PRESENT_R}$ are valid, the AP must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need to be set are VAC_OVP, VBUS_OVP, IBUS_OCP, IBUS_UCP, VOUT_OVP, VBAT_OVP, IBAT_OCP, TSBAT_FLT and TDIE_OTP. If one of the protection trigger conditions is met,

the charger stops switching. It will also be turned off the corresponding external OVPFET when VAC_OVP or VBUS_SCP event occurs.

After setting protections, the VBUS voltage is checked to be between VBUS_ERRLO and VBUS_ERRHI to allow forward charge mode operation. When the AP configures bypass or voltage divider mode and then set CHG_EN = 1, charging is enabled and current flows into the battery, and CP_SWITCHING_STAT bit is set to 1 to indicate charging is active. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I²C serial interface.

Device HIZ State

The HIZ mode is activated when the AP sets HIZ_EN bit from 0 to 1. When the SGM41608 enters HIZ mode, the charging stops, ADC conversion discontinues, ACDRV and REGN LDO are turned off regardless of the presence of the adapter or absence of any fault conditions. To exit HIZ mode, the AP should set HIZ_EN bit to 0, or the device POR occurs.

REGN Management

REGN provides the power required for the analog section. When V_{VBUS} rises above $V_{BUS_PRESENT_R}$, REGN is powered up and ramps up to 5V (TYP). A 4.7μF or larger capacitor is required on the REGN pin.

When the faults, including VBUS_OVP, VBAT_OVP, VOUT_OVP, IBUS_OCP, IBAT_OCP, IBUS_UCP, VBUS_SCP, VAC_OVP, TSBAT_FLT and TDIE_OTP, are triggered, the converter switching stops and CHG_EN bit is reset to 0, but the REGN LDO remains powered up. Refer to the device protection section for more details.

DETAILED DESCRIPTION (continued)

Input Power Path Management

ACDRV Turn-on Condition

For most of the 2 configurations, the ACDRV controls the input power path for both SGM41608 and main charger. The ACDRV can be turned on when all of the following conditions are met:

1. The corresponding ACFET-RBFET is populated: VAC is connected to the input power and ACDRV is not short to GND.
2. V_{VAC} exceeds V_{VAC_PRESENT_R} and not higher than V_{VAC_OVP}

thresholds.

3. DIS_ACDRV bit is not set to 1.
4. Not in HIZ mode: HIZ_EN bit is not set to 1.
5. V_{VBUS} is below V_{VBUS_PRESENT_F} threshold.

Single Input without ACFET-RBFET

In this configuration, the SGM41608 is not responsible for controlling the external OVPFET. VAC is connected to VBUS directly, while ACDRV is short to GND. The following table summarizes the related pin connections and the control function of relevant registers.

Table 1. Settings Used to Control ACDRV in Forward Operation

	Auto-Mode	Manual Mode	
	Enable	Turn-On	Turn-Off
ACDRV	ACDRV_MANUAL_EN = 0	ACDRV_MANUAL_EN = 1 and ACDRV_EN = 1	ACDRV_MANUAL_EN = 1 and ACDRV_EN = 0

Table 2. Single Input without External OVPFET

Input Configuration	Single Input
External FET Connection	No external FET
Input Sense Pin Connection	VAC tied to VBUS
ACDRV Pin Connection	ACDRV short to GND
HIZ_EN	No impact on ACDRV

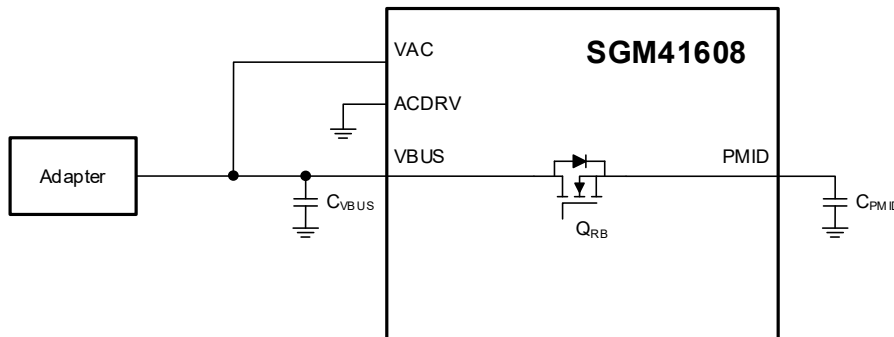


Figure 9. Single Input without ACFET-RBFET

DETAILED DESCRIPTION (continued)

Single Input with ACFET

In this configuration, only one input N-channel MOSFET for VAC (ACFET) is placed. VAC and ACDRV are connected to the drain and the gate of ACFET, respectively. The structure supports single input from VAC. The following table summarizes the related pin connections and the control function of relevant registers, as well as the status bits.

OTG Mode Operation

If the switching charger works in OTG mode and the back-to-back N-MOSFET is controlled by SGM41608, they must be turned on/off manually. The external OVPFET will be turned off when VAC_OVP or VBUS_OVP fault occurs.

To enter OTG mode, the AP needs to follow the steps outlined below:

1. The AP enables OTG mode for switching charger.
2. The AP writes OTG_EN = 1.
3. The AP writes ACDRV_MANUAL_EN = 1 and ACDRV_EN = 1.
4. If VAC_OVP or VBUS_OVP fault occurs, SGM41608 will

turn off the external OVPFET but will not reset OTG_EN bit. After the fault is cleared, the ACDRV will turn on again. It is recommended to set V_{AC_OVP} to the same threshold in OTG mode.

5. To disable OTG output, the AP needs to set ACDRV_EN = 0 or DIS_ACDRV = 1, and can write 1 to the VAC/VBUS pull-down resistor enable bits (VAC_PD_EN/VBUS_PD_EN) as needed to discharge the residual energy.

To exit OTG mode, the AP needs to follow the steps outlined below:

1. The AP disables OTG mode for switching charger.
2. The AP writes 1 to the VAC/VBUS pull-down resistor enable bits (VAC_PD_EN/VBUS_PD_EN) as needed to discharge the residual energy.
3. After VBUS and VAC is discharged, the AP writes ACDRV_EN = 0 or DIS_ACDRV = 1 to turn off ACDRV.
4. The AP writes OTG_EN = 0 and ACDRV_MANUAL_EN = 0 to exit OTG mode.

Table 3. Single Input with Single OVPFET

Input Configuration	Single Input
External FET Connection	Only ACFET, no RBFET
Input Sense Pin Connection	VAC tied to the input source
ACDRV Pin Connection	ACDRV tied to the gate of ACFET
ACDRV_MANUAL_EN	0 = ACDRV Auto-mode (default) 1 = ACDRV Manual-mode
ACDRV_EN	0 = ACDRV is turned OFF 1 = ACDRV is turned ON
DIS_ACDRV	1 = Force ACDRV OFF 0 = ACDRV can be turned on when the activation conditions of ACDRV are valid
HIZ_EN	1 = Enter HIZ mode, force ACDRV OFF 0 = Exit HIZ mode, ACDRV can be turned on when the activation conditions of ACDRV are valid

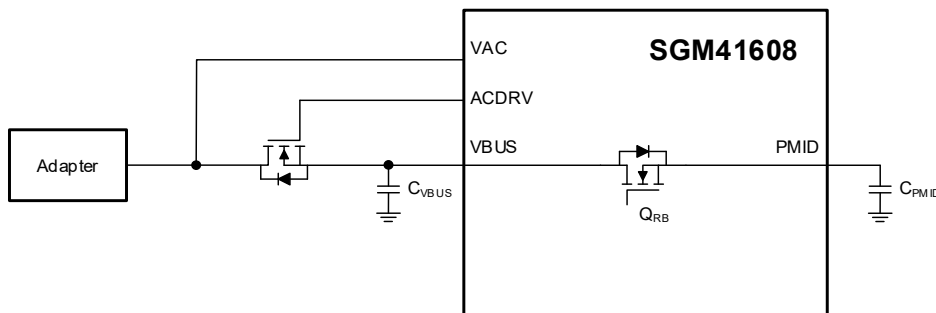


Figure 10. Single Input with ACFET

DETAILED DESCRIPTION (continued)

Reverse Manual Mode

When the OVPFET operates in reverse mode, it must be turned on/off manually. The external OVPFET will be turned off to enter reverse operation mode, the AP should follow the steps below:

1. The AP writes OTG_EN = 1, ACDRV_MANUAL_EN = 1 and ACDRV_EN = 0.
2. The AP writes MODE[1:0] = 10/11.
3. The AP writes CHG_EN = 1, and SGM41608 starts the reverse operation.
4. SGM41608 sets RVS_SSOK_FLAG = 1 when soft-start is OK in reverse mode and generate an INT pulse to notify the AP.
5. The AP writes ACDRV_EN = 1.
6. If VAC_OVP or VBUS_OVP or VBUS_SCP fault occurs, SGM41608 will turn off the external OVPFET although ACDRV_EN bit is still 1, and then reset CHG_EN = 0 to stop reverse operation and turn off the Q_{RB}, and finally generate an INT pulse to notify the AP.
7. The AP needs to reset ACDRV_EN = 0, and can write 1 to the VAC/VBUS pull-down resistor enable bits as needed to discharge the residual energy.

To exit reverse operation mode, the AP should follow the steps below:

1. The AP writes ACDRV_EN = 0, and SGM41608 turns off the external OVPFET.
2. The AP writes CHG_EN = 0.
3. SGM41608 stops reverse operation and turns off the Q_{RB}.
4. The AP writes OTG_EN = 0 and ACDRV_MANUAL_EN = 0.
5. The AP can write 1 to the VAC/VBUS pull-down resistor enable bits as needed to discharge the residual energy.

ADC

The SGM41608 integrates a fast 8-channel, 12-Bit ADC converter to monitor input/output currents and voltages, as well as the temperature of the device and battery. The ADC is controlled by the ADC_CONTROL 1 and ADC_CONTROL 2 registers. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC_AVG bit is utilized to enable or disable ADC averaging (disabled default),

and the ADC_AVG_INIT bit can be used to choose the average initial value (use an existing register value or a new value). The ADC operates independent of the faults, unless the AP sets the ADC_EN bit to 0.

The ADC can operate if $V_{VAC} > V_{AC_PRESENT_R}$ or $V_{VBUS} > V_{BUS_PRESENT_R}$ or $V_{VOUT} > V_{OUT_PRESENT_R}$ condition is valid. Otherwise, the ADC conversion is postponed until one of TSBAT is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CONTROL 1 and ADC_CONTROL 2 registers. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

I²C Address

BATN_SRP_ADDR Pin State	7- Bit Address
GND	0b1100 001 + W/R
Hi-Z	0b1100 011 + W/R

Parallel Operation

To achieve higher charging current, it is feasible to use two devices in parallel, with one configured in primary mode and the other in secondary mode. Using two devices in parallel can also enable each device to operate at a lower charging current, resulting the higher efficiency compared with single device at the same total charging current.

The parallel charging configuration for dual charger is shown in Figure 11. When set as the primary, the TSBAT_SYNCOUT pin functions as the synchronization signal output pin, while the SRN_SYNCIN pin operates as SRN. When set as the secondary, the SRN_SYNCIN pin functions as the synchronization signal input pin, and the TSBAT_SYNCOUT pin operates as TSBAT. The TSBAT_SYNCOUT pin of the primary should be tied to the SRN_SYNCIN pin of the secondary. The external OVPFET are controlled by the primary, and the ACDRV pins of the secondary should short to GND.

DETAILED DESCRIPTION (continued)

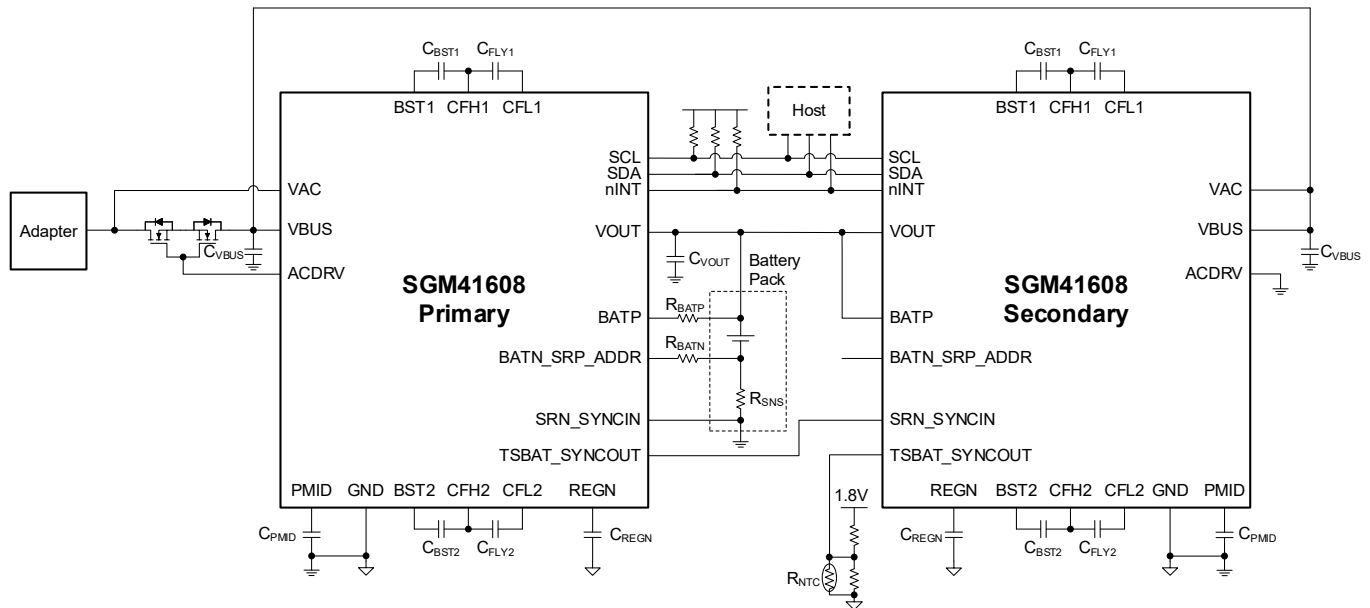


Figure 11. Parallel Operation of SGM41608

The parallel charging configuration can operate in both bypass mode and voltage divider mode. The distribution of current between the primary and secondary is influenced by the loop impedance, and the chargers do not automatically balance it. To achieve current balance, it is essential to design the board layout with maximum symmetry.

nINT Pin, STAT, Flag and Mask Bits

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of t_{INT} to notify the AP when it is triggered by an event. See the register map for all event flag and control bits.

When an event occurs, a nINT signal is sent to the AP, and the corresponding status and flag bits are set to 1. The flag bit can be read to clear but the status bit remains as 1 if the event is still present. The nINT signal is not sent again if an event is still present after the flag bit is read cleared, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.

Input Over-Voltage Protection (VAC_OVP)

The SGM41608 monitors the adapter voltage on the VAC pin to use the ACDRV output to control the external OVPFETs respectively. Taking VAC_OVP as an example, the VAC over-voltage protection circuit is enabled if V_{VAC} rises above $V_{AC_PRESENT_R}$. If V_{VAC} is above $V_{AC_PRESENT_R}$ for at least $t_{VAC_IN_DEG}$ time and $DIS_ACDRV = 0$, the ACDRV will output

drive signal to turn on the ACFET-RBFET. If the VAC reaches the $V_{AC_OVP_R}$ threshold, the gate voltage starts to drop and eventually the ACFET-RBFET is fully turned off. Figure 12 shows the VAC_OVP and ACDRV operation timings. The $V_{AC_OVP_R}$ threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC pin and the external OVPFETs.

Input Short-Circuit Protection (VBUS_SCP)

The VBUS_SCP function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFET are turned on or if V_{VBUS} rises above $V_{BUS_PRESENT_R}$. If the V_{VBUS} falls below 2V, the OVPFET are turned off, and charging is stopped. CHG_EN bit is reset to 0 (disable). Also, VBUS_SHORT_STAT and VBUS_SHORT_FLAG bits are set to 1, and an INT pulse is asserted. The device will wait for 760ms before automatically re-enabling and initiating startup sequence.

VBUS Charge Voltage Range (VBUS_ERRLO & VBUS_ERRHI)

The VBUS_ERRLO and VBUS_ERRHI functions are included to avoid problems due to wrong VBUS setting for forward charging. In bypass mode or in voltage divider charging mode, if V_{VBUS} is beyond the range between V_{BUS_ERRLO} and V_{BUS_ERRHI} , CHG_EN bit will still be 1. Once V_{VBUS} is within the charge range, charging will start and VBUS_ERRLO and VBUS_ERRHI functions will be disabled.

DETAILED DESCRIPTION (continued)

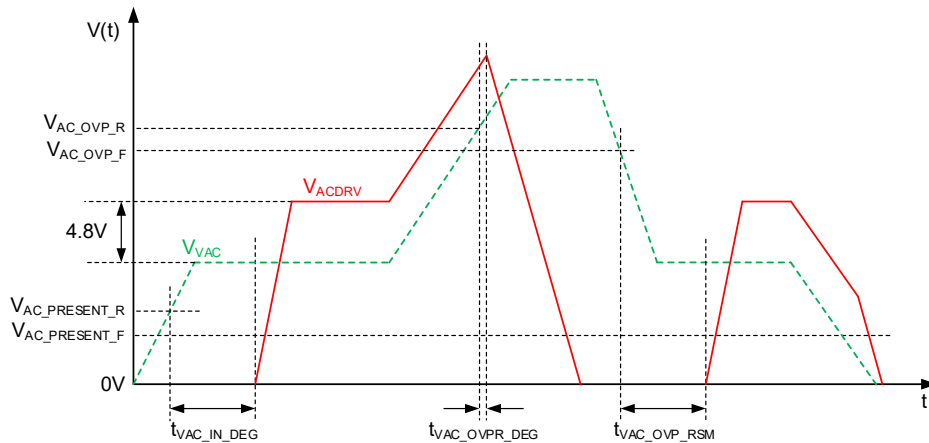


Figure 12. ACDRV Operation Timing

Input, Output and Battery Over-Voltage Protection (VBUS_OVP, VOUT_OVP and VBAT_OVP)

The VBUS_OVP, VOUT_OVP and VBAT_OVP functions detect input and output voltage conditions. If either input or output voltage is higher than the protection threshold, the device stops charging and resets CHG_EN bit to 0 (disable). The VBUS_OVP function monitors VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBAT_OVP uses BATH and BATN_SRP_ADDR remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, two 100Ω resistors are needed to connect in series to the BATH and BATN_SRP_ADDR pins respectively. The VBUS_OVP, VOUT_OVP and VBAT_OVP thresholds can be set by I²C serial interface.

Input and Battery Over-Current Protection (IBUS_OCP and IBAT_OCP)

The IBUS_OCP function monitors the input current via Q_{RB}. If CHG_EN bit are set to enable charge, the Q_{RB} is turned on and the IBUS_OCP function starts detecting the input current. If the I_{BUS} reaches I_{BUS_OCP} threshold, the device stops charging and resets CHG_EN bit to 0 (disable). The battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between BATN_SRP_ADDR and SRN_SYNCIN pins. If I_{BAT_OCP} threshold is reached, the device stops charging and resets CHG_EN bit to 0 (disable). The IBUS_OCP and IBAT_OCP thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q_{RB} during forward charging. After charging is started and soft-start time expired, if I_{BUS} is below I_{BUS_UCP} with t_{IBUS_UCP_DEG} deglitch time, the charging will be stopped and CHG_EN bit is reset to 0 (disable). The t_{IBUS_UCP_DEG} timer can be set by I²C serial interface.

CFLY Diagnosis (CFLY_SHORT)

The CFLY diagnosis function identifies the health of flying capacitors before and during voltage divider switching (charging). The device initialization process is started after CHG_EN bit is set to 1. When V_{VBUS} and V_{BAT} are in the charge range, the flying capacitors in both channels are pre-charged. A CFLY short-circuit is detected if they cannot be charged, and the voltage between V_{CFHx} and V_{CFLx} remains below (V_{VOUT} - 0.6V). If so, the initialization process is stopped and CHG_EN bit is reset to 0 (disable). Even if CFLY capacitors pass the short-circuit test in the initialization process, the CFLY diagnosis function remains active and whenever a V_{CFLY} voltage falls below (V_{VOUT} - 0.6V), the operation is stopped and CHG_EN bit is reset to 0 (disable). The PIN_DIAG_FAIL_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY short-circuit event, other protection events such as IBUS_OCP, VBAT_OVP or PEAK_OCP may occur.

Converter Peak Over-Current Protection (PEAK_OCP)

The PEAK_OCP function monitors the converter switch operating currents. If the Q_{CLx} or Q_{DLx} current reaches switch OCP threshold (I_{CONV_OCP}) during charging, the charging is stopped and CHG_EN bit is reset to 0.

DETAILED DESCRIPTION (continued)

TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents operation in over-temperature condition. The die temperature is monitored and if the T_{DIE_OTP_R} threshold is reached, the charging is stopped and CHG_EN bit is reset to 0 (disable). The startup sequence cannot be initiated again until the die temperature falls down with a 30°C hysteresis. The TDIE_OTP threshold can be set by I²C serial interface.

Battery Temperature Monitoring (TSBAT_FLT)

The SGM41608 monitors battery temperature through the TSBAT_SYNCOUT pin, which are connected to the external resistor divider that is pulled up to 1.8V. A negative coefficient thermistor (NTC) is needed in parallel with the low-side resistor. When the voltage on the TSBAT_SYNCOUT pin drops below the specific threshold, it indicates a "hot" temperature condition. In response, the device will stop charging and reset CHG_EN bit to 0. The startup sequence cannot be initiated again until the battery temperature fall down, which resulting a voltage rising on TSBAT_SYNCOUT pin. The TSBAT_FLT threshold can be set by I²C serial interface.

Take TSBAT_SYNCOUT pin as example, the external bias resistors network is shown as Figure 13. The selection of R_{T1} and R_{T2} resistors depends on the NTC utilized. For a 10kΩ NTC, R_{T1} and R_{T2} should be 10kΩ resistors. If a 100kΩ NTC is selected, choose 100kΩ resistors as R_{T1} and R_{T2}.

The voltage percentage of the TSBAT_SYNCOUT pin (V_{TS}/1.8V × 100%) may vary from 0% to 50%, and the voltage on the TSBAT_SYNCOUT pin is determined by the following equation:

$$V_{TSBAT} (V) = \frac{1}{\left(\frac{1}{R_{NTC}} + \frac{1}{R_{T1}}\right)} \times 1.8V \div \left(R_{T2} + \left(\frac{1}{\frac{1}{R_{NTC}} + \frac{1}{R_{T1}}}\right)\right) \tag{8}$$

The voltage percentage of the TSBAT_SYNCOUT pin is determined by the following equation:

$$TSBAT (\%) = \frac{1}{\left(\frac{1}{R_{NTC}} + \frac{1}{R_{T1}}\right)} \div \left(R_{T2} + \left(\frac{1}{\frac{1}{R_{NTC}} + \frac{1}{R_{T1}}}\right)\right) \tag{9}$$

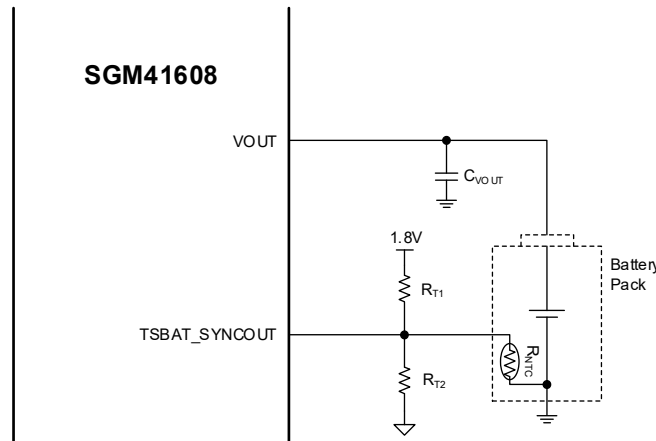


Figure 13. TSBAT_SYNCOUT Thermistor and Bias Network

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
MS	--	--	--	--	0x0E[7:6]	--
DEVICE_REV	--	--	--	0x03[7:4]	--	--
DEVICE_ID	--	--	--	0x03[3:0]	--	--
REG_RST	--	--	--	--	0x09[3]	--
HIZ_EN	--	--	--	--	0x07[0]	--
OTG_EN	--	--	--	--	0x0D[4]	--
CHG_EN	--	--	--	--	0x0C[7]	--
SCC_MODE	--	--	--	0x09[1:0]	--	--
VBUS_ERRLO	0x12[2]	0x16[2]	0x1A[2]	--	0x0E[5]	--
VBUS_ERRHI	0x12[3]	0x16[3]	0x1A[3]	--	0x0E[4]	--
ACDRV_CTRL	--	--	--	--	0x0D[6:5]	--
WD_TIMEOUT	0x14[0]	0x18[0]	0x1C[0]	0x0A[1:0]	0x0D[7]	--
FSW_SET	--	--	--	0x0B[3:0]	--	--
FREQ_SHIFT	--	--	--	0x0B[5:4]	--	--
RSNS	--	--	--	0x09[7]	--	--
SS_TIMEOUT	0x14[1]	0x18[1]	0x1C[1]	0x0A[7:5]	--	--
ADC	0x12[7]	0x16[7]	0x1A[7]	--	0x1D[7]	--
VAC_PD_EN	--	--	--	--	0x09[6]	--
VBUS_PD_EN	--	--	--	--	0x09[4]	--
VAC_OVP	0x13[6]	0x17[6]	0x1B[6]	0x02[5:3]	0x02[6]	--
VBUS_OVP	0x13[2]	0x17[2]	0x1B[2]	0x02[2:0]	0x02[7]	0x0F[2]
IBUS_UCP	0x13[5]	0x17[5]	0x1B[5]	0x07[5]	0x0D[0]	0x10[7:6]
IBUS_OCP	0x13[4]	0x17[4]	0x1B[4]	0x04[6:0]	0x04[7]	0x10[5:4]
VOUT_OVP	0x13[1]	0x17[1]	0x1B[1]	0x0E[3:2]	0x09[2]	0x0F[1]
VBAT_OVP	0x13[0]	0x17[0]	0x1B[0]	0x00[6:0]	0x00[7]	0x10[3:2]
CONV_OCP	0x11[6]	0x15[6]	0x19[6]	--	0x07[1]	--
PMID2VOUT_OVP	0x14[4]	0x18[4]	0x1C[4]	0x05[2:0]	0x05[7]	0x0F[6]
PMID2VOUT_UVP	0x14[5]	0x18[5]	0x1C[5]	0x06[2:0]	0x06[7]	0x0F[7]
VBUS_SCP	0x12[4]	0x16[4]	0x1A[4]	--	--	--
IBAT_OCP	0x13[3]	0x17[3]	0x1B[3]	0x01[6:0]	0x01[7]	0x0F[5:4]
PIN_DIAG	0x12[6]	0x16[6]	0x1A[6]	--	0x0C[4]	--
TSBAT_FLT	0x14[2]	0x18[2]	0x1C[2]	0x08[5:0]	0x08[7]	--
TDIE_OTP	0x14[3]	0x18[3]	0x1C[3]	--	0x0D[1]	--
VOUTPRESENT	0x11[4:3]	0x15[4:3]	0x19[4:3]	--	--	--
VAC_INSERT	0x11[1]	0x15[1]	0x19[1]	--	--	--
VBUSPRESENT	0x11[2]	0x15[2]	0x19[2]	--	--	--

REGISTER MAPS (continued)

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

REG0x00: BATOVP Register [reset = 0x5A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOVP_DIS	0	R/W	Disable BATOVP 0 = Enable (Default) 1 = Disable	REG_RST
D[6:0]	BATOVP[6:0]	1011010	R/W	VBAT OVP Rising Threshold Setting Bits $V_{BAT_OVP_R} = BATOVP[6:0] \times 0.01V + 3.84V$ Offset: 3.84V Step: 10mV Range: 4.04V (b0010100) - 5.11V (b1111111) Default: 4.74V (b1011010) Any setting lower than b0010100 is clamped to b0010100 (4.04V)	REG_RST

REG0x01: BATOCP Register [reset = 0x51]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATOCP_DIS	0	R/W	IBAT OCP Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	BATOCP[6:0]	1010001	R/W	IBAT OCP Threshold Setting Bits $I_{BAT_OCP} = BATOCP[6:0] \times 0.1A$ Offset: 0A Step: 100mA Range: 0.5A (b0000101) - 12.7A (b1111111) Default: 8.1A (b1010001) Any setting lower than b0000101 is clamped to b0000101 (0.5A)	REG_RST

REGISTER MAPS (continued)

REG0x02: VAC_VBUS OVP Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUSOVP_DIS	0	R/W	VBUS OVP Disable Bit 0 = Enable the VBUS_OVP (default) 1 = Disable the VBUS_OVP	REG_RST
D[6]	VAC_OVP_DIS	0	R/W	VAC OVP Disable Bit 0 = Enable the VAC_OVP (default) 1 = Disable the VAC_OVP	REG_RST
D[5:3]	VAC_OVP[2:0]	000	R/W	VAC OVP Rising Threshold Setting Bits 000 = 6.5V (default) 001 = 11V 010 = 12V 011 = 13V 100 = 14V 101 = 15V 110 = 16V 111 = 18V	REG_RST
D[2:0]	VBUS_OVP[2:0]	000	R/W	VBUS OVP Rising Threshold Setting Bits. Forward 2:1 mode/Reverse 1:2 mode: $V_{BUS_OVP_R} = VBUS_OVP[2:0] \times 0.5V + 10.5V$ Offset: 10.5V Step: 500mV Range: 10.5V (b000) - 14V (b111) Default: 10.5V (b000) Forward 1:1 mode/Reverse 1:1 mode: $V_{BUS_OVP_R} = VBUS_OVP[2:0] \times 0.25V + 5.25V$ Offset: 5.25V Step: 250mV Range: 5.25V (b000) - 7V (b111) Default: 5.25V (b000)	REG_RST

REG0x03: DEVICE_INFO Register [reset = 0x91]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	DEVICE_REV[3:0]	1001	R	Device Revision Default: 1001	N/A
D[3:0]	DEVICE_ID[3:0]	0001	R	Device ID Default: 0001	N/A

REG0x04: BUSOCP Register [reset = 0x46]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUSOCP_DIS	0	R/W	IBUS OCP Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6:0]	BUSOCP[6:0]	1000110	R/W	IBUS OCP Threshold Setting Bits $I_{BUS_OCP} = BUSOCP[6:0] \times 0.05A$ Offset: 0A Step: 50mA Range: 1A (0010100) - 6.35A (1111111) Default: 3.5A (1000110) Any setting lower than b0010100 is clamped to b0010100 (1A)	REG_RST

REGISTER MAPS (continued)

REG0x05: PMID2VOUT_OVP Register [reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2VOUT_OVP_DIS	0	R/W	PMID2VOUT_OVP Disable Bit 0 = Enable PMID2VOUT over-voltage protection (default) 1 = Disable PMID2VOUT over-voltage protection	REG_RST
D[6]	Reserved	0	R/W	Reserved	REG_RST
D[5]	PMID2VOUT_OVP_CFG	0	R/W	PMID2VOUT_OVP Configure Bit 0 = Set the PMID2VOUT_OVP threshold based on PMID2VOUT_OVP[2:0] (default) 1 = Set the PMID2VOUT threshold as PMID2VOUT_OVP[2:0] + 1V	REG_RST
D[4:3]	Reserved	00	R/W	Reserved	REG_RST
D[2:0]	PMID2VOUT_OVP[2:0]	001	R/W	PMID/n-VOUT Over-Voltage Protection Setting n = 1 or 2, depends on the MODE register configuration $V_{PMID2VOUT_OVP} = PMID2VOUT_OVP[2:0] \times 100mV + 400mV$ Offset: 400mV Step: 100mV Range: 400mV (b000) - 1100mV (b111) Default: 500mV (b001)	REG_RST

REG0x06: PMID2VOUT_UVP Register [reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2VOUT_UVP_DIS	0	R/W	PMID2VOUT_UVP Disable Bit 0 = Enable PMID2VOUT under-voltage protection (default) 1 = Disable PMID2VOUT under-voltage protection	REG_RST
D[6:3]	Reserved	0000	R/W	Reserved	REG_RST
D[2:0]	PMID2VOUT_UVP[2:0]	001	R/W	PMID/n-VOUT Under-Voltage Protection Setting n = 1 or 2, depends on the MODE register configuration $V_{PMID2VOUT_UVP} = PMID2VOUT_UVP[2:0] \times (-50mV) - 100mV$ Offset: -100mV Step: -50mV Range: -100mV (b000) - -450mV (b111) Default: -150mV (b001) The threshold is effective for all four modes.	REG_RST

REG0x07: MIX_CONTROL Register [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	I2C_HI_DET	0	R/W	I ² C High Level Input Voltage Threshold Setting Bit 0 = 1.2V (default) 1 = 1.8V	REG_RST
D[6]	PEAK_OCP_RVS_DIS	0	R/W	PEAK_OCP_RVS Protection Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[5]	BUSUCP	0	R/W	BUSUCP Setting Bit 0 = $I_{BUS_UCP_R} = 500mA$, $I_{BUS_UCP_F} = 250mA$ (default) 1 = $I_{BUS_UCP_R} = 300mA$, $I_{BUS_UCP_F} = 150mA$	REG_RST
D[4:3]	PEAK_OCP_SET[1:0]	01	R/W	Q _{CLX} and Q _{DLX} Peak OCP Threshold Setting Bits 00 = 11A 01 = 13A (default) 10 = 15A 11 = 17A	REG_RST
D[2]	PEAK_OCP_RVS	0	R/W	Reverse PEAK OCP Threshold Setting Bit 0 = 20mV (default) 1 = 30mV	REG_RST
D[1]	CONV_OCP_DIS	0	R/W	CONV_OCP Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[0]	HIZ_EN	0	R/W	HIZ Mode Enable Bit 0 = Disable HIZ mode (default) 1 = Enable HIZ mode When device is in HIZ mode, converter stops switching, ADC stops converting, ACDRV is turned off and the REGN LDO is forced off.	REG_RST

REGISTER MAPS (continued)

REG0x08: TSBAT_FLT Register [reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSBAT_FLT_DIS	0	R/W	TSBAT_FLT Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6]	Reserved	0	R/W	Reserved	REG_RST
D[5:0]	TSBAT_FLT[5:0]	011000	R/W	TSBAT Voltage Falling Threshold $V_{TSBAT_F} = TSBAT_FLT[5:0] \times 0.025V$ Offset: 0V Step: 25mV Range: 0V (b000000) - 1.575V (b111111) Default: 0.6V (b011000)	REG_RST

REG0x09: CHARGER_CONTROL 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_RSNS	0	R/W	External IBAT Current Sense Resistor Setting Bit 0 = 2mΩ (default) 1 = 5mΩ	REG_RST
D[6]	VAC_PD_EN	0	R/WC	VAC Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VAC is pulled down by 35mA. When enabled, the VAC is pulled down for 750ms and then this bit is automatically reset to 0.	REG_RST
D[5]	PMID_PD_EN	0	R/W	PMID Pull-Down Resistor Enable Bit 0 = PMID pull-down disabled (default) 1 = PMID pull-down enabled	REG_RST
D[4]	VBUS_PD_EN	0	R/W	VBUS Pull-Down Resistor Enable Bit 0 = VBUS pull-down disabled (default) 1 = VBUS pull-down enabled	REG_RST
D[3]	REG_RST	0	R/WC	Register Reset Bit 0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default values and then this bit is automatically reset to 0.	REG_RST
D[2]	VOUT_OVP_DIS	0	R/W	VOUT OVP Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[1:0]	MODE[1:0]	00	R/W	These bits decide the operation mode. 00 = Forward 2:1 charger mode (default) 01 = Forward 1:1 charger mode 10 = Reverse 1:2 converter mode 11 = Reverse 1:1 converter mode Mode registers cannot be changed when CHG_EN = 1	REG_RST

REGISTER MAPS (continued)

REG0x0A: CHARGER_CONTROL 2 Register [reset = 0xE0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	SS_TIMEOUT[2:0]	111	R/W	Soft-Start Timeout Setting Bits After soft-start timeout, the device checks if I _{BUS} is above IBUS_UCP threshold. 000 = SS timeout disabled 001 = 10ms 010 = 20ms 011 = 40ms 100 = 80ms 101 = 320ms 110 = 1.28s 111 = 10.24s (default)	REG_RST
D[4:3]	Reserved	00	R/W	Reserved	REG_RST
D[2]	FORCE_VAC_OK	0	R/W	0 = CHG_EN is allowed to be set to '1' when VAC_INSERT_STAT = 1 and VBUS_PRESENT_STAT = 1 (default) 1 = CHG_EN is allowed to be set to '1' when VBUS_PRESENT_STAT = 1 Note: If MODE[1:0] = 10 or 11, CHG_EN is allowed to be set 1 regardless of VAC_INSERT_STAT and VBUS_PRESENT_STAT bits.	REG_RST
D[1:0]	WDT_TIMER[1:0]	00	R/W	Watchdog Timer Setting Bits 00 = 0.5s (default) 01 = 1s 10 = 5s 11 = 30s	REG_RST

REG0x0B: CHARGER_CONTROL 3 Register [reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	REG_RST
D[6]	FREQ_DIV	0	R/W	f _{sw} Divide Bit 0 = Set the CP switching frequency based on FSW_SET (default) 1 = Set the CP switching frequency as 1/4 FSW_SET	REG_RST
D[5:4]	FREQ_SHIFT[1:0]	00	R/W	Adjust f _{sw} for EMI 00 = Nominal frequency (default) 01 = -10% 10 = +10% 11 = Spread spectrum varies frequency ±10%	REG_RST
D[3:0]	FSW_SET[3:0]	0011	R/W	Set the CP switching frequency f _{sw} = FSW_SET[3:0] × 100kHz + 500kHz Offset: 500kHz (b0000) Step: 100kHz Range: 500kHz (b0000) - 2000kHz (b1111) Default: 800kHz (b0011)	REG_RST

REGISTER MAPS (continued)

REG0x0C: CHARGER_CONTROL 4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CHG_EN	0	R/W	Charge Enable Bit 0 = Disabled (default) 1 = Enabled. If any fault has occurred, device returns to standby mode and this bit is automatically cleared to 0.	REG_RST or Watchdog
D[6]	Reserved	0	R/W	Reserved	REG_RST
D[5]	VBUS_SHORT_DIS	0	R/W	VBUS_SHORT Disable Bit 0 = Enable the VBUS_SHORT protection (default) 1 = Disable the VBUS_SHORT protection	REG_RST
D[4]	PIN_DIAG_DIS	0	R/W	Pin Diagnosis Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[3:2]	OVPGATE_ISET[1:0]	00	R/W	External OVPFET Gate Drive Current Setting Bit 00 = 10µA (default) 01 = 20µA 10 = 40µA 11 = 120µA	REG_RST
D[1]	IBATSNS_HS_EN	0	R/W	External IBAT Current Sense Resistor Setting Bit 0 = The device supports low-side IBAT sense (default) 1 = The device supports high-side IBAT sense	REG_RST
D[0]	EN_IBATSNS	0	R/W	IBAT Current Sense Function Setting Bit 0 = Enable IBATSNS only when CHG_EN = 1 (default) 1 = Enable IBATSNS when CHG_EN = 0	REG_RST

REG0x0D: CHARGER_CONTROL 5 Register [reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WDT_DIS	1	R/W	Watchdog Timer Disable Bit 0 = Enable watchdog 1 = Disable watchdog (default)	REG_RST
D[6]	ACDRV_MANUAL_EN	0	R/W	ACDRV Operation Mode Setting Bit 0 = ACDRV Auto-mode (default) 1 = ACDRV Manual-mode	REG_RST
D[5]	ACDRV_EN	0	R/W	Status and Control Bit of ACDRV Driver 0 = ACDRV is turned OFF (default) 1 = ACDRV is turned ON	REG_RST
D[4]	OTG_EN	0	R/W	Power Path Control Enable Bit During OTG Mode 0 = OTG precondition is VAC_OK 1 = OTG precondition is VBUS_PRESENT	REG_RST or Watchdog
D[3]	Reserved	0	R/W	Reserved	REG_RST
D[2]	DIS_ACDRV	0	R/W	Disable Bit for ACDRV When this bit is set, the device forces ACDRV off. 0 = ACDRV is allowed to be turned on (default) 1 = ACDRV is forced off	REG_RST
D[1]	TSHUT_DIS	0	R/W	TSHUT Protection Disable Bit 0 = Enable the thermal shutdown protection (default) 1 = Disable the thermal shutdown protection	REG_RST
D[0]	BUSUCP_DIS	0	R/W	IBUS UCP Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST

REGISTER MAPS (continued)

REG0x0E: CHARGER_CONTROL 6 Register [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SYNC_FUNCTION_EN	0	R/W	Parallel Function Enable Bit 0 = Disable master and slave parallel function (default) 1 = Enable master and slave parallel function This bit can only be revised when CHG_EN = 0	REG_RST
D[6]	SYNC_MASTER_EN	0	R/W	Parallel Function Configure Bit 0 = Configure as slave (default) 1 = Configure as master This bit can only be revised when CHG_EN = 0	REG_RST
D[5]	VBUS_ERRLO_DIS	0	R/W	VBUS_ERRLO Protection Disable Bit 0 = Enable, converter does not switching, but Q _{RB} is turned on when device is in VBUS_ERRLO (default) 1 = Disable, both converter and Q _{RB} are turned on when device is in VBUS_ERRLO	REG_RST
D[4]	VBUS_ERRHI_DIS	0	R/W	VBUS_ERRHI Protection Disable Bit 0 = Enable, converter does not switching, but Q _{RB} is turned on when device is in VBUS_ERRHI (default) 1 = Disable, both converter and Q _{RB} are turned on when device is in VBUS_ERRHI	REG_RST
D[3:2]	VOUT_OVP[1:0]	11	R/W	VOUT OVP Rising Threshold Setting Bits 00 = 4.7V 01 = 4.8V 10 = 4.9V 11 = 5.0V (default)	REG_RST
D[1]	Reserved	0	R/W	Reserved	REG_RST
D[0]	CFLY_SHORT_SEL	0	R/W	CFLY Short Detection Threshold Selection Bit 0 = V _{VOUT} - 0.6V (default) 1 = V _{VOUT} - 1.2V	REG_RST

REG0x0F: Deglitch Time1 Register [reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2VOUT_UVP_DEG	0	R/W	PMID2VOUT_UVP Deglitch Time 0 = 100ns (default) 1 = 1μs	REG_RST
D[6]	PMID2VOUT_OVP_DEG	0	R/W	PMID2VOUT_OVP Deglitch Time 0 = 100ns (default) 1 = 1μs	REG_RST
D[5:4]	IBAT_OCP_DEG[1:0]	01	R/W	IBAT OCP Deglitch Time 00 = 80μs 01 = 320μs (default) 10 = 640μs 11 = 5ms	REG_RST
D[3]	Reserved	0	R/W	Reserved	REG_RST
D[2]	VBUS_OVP_DEG	0	R/W	VBUS OVP Deglitch Time 0 = 1μs (default) 1 = 10μs	REG_RST
D[1]	VOUT_OVP_DEG	0	R/W	VOUT OVP Deglitch Time 0 = 10μs (default) 1 = 5ms	REG_RST
D[0]	Reserved	0	R/W	Reserved	REG_RST

REGISTER MAPS (continued)**REG0x10: Deglitch Time2 Register [reset = 0x58]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	IBUSUCP_FALL_DEG[1:0]	01	R/W	IBUS UCP Deglitch Time Setting Bits 00 = 10µs 01 = 5ms (default) 10 = 50ms 11 = 150ms	REG_RST
D[5:4]	IBUS_OCP_DEG[1:0]	01	R/W	IBUS OCP Deglitch Time 00 = 80µs 01 = 320µs (default) 10 = 640µs 11 = 5ms	REG_RST
D[3:2]	VBAT_OVP_DEG[1:0]	10	R/W	VBAT OVP Deglitch Time 00 = 8µs 01 = 640µs 10 = 1.28ms (default) 11 = 5ms	REG_RST
D[1:0]	Reserved	00	R/W	Reserved	REG_RST

REG0x11: STAT 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CP_SWITCHING_STAT	0	R	Converter Active Status 0 = Switched cap is not switching (default) 1 = Switched cap is switching	N/A
D[6]	CONV_OCP_STAT	0	R	CONV_OCP_STAT Bit 0 = Not in CONV_OCP_STAT (default) 1 = In CONV_OCP_STAT	N/A
D[5]	PEAK_OCP_RVS_STAT	0	R	PEAK_OCP_RVS_STAT Bit 0 = Not in PEAK_OCP_RVS_STAT (default) 1 = In PEAK_OCP_RVS_STAT	N/A
D[4]	VOUT_TH_REV_EN_STAT	0	R	VOUT Voltage Status 0 = VOUT voltage is lower than VOUT_TH_REV_EN falling threshold (default) 1 = VOUT voltage is higher than VOUT_TH_REV_EN rising threshold	N/A
D[3]	VOUT_TH_CHG_EN_STAT	0	R	VOUT Voltage Status 0 = VOUT voltage is lower than VOUT_TH_CHG_EN falling threshold (default) 1 = VOUT voltage is higher than VOUT_TH_CHG_EN rising threshold	N/A
D[2]	VBUS_PRESENT_STAT	0	R	VBUS Voltage Status 0 = VBUS voltage is lower than VBUS_PRESENT falling threshold (default) 1 = VBUS voltage is higher than VBUS_PRESENT rising threshold	N/A
D[1]	VAC_INSERT_STAT	0	R	VAC Voltage Status 0 = VAC voltage is lower than VAC_UVLO falling threshold (default) 1 = VAC voltage is higher than VAC_UVLO rising threshold	N/A
D[0]	VOUT_INSERT_STAT	0	R	VOUT Voltage Status 0 = VOUT voltage is lower than VOUT_UVLO falling threshold (default) 1 = VOUT voltage is higher than VOUT_UVLO rising threshold	N/A

REGISTER MAPS (continued)**REG0x12: STAT 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_STAT	0	R	ADC Conversion Status Bit (in One-Shot Mode Only) 0 = Conversion not complete (default) 1 = Conversion complete	N/A
D[6]	PIN_DIAG_FAIL_STAT	0	R	PIN_DIAG_FAIL Status Bit 0 = Not in PIN_DIAG_FAIL (default) 1 = In PIN_DIAG_FAIL status	N/A
D[5]	IBUS_UCP_RISE_STAT	0	R	BUSUCP Status Bit 0 = Not in BUSUCP (default) 1 = In BUSUCP status	N/A
D[4]	VBUS_SHORT_STAT	0	R	BUSSCP Status Bit 0 = Not in BUSSCP (default) 1 = In BUSSCP status	N/A
D[3]	VBUS_ERRHI_STAT	0	R	VBUS_ERRHI Status Bit 0 = Not in VBUS_ERRHI status (default) 1 = In VBUS_ERRHI status	N/A
D[2]	VBUS_ERRLO_STAT	0	R	VBUS_ERRLO Status Bit 0 = Not in VBUS_ERRLO status (default) 1 = In VBUS_ERRLO status	N/A
D[1]	RVS_SSOK_STAT	0	R	Reverse Mode Soft-Start OK State Bit 0 = No SS OK (default) 1 = SS OK and VBUS or VAC can load current	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x13: STAT 3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	VAC_OVP_STAT	0	R	VAC_OVP Status Bit 0 = Not in VAC_OVP (default) 1 = In VAC_OVP status	N/A
D[5]	IBUS_UCP_FALL_STAT	0	R	IBUS_UCP_FALL Status Bit 0 = Not in IBUS_UCP_FALL (default) 1 = In IBUS_UCP_FALL status	N/A
D[4]	IBUS_OCP_STAT	0	R	IBUS_OCP Status Bit 0 = Not in IBUS_OCP (default) 1 = In IBUS_OCP status	N/A
D[3]	IBAT_OCP_STAT	0	R	IBAT_OCP Status Bit 0 = Not in IBAT_OCP (default) 1 = In IBAT_OCP status	N/A
D[2]	VBUS_OVP_STAT	0	R	VBUS_OVP Status Bit 0 = Not in VBUS_OVP (default) 1 = In VBUS_OVP status	N/A
D[1]	VOOUT_OVP_STAT	0	R	VOOUT_OVP Status Bit 0 = Not in VOOUT_OVP (default) 1 = In VOOUT_OVP status	N/A
D[0]	VBAT_OVP_STAT	0	R	VBAT_OVP Status Bit 0 = Not in VBAT_OVP (default) 1 = In VBAT_OVP status	N/A

REGISTER MAPS (continued)

REG0x14: STAT 4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	PMID2VOUT_UVP_STAT	0	R	PMID2VOUT_UVP Status Bit 0 = Not in PMID2VOUT_UVP (default) 1 = In PMID2VOUT_UVP status	N/A
D[4]	PMID2VOUT_OVP_STAT	0	R	PMID2VOUT_OVP Status Bit 0 = Not in PMID2VOUT_OVP (default) 1 = In PMID2VOUT_OVP status	N/A
D[3]	TSHUT_STAT	0	R	TSHUT Status Bit 0 = Not in TSHUT (default) 1 = In TSHUT status	N/A
D[2]	TSBAT_FLT_STAT	0	R	TSBAT_FLT Status Bit 0 = Not in TSBAT_FLT (default) 1 = In TSBAT_FLT status	N/A
D[1]	SS_TIMEOUT_STAT	0	R	SS_TIMEOUT Status Bit 0 = Not in SS_TIMEOUT (default) 1 = In SS_TIMEOUT status	N/A
D[0]	WD_TIMEOUT_STAT	0	R	WD_TIMEOUT Status Bit 0 = Not in WD_TIMEOUT (default) 1 = In WD_TIMEOUT status	N/A

REG0x15: FLAG 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CP_SWITCHING_FLAG	0	RC	Converter Active Flag 0 = Switched cap is not switching (default) 1 = Switched cap is switching. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	CONV_OCP_FLAG	0	RC	CONV_OCP Flag Bit 0 = No CONV_OCP Fault (default) 1 = CONV_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	PEAK_OCP_RVS_FLAG	0	RC	PEAK_OCP_RVS Flag Bit 0 = No PEAK_OCP_RVS Fault (default) 1 = PEAK_OCP_RVS fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	VOUT_TH_REV_EN_FLAG	0	RC	VOUT_TH_REV_EN Flag Bit 0 = VOUT voltage is lower than VOUT_TH_REV_EN falling threshold (default) 1 = VOUT voltage is higher than VOUT_TH_REV_EN rising threshold It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	VOUT_TH_CHG_EN_FLAG	0	RC	VOUT_TH_CHG_EN Flag Bit 0 = VOUT voltage is lower than VOUT_TH_CHG_EN falling threshold (default) 1 = VOUT voltage is higher than VOUT_TH_CHG_EN rising threshold It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	VBUS_PRESENT_FLAG	0	RC	VBUS Voltage Flag 0 = VBUS voltage is lower than VBUS_PRESENT falling threshold (default) 1 = VBUS voltage is higher than VBUS_PRESENT rising threshold It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	VAC_INSERT_FLAG	0	RC	VAC Voltage Flag 0 = VAC voltage is lower than VAC_UVLO falling threshold (default) 1 = VAC voltage is higher than VAC_UVLO rising threshold It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	VOUT_INSERT_FLAG	0	RC	VOUT Voltage Flag 0 = VOUT voltage is lower than VOUT_UVLO falling threshold (default) 1 = VOUT voltage is higher than VOUT_UVLO rising threshold It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x16: FLAG 2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_FLAG	0	RC	ADC Conversion Flag Bit (in One-Shot Mode Only) 0 = Conversion not complete (default) 1 = Conversion complete. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	PIN_DIAG_FAIL_FLAG	0	RC	PIN_DIAG_FAIL Flag Bit 0 = No PIN_DIAG_FAIL (default) 1 = PIN_DIAG_FAIL fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	IBUS_UCP_RISE_FLAG	0	RC	BUS_UCP Flag Bit 0 = VBUS current is lower than IBUS_UCP_R threshold (default) 1 = VBUS current is higher than IBUS_UCP_R threshold and Soft-Start Timeout. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	VBUS_SHORT_FLAG	0	RC	BUS_SCP Flag Bit 0 = No BUS_SCP (default) 1 = BUS_SCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	VBUS_ERRHI_FLAG	0	RC	VBUS High Voltage Fault Flag Bit 0 = No VBUS high voltage fault (default) 1 = Device in VBUS high voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	VBUS_ERRLO_FLAG	0	RC	VBUS Low Voltage Fault Flag Bit 0 = No VBUS low voltage fault (default) 1 = Device in VBUS low voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	RVS_SSOK_FLAG	0	RC	Reverse Mode Soft-Start OK Flag Bit 0 = No SS OK (default) 1 = SS OK and VBUS or VAC can load current. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	Reserved	0	RC	Reserved	N/A

REGISTER MAPS (continued)

REG0x17: FLAG 3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	POR_FLAG	0	RC	POR Flag Bit 0 = Normal 1 = POR signal rising edge detected. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	VAC_OVP_FLAG	0	RC	VAC OVP Flag Bit 0 = No VAC OVP (default) 1 = VAC_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	IBUS_UCP_FALL_FLAG	0	RC	IBUS_UCP_FALL Flag Bit 0 = No IBUS_UCP_FALL (default) 1 = IBUS_UCP_FALL fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	IBUS_OCP_FLAG	0	RC	IBUS_OCP Flag Bit 0 = No IBUS_OCP (default) 1 = IBUS_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	IBAT_OCP_FLAG	0	RC	IBAT_OCP Flag Bit 0 = No IBAT_OCP (default) 1 = IBAT_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	VBUS_OVP_FLAG	0	RC	VBUS_OVP Flag Bit 0 = No VBUS_OVP (default) 1 = VBUS_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	VOUT_OVP_FLAG	0	RC	VOUT_OVP Flag Bit 0 = No VOUT_OVP (default) 1 = VOUT_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	VBAT_OVP_FLAG	0	RC	VBAT_OVP Flag Bit 0 = No VBAT_OVP (default) 1 = VBAT_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x18: FLAG 4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	RC	Reserved	N/A
D[5]	PMID2VOUT_UVP_FLAG	0	RC	PMID2VOUT_UVP Flag Bit 0 = No PMID2VOUT_UVP (default) 1 = PMID2VOUT_UVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	PMID2VOUT_OVP_FLAG	0	RC	PMID2VOUT_OVP Flag Bit 0 = No PMID2VOUT_OVP (default) 1 = PMID2VOUT_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	TSHUT_FLAG	0	RC	TSHUT Flag Bit 0 = No TSHUT (default) 1 = TSHUT fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	TSBAT_FLT_FLAG	0	RC	TSBAT_FLT Flag Bit 0 = No TSBAT_FLT (default) 1 = TSBAT_FLT fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	SS_TIMEOUT_FLAG	0	RC	SS_TIMEOUT Flag Bit 0 = No soft-start timeout event (default) 1 = Soft-start timeout event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	WD_TIMEOUT_FLAG	0	RC	WD_TIMEOUT Flag Bit 0 = No watchdog timeout event (default) 1 = Watchdog timeout event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REG0x19: MASK 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CP_SWITCHING_MASK	0	R/W	Mask CP_SWITCHING Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[6]	CONV_OCP_MASK	0	R/W	Mask CONV_OCP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[5]	PEAK_OCP_RVS_MASK	0	R/W	Mask PEAK_OCP_RVS Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[4]	VOUT_TH_REV_EN_MASK	0	R/W	Mask VOUT_TH_REV_EN Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[3]	VOUT_TH_CHG_EN_MASK	0	R/W	Mask VOUT_TH_CHG_EN Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[2]	VBUS_PRESENT_MASK	0	R/W	Mask VBUS_PRESENT Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[1]	VAC_INSERT_MASK	0	R/W	Mask VAC_INSERT Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[0]	VOUT_INSERT_MASK	0	R/W	Mask VOUT_INSERT Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST

REGISTER MAPS (continued)**REG0x1A: MASK 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_DONE_MASK	0	R/W	Mask ADC_DONE Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[6]	PIN_DIAG_FAIL_MASK	0	R/W	Mask PIN_DIAG_FAIL Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[5]	IBUS_UCP_RISE_MASK	0	R/W	Mask IBUS_UCP_RISE Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[4]	VBUS_SHORT_MASK	0	R/W	Mask VBUS_SHORT Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[3]	VBUS_ERRHI_MASK	0	R/W	Mask VBUS_ERRHI Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[2]	VBUS_ERRLO_MASK	0	R/W	Mask VBUS_ERRLO Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[1]	RVS_SSOK_MASK	0	R/W	MASK RVS_SSOK Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[0]	Reserved	0	R/W	Reserved	REG_RST

REG0x1B: MASK 3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	REG_RST
D[6]	VACOV_P_MASK	0	R/W	MASK VACOV_P Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[5]	IBUS_UCP_FALL_MASK	0	R/W	MASK IBUS_UCP_FALL Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[4]	IBUS_OCP_MASK	0	R/W	MASK IBUS_OCP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[3]	IBAT_OCP_MASK	0	R/W	MASK IBAT_OCP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[2]	VBUS_OVP_MASK	0	R/W	MASK VBUS_OVP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[1]	VOUT_OVP_MASK	0	R/W	MASK VOUT_OVP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[0]	VBAT_OVP_MASK	0	R/W	MASK VBAT_OVP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST

REGISTER MAPS (continued)**REG0x1C: MASK 4 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R/W	Reserved	REG_RST
D[5]	PMID2VOUT_UVP_MASK	0	R/W	MASK PMID2VOUT_UVP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[4]	PMID2VOUT_OVP_MASK	0	R/W	MASK PMID2VOUT_OVP Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[3]	TSHUT_MASK	0	R/W	MASK TSHUT Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[2]	TSBAT_FLT_MASK	0	R/W	MASK TSBAT_FLT Fault Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[1]	SS_TIMEOUT_MASK	0	R/W	MASK SS_TIMEOUT Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST
D[0]	WD_TIMEOUT_MASK	0	R/W	MASK WD_TIMEOUT Event Interrupt 0 = Not Masked (default) 1 = Masked	REG_RST

REG0x1D: ADC_CONTROL 1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Conversion Enable 0 = Disabled (default) 1 = Enabled Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0.	REG_RST or Watchdog
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = 1 shot	REG_RST
D[5]	ADC_AVG	0	R/W	ADC Average Enable Bit 0 = Single value (default) 1 = Running average	REG_RST
D[4]	ADC_AVG_INIT	0	R/W	ADC Average Initial Value Setting Bit 0 = Start average using the existing register value (default) 1 = Start average using a new conversion	REG_RST
D[3:0]	Reserved	0000	R/W	Reserved	REG_RST

REGISTER MAPS (continued)**REG0x1E: ADC_CONTROL 2 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[6]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[5]	VAC_ADC_DIS	0	R/W	VAC ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[4]	VOUT_ADC_DIS	0	R/W	VOUT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[3]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[2]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[1]	TSBAT_ADC_DIS	0	R/W	TSBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[0]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control 0 = Enable (default) 1 = Disable	REG_RST

REG0x1F: IBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBUS_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC IBUS Data (resolution: 2.5mA, range: 0A - 10.24A) MSB<3:0>: 5120mA, 2560mA, 1280mA, 640mA	N/A

REG0x20: IBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC IBUS Data (resolution: 2.5mA, range: 0A - 10.24A) LSB<7:0>: 320mA, 160mA, 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA	N/A

REG0x21: VBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBUS_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC VBUS Data (resolution: 3.75mV, range: 0V - 14V) MSB<3:0>: 7680mV, 3840mV, 1920mV, 960mV	N/A

REGISTER MAPS (continued)**REG0x22: VBUS_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC VBUS Data (resolution: 3.75mV, range: 0V - 14V) LSB<7:0>: 480mV, 240mV, 120mV, 60mV, 30mV, 15mV, 7.5mV, 3.75mV	N/A

REG0x23: VAC_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VAC_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC VAC Data (resolution: 5mV, range: 0V - 14V) MSB<3:0>: 10240mV, 5120mV, 2560mV, 1280mV	N/A

REG0x24: VAC_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC VAC Data (resolution: 5mV, range: 0V - 14V) LSB<7:0>: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV, 5mV	N/A

REG0x25: VOUT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VOUT_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC VOUT Data (resolution: 1.25mV, range: 0V - 5.12V) MSB<3:0>: 2560mV, 1280mV, 640mV, 320mV	N/A

REG0x26: VOUT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC VOUT Data (resolution: 1.25mV, range: 0V - 5.12V) LSB<7:0>: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	N/A

REG0x27: VBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC VBAT Data (resolution: 1.25mV, range: 0V - 5.12V) MSB<3:0>: 2560mV, 1280mV, 640mV, 320mV	N/A

REGISTER MAPS (continued)**REG0x28: VBAT_ADC0 Register [reset = 0x00]**

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC VBAT Data (resolution: 1.25mV, range: 0V - 5.12V) LSB<7:0>: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	N/A

REG0x29: IBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBAT_ADC[11:8]	0000	R	High 4 Bits of the 12-Bit ADC IBAT Data (resolution: 3.125mA, range: 0A - 12.8A) MSB<3:0>: 6400mA, 3200mA, 1600mA, 800mA	N/A

REG0x2A: IBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC IBAT Data (resolution: 3.125mA, range: 0A - 12.8A) LSB<7:0>: 400mA, 200mA, 100mA, 50mA, 25mA, 12.5mA, 6.25mA, 3.125mA	N/A

REG0x2B: TSBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	TSBAT_ADC[11:8]	0000	R	Higher 4 bits of the 12-Bit ADC TSBAT Data (resolution: 0.44mV, range: 0V - 1.8V) MSB<3:0>: 901.12mV, 450.56mV, 225.28mV, 112.64mV Range: 0V - 1.8V	N/A

REG0x2C: TSBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_ADC[7:0]	00000000	R	Low Byte of the 12-Bit ADC TSBAT Data (resolution: 0.44mV, range: 0V - 1.8V) LSB<7:0>: 56.32mV, 28.16mV, 14.08mV, 7.04mV, 3.52mV, 1.76mV, 0.88mV, 0.44mV	N/A

REG0x2D: TDIE_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000000	R	Reserved	N/A
D[0]	TDIE_ADC[8]	0	R	Higher 1 bit of the 9-Bit ADC TDIE Data (resolution: 0.5°C, range: 0°C - 150°C) MSB<0>: 128°C	N/A

REG0x2E: TDIE_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	00000000	R	Low Byte of the 9-Bit ADC TDIE Data (resolution: 0.5°C, range: 0°C - 150°C) LSB<7:0>: 64°C, 32°C, 16°C, 8°C, 4°C, 2°C, 1°C, 0.5°C	N/A

APPLICATION INFORMATION

Input Capacitors (C_{VAC}, C_{VBUS} and C_{PMID})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage.
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For C_{VAC} and C_{VBUS}, use low ESR bypass ceramic capacitors to place close to the VAC/VBUS and GND pins respectively. The C_{PMID} is determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, a 10μF or larger X5R ceramic capacitors are sufficient to meet the C_{PMID} requirements of two channels. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFETs (ACFET-RBFET)

The maximum recommended input range is 12V. If the supplied VAC voltage is above 12V, two sets of back-to-back N-channel OVPFETs are recommended between the adapter inputs and the SGM41608. Choose a low R_{DS(on)} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors (C_{FLY})

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to different DC voltages according to the operation mode. To trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of the V_{VOUT} as a good starting point. The C_{FLY} for each channel can be calculated by Equation 10:

$$C_{FLY} = \frac{I_{BAT}}{4f_{SW}V_{CFLY_RPP}} = \frac{I_{BAT}}{8\%f_{SW}V_{DC_CFLY}} \quad (10)$$

where I_{BAT} is the charging current and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

Choosing a too small capacitor for C_{FLY} results in lower efficiency and high output voltage/current ripples. However choosing a too large C_{FLY} only provides minor efficiency and output ripple improvements.

The default switching frequency is f_{SW} = 800kHz. It can be adjusted by FSW_SET[3:0] bits in REG0x0B. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Output Capacitor (C_{VOUT})

C_{VOUT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{VOUT} value results in less output voltage ripple, but due to the dual-channel operation, the C_{VOUT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{VOUT} as given in Equation 11:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT_RPP}} \quad (11)$$

where t_{DEAD} is the dead time between the two channels and V_{VOUT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{VOUT}.

C_{VOUT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically a 22μF, X5R or better grade ceramic capacitors placed close to the VOUT and GND pins provide stable performance of two channels.

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41608. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to GND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. C_{FLY} pours of the two channels should be as symmetrical as possible.
7. Connect and reference all power signals to the GND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.

The reference layout is shown in Figure 14.

APPLICATION INFORMATION (continued)

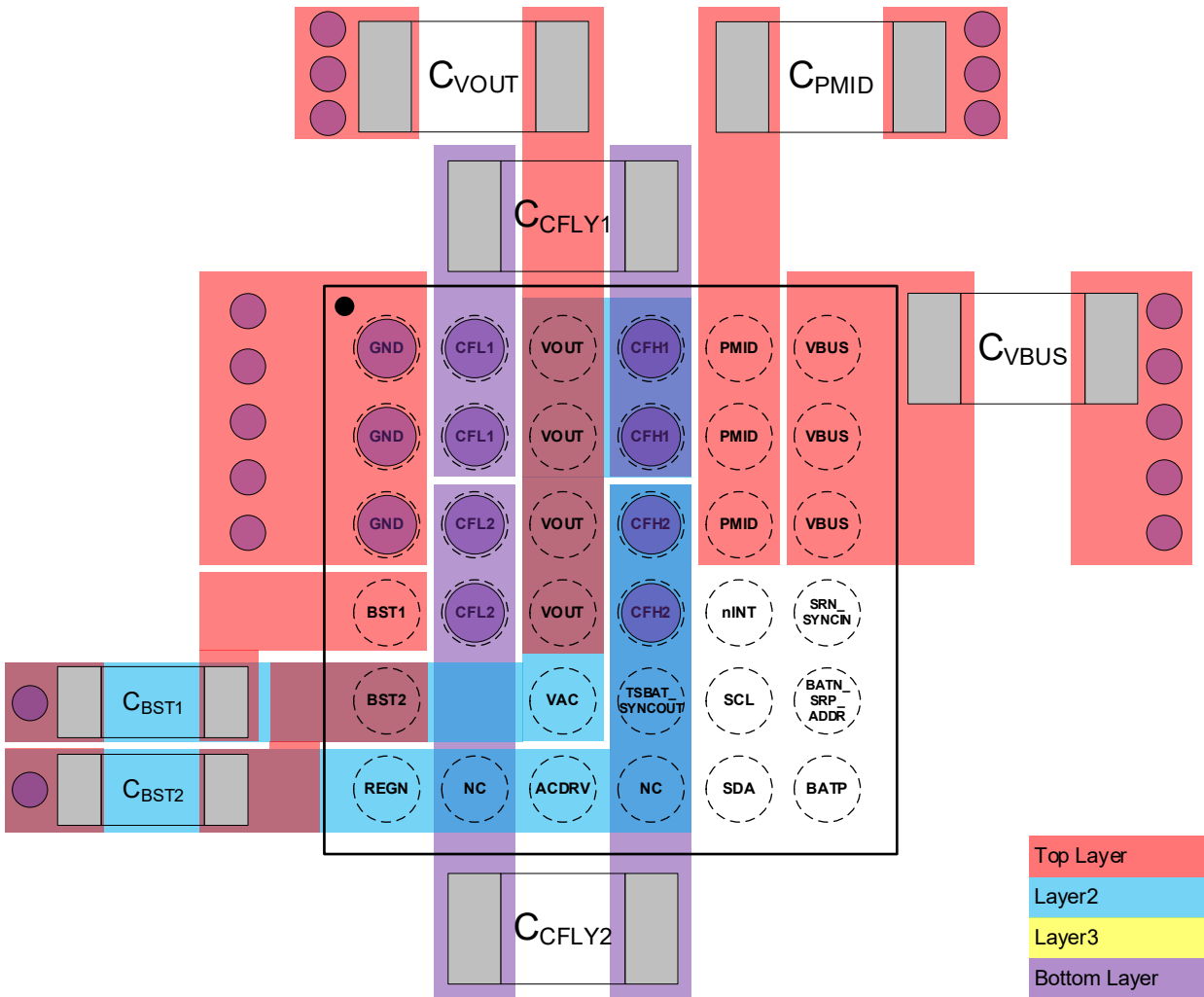


Figure 14. Reference Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (MARCH 2026)

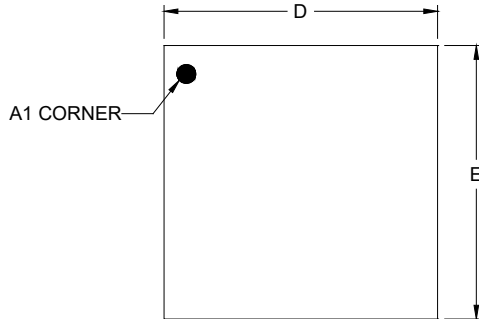
Page

Changed from product preview to production data All

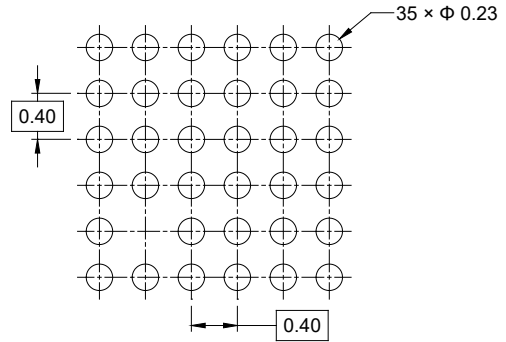
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

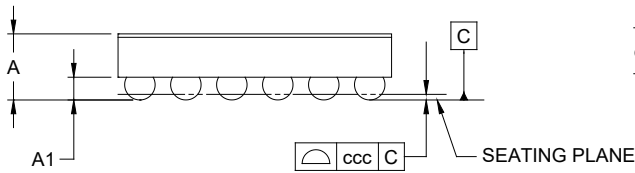
WLCSP-2.38×2.38-35B



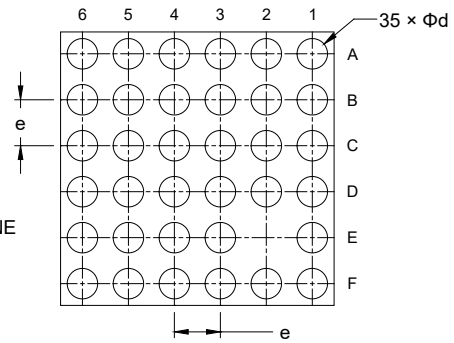
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

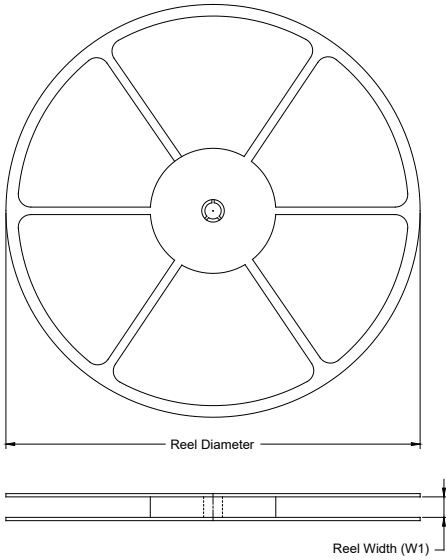
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.620
A1	0.178	-	0.218
D	2.350	-	2.410
E	2.350	-	2.410
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

NOTE: This drawing is subject to change without notice.

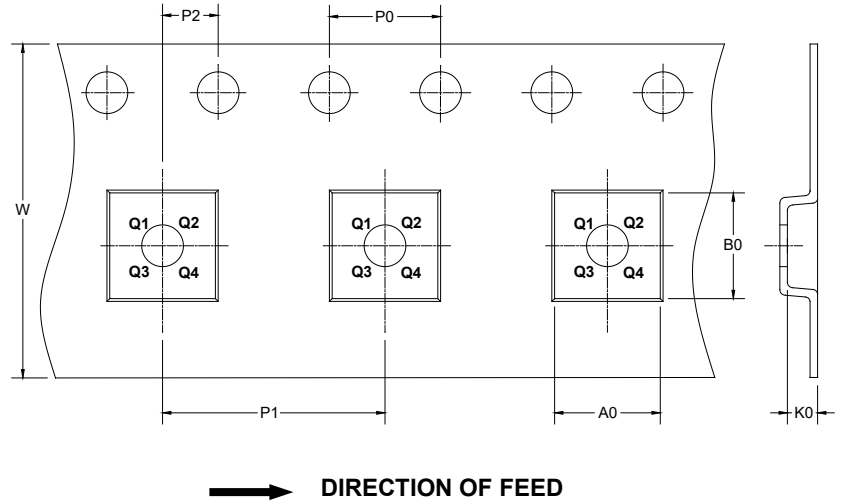
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

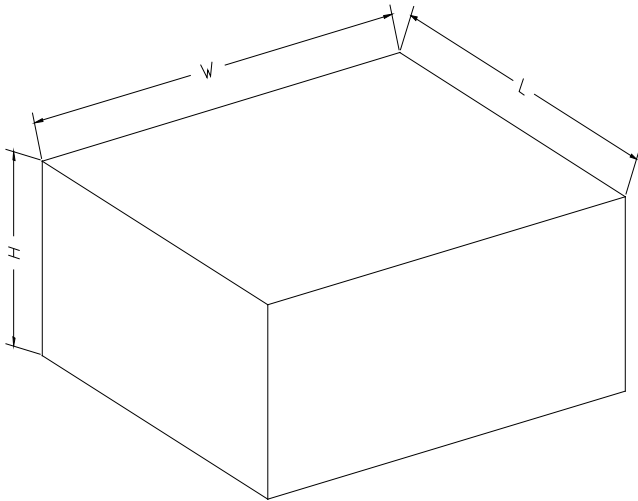
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.38×2.38-35B	7"	9.5	2.54	2.54	0.76	4.0	4.0	2.0	8.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

D00002