SGM61042
2.4V to 5.5V Input, 4A Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61042 is a high power density synchronous Buck converter, which are capable of delivering up to 4A continuous output current from 2.4V to 5.5V input voltage range. The device only consumes 5μA (TYP) quiescent current.

The device implements auto PFM mode operation to maximize the efficiency at light load condition. At moderate to heavy load, the device automatically switches to CCM operation with a 2.2MHz (TYP) switching frequency. Forced PWM (FPWM) is also available via the VSET/MODE pin for low output voltage ripple requirement.

The SGM61042 implements the COT control architecture that incorporates the benefits of fast load and line transient responses and low output voltage ripple, which is beneficial for RF and noise sensitive applications. The device features the hiccup short-circuit protection and thermal shutdown.

The SGM61042 is available in a Green TQFN-1.5×2.5-9L package.

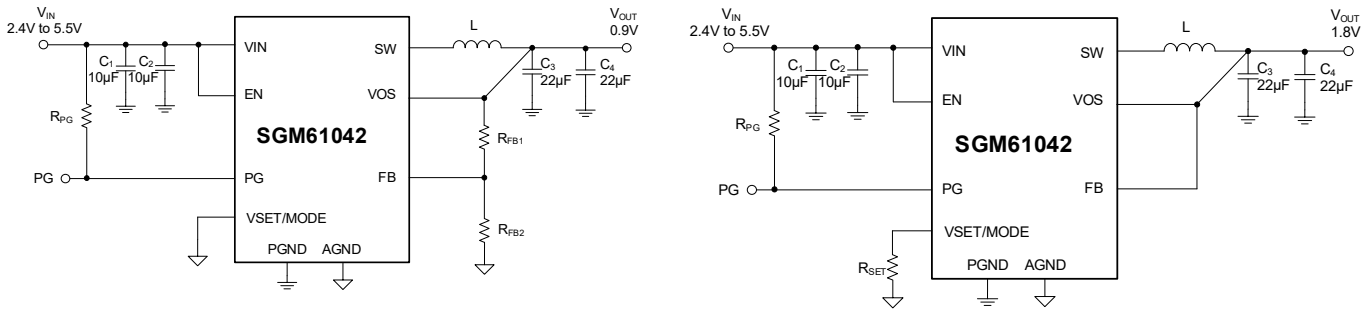
FEATURES

- **2.4V to 5.5V Input Voltage Range**
- **5μA (TYP) Quiescent Current**
- **2.2MHz (TYP) Switching Frequency**
- **14mΩ and 9.5mΩ Internal Power MOSFETs**
- **Fixed and Adjustable Output Voltage Options**
- **Forced PWM or Power-Save Mode**
- **4A Output Current**
- **Output Voltage Discharge**
- **Hiccup Short-Circuit Protection**
- **Power Good Indicator**
- **Thermal Shutdown**
- **COT-Control Topology for Fast Transient Response**
- **Available in a Green TQFN-1.5×2.5-9L Package**

APPLICATIONS

Core Supply for FPGAs, CPUs, ASICs or Video Chipsets
SSD
Optical Modules

SIMPLIFIED SCHEMATIC



Adjustable Output Voltage **Fixed Output Voltage**

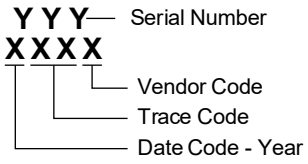
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61042	TQFN-1.5×2.5-9L	-40℃ to +125℃	SGM61042XTVY9G/TR	1QC XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, EN, VOS, FB, PG, VSET/MODE ..... -0.3V to 6V
SW, DC Voltage ..... -0.3V to V_{IN} + 0.3V
Sink Current at PG, I_{SINK_PG} 1mA
Package Thermal Resistance
TQFN-1.5×2.5-9L, θ_{JA} ..... 75.5℃/W
TQFN-1.5×2.5-9L, θ_{JB} ..... 6.6℃/W
TQFN-1.5×2.5-9L, θ_{JC} ..... 57.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 2.4V to 5.5V
Output Current, I_{OUT} ..... 4A (MAX)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

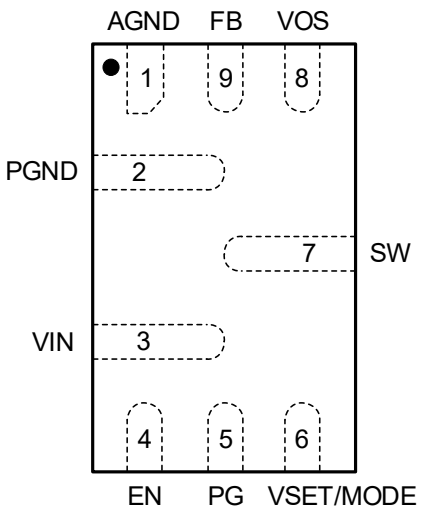
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-1.5×2.5-9L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	AGND	G	Analog Ground Pin.
2	PGND	G	Power Ground Pin.
3	VIN	P	Power Supply Input. Connect ceramic capacitors close to this pin and PGND.
4	EN	I	Device Enable Pin. Logic high on this pin enables the device, and logic low on this pin disables the device. Do not leave it floating.
5	PG	O	Power Good Open-Drain Output Pin. The pull-up resistor should be connected to the VIN. Leave it floating when not used.
6	VSET/MODE	I/O	Output Voltage Set or Mode Select Pin. In fixed output voltage applications, a resistor should be connected from the VSET/MODE pin to GND to program the output voltage. In adjustable output voltage applications, set VSET/MODE = high to enable forced PWM operation, or set VSET/MODE = low to enable power-save mode operation.
7	SW	P	Switching Node Pin. This pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
8	VOS	P	Output Voltage Sense Input. This pin should be connected to the output capacitors.
9	FB	I/O	Feedback Pin. In fixed output voltage applications, the pin should be connected to the output directly.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

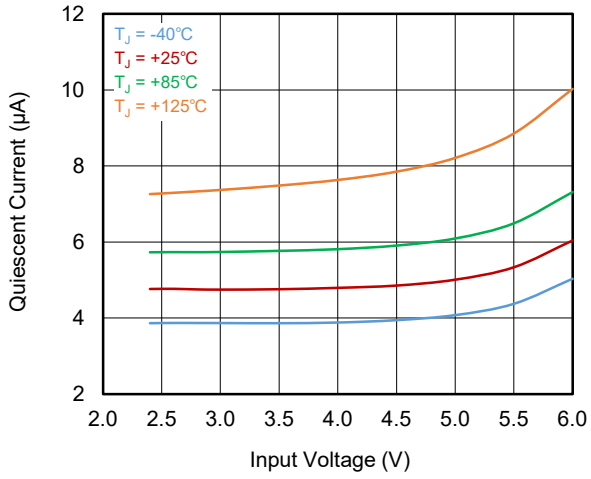
(T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃ and V_{IN} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Quiescent Current	I_Q	EN = high, no load, device not switching			5	17	μA
Operating Quiescent Current into VOS Pin	I_{Q_VOS}	EN = high, no load, device not switching, V_{VOS} = 1.8V			0.55		μA
Shutdown Current	I_{SD}	T_J = -40℃ to +85℃, EN = low			0.2	1	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.0	2.21	2.4	V
		V_{IN} falling		1.9	2.15	2.3	V
Thermal Shutdown Threshold	T_{SD}	T_J rising			155		℃
Thermal Shutdown Hysteresis		T_J falling			130		℃
Logic Interface							
High-Level Input Threshold Voltage at EN and VSET/MODE	V_{IH}			0.9			V
Low-Level Input Threshold Voltage at EN and VSET/MODE	V_{IL}					0.3	V
Input Leakage Current into EN Pin	I_{EN_LKG}				0.01	0.3	μA
Start-up, Power Good							
Enable Delay Time	t_{DLY}	Time from EN high to device starts switching, R_1 = 249kΩ		340	660	950	μs
Output Voltage Ramp Time	t_{RAMP}	Time from device starts switching to power good		0.4	1.6	2.8	ms
Power Good Lower Threshold	V_{PG}	V_{VOS} referenced to V_{OUT} nominal		85	91	97	%
Power Good Upper Threshold		V_{VOS} referenced to V_{OUT} nominal		105	111	117	%
Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA, PG pin version				0.36	V
Power Good Deglitch Delay	t_{PG_DLY}	Rising and falling edges			50		μs
Output							
Output Voltage Accuracy	V_{OUT}	T_J = 0℃ to +125℃, FPWM, no load	V_{OUT} ≥ 1.4V	-2.3		2.3	%
			1.4V > V_{OUT} ≥ 0.95V	-3.5		3.5	
			V_{OUT} < 0.95V	-5		5	
Feedback Voltage	V_{FB}	Adjustable voltage operation		582	600	618	mV
Input Leakage into FB Pin	I_{FB_LKG}	Adjustable voltage operation, V_{FB} = 0.6V			0.03	0.4	μA
Input Leakage Current into VOS Pin	I_{VOS_LKG}	Output discharge disabled, V_{VOS} = 1.8V			0	0.5	μA
Output Discharge Resistor	R_{DIS}				15		Ω
Load Regulation		V_{OUT} = 0.9V, FPWM			0.15		%/A
Power Switch							
High-side FET On-Resistance	R_{DSON}				14		mΩ
Low-side FET On-Resistance					9.5		mΩ
High-side FET Forward Current Limit	I_{LIM}			4.8	7.5	9.3	A
Low-side FET Forward Current Limit	I_{LIM}				5.6		A
Low-side FET Negative Current Limit	I_{LIM}				-3.2		A
PWM Switching Frequency	f_{SW}	I_{OUT} = 1A, V_{OUT} = 0.9V			2.2		MHz

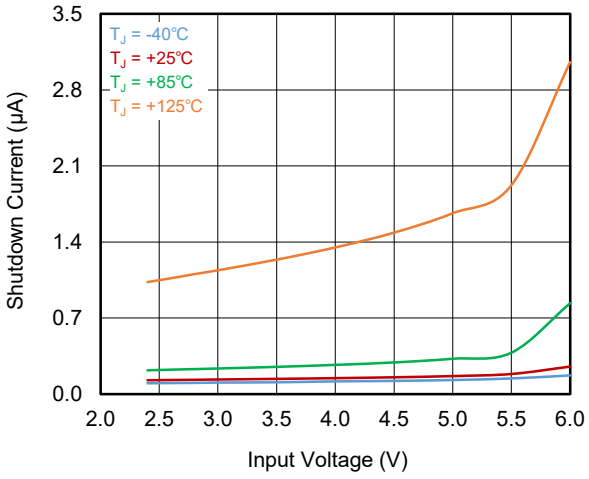
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 5.0V, V_{OUT} = 0.9V, unless otherwise noted.

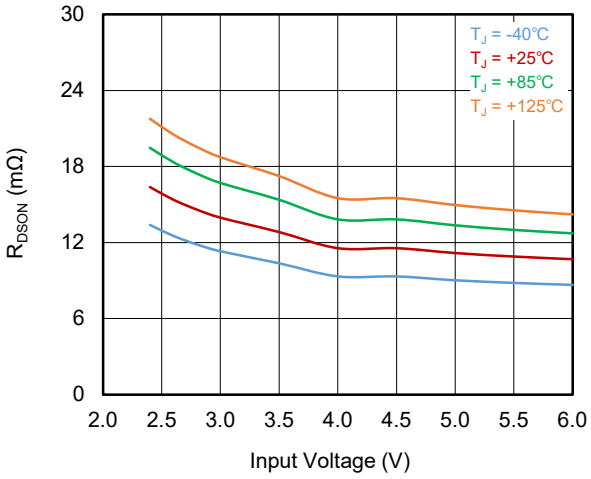
Quiescent Current vs. Input Voltage



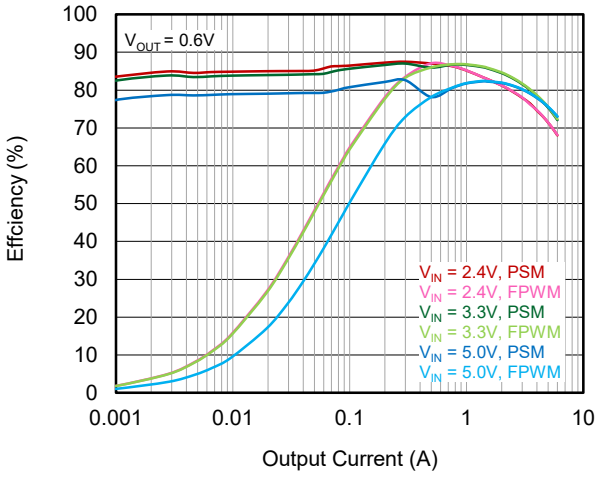
Shutdown Current vs. Input Voltage



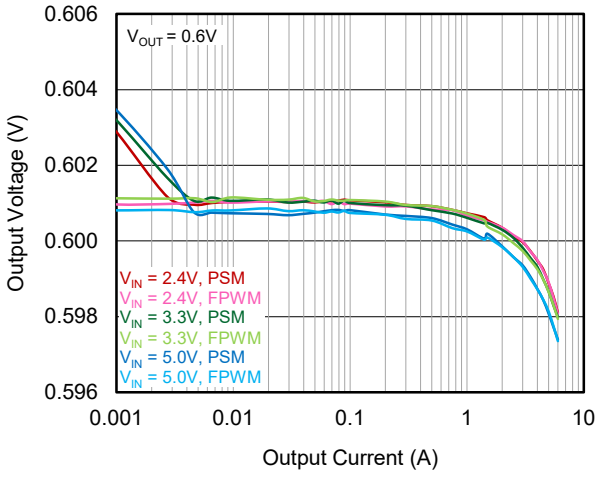
Low-side FET On-Resistance vs. Input Voltage



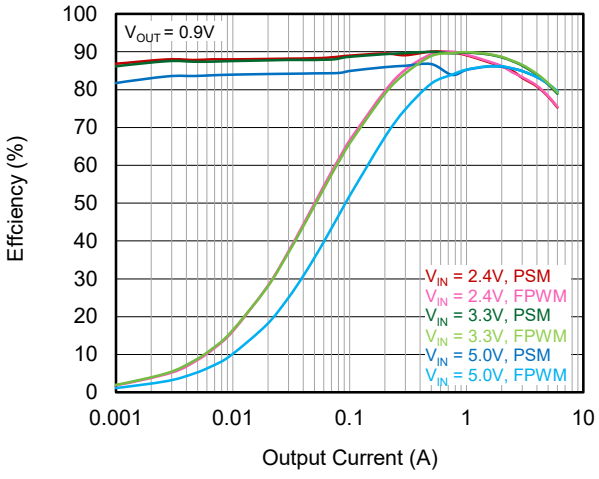
Efficiency vs. Output Current



Output Voltage vs. Output Current



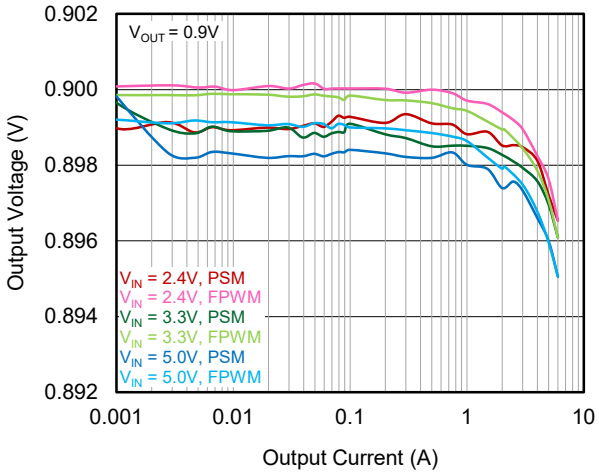
Efficiency vs. Output Current



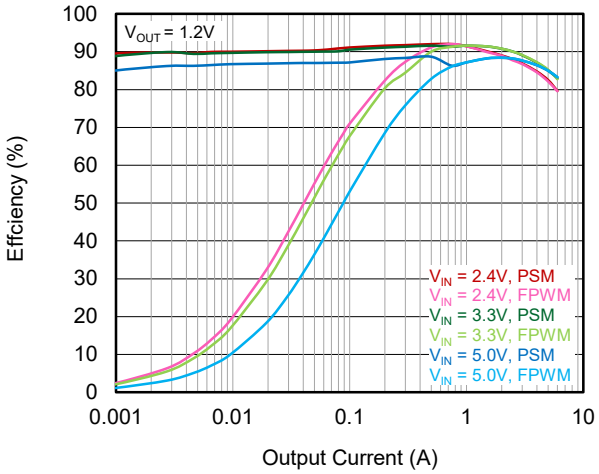
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 5.0V, V_{OUT} = 0.9V, unless otherwise noted.

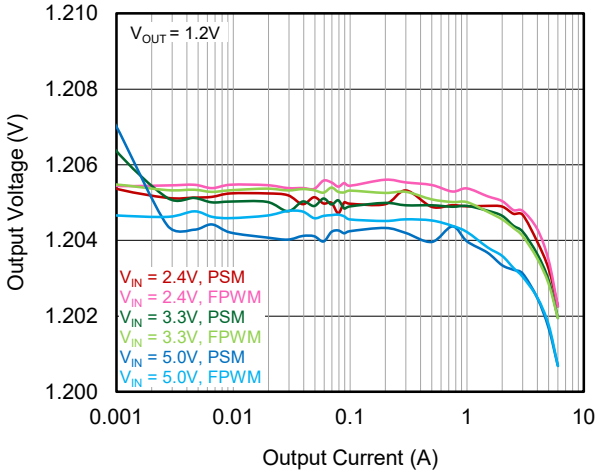
Output Voltage vs. Output Current



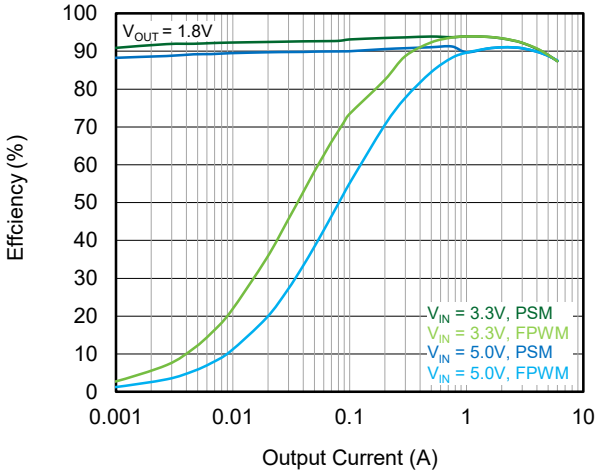
Efficiency vs. Output Current



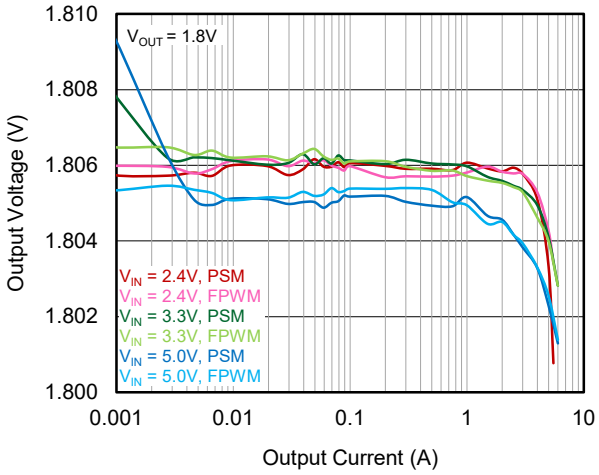
Output Voltage vs. Output Current



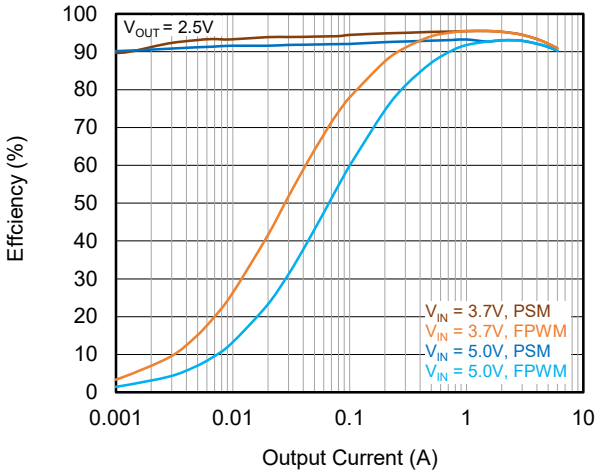
Efficiency vs. Output Current



Output Voltage vs. Output Current



Efficiency vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS

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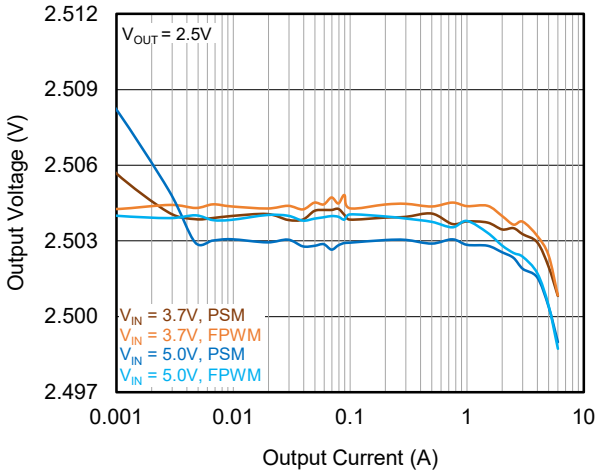
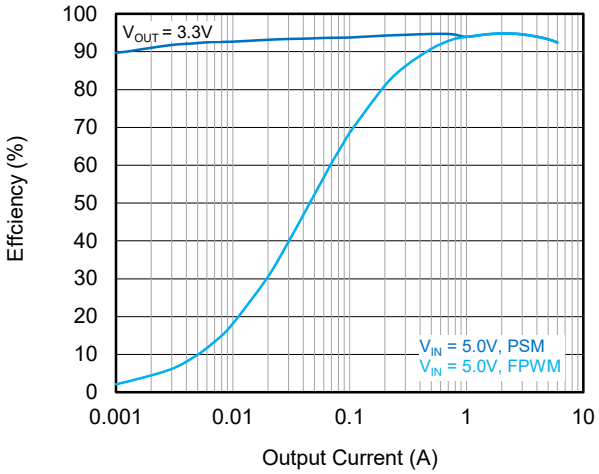
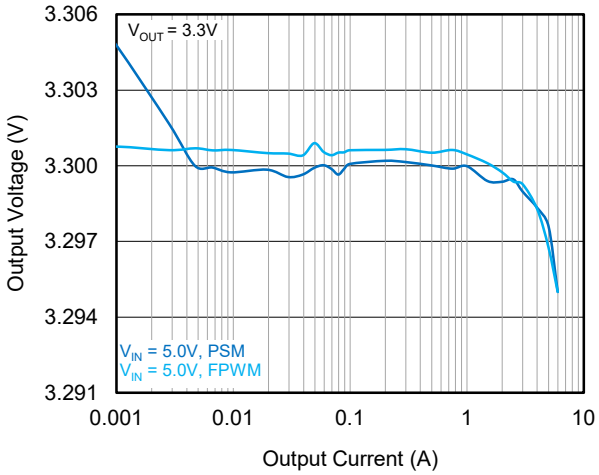
Output Voltage vs. Output Current



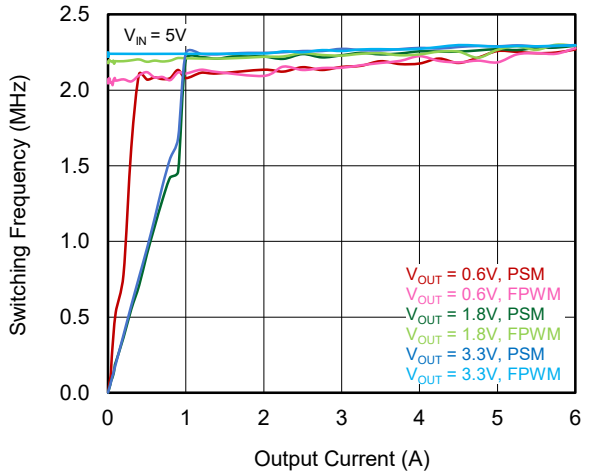
Efficiency vs. Output Current



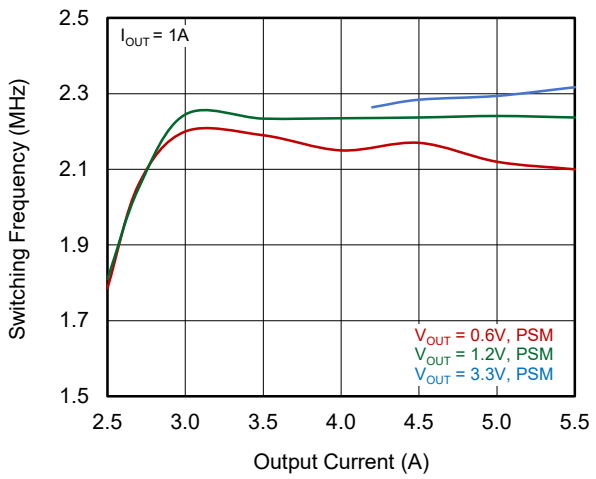
Output Voltage vs. Output Current



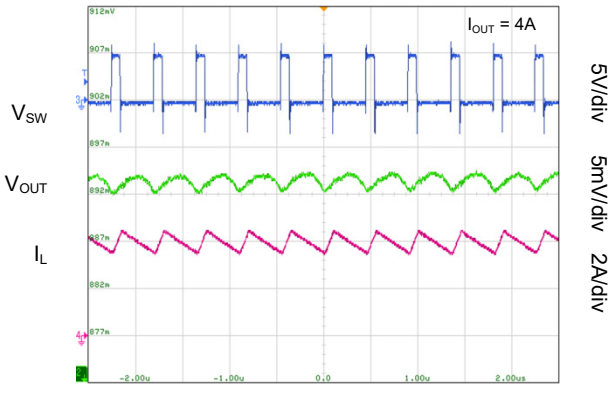
Switching Frequency vs. Output Current



Switching Frequency vs. Output Current



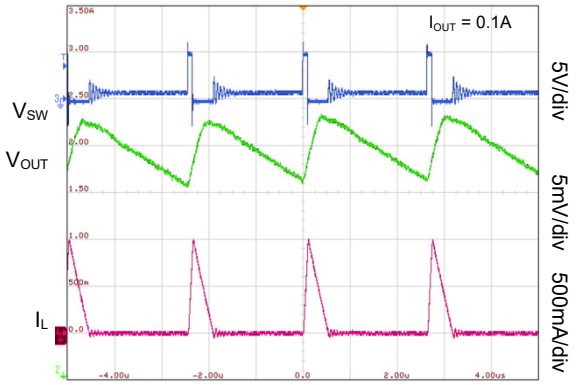
PWM Operation



TYPICAL PERFORMANCE CHARACTERISTICS

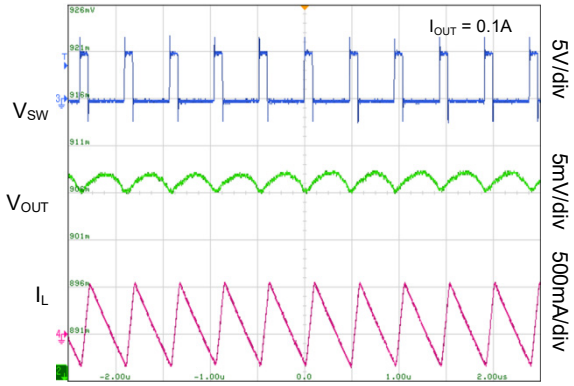
T_A = +25℃, V_{IN} = 5.0V, V_{OUT} = 0.9V, unless otherwise noted.

PSM Operation



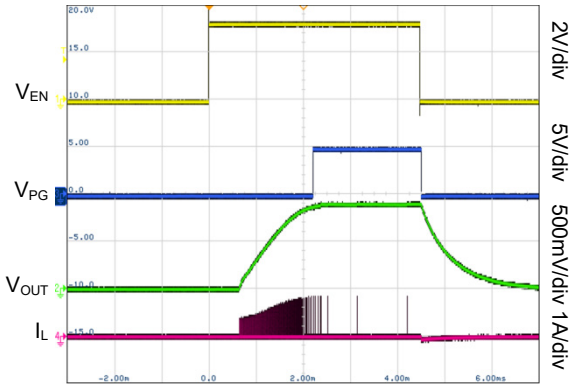
Time (1μs/div)

Forced PWM Operation



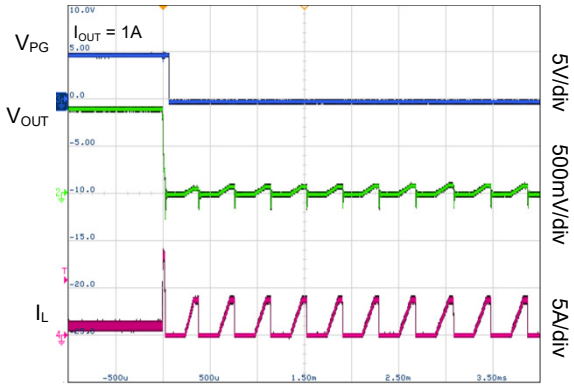
Time (500ns/div)

Startup with No Load



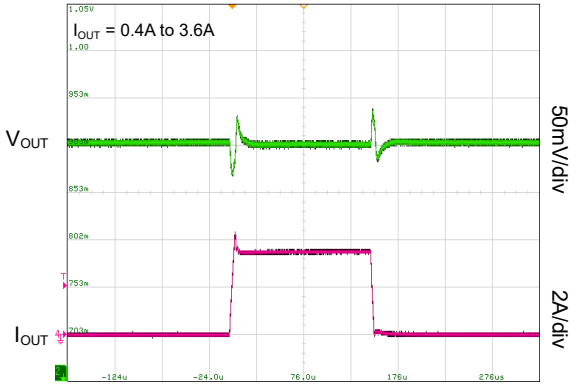
Time (1ms/div)

HICCUP Short-Circuit Protection



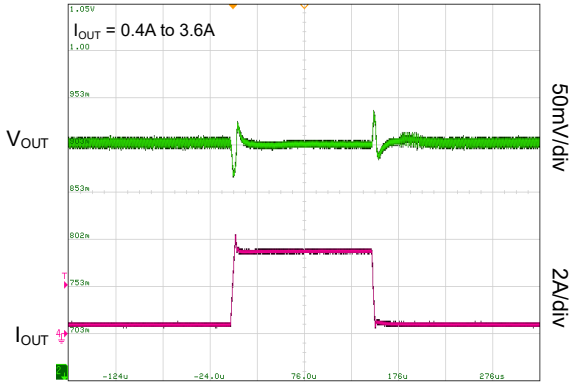
Time (500μs/div)

Load Transient - FPWM Operation



Time (50μs/div)

Load Transient - PSM Operation



Time (50μs/div)

FUNCTIONAL BLOCK DIAGRAM

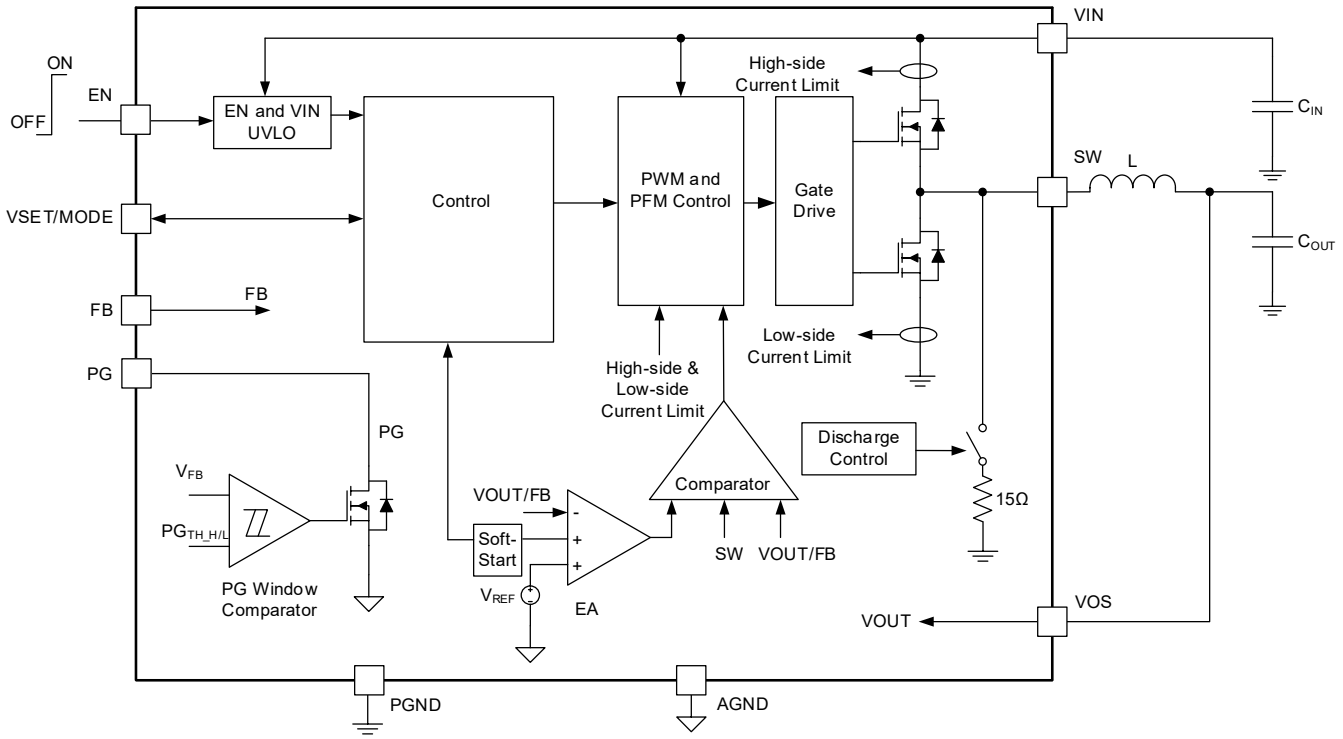


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61042 synchronous Buck converter consumes 5μA (TYP) quiescent current and offers up to 4A of DC load current. The device adopts the constant on-time (COT) architecture to provide superior load transient performance. In addition, the advanced control architecture offers excellent load and line regulation performance.

The device operates in PWM mode with 2.2MHz (TYP) fixed switching frequency at medium to heavy load. At light load, the device automatically operates in power-save mode to provide excellent light load efficiency. The device only requires two 22μF ceramic output capacitors to achieve minimal output voltage ripple at light load and heavy load.

Feature Description

Power-Save Mode

As the load current decreases, the inductor current reaches around 0A in a switching cycle, and the operation mode becomes discontinuous. The SGM61042 automatically enters power-save mode (PSM) in discontinuous mode. Equation 1 below calculates the device on-time in PSM.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 416ns \quad (1)$$

In order to maintain regulation, the output voltage is slightly increased above the programmed voltage. Adding more output capacitors will minimize the output voltage rise in PSM.

Forced PWM Mode

The SGM61042 is able to operate in FPWM mode to achieve fixed switching frequency and output ripple across the entire operating load range. FPWM operation is configurable via the resistor between VSET/MODE and GND pins (R_{SET} = 249kΩ) or the VSET/MODE voltage level (logic high).

Start-up

When the input voltage is above the UVLO rising threshold of 2.21V (TYP), toggling the enable pin to logic high to start up the device. Before the output voltage starts ramping up, the device has an enable delay of 660μs (TYP). During the enable delay, the device establishes the internal reference, and reads the resistor connected to the VSET/MODE pin to determine the start-up output voltage.

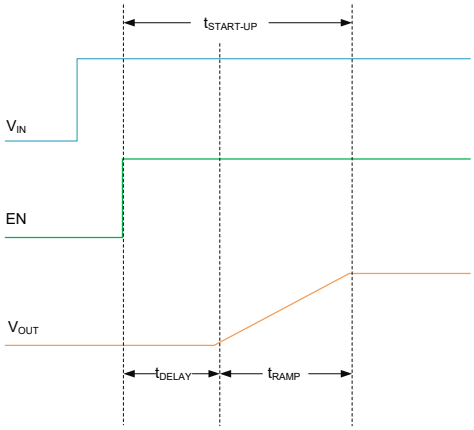


Figure 3. Start-up Sequence

The device initiates an internal soft-start when the enable delay finishes. The internal soft-start time is fixed to 1ms to ramp up the output voltage from 0V to the programmed output voltage. The soft-start mechanism effectively reduces the inrush current drawn from the input source, as well as providing a controlled output voltage rising ramp. For pre-biased output voltage start-up, the device starts up from the pre-biased voltage to the programmed output voltage.

Switch Current Limit and Hiccup Short-Circuit Protection

The device implements the over-current protection when the load exceeds the maximum allowed 4A to prevent excessive current drawn from battery type inputs. During an output short scenario or a saturated inductor, the inductor current will reach the current limit threshold. When current limit threshold is reached, the device turns off the high-side switch to terminate the inductor current from further increase, and the low-side switch turns on to ramp down the inductor current to the low-side switch current limit.

During the short-circuit event, as the output voltage drops below 0.3V, the current limit threshold is foldback to about 65% to prevent the device from excessive temperature rise. When the high-side switch current limit and low-side current limit are triggered for 64 consecutive times, the switching is terminated immediately to enter hiccup short protection mode of 128μs hiccup off-time. The device resumes operation after hiccup off-time with the soft-start sequence. If the over-current or short condition remains, the device remains in the hiccup cycle until the fault condition is removed.

DETAILED DESCRIPTION (continued)

Under-Voltage Lockout (UVLO)

The SGM61042 offers input under-voltage lockout to prevent false triggering with unstable input source. The device's UVLO rising voltage is 2.21V (TYP) and falling threshold is 2.15V (TYP). The device stops operation as soon as the input voltage drops below the falling threshold. The output voltage discharge is active when UVLO falling threshold is reached.

Thermal Warning and Shutdown

As the junction temperature exceeds above the T_{SD}, the device stops switching, enabling active discharge to discharge the output voltage and enters thermal shutdown. The device has a 25℃ (TYP) thermal shutdown hysteresis to allow the device to resume operation automatically with internal soft-start.

Enable and Disable (EN)

When the EN pin is toggled to logic low, power FETs are off as well as the internal control circuits. The device enters shutdown mode when EN pin is logic low. The EN pin supports 1.2V I/O logic with 0.9V rising threshold and 0.3V falling threshold.

Output Discharge

There are three scenarios to discharge the output voltage: EN pin is toggled to logic low, input voltage UVLO or device thermal shutdown. The internal discharge path discharges the output voltage through the SW pin to ground.

The output discharge function remains active as long as the input voltage is higher than 1V (TYP).

Output Voltage Setting and Mode Selection (VSET/MODE)

In start-up phase, during the enable delay period, the resistor is connected to VSET/MODE pin to program the output voltage as well as operation mode through an internal R2D (resistor to digital) converter. Table 1 lists the programmable options.

Table 1. Start-up Output Voltage

OUTPUT VOLTAGE (TYP)	RESISTOR OR LOGIC LEVEL (E96 SERIES, ±1% ACCURACY) AT VSET/MODE PIN	OPERATION MODE
Adjustable	249kΩ or logic high	FPWM
3.30V	205kΩ	PSM
2.5V	162kΩ	PSM
1.8V	133kΩ	PSM
1.5V	105kΩ	PSM
Reserved	86.6kΩ	PSM
1.35V	68.1kΩ	PSM
1.2V	56.2kΩ	PSM
1.1V	44.2kΩ	PSM
1.05V	36.5kΩ	PSM
1.00V	28.7kΩ	PSM
0.95V	23.7kΩ	PSM
0.90V	18.7kΩ	PSM
0.85V	15.4kΩ	PSM
0.80V	12.1kΩ	PSM
Adjustable	10kΩ or logic low	PSM

DETAILED DESCRIPTION (continued)

During the enable delay time, a current source is applied on the V_{SET} resistor. The internal ADC converts the voltage on the VSET/MODE pin to a digital signal to program the output voltage and operation mode. Once this R2D conversion completes, the current source is turned off to avoid unnecessary current consumption. Any capacitance higher than 30pF is not recommended to connect between the VSET/MODE pin to ground.

Power Good

The SGM61042 offers variants for an open-drain power good option, whose sink current is up to 1mA. The PG has a deglitch delay of 50μs (TYP). The PG pin remains High-Z status as long as the output voltage is within 91% to 111% of the programmed output voltage. PG status during different conditions is shown in Table 2.

Table 2. PG Function Table

DEVICE CONDITIONS		PG PIN
Enable	$0.91 \times V_{OUT\_NOM} \le V_{VOS} \le 1.11 \times V_{OUT\_NOM}$	Hi-Z
	$V_{VOS} < 0.91 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.11 \times V_{OUT\_NOM}$	Low
Shutdown	EN = low	Low
Thermal Shutdown	$T_J > T_{SD}$	Low
UVLO	$1.8V < V_{IN} < V_{UVLO}$	Low
Power Supply Removal	$V_{IN} < 1.8V$	Undefined

APPLICATION INFORMATION

Typical Application

Figure 4 below shows a typical schematic for a 0.9V output application of SGM61042 with a wide input voltage range.

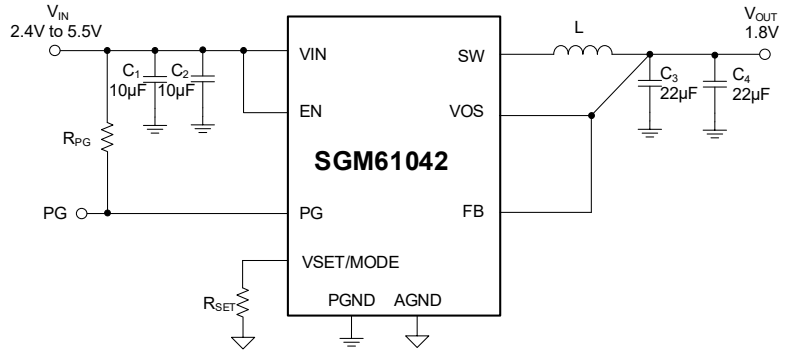


Figure 4. Fixed Output Voltage Typical Application Scheme

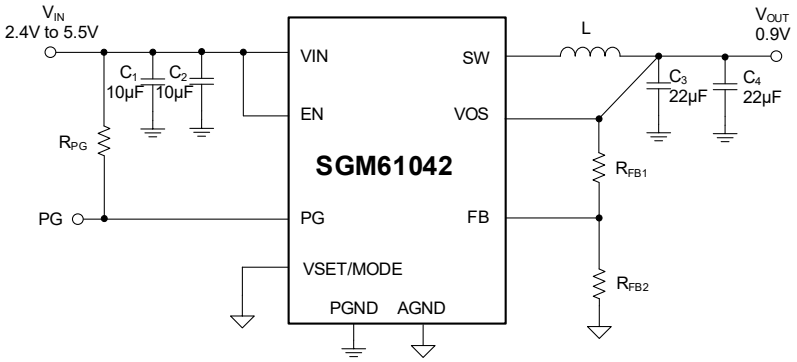


Figure 5. Adjustable Output Voltage Typical Application Scheme

Design Requirements

Table 3 below shows the operation conditions of this design example.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	2.4V to 5.5V
Output Voltage	0.9V
Maximum Output Current	4A

There are two ways shown in Figure 4 and Figure 5 to achieve the design requirements. Since the SGM61042 can be configured to either set a fixed output voltage through the VSET/MODE pin or set an adjustable voltage through the voltage divider resistors of the FB pin.

Table 4 lists the components used for the fixed output voltage application scheme shown in Figure 4.

Table 4. List of Components in Fixed Output Voltage Scheme

REFERENCE	DESCRIPTION	MANUFACTURER
C_1, C_2	10μF, ceramic capacitor, 6.3V, X7R, size 0603, CL10B106MQ8NRNC	Samsung
C_3, C_4	22μF, ceramic capacitor, 6.3V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L	0.22μH, power inductor, size 0806, FE201612E-R24M=P2/size 1616, XAL4020-221MEC	Murata/Coilcraft
R_{SET}	18.7kΩ, SMD resistor, size 0603	Std
R_{PG}	10kΩ, SMD resistor, size 0603	Std

APPLICATION INFORMATION (continued)

Table 5 lists the components used for the adjustable output voltage application scheme shown in Table 5.

Table 5. List of Components in Adjustable Output Voltage Scheme

REFERENCE	DESCRIPTION	MANUFACTURER
C_1, C_2	10μF, ceramic capacitor, 6.3V, X7R, size 0603, CL10B106MQ8NRNC	Samsung
C_3, C_4	22μF, ceramic capacitor, 6.3V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L	0.22μH, power inductor, size 0806, FE201612E-R24M=P2/size 1616, XAL4020-221MEC	Murata/Coilcraft
R_{FB1}	Depending on the output voltage and R_{FB2} selection, size 0603	Std
R_{FB2}	Depending on the output voltage, size 0603 (It is recommended to select the resistor from 50kΩ to 200kΩ.)	Std
R_{PG}	10kΩ, SMD resistor, size 0603	Std

Layout Guidelines

The layout of SGM61042 can refer to Figure 6. Note that AGND and PGND need to be connected at a single point.

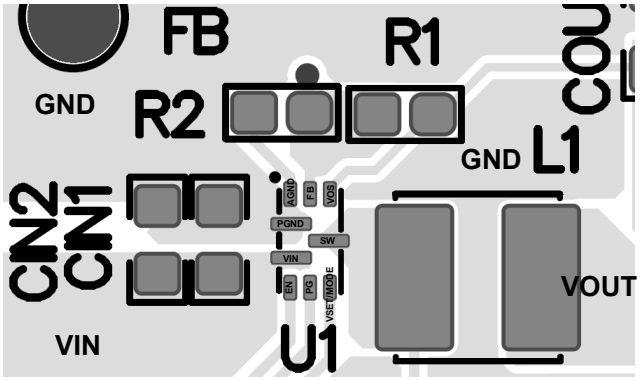


Figure 6. PCB Layout

REVISION HISTORY

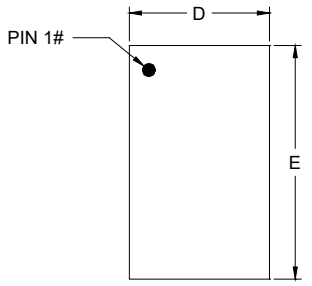
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from REV.A to REV.A.1 (FEBRUARY 2026)	Page
Typical Performance Characteristics, Table 1 and Application Information	8, 11, 13, 14

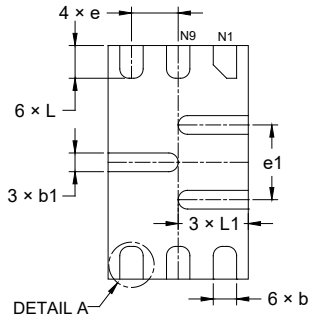
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

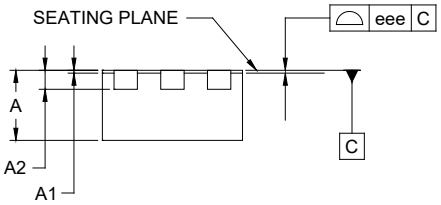
TQFN-1.5×2.5-9L



TOP VIEW

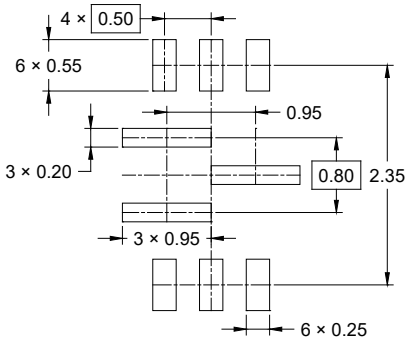


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



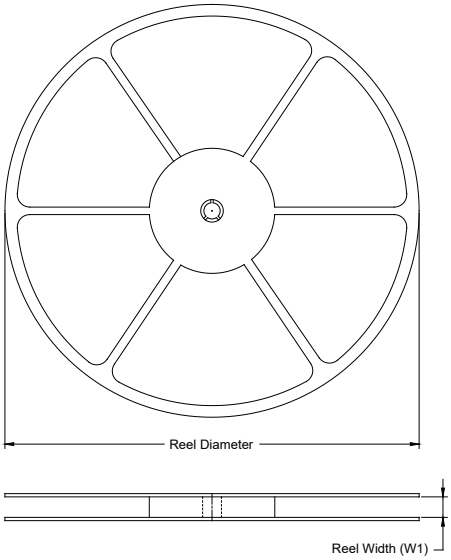
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
b1	0.150	-	0.250
D	1.400	-	1.600
E	2.400	-	2.600
e		0.500 BSC	
e1		0.800 BSC	
L	0.250	-	0.450
L1	0.650	-	0.850
eee		0.080	

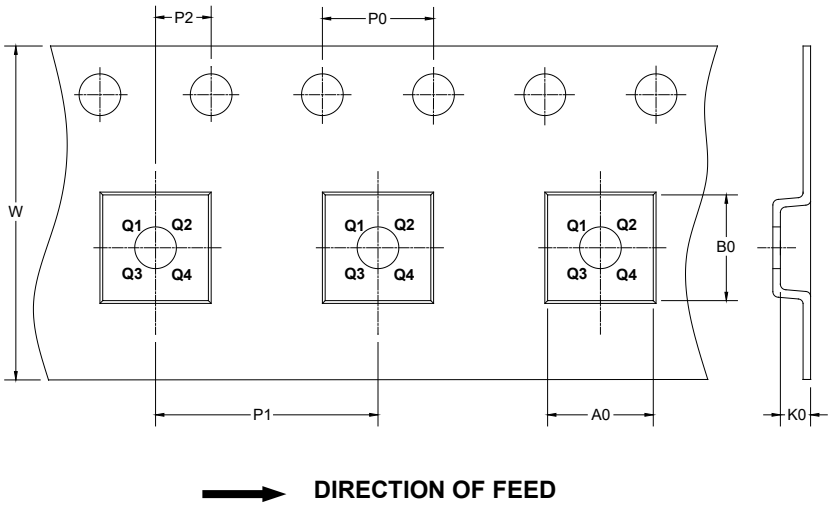
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



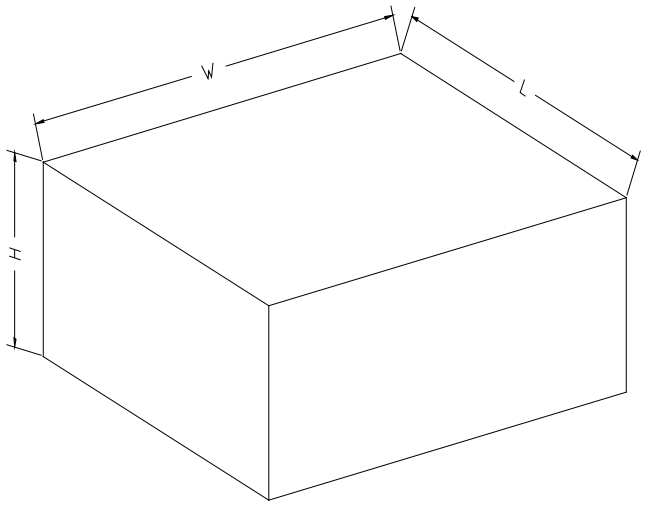
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-1.5×2.5-9L	7"	9.5	1.70	2.70	0.95	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002