SGM2217Q
Automotive, 1.5A, Low Dropout Positive Regulator

GENERAL DESCRIPTION

The SGM2217Q is a low noise, high current and low dropout voltage linear regulator. It is capable of supplying 1.5A output current with typical dropout voltage of 1.32V. The operating input voltage range is from 2.8V to 30V. The adjustable output voltage range is from 1.25V to 26V.

Other features include short-circuit current limit and thermal shutdown protection.

This device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM2217Q is available in a Green SOIC-8 (Exposed Pad) package. It operates over an operating temperature range of -40℃ to +125℃.

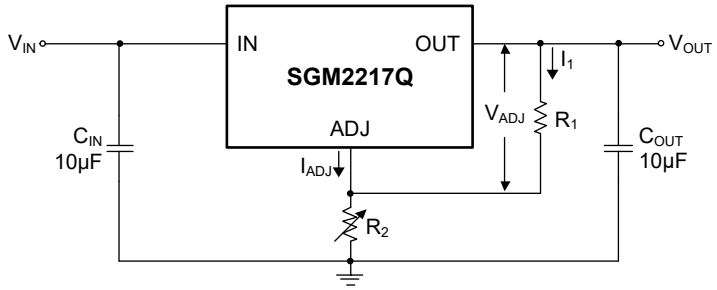
FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Wide Input Voltage Range: 2.8V to 30V**
- **Adjustable Output from 1.25V to 26V**
- **1.5A Output Current**
- **Low Dropout Voltage: 1.32V (TYP) at 1.5A**
- **Line Regulation: 0.05% (TYP)**
- **Load Regulation: 0.01% (TYP)**
- **Current Limiting and Thermal Protection**
- **Excellent Load and Line Transient Responses**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Automotive Application
Battery Chargers
Automotive Inverter

TYPICAL APPLICATION



$V_{OUT} = V_{ADJ} \times (1 + R_2/R_1) + I_{ADJ} \times R_2$, $I_1 = V_{ADJ}/R_1$
If I_{ADJ} is far less than I_1, $V_{OUT} = V_{ADJ} \times (1 + R_2/R_1)$.
Where V_{OUT} is output voltage and V_{ADJ} = 1.25V.

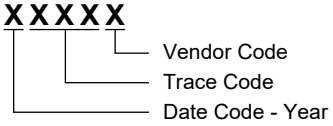
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2217Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2217QPS8G/TR	0FCPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input to Output Voltage 31V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA} ..... 38℃/W
SOIC-8 (Exposed Pad), θ_{JB} ..... 15℃/W
SOIC-8 (Exposed Pad), $\theta_{JC(TOP)}$ ..... 52℃/W
SOIC-8 (Exposed Pad), $\theta_{JC(BOT)}$ ..... 4.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.8V to 30V
Input Effective Capacitance, C_{IN} ..... 2.3μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 2.3μF to 100μF
Capacitor Effective Series Resistance, ESR ..... 1mΩ to 8Ω
Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

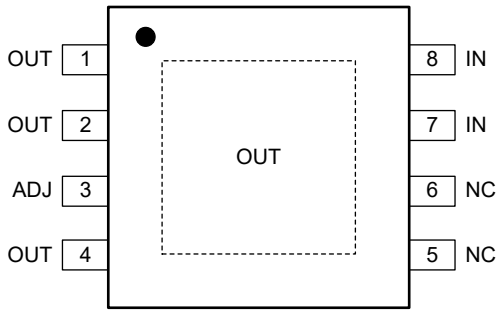
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM2217Q (TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2, 4	OUT	Regulator Output Pin. Pin 4 must be tied to the other OUT pins directly. It is recommended to use output capacitor with effective capacitance in the range of 2.3μF to 100μF with an ESR of 8Ω or less.
3	ADJ	Feedback Voltage Input Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
5, 6	NC	No Connection.
7, 8	IN	Input Supply Voltage Pin. It is recommended to use a 4.7μF or larger ceramic capacitor from IN pin to ground. This ceramic capacitor should be placed as close as possible to IN pin.
Exposed Pad	OUT	Exposed Pad. The exposed pad must be connected to OUT directly to improve thermal performance.

FUNCTIONAL BLOCK DIAGRAM

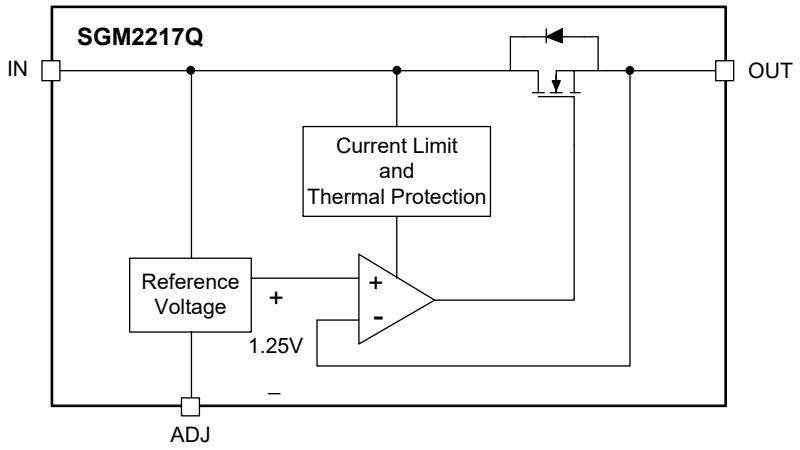


Figure 2. Internal Block Diagram

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 1.25V, C_{IN} = 10μF and C_{OUT} = 10μF (ceramic capacitor), T_J = -40℃ to +125℃ (1), typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	V_{ADJ}	I_{OUT} = 10mA, (V_{IN} - V_{OUT}) = 3V, T_J = +25℃	1.238	1.25	1.262	V
		I_{OUT} = 10mA to 1.5A (2), V_{IN} = (1.6V + V_{OUT}) to 30V	1.225		1.275	
ADJ Pin Current (3)	I_{ADJ}	I_{OUT} = 10mA, (V_{IN} - V_{OUT}) = 3V		8	20	μA
ADJ Pin Current Change	ΔI_{ADJ}	I_{OUT} = 10mA to 1.5A (2), (V_{IN} - V_{OUT}) = 1.6V to 15V		0.05	2	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	I_{OUT} = 10mA, V_{IN} = (1.6V + V_{OUT}) to 30V		0.05	0.2	%
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	I_{OUT} = 10mA to 1.5A, (V_{IN} - V_{OUT}) = 3V		0.01	0.2	%
Dropout Voltage	V_{DROP}	I_{OUT} = 1.5A, ΔV_{OUT} = 1%		1.32	1.6	V
Output Current Limit	I_{LIMIT}	(V_{IN} - V_{OUT}) = 5V, ΔV_{OUT} = 5%	1.52	2.9		A
		(V_{IN} - V_{OUT}) = 25V, V_{OUT} = 0V	0.04	0.26		
Minimum Load Current (4)	I_{OUT_MIN}	V_{IN} = 30V		3	10	mA
Turn-On Time	t_{ON}	I_{OUT} = 10mA, (V_{IN} - V_{OUT}) = 3V, from assertion of V_{IN} to V_{OUT} = 95% × $V_{OUT(NOM)}$		0.42	1	ms
Temperature Stability				0.5		%
Power Supply Rejection Ratio	PSRR	I_{OUT} = 1.5A, (V_{IN} - V_{OUT}) = 3V, ΔV_{RIPPLE} = $2V_{P-P}$, f_{RIPPLE} = 120Hz, C_{OUT} = 20μF		72		dB
Output Voltage Noise	e_n	I_{OUT} = 0.5A, (V_{IN} - V_{OUT}) = 3V, f = 10Hz to 10kHz		0.004		%
Thermal Regulation		30ms Pulse, T_J = +25℃		0.01	0.05	%/W
Thermal Shutdown Temperature	T_{SHDN}			180		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}			20		℃

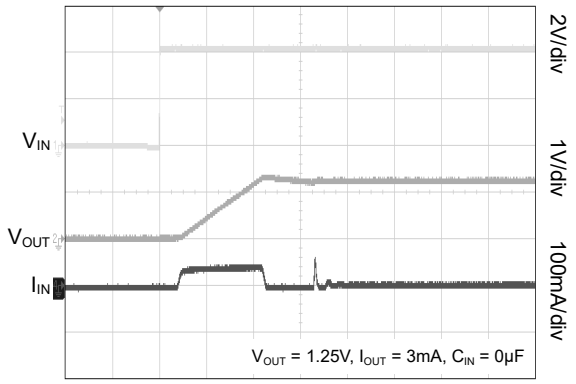
NOTES:

1. Tested under pulse load conditions, so $T_J \approx T_A$.
2. Output current limit is a function of input-to-output voltage. See short circuit current curve for available output current at the input-to-output differential.
3. See Figure 1, $V_{OUT} = V_{ADJ} \times (1 + R_2/R_1) + I_{ADJ} \times R_2$, $I_1 = V_{ADJ}/R_1$. To minimize the voltage error introduced by I_{ADJ}, choose an appropriate value for R_1.
4. The minimum output current required to maintain regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

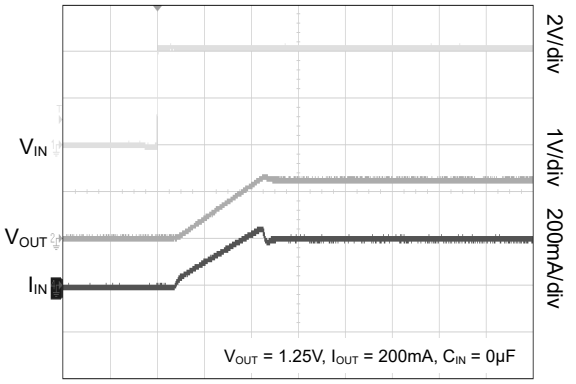
T_J = +25℃, (V_{IN} - V_{OUT}) = 3V, C_{IN} = C_{OUT} = 10μF (ceramic capacitor), unless otherwise noted.

VIN Power-Up Output Waveform



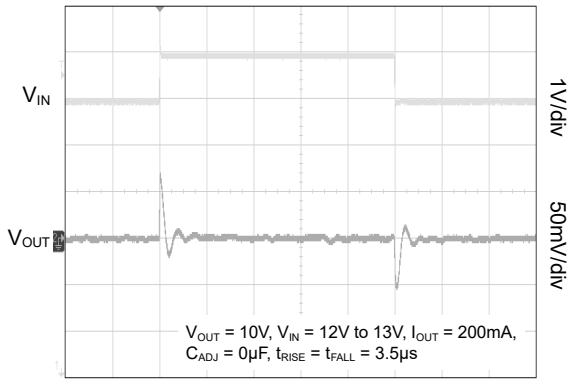
Time (200μs/div)

VIN Power-Up Output Waveform



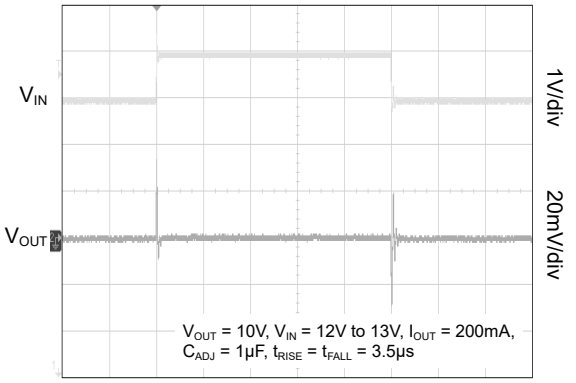
Time (200μs/div)

Line Transient Response



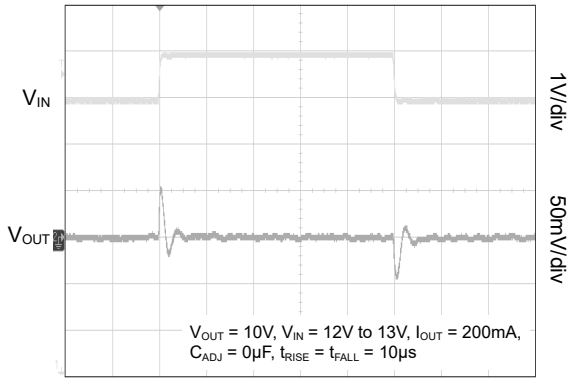
Time (100μs/div)

Line Transient Response



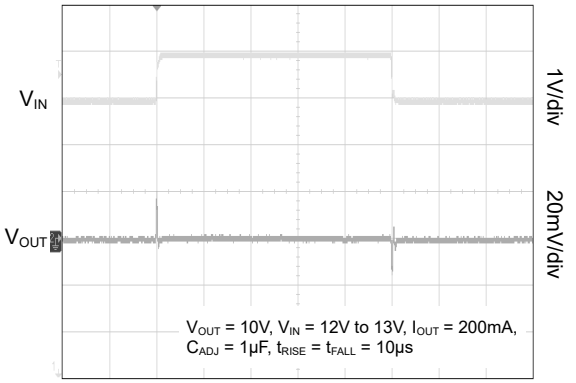
Time (100μs/div)

Line Transient Response



Time (100μs/div)

Line Transient Response

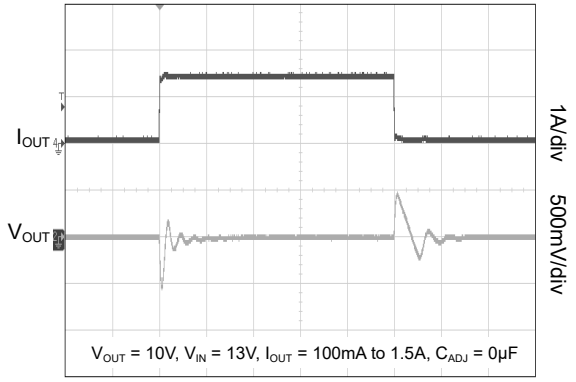


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

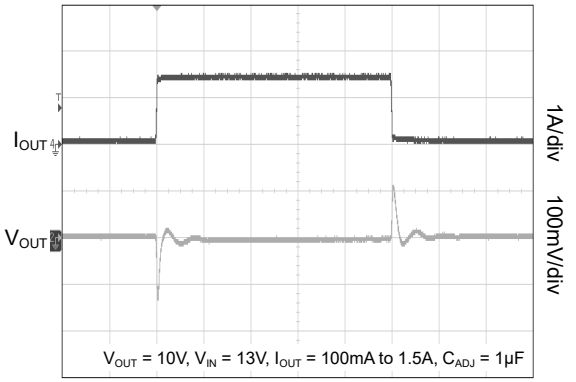
T_J = +25℃, (V_{IN} - V_{OUT}) = 3V, C_{IN} = C_{OUT} = 10μF (ceramic capacitor), unless otherwise noted.

Load Transient Response



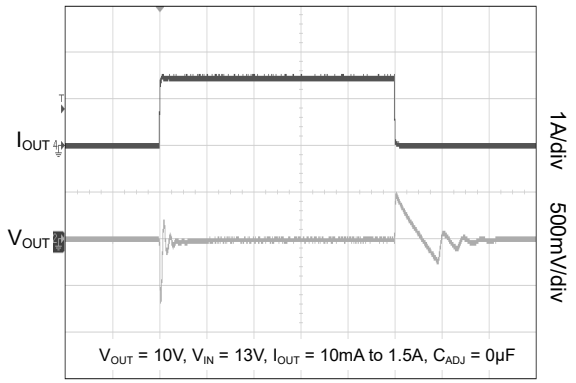
Time (100μs/div)

Load Transient Response



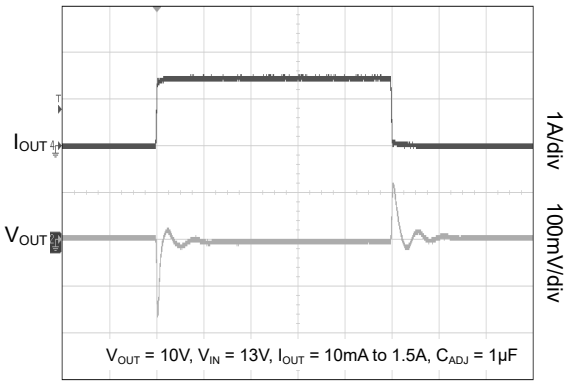
Time (50μs/div)

Load Transient Response



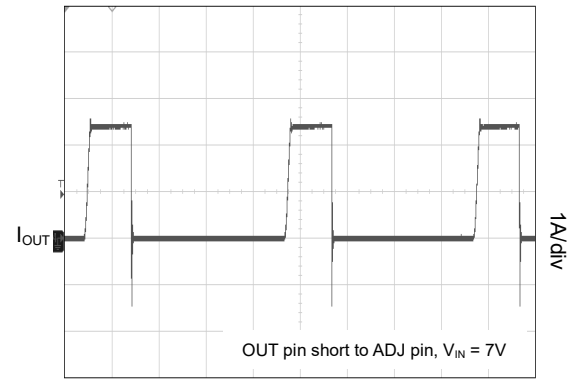
Time (200μs/div)

Load Transient Response



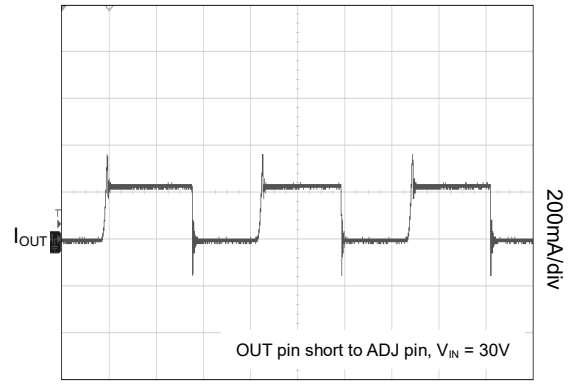
Time (50μs/div)

Thermal Protection



Time (500μs/div)

Thermal Protection

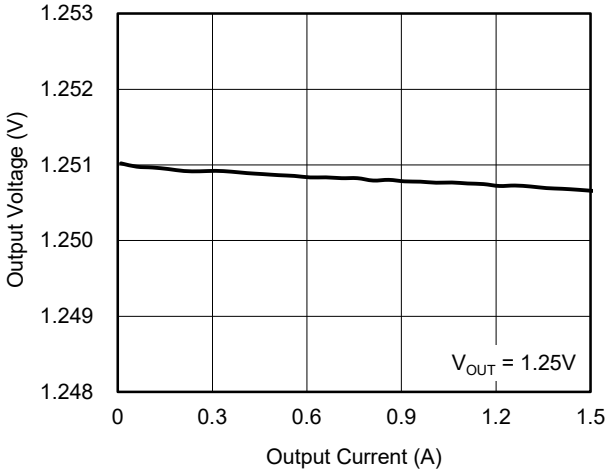


Time (200μs/div)

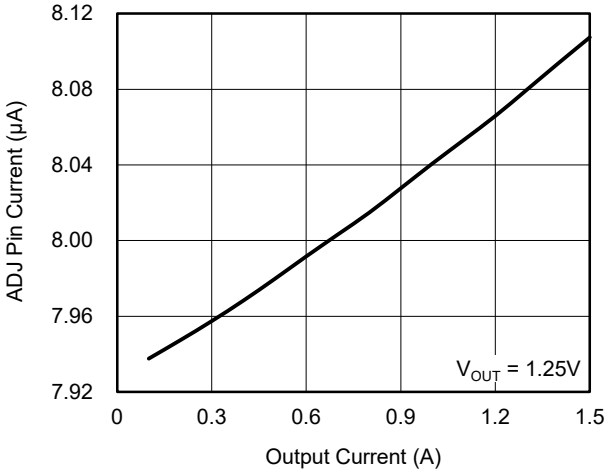
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, (V_{IN} - V_{OUT}) = 3V, C_{IN} = C_{OUT} = 10μF (ceramic capacitor), unless otherwise noted.

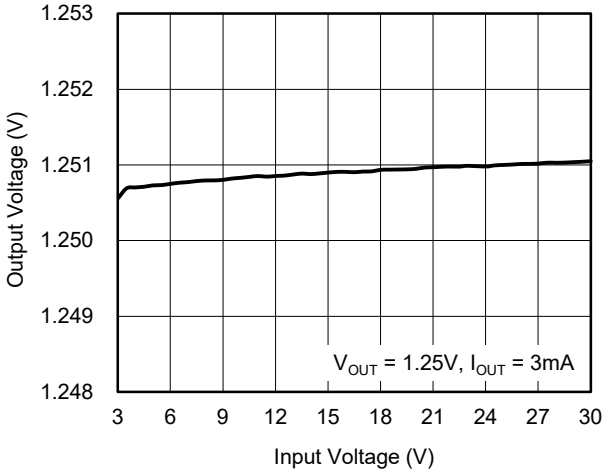
Output Voltage vs. Output Current



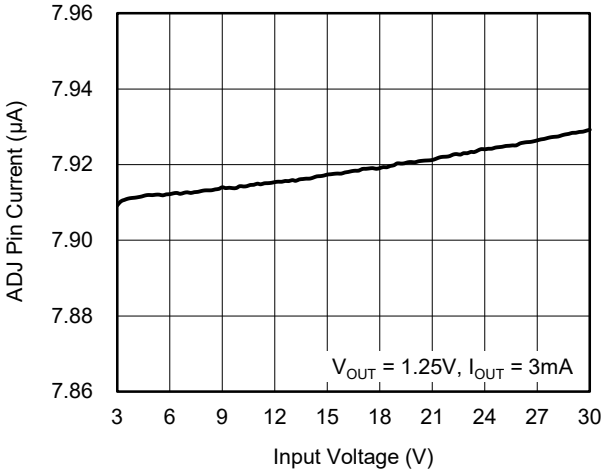
ADJ Pin Current vs. Output Current



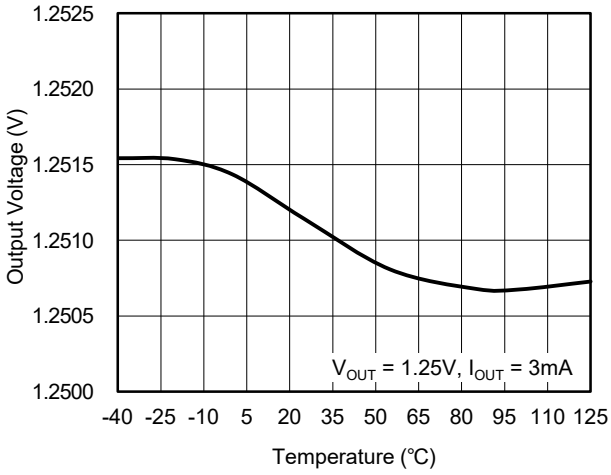
Output Voltage vs. Input Voltage



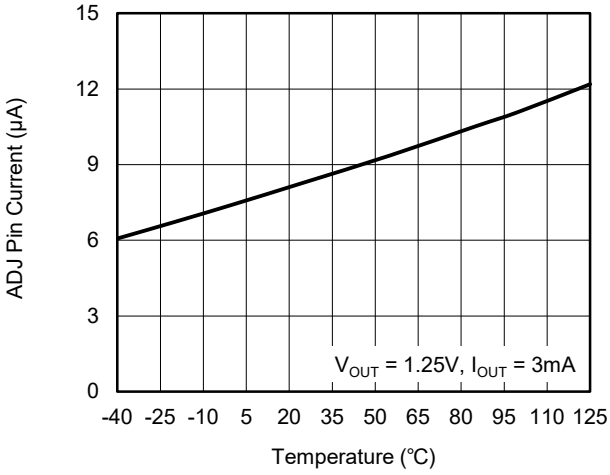
ADJ Pin Current vs. Input Voltage



Output Voltage vs. Temperature



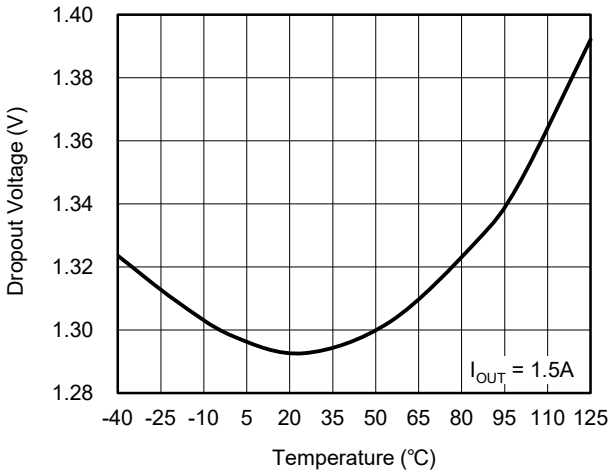
ADJ Pin Current vs. Temperature



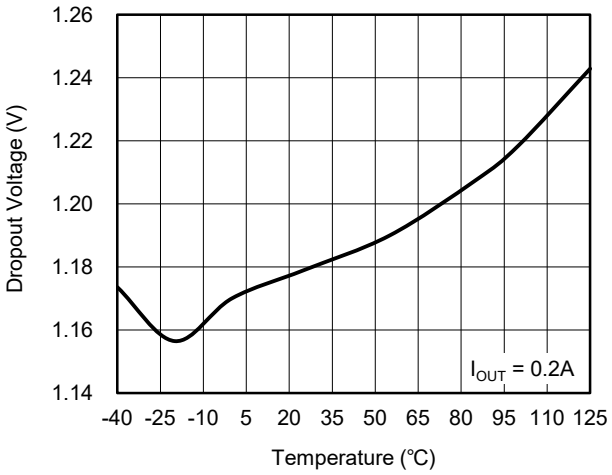
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, (V_{IN} - V_{OUT}) = 3V, C_{IN} = C_{OUT} = 10μF (ceramic capacitor), unless otherwise noted.

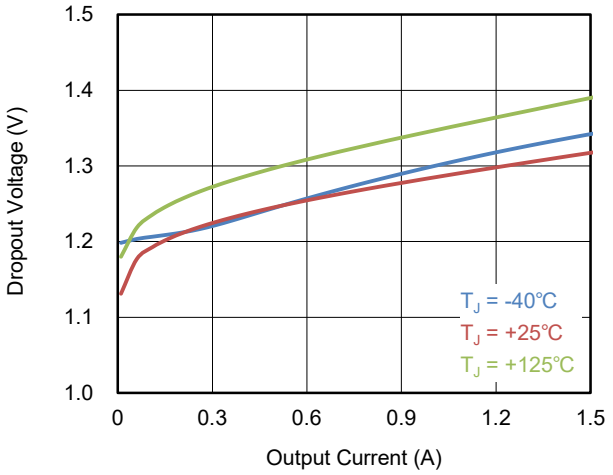
Dropout Voltage vs. Temperature



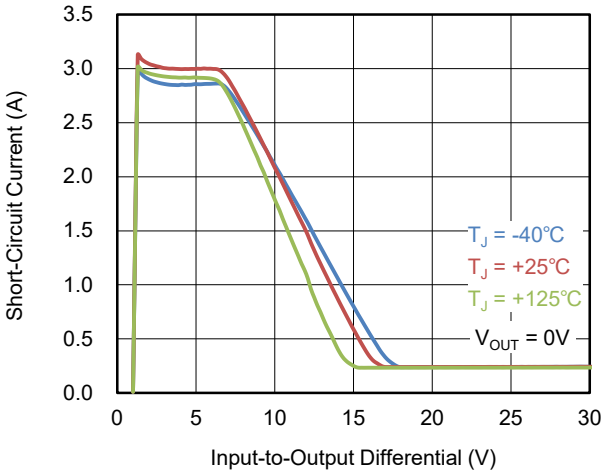
Dropout Voltage vs. Temperature



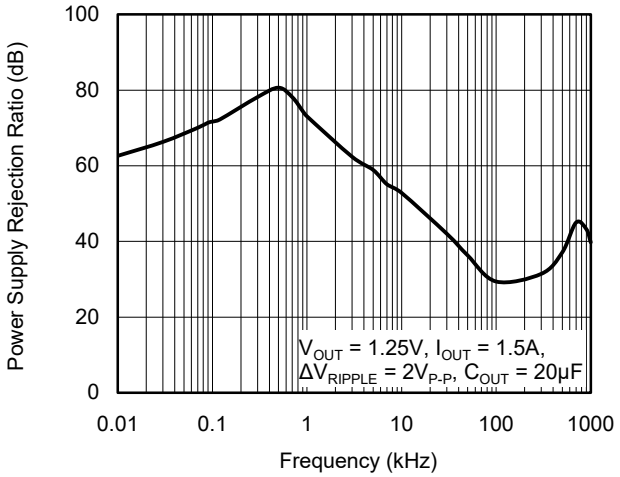
Dropout Voltage vs. Output Current



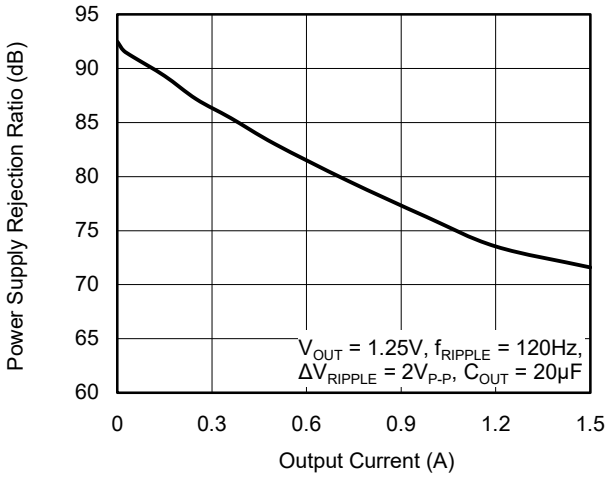
Short-Circuit Current vs. Input-to-Output Differential



Power Supply Rejection Ratio vs. Frequency



Power Supply Rejection Ratio vs. Output Current



APPLICATION INFORMATION

The SGM2217Q is a low noise, high current and low dropout LDO and provides 1.5A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2217Q useful in a variety of applications. The SGM2217Q provides protection functions for output overload, output short-circuit condition and overheating.

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin for ensuring the device stability. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

One or more output capacitors are required to maintain the stability of the LDO, and the output capacitors should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R and X5R ceramic capacitors as output capacitors. Ceramic capacitors have low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitors is affected by temperature, DC bias and package size.

For example, Figure 3 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10μF±10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

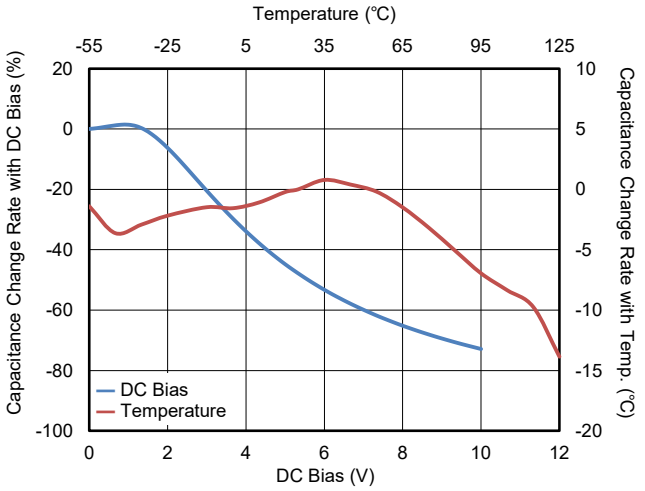


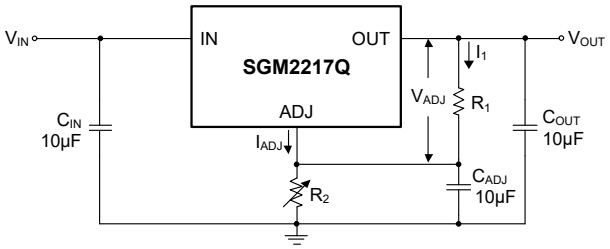
Figure 3. Capacitance vs. DC Bias and Temperature Characteristics

The SGM2217Q requires an output capacitor with effective capacitance in the range of 2.3μF to 100μF with an ESR of 8Ω or less. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Adjustable Regulator

The output voltage of the SGM2217Q can be adjusted from 1.25V to 26V. The ADJ pin will be connected to two external resistors as shown in Figure 4.

The PSRR and noise of adjustable LDO circuit can be modified slightly to levels close to that of the unity-gain LDO. The adjustment terminal can be bypassed to ground with a capacitor (C_{ADJ}). The impedance of the C_{ADJ} should be equal to or less than R_2 at the desired frequency.



$V_{OUT} = V_{ADJ} \times (1 + R_2/R_1) + I_{ADJ} \times R_2$, $I_1 = V_{ADJ}/R_1$
If I_{ADJ} is far less than I_1, $V_{OUT} = V_{ADJ} \times (1 + R_2/R_1)$.
Where V_{OUT} is output voltage and V_{ADJ} = 1.25V.

Figure 4. Adjustable Output Voltage Application

APPLICATION INFORMATION (continued)

Reverse Current Protection

The power transistor has an inherent body diode. This body diode will be forward biased when V_{OUT} > (V_{IN} + 0.3V). When V_{OUT} > (V_{IN} + 0.3V), the reverse current flowing from the OUT pin to the IN pin will damage the SGM2217Q. If V_{OUT} > (V_{IN} + 0.3V) event would happen in system, one external Schottky diode will be added between OUT pin and IN pin in circuit design to protect the SGM2217Q.

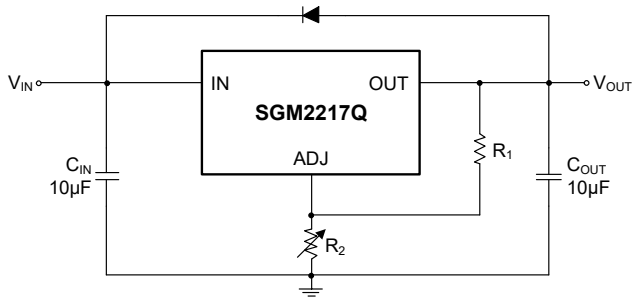


Figure 5. Reverse Protection Reference Design

Output Current Limit and Short-Circuit Protection

The current limiting circuit reduces the output current as the input-to-output differential increases after 2ms of power-on. The current limit is reduced from 2.9A to 0.26A when the V_{IN} - V_{OUT} voltage is greater than about 20V.

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2217Q will be in shutdown state and it will remain in this state until the die temperature decreases to +160℃.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2217Q can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2217Q is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)}$ - T_A), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (1)$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN pin and OUT pin separately.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2026 – REV.A.2 to REV.A.3 **Page**

Updated Typical Application section 1
Updated Absolute Maximum Ratings section 2
Updated Functional Block Diagrams section 4
Updated Electrical Characteristics section 5

MARCH 2025 – REV.A.1 to REV.A.2 **Page**

Updated Package Outline Dimensions 13

NOVEMBER 2024 – REV.A to REV.A.1 **Page**

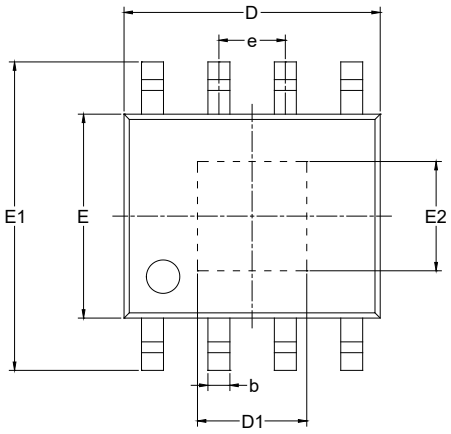
Updated Pin Description section 3
Updated Functional Block Diagram section 4
Updated Application Information section 10, 11

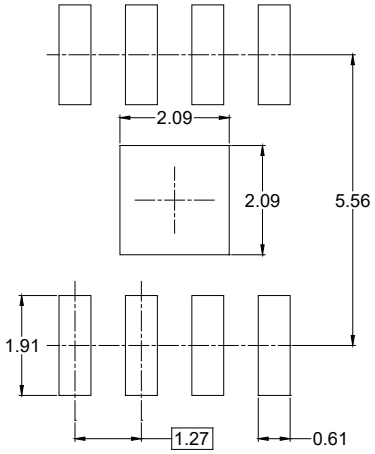
Changes from Original (NOVEMBER 2023) to REV.A **Page**

Changed from product preview to production data ..... All

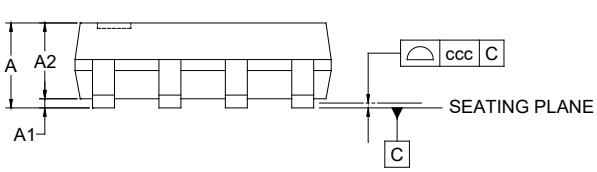
PACKAGE OUTLINE DIMENSIONS

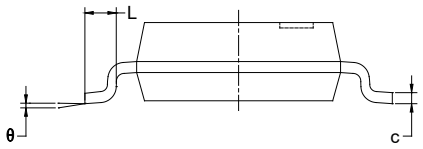
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



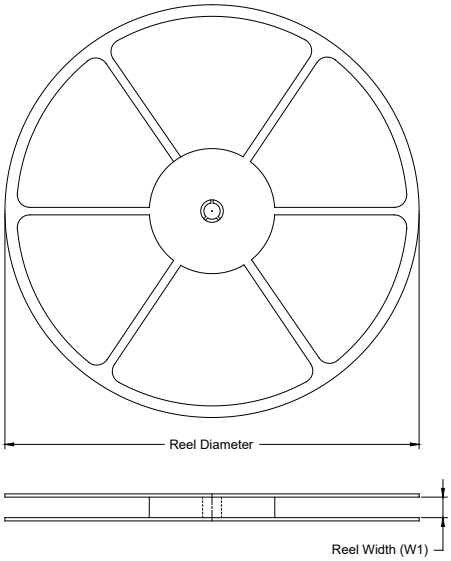


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	1.890	-	2.290
E	3.800	-	4.000
E1	5.800	-	6.200
E2	1.890	-	2.290
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

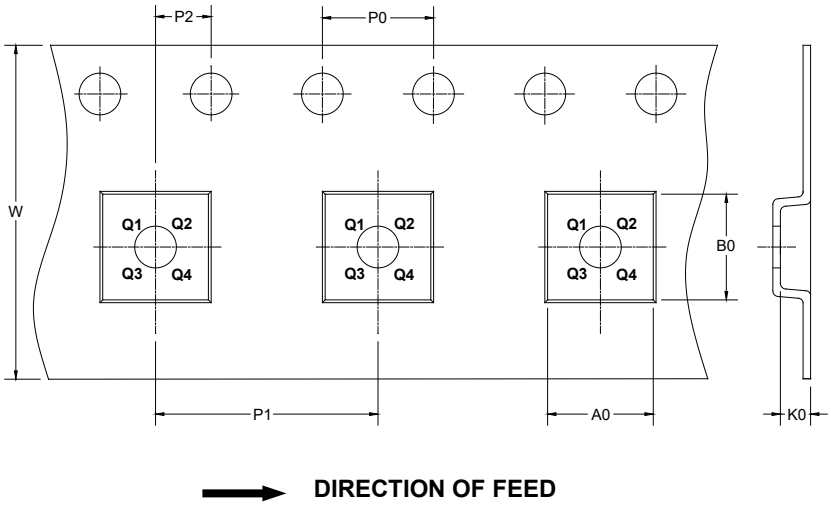
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



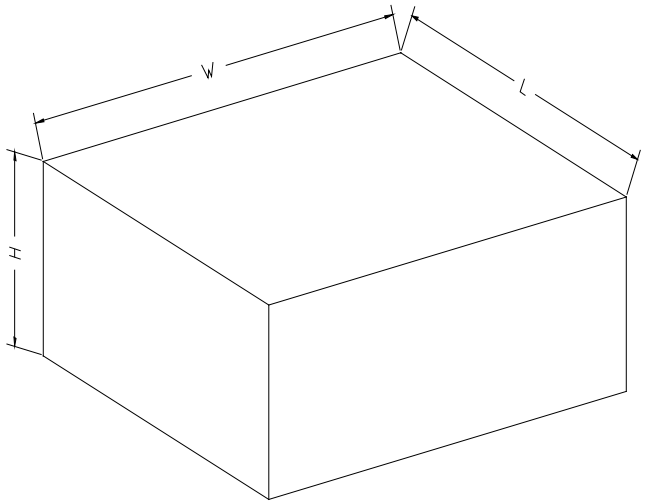
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002