SGM8558-1/SGM8558-2/SGM8558-3/SGM8558-4
15MHz, 8V/μs, High Output Drive, High Precision, Low Noise Operational Amplifiers

GENERAL DESCRIPTION

The SGM8558-1 (single), SGM8558-2 (dual), SGM8558-3 (single with shutdown), and SGM8558-4 (quad) are low noise, high precision CMOS operational amplifiers that provide a high output current of 230mA, rail-to-rail output operation from a range of 2.8V to 5.5V single supply. The SGM8558-3 is available with shutdown pins that drive the output voltage low.

The SGM8558-1/2/3/4 offer low input offset voltage, low input offset voltage drift and high output current drive. These devices also can achieve a high 15MHz gain-bandwidth product and a high 8V/μs slew rate.

The SGM8558-1/2/3/4 are specifically designed to drive high current load, such as 32Ω headset, V_{BIAS} of RF power amplifier, etc.

The SGM8558-1 is available in Green SOIC-8 and SOT-23-5 packages. The SGM8558-2 is available in Green TDFN-3×3-8L and SOIC-8 packages. The SGM8558-3 is available in a Green SOT-23-6 package. The SGM8558-4 is available in a Green SOIC-14 package. They operate over an ambient temperature range of -40℃ to +125℃.

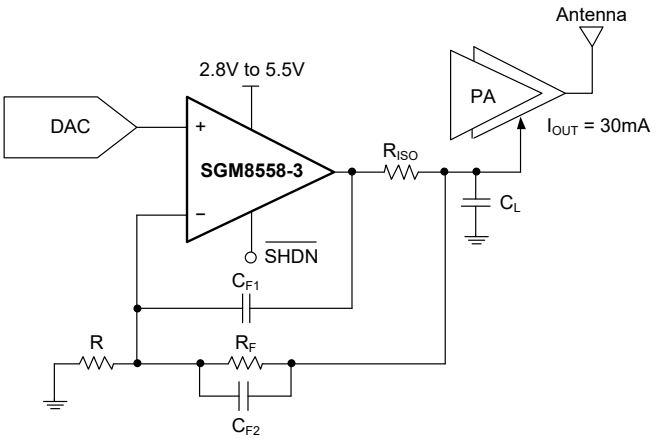
APPLICATIONS

Battery-Powered Equipment
Audio System
Optical Module
DAC Buffer
Industrial Equipment

FEATURES

- **Output Drive Capability: 230mA**
- **Low Input Offset Voltage: 15μV (MAX)**
- **Low Noise: 8nV/$\sqrt{Hz}$ at 1kHz**
- **Unity-Gain Stable for Capacitive Loads to 780pF**
- **Gain-Bandwidth Product: 15MHz**
- **High Slew Rate: 8V/μs**
- **Open-Loop Voltage Gain (R_L = 2kΩ): 139dB**
- **Power Supply Rejection Ratio: 130dB**
- **Current Limitation: 230mA**
- **Over-Temperature Protection**
- **No Phase Reversal for Overdriven Inputs**
- **Supply Voltage Range: 2.8V to 5.5V**
- **Supply Current:**
  0.86mA/Amplifier (TYP)
  0.2μA (TYP) Shutdown Current for SGM8558-3
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8558-1 Available in Green SOIC-8 and SOT-23-5 Packages
  SGM8558-2 Available in Green TDFN-3×3-8L and SOIC-8 Packages
  SGM8558-3 Available in a Green SOT-23-6 Package
  SGM8558-4 Available in a Green SOIC-14 Package

TYPICAL APPLICATION



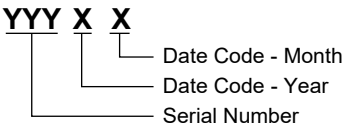
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8558-1	SOIC-8	-40℃ to +125℃	SGM8558-1XS8G/TR	SGM 85581XS8 XXXXX	Tape and Reel, 2500
	SOT-23-5	-40℃ to +125℃	SGM8558-1XN5G/TR	GFBXX	Tape and Reel, 3000
SGM8558-2	TDFN-3×3-8L	-40℃ to +125℃	SGM8558-2XTDB8G/TR	SGM 85582DB XXXXX	Tape and Reel, 4000
	SOIC-8	-40℃ to +125℃	SGM8558-2XS8G/TR	SGM 85582XS8 XXXXX	Tape and Reel, 2500
SGM8558-3	SOT-23-6	-40℃ to +125℃	SGM8558-3XN6G/TR	GFCXX	Tape and Reel, 3000
SGM8558-4	SOIC-14	-40℃ to +125℃	SGM8558-4XS14G/TR	SGM85584XS14 XXXXX	Tape and Reel, 2500

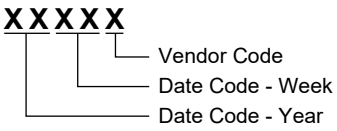
MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code and Vendor Code.

SOT-23-5/SOT-23-6



SOIC-8/TDFN-3×3-8L/SOIC-14



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 6V
All Other Pins ..... ($-V_S$) - 0.3V to ($+V_S$) + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃
Operating Supply Voltage Range ..... 2.8V to 5.5V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

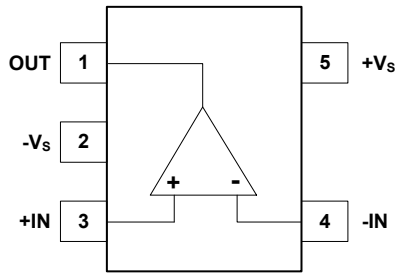
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

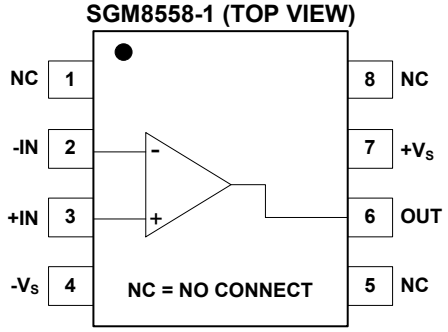
PIN CONFIGURATIONS

SGM8558-1 (TOP VIEW)



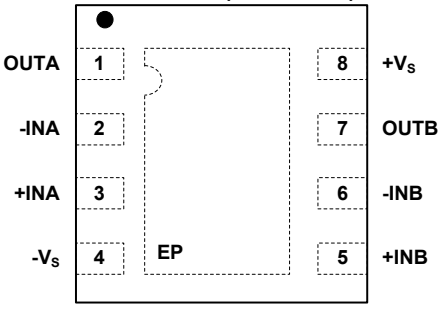
SOT-23-5

SGM8558-1 (TOP VIEW)



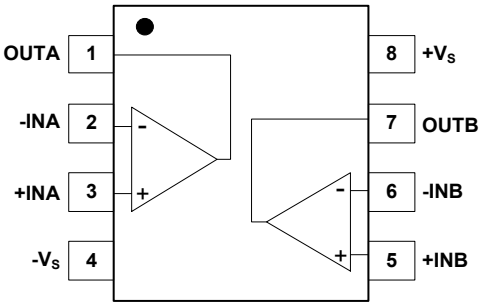
SOIC-8

SGM8558-2 (TOP VIEW)



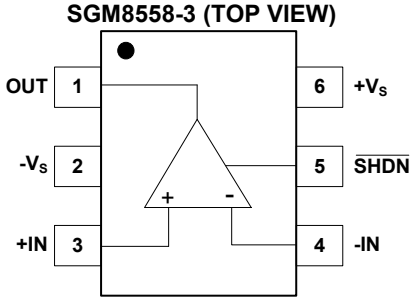
TDFN-3×3-8L

SGM8558-2 (TOP VIEW)



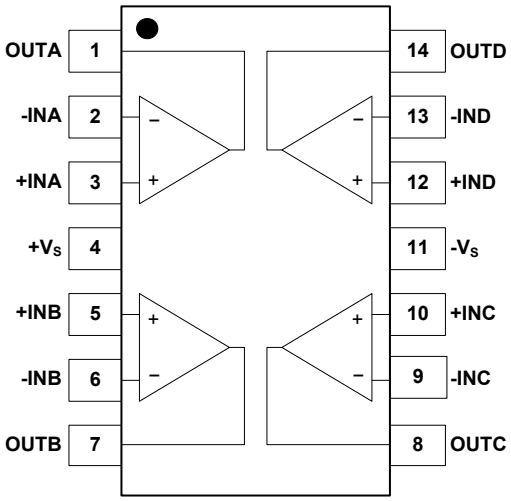
SOIC-8

SGM8558-3 (TOP VIEW)



SOT-23-6

SGM8558-4 (TOP VIEW)



SOIC-14

NOTE: For the TDFN-3×3-8L package, the exposed pad must be connected to $-V_S$ or left floating. Connect it to $-V_S$ plane can maximize thermal performance.

ELECTRICAL CHARACTERISTICS

(+V_S = 2.8V, -V_S = 0V, V_{CM} = +V_S/2, V_{OUT} = +V_S/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics						
Input Offset Voltage (V_{OS})		+25℃		1.5	15	μV
Input Common Mode Voltage Range (V_{CM})		Full	(-V_S) - 0.1		(+V_S) + 0.1	V
Common Mode Rejection Ratio (CMRR)	(-V_S) - 0.1V < V_{CM} < (+V_S) + 0.1V	+25℃	96	118		dB
		Full	90			
Open-Loop Voltage Gain (A_{OL})	(-V_S) + 0.3V < V_{OUT} < (+V_S) - 0.3V, R_L = 2kΩ	+25℃	108	131		dB
		Full	105			
	(-V_S) + 0.3V < V_{OUT} < (+V_S) - 0.3V, R_L = 200Ω	+25℃	106	130		
		Full	103			
Output Characteristics						
Output Voltage Swing from Rail	R_L = 2kΩ	+25℃		5	11	mV
		Full			12	
	R_L = 200Ω	+25℃		45	55	
		Full			66	
Output Short-Circuit Current (I_{SC})		+25℃	96	120		mA
		Full	75			
Power Supply						
Specified Voltage Range (V_S)		Full	2.8		5.5	V
Quiescent Current/Amplifier (I_Q)	I_{OUT} = 0A	+25℃		827	1250	μA
		Full			1450	
Power Supply Rejection Ratio (PSRR)	V_S = 2.8V to 5.5V, V_{CM} = 0.2V	+25℃	102	130		dB
		Full	100			
Dynamic Performance						
Gain-Bandwidth Product	G = +100	+25℃		14		MHz
Slew Rate	G = +1, V_{OUT} = 2V_{P-P}	+25℃		8		V/μs
Noise						
Input Voltage Noise	f = 0.1Hz to 10Hz	+25℃		0.3		μV_{P-P}
Input Voltage Noise Density	f = 1kHz	+25℃		11		nV/$\sqrt{Hz}$
	f = 10kHz	+25℃		11		

ELECTRICAL CHARACTERISTICS (continued)

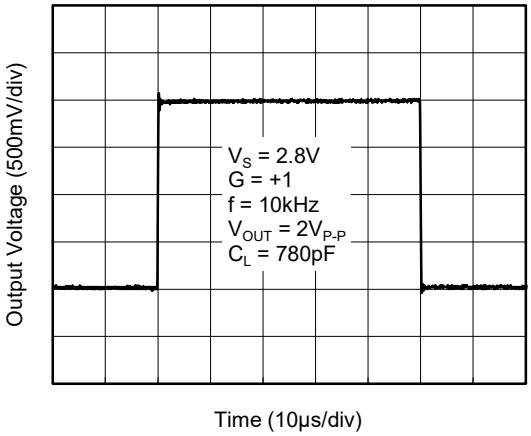
(+V_S = 5V, -V_S = 0V, V_{CM} = +V_S/2, V_{OUT} = +V_S/2, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage (V_{OS})			+25℃		1.5	15	μV
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)			Full		13	66	nV/℃
Input Bias Current (I_B)			+25℃		0.6	3	nA
Input Offset Current (I_{OS})			+25℃		1.2	5.2	nA
Input Common Mode Voltage Range (V_{CM})			Full	(-V_S) - 0.1		(+V_S) + 0.1	V
Common Mode Rejection Ratio (CMRR)		(-V_S) - 0.1V < V_{CM} < (+V_S) + 0.1V	+25℃	102	126		dB
			Full	97			
Open-Loop Voltage Gain (A_{OL})		(-V_S) + 0.3V < V_{OUT} < (+V_S) - 0.3V, R_L = 2kΩ	+25℃	116	139		dB
			Full	113			
		(-V_S) + 0.3V < V_{OUT} < (+V_S) - 0.3V, R_L = 200Ω	+25℃	114	136		
			Full	110			
Output Characteristics							
Output Voltage Swing from Rail		R_L = 2kΩ	+25℃		7	16	mV
			Full			18	
		R_L = 200Ω	+25℃		63	88	
			Full			104	
Output Short-Circuit Current (I_{SC})			+25℃	193	230		mA
			Full	173			
Power-Down Disable (SGM8558-3 Only)							
Logic Threshold	V_{IH}	Normal mode	+25℃	2.0			V
	V_{IL}	Shutdown mode	+25℃			0.8	
Shutdown Supply Current		V_{EN} = 0V	+25℃		0.2	1.5	μA
Power Supply							
Specified Voltage Range (V_S)			Full	2.8		5.5	V
Quiescent Current/Amplifier (I_Q)		I_{OUT} = 0A	+25℃		860	1280	μA
			Full			1500	
Dynamic Performance							
Gain-Bandwidth Product		G = +100	+25℃		15		MHz
Slew Rate		G = +1, V_{OUT} = $2V_{P-P}$	+25℃		8		V/μs
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		0.2		μV_{P-P}
Input Voltage Noise Density		f = 1kHz	+25℃		8		$nV/\sqrt{Hz}$
		f = 10kHz	+25℃		8		

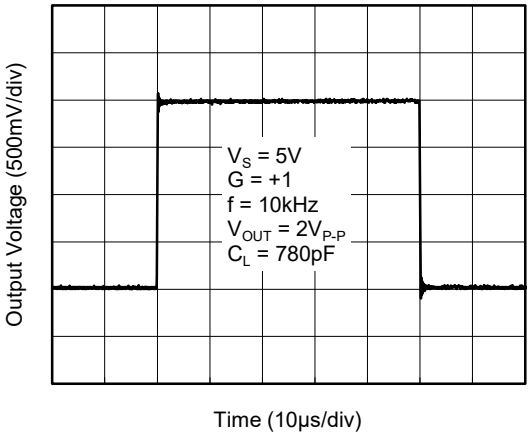
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = 5V, unless otherwise noted.

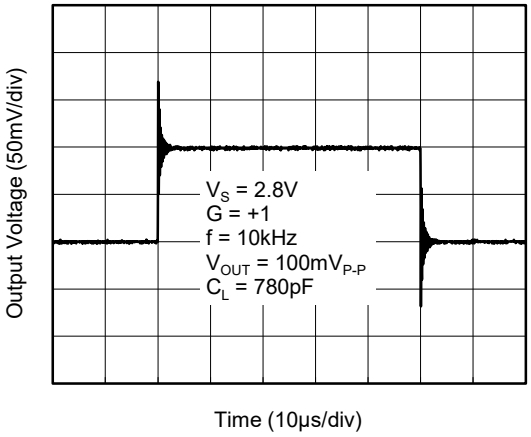
Large-Signal Transient Response with Capacitive Load



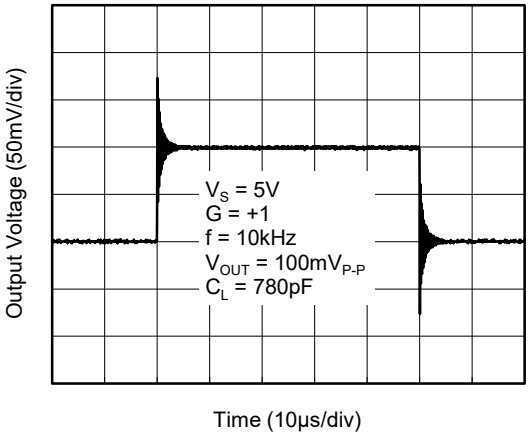
Large-Signal Transient Response with Capacitive Load



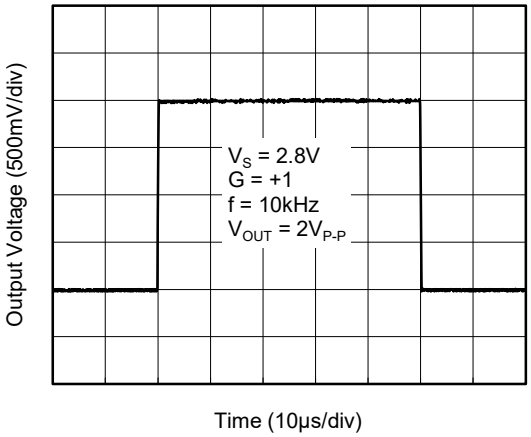
Small-Signal Transient Response with Capacitive Load



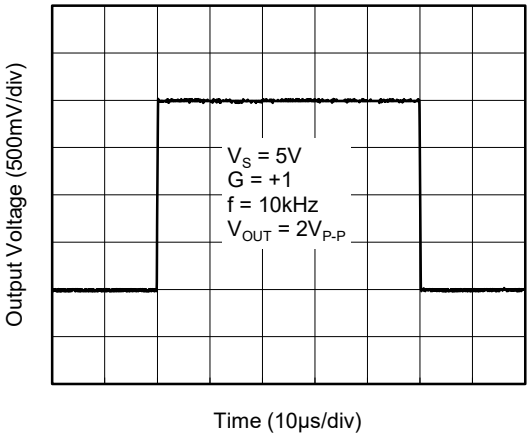
Small-Signal Transient Response with Capacitive Load



Large-Signal Step Response



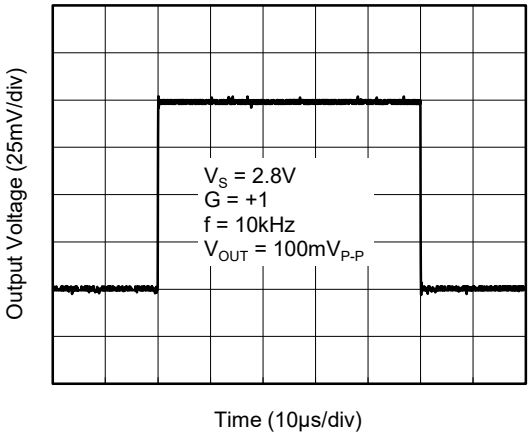
Large-Signal Step Response



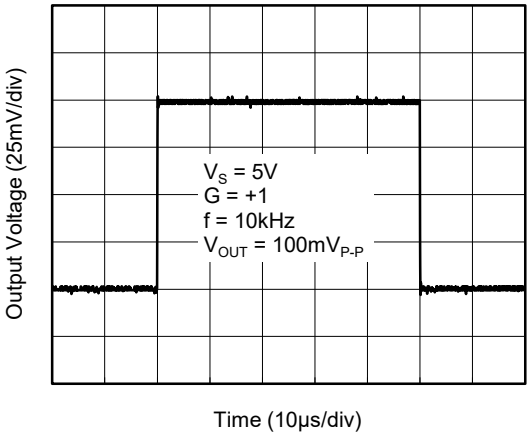
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 5V, unless otherwise noted.

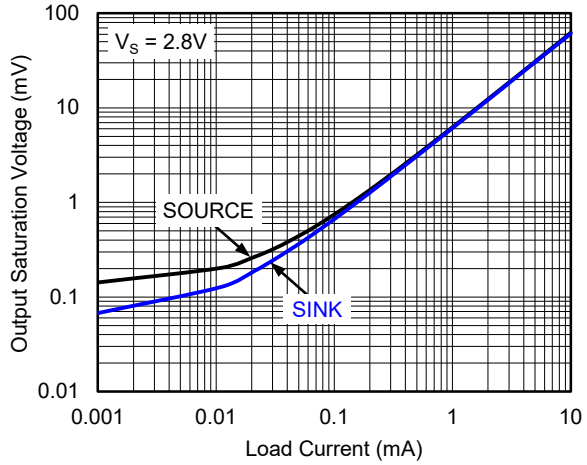
Small-Signal Step Response



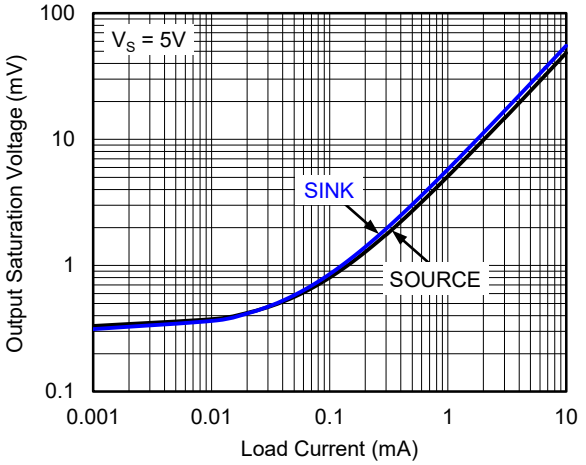
Small-Signal Step Response



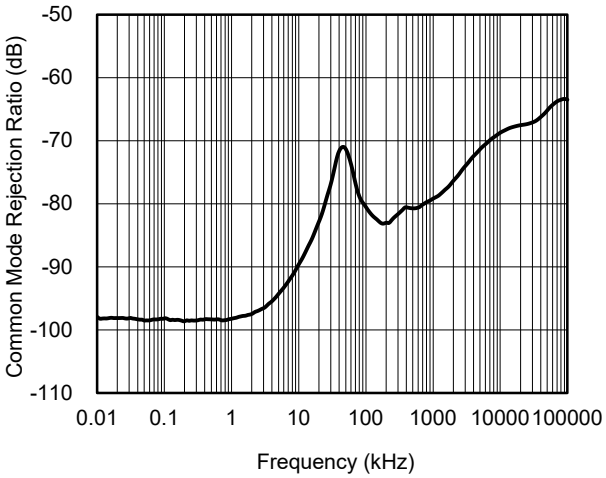
Output Saturation Voltage vs. Load Current



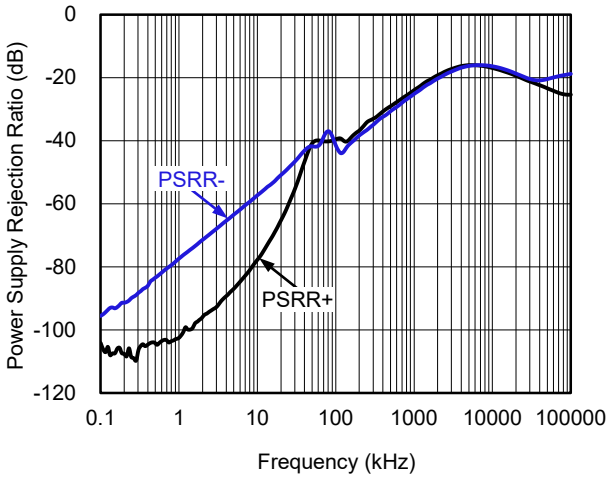
Output Saturation Voltage vs. Load Current



CMRR vs. Frequency



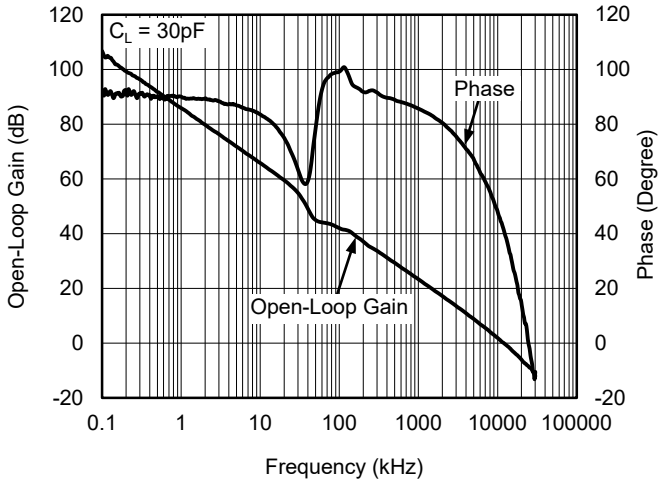
PSRR vs. Frequency



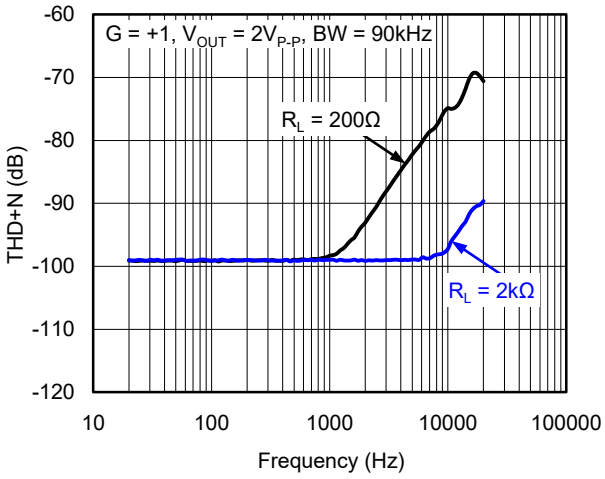
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 5V, unless otherwise noted.

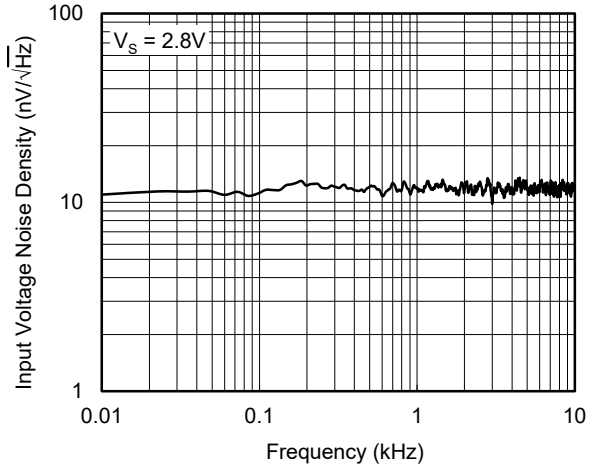
Open-Loop Gain and Phase vs. Frequency



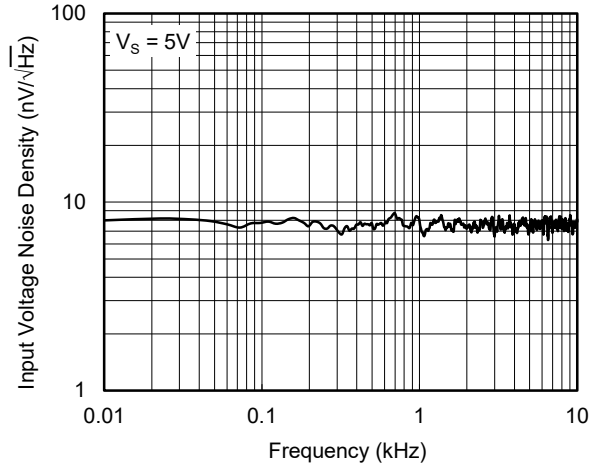
THD+N vs. Frequency



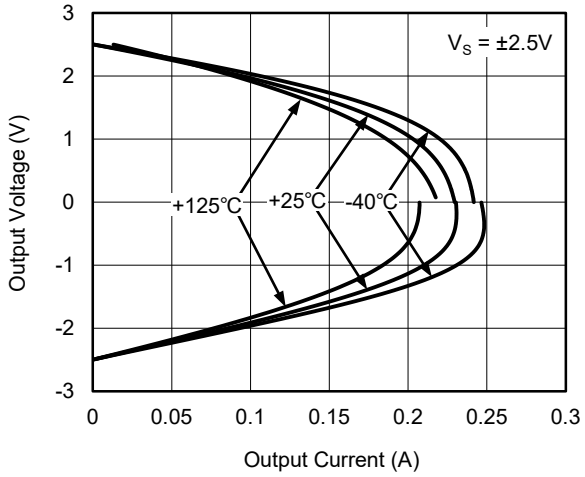
Input Voltage Noise Density vs. Frequency



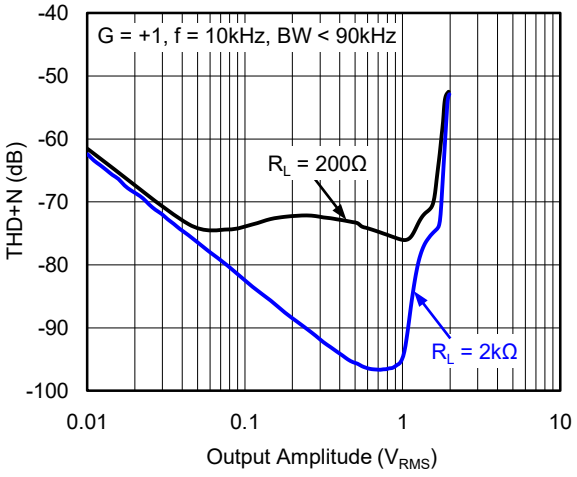
Input Voltage Noise Density vs. Frequency



Output Voltage Swing vs. Output Current

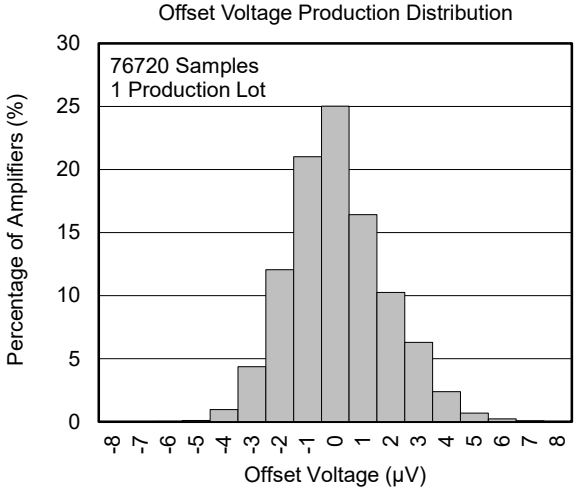


THD+N vs. Output Amplitude



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 5V, unless otherwise noted.



APPLICATION INFORMATION

Single-Supply Stereo Headphone Driver

A single-supply stereo headphone driver is shown in Figure 1 as an example to explain the simplified design procedure.

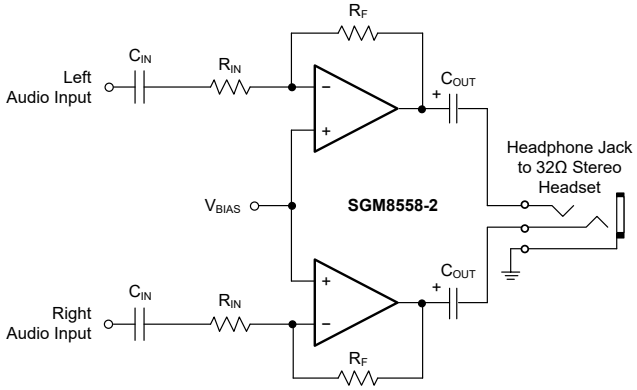


Figure 1. Stereo Headphone Driver

In this circuit, C_{IN} and R_{IN} form a high-pass filter, the DC bias is removed from the incoming signal. The -3dB point of the high-pass filter is using Equation 1:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad (1)$$

The gain of driver is $-R_F/R_{IN}$. The C_{OUT} and the load impedance form a high-pass filter with the -3dB point determined by Equation 2:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}} \quad (2)$$

Bridge Amplifier

A bridge amplifier circuit which can provide 200mW at 3V is shown in Figure 2. Due to differential output, this structure eliminates the large coupling capacitors in Figure 1. The voltage gain is 10V/V and the gain can be changed by changing R_2.

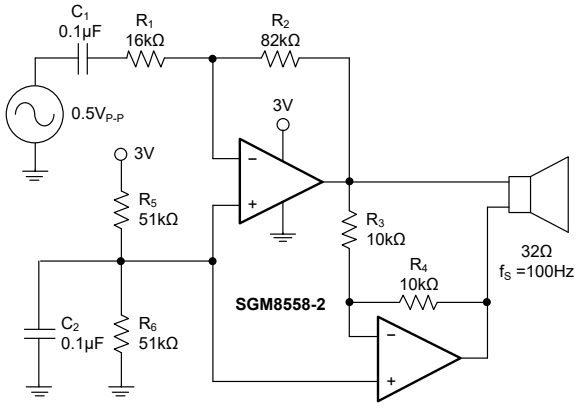


Figure 2. 200mW Bridge Amplifier at 3V

Cancel Input Capacitance

The C_{IN} (20pF TYP) at inverting input pin will generate a pole at frequency $(2\pi R' C_{IN})^{-1}$, where R′ is the parallel combination of the gain-setting resistor for the inverting or non-inverting amplifier in Figure 3. If the pole-frequency is less than or comparable to the unity-gain bandwidth (15MHz), the phase margin will be reduced, ringing in the step response or sustained oscillation will be generated. To cancel this pole, C_F is used to compensate C_{IN} in Figure 3. Equation 3 gives the C_F feedback capacitance.

$$C_F = 8\times(R/R_F)\ pF \quad (3)$$

where:
R_F is the feedback resistor.
R is the gain-setting resistor.

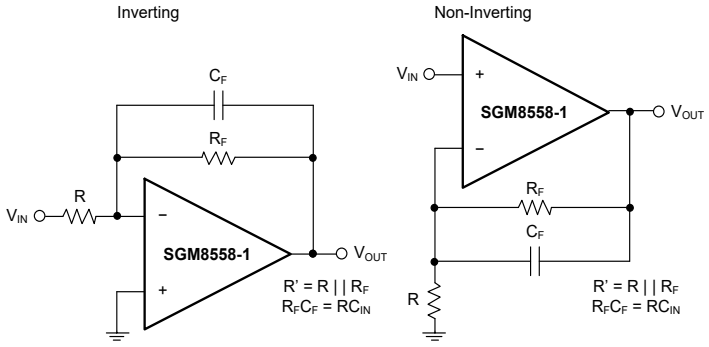


Figure 3. Inverting and Non-Inverting Amplifiers with C_F to Compensate C_{IN}

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 4, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is to contribute thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

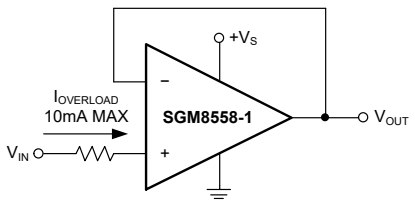


Figure 4. Input Current-Limit Protection

APPLICATIONS INFORMATION (continued)

Rail-to-Rail Output

The SGM8558-1/2/3/4 support rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 5V, $-V_S$ = GND, 2kΩ load resistor is tied from OUT pin to $V_S/2$, the typical output swing range is from 0.007V to 4.993V.

Driving Capacitive Loads

The SGM8558-1/2/3/4 are designed for unity-gain stable for capacitive load up to 780pF. In Figure 5, it shows the transient response with capacitive load (C_L). If greater capacitive load must be driven in application, the circuit in Figure 6 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

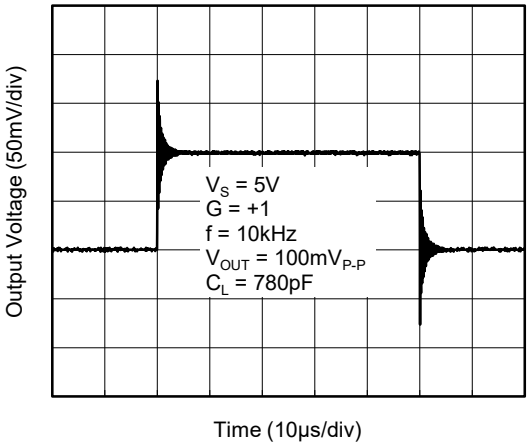


Figure 5. Small-Signal Transient Response (Capacitive Load)

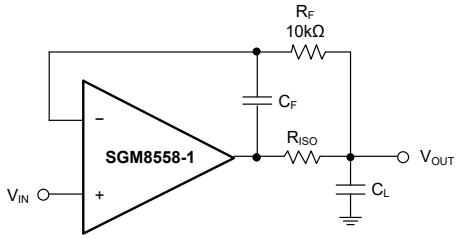


Figure 6. Circuit to Drive Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifiers through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 7. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

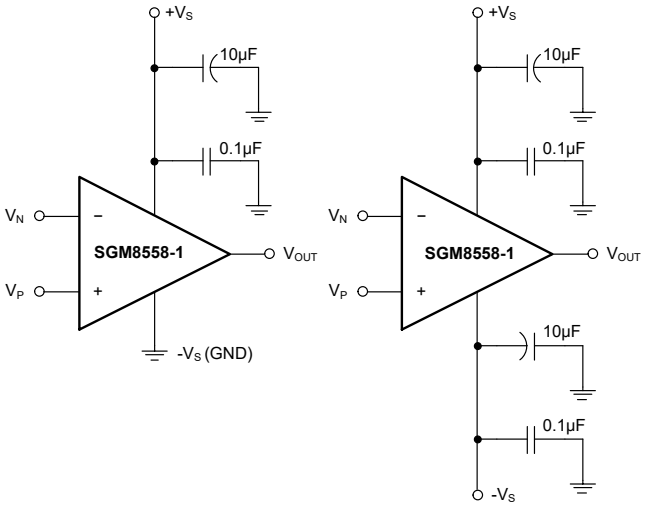


Figure 7. Amplifier Power Supply Bypassing

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2022 – REV.A.2 to REV.A.3	Page
Updated Electrical Characteristics section	4, 5
Updated Typical Performance Characteristics section	7, 8

MARCH 2022 – REV.A.1 to REV.A.2	Page
Updated Typical Performance Characteristics section	8

JANUARY 2019 – REV.A to REV.A.1	Page
Changed Figure 2	10

Changes from Original (SEPTEMBER 2018) to REV.A	Page
Changed from product preview to production data	All