SGM31030
Constant Current RGB LED Driver with I²C Interface

GENERAL DESCRIPTION

The SGM31030 is a 3-channel LED current sink driver featuring a 1MHz I²C-compatible interface. Each LED channel supports an 8-bit DC current scaling register per channel and 6-bit global current scaling register. This architecture also enables up to 256 levels of linear PWM dimming.

The device operates over a supply voltage range of 2.5V to 5.5V, with ultra-low quiescent and shutdown current consumption for power-sensitive applications.

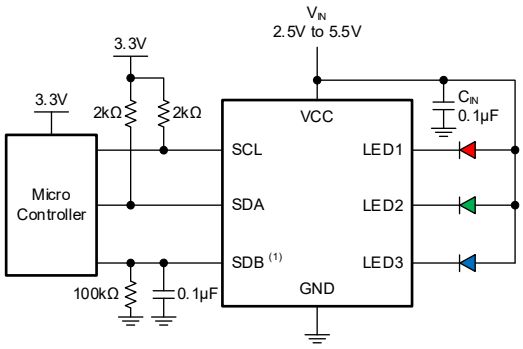
The SGM31030 supports three primary operating modes. PWM & current level mode allows independent output current per channel, facilitating precise color mixing. Simultaneously, the PWM duty cycle for each channel is configurable with 256-step resolution to enable fine-grained brightness and color control. Current level mode provides a continuous current sink output per channel with no PWM modulation, and is suitable for applications requiring steady-state LED illumination. Pattern mode enables per-channel timing adjustment for RGB outputs to maintain predefined output sequence autonomously, without host MCU intervention, thereby offloading timing control and conserving system resources.

The SGM31030 is available in Green UTDFN-1.5×1.5-8L and UTQFN-1.5×1.5-9AL packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Input Voltage Range: 2.5V to 5.5V**
- **Less than 1.8μA Shutdown Current**
- **3 Current Sinks, I_{OUT} = 25mA (MAX)**
- **±4% Accuracy and Mismatch**
- **Accurate Color Rendition**
  - **8-Bit PWM/Channel**
  - **8-Bit Current Level/Channel**
  - **6-Bit Global DC Current Adjustment**
- **Auto Breath Function**
  - **Auto Breath Pattern for 3 Channels**
  - **4-Color Pattern Registers for Color Breath**
  - **Programmable Ramp-Up and Ramp-Down Time**
- **Internal Reset Register**
- **Fast Mode plus I²C Interface**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green UTDFN-1.5×1.5-8L and UTQFN-1.5×1.5-9AL Packages**

TYPICAL APPLICATION



NOTE: 1. UTQFN-1.5×1.5-9AL package only.

Figure 1. Typical Application Circuit

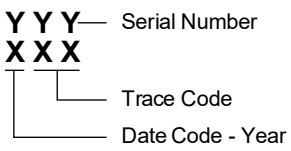
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM31030	UTDFN-1.5×1.5-8L	-40℃ to +85℃	SGM31030YUDW8G/TR	1Y1 XXX	Tape and Reel, 4000
	UTQFN-1.5×1.5-9AL	-40℃ to +85℃	SGM31030YUXI9G/TR	1Y5 XXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.

UTDFN-1.5×1.5-8L/UTQFN-1.5×1.5-9AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VCC, LED1, LED2, LED3 to GND ..... -0.3V to 6V
SCL, SDA to GND ..... -0.3V to 6V
SDB ..... -0.3V to 6V
Package Thermal Resistance
UTDFN-1.5×1.5-8L, θ_{JA} ..... 122.8℃/W
UTDFN-1.5×1.5-8L, θ_{JB} ..... 70.5℃/W
UTDFN-1.5×1.5-8L, $\theta_{JC\ (TOP)}$ ..... 85.9℃/W
UTDFN-1.5×1.5-8L, $\theta_{JC\ (BOT)}$ ..... 59.4℃/W
UTQFN-1.5×1.5-9AL, θ_{JA} ..... 125.3℃/W
UTQFN-1.5×1.5-9AL, θ_{JB} ..... 55.6℃/W
UTQFN-1.5×1.5-9AL, θ_{JC} ..... 102.8℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.5V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

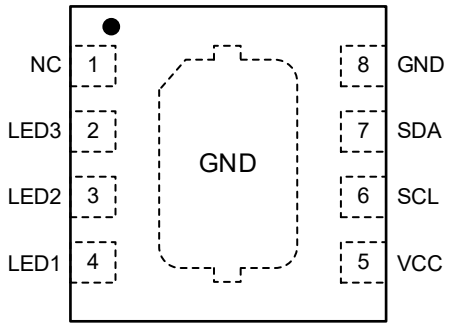
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

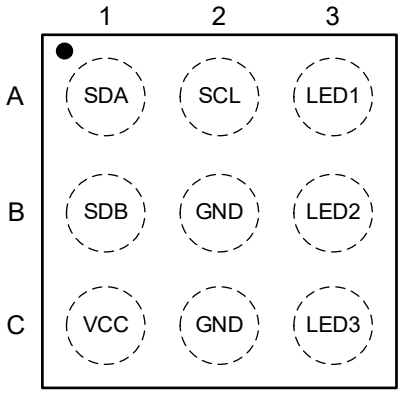
PIN CONFIGURATIONS

(TOP VIEW)



UTDFN-1.5×1.5-8L

(TOP VIEW)



UTQFN-1.5×1.5-9AL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
UTDFN-1.5×1.5-8L	UTQFN-1.5×1.5-9AL			
1	—	NC	I	No Connection.
2	C3	LED3	O	Current Sink 3. The LED3 current and ON/OFF state can be set by programmable I²C interface.
3	B3	LED2	O	Current Sink 2. The LED2 current and ON/OFF state can be set by programmable I²C interface.
4	A3	LED1	O	Current Sink 1. The LED1 current and ON/OFF state can be set by programmable I²C interface.
5	C1	VCC	P	Power Supply Pin.
6	A2	SCL	I	I²C Clock Signal.
7	A1	SDA	I/O	I²C Data Signal.
8	B2, C2	GND	G	Ground Pin.
—	B1	SDB	I	Shutdown Pin.
Exposed Pad	—	GND	—	Exposed Pad. It should be soldered to the ground.

NOTE: I = input; O = output; I/O = input or output; G = ground; P = power for the circuit.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.6V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Voltage	V_{CC}		2.5		5.5	V
Quiescent Power Supply Current	I_{CC}	all channels PWM = 0x00, PWM frequency = 200Hz, all LEDs off		85	110	μA
		one channel I_{OUT} = 25mA, PWM frequency = 200Hz		195	225	
		all channels I_{OUT} = 25mA, PWM frequency = 200Hz		405	450	
Shutdown Current	I_{SD}	V_{SDB} = 0V		0.3	1.8	μA
		V_{SDB} = V_{CC} = 3.6V, REG0x01 register written “0000 0000”		0.3	1.8	
Maximum Constant Current of LEDx	I_{OUT}	I_{OUT} = 25mA, GCC[5:0] = 0x3F, COLx_ILEDy[7:0] = 0xFF	24	25	26	mA
Between Channels	ΔI_{MAT}	I_{OUT} = 25mA, GCC[5:0] = 0x3F, COLx_ILEDy[7:0] = 0xFF	-4		4	%
Between Device to Device	ΔI_{ACC}	I_{OUT} = 25mA, GCC[5:0] = 0x3F, COLx_ILEDy[7:0] = 0xFF	-4		4	%
PWM Frequency of Output	f_{OUT}	PFS = 0	190	200	210	Hz
		PFS = 1	380	400	420	Hz
Current Sink Headroom Voltage	V_{HR}	I_{OUT} = 25mA		240	330	mV
Thermal Shutdown	T_{SD}			155		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			18		℃
Logic Electrical Characteristics (SDA, SCL, SDB)						
Input Logic Low Threshold Voltage	V_{IL}	V_{CC} = 2.5V to 5.5V			0.38	V
Input Logic High Threshold Voltage	V_{IH}	V_{CC} = 2.5V to 5.5V	0.9			V
Input Logic Low Leakage Current	I_{IL}	V_{INPUT} = 0V		5		nA
Input Logic High Leakage Current	I_{IH}	V_{INPUT} = V_{CC}		5		nA

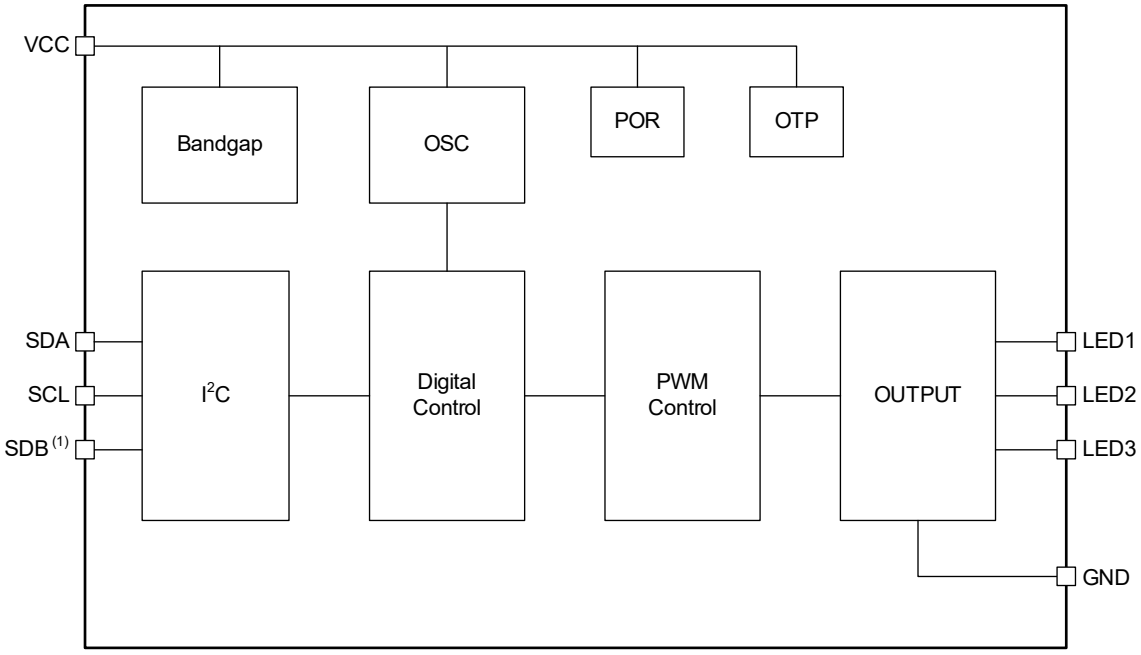
I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		400		1000	kHz
Bus-Free Time between STOP and START Condition	t_{BUF}	1.3		0.5		μs
START or Repeated START Hold Time	$t_{HD;STA}$	0.6		0.26		μs
Repeated START Setup Time	$t_{SU;STA}$	0.6		0.26		μs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		0.26		μs
Data Hold Time	$t_{HD,DAT}$	0		0		μs
Data Setup Time	$t_{SU;DAT}$	100		50		ns
SCL Low Period	t_{LOW}	1.3		0.5		μs
SCL High Period	t_{HIGH}	0.6		0.26		μs
SDA and SCL Rise Time	t_R		300		120	ns
SDA and SCL Fall Time	t_F	20 × (V_{DD}/5.5)	300	20 × (V_{DD}/5.5)	120	ns
Data Valid Time	$t_{VD;DAT}$		0.9		0.45	μs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9		0.45	μs

NOTE:

1. Industry standard I²C timing characteristics are according to I²C-Bus Specification.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. UTQFN-1.5×1.5-9AL package only.

Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Operation Description

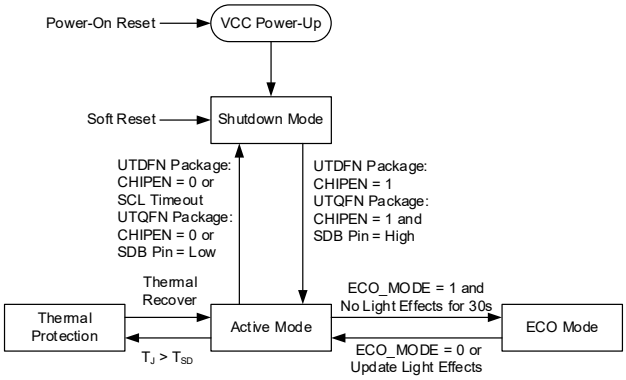


Figure 3. SGM31030 Operation State Diagram

Power-On Reset

Upon initial VCC power-up, SGM31030 is reset. All registers are reset to default values, and the LED driver is shut down. Once V_{CC} falls below the threshold voltage of POR, SGM31030 will be reset again.

It is required to wait for at least 200μs before I^2C write and read operation when V_{CC} rises above the POR threshold and to wait for another 200μs before LED light effects are enabled.

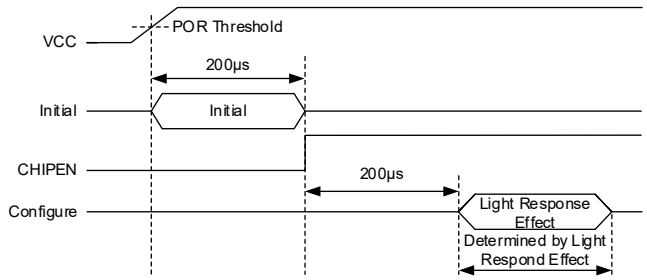


Figure 4. Power-Up Timing

Register Soft Reset

By writing 0x00 to REG0x30 to reset register, the software reset is triggered. After software reset, all registers are reset to the default values and enter shutdown mode.

After the software reset command is acknowledged via I^2C bus, it is required to wait for at least 200μs before LED light effects are enabled.

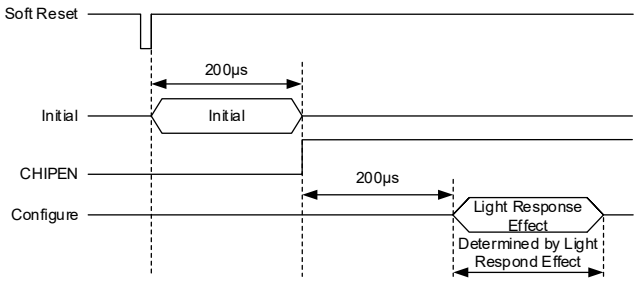


Figure 5. Software Reset Timing

Shutdown Mode

SGM31030 enters shutdown mode in several cases below:

(1) SDB is pulled from high to low (only valid for UTQFN-1.5×1.5-9AL package)
(2) SCL timeout, when SCL pin pulls low for 130ms. (only valid for UTDFN-1.5×1.5-8L package)
(3) CHIPEN bit is set from 1 to 0.
(4) VCC POR in active mode.
(5) Soft reset in active mode.

In shutdown mode, I^2C interface is accessible and all registers are retained. All analog blocks are powered down and CHIPEN will be reset manually or automatically. By setting CHIPEN bit from 0 to 1, SGM31030 can re-enter the active mode.

Active Mode

When SDB is high and CHIPEN bit is set to 1, SGM31030 enters the active mode.

ECO Mode

When ECO_MODE is set to 1, the auto ECO mode is enabled. If ECO_MODE = 1 and no light effects for longer than 30s, the chip automatically enters ECO mode. Once update the light effects or set ECO_MODE bit to 0, the chip exits ECO mode and enters active mode immediately.

Over-Temperature Protection

Over-temperature protection is only enabled in active mode. The SGM31030 will shut down all outputs when the temperature rises above +155℃.

DETAILED DESCRIPTION (continued)

LED Operation Mode

SGM31030 has three operation modes for each channel. It can be configured in REG0x02 register.

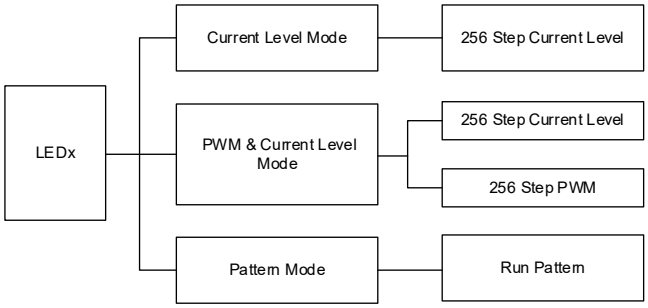


Figure 6. Operation Mode

Current Level Mode

The output is pure DC current with no pulse width modulation. The output DC current by default is:

$$I_{OUT} = 25mA \times \frac{GCC}{63} \times \frac{COL}{255}, LCAI = 0 \quad (1)$$

where

I_{OUT} is the average current of the outputs;

GCC is the decimal number of GCC[5:0];

COL is the decimal number of COL1_ILEDy[7:0] (y = 1, 2, 3) depending on the output channel.

If the low current accuracy improvement function is enabled, the low output DC current is:

$$I_{OUT} = 6.25mA \times \frac{GCC}{63} \times \frac{COL}{255}, LCAI = 1 \quad (2)$$

The fade in/out function can be used in current level mode. By 0% to 100% PWM duty cycle linearly sweeping, the output current can transit to high output current. Similarly, by 100% to 0% PWM duty cycle linearly sweeping, the output current can transit to low output current.

PWM & Current Level Mode

The output is DC current modulated with the pulse width. The current registers determine the peak of the output current and the PWM registers control the duty cycle of the outputs. Hence, the average output current is:

$$I_{OUT} = \begin{cases} 25mA \times \frac{GCC}{63} \times \frac{COL}{255} \times \frac{PWM}{256}, LCAI = 0 \\ 6.25mA \times \frac{GCC}{63} \times \frac{COL}{255} \times \frac{PWM}{256}, LCAI = 1 \end{cases} \quad (3)$$

where PWM is the decimal number of LEDy_PWM[7:0] (y = 1, 2, 3) depending on the output channels.

If PWM register sets to 255, the PWM value in the equation will change to 256, so that the output can get a full PWM duty cycle.

It is required to update the PWM register by writing 0x00 in PWM update register REG0x20 after the PWM values are written. The fade in/out function is not implemented in this mode. But the light effect can be realized by continuously writing PWM values and PWM update.

Pattern Mode

By setting the LED mode configuration register, LEDx_MODE[1:0] to 0b01, the corresponding output will enter into pattern mode. The pattern color current, breathing timing, and loop count are required to be configured in advance. Once color update and PWM time update registers updating, the light effect will start.

Color Pattern

There are 4 color patterns in the pattern mode. Each color mode is configured in COLx_ILED1[7:0], COLx_ILED2[7:0], or COLx_ILED3[7:0]. The single color pattern loop count is configured in COLx_CNT[1:0], which has 1 time, 2 times, 3 times, and endless options. If COLx_EN is set to 0, the corresponding color pattern will not be used, so its count is 0. See Table 1.

The breathing pattern timing parameters are configured by $t_{INITIAL}$, t_{RISE}, t_{HOLD}, t_{FALL}, t_{PULSE} and t_{OFF}. The pattern timing sequence is shown in Figure 7.

Table 1. Color Pattern Configuration Registers

Mode	Color Pattern	Color of ILED1	Color of ILED2	Color of ILED3	Color Enable	Color Loop Count
Pattern	Color Pattern 1	REG0x0B	REG0x0C	REG0x0D	REG0x1A[0] = 1	REG0x1B[1:0]
	Color Pattern 2	REG0x0E	REG0x0F	REG0x10	REG0x1A[1] = 1	REG0x1B[3:2]
	Color Pattern 3	REG0x11	REG0x12	REG0x13	REG0x1A[2] = 1	REG0x1B[5:4]
	Color Pattern 4	REG0x14	REG0x15	REG0x16	REG0x1A[3] = 1	REG0x1B[7:6]

DETAILED DESCRIPTION (continued)

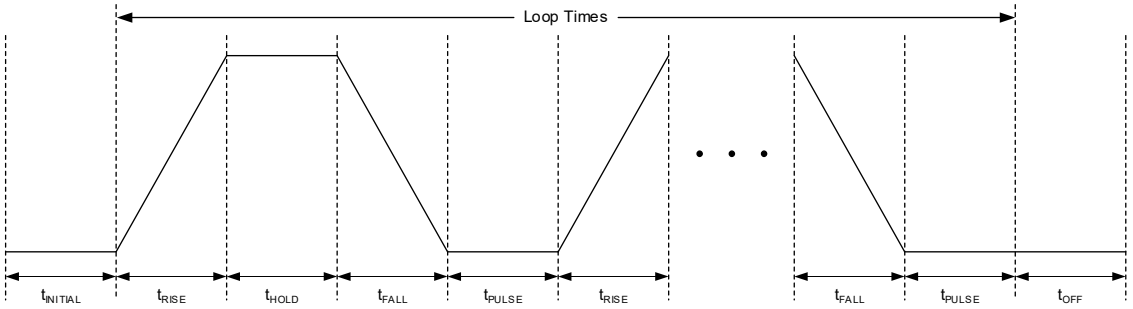


Figure 7. Pattern Timing Sequence

Gamma Correction

Gamma correction is used to map linear luminance to the non-linear behavior of displays. Since the SGM31030 can control LED brightness in 256 levels, gamma correction is applied when computing each LED's intensity to ensure the brightness transitions align with the human eye's perception.

The SGM31030 offers 2.2 gamma correction option and linear option, which can be configured by the PAT_GAM bit in the pattern GAM register (REG0x1D). The gamma correction is shown in Figure 8.

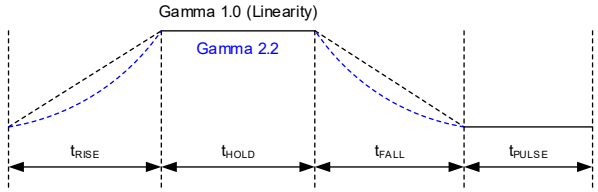


Figure 8. Gamma Correction

Pattern Loop

The total pattern loop count is a combination of CNT_GAIN0, CNT_GAIN1 and LOOP_CNT. The total pattern loop count is given by Equation 4:

$$\text{Total Loop Count} = \text{CNT\_GAIN1} \times \text{CNT\_GAIN0} \times \text{LOOP\_CNT} \quad (4)$$

The entire pattern timing diagram is shown in Figure 9.

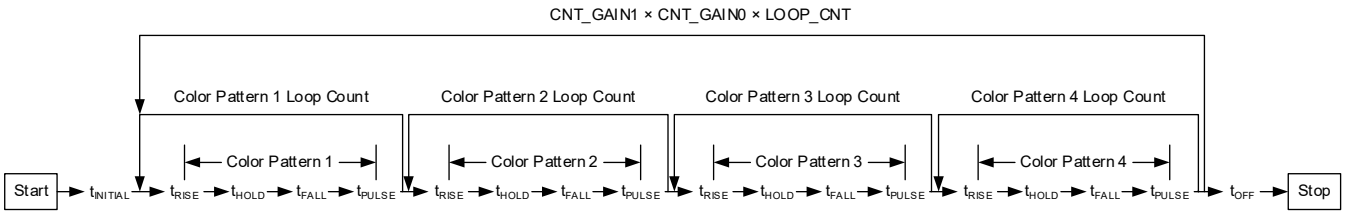


Figure 9. Pattern Mode

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM31030 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM31030 operates as a slave device that address is 0x32 (32H). It has thirty five 8-bit registers, numbered from REG0x00 to REG0x30.

Physical Layer

The standard I²C interface of SGM31030 supports standard mode, fast mode and fast mode plus communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s and the fast mode plus is up to 1Mbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 10. All transactions are started by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

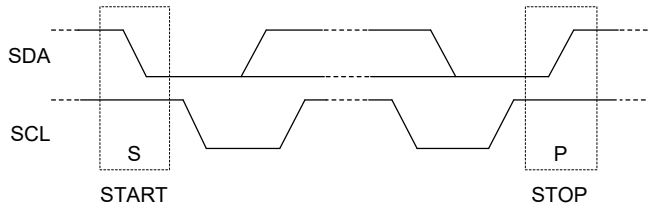


Figure 10. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 11.

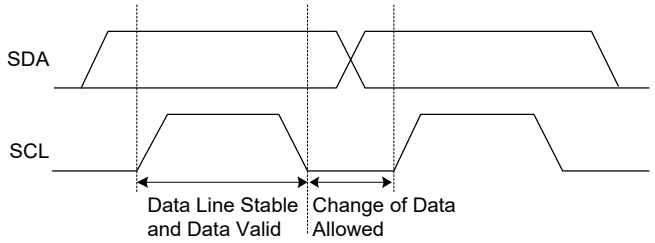


Figure 11. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 12 shows the byte transfer process with I²C interface.

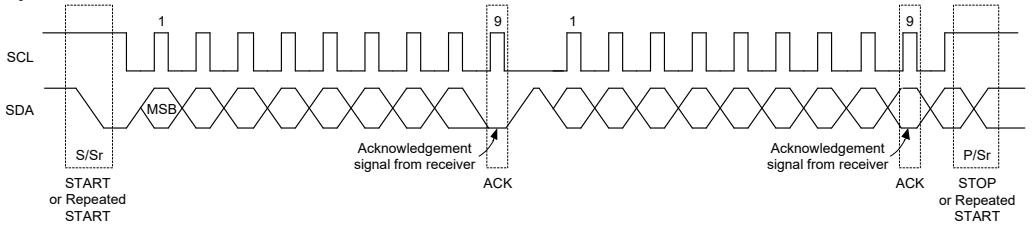


Figure 12. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 13.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 14 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 15), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

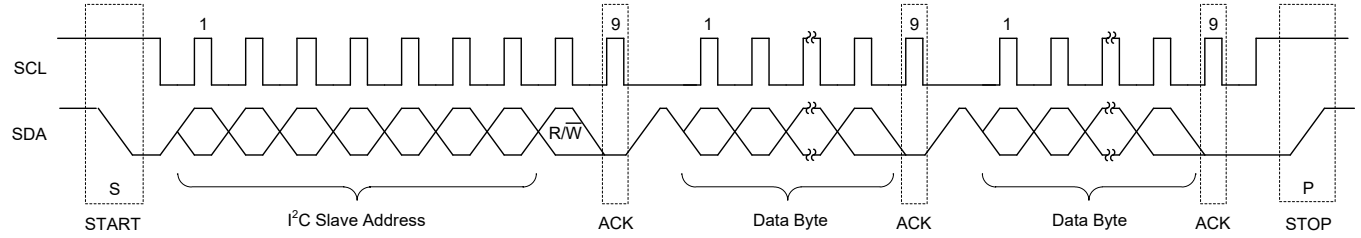


Figure 13. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

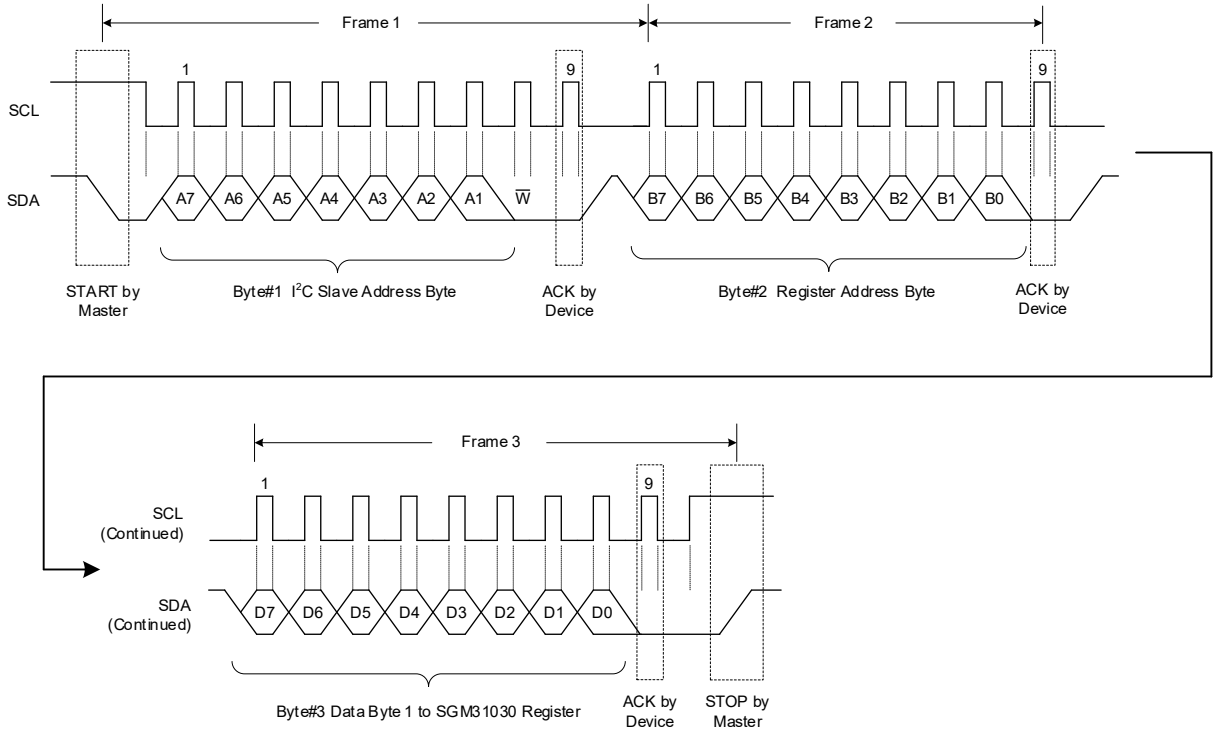


Figure 14. A Single Write Transaction

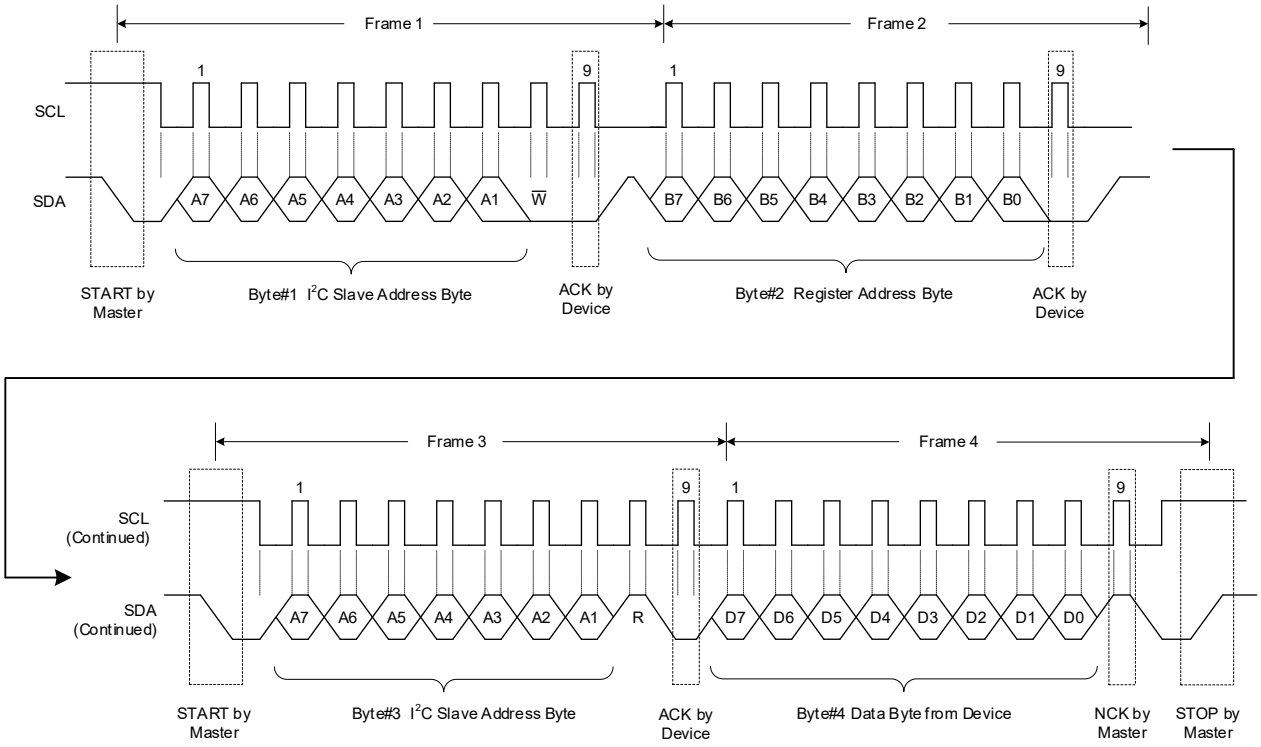


Figure 15. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM31030 for REG0x00 through REG0x30 registers, as explained in Figure 16 and Figure 17. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

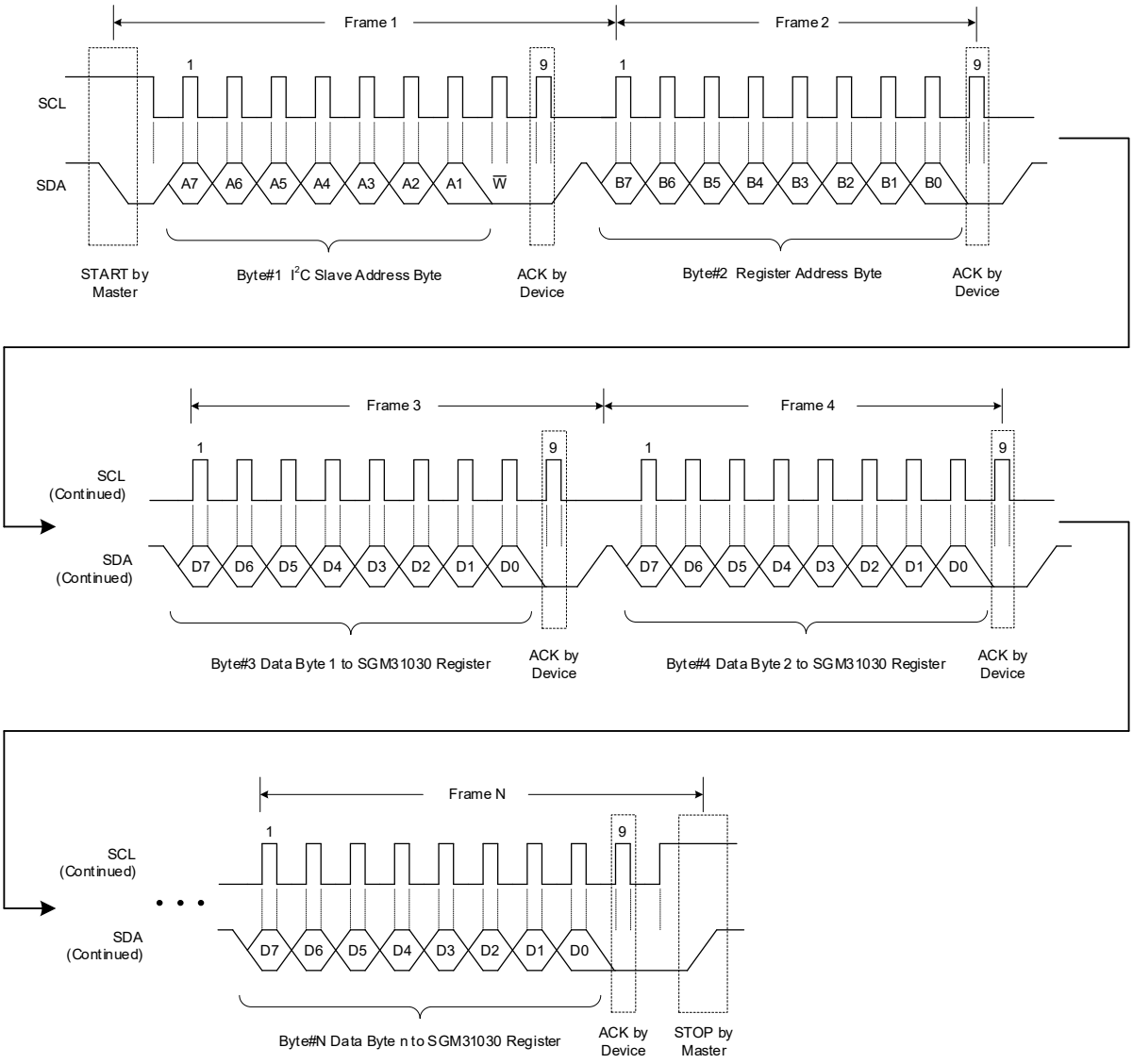


Figure 16. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

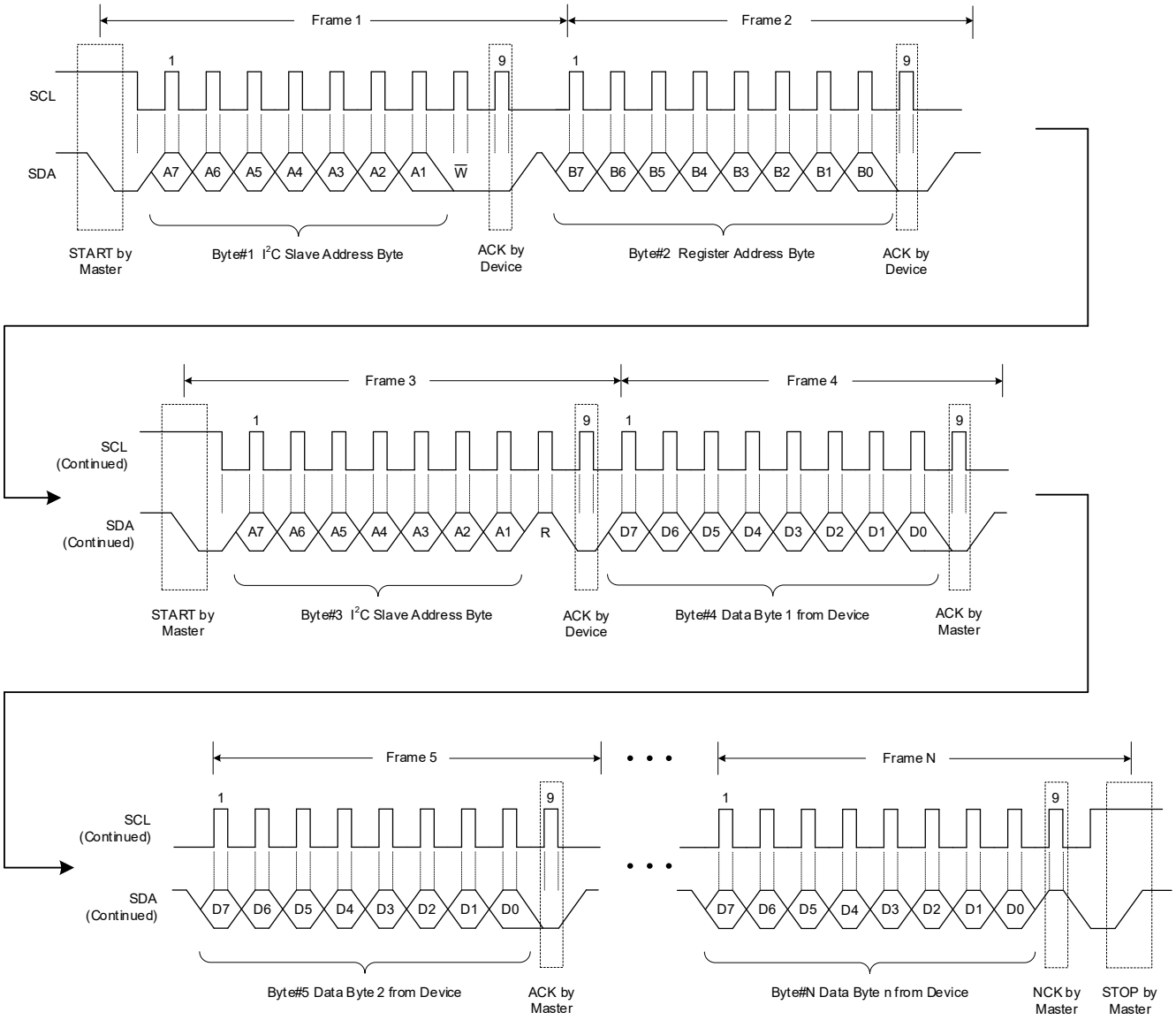


Figure 17. A Multi-Read Transaction

REGISTER MAPS

REGISTER NAME	FUNCTION	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
REG0x00	Chip ID	0000 0011							
REG0x01	Global Control	Reserved		CHIPEN	ECO_MODE	PFS	LED3_EN	LED2_EN	LED1_EN
REG0x02	LED_MODE	Reserved		LED3_MODE[1:0]		LED2_MODE[1:0]		LED1_MODE[1:0]	
REG0x03	LED1_FADE	Reserved					LED1_FADE_OUT	LED1_FADE_IN	Reserved
REG0x04	LED2_FADE	Reserved					LED2_FADE_OUT	LED2_FADE_IN	Reserved
REG0x05	LED3_FADE	Reserved					LED3_FADE_OUT	LED3_FADE_IN	Reserved
REG0x06	GCC	Reserved	LCAI	GCC[5:0]					
REG0x07	PWM CONFIG	Reserved					PFA[2:0]		
REG0x08	LED1_PWM	LED1 PWM used in PWM & Current Level Mode							
REG0x09	LED2_PWM	LED2 PWM used in PWM & Current Level Mode							
REG0x0A	LED3_PWM	LED3 PWM used in PWM & Current Level Mode							
REG0x0B	COL1_ILED1	LED1 Current in Current Mode or in Color Configuration1							
REG0x0C	COL1_ILED2	LED2 Current in Current Mode or in Color Configuration1							
REG0x0D	COL1_ILED3	LED3 Current in Current Mode or in Color Configuration1							
REG0x0E	COL2_ILED1	LED1 Current in Color Configuration2							
REG0x0F	COL2_ILED2	LED2 Current in Color Configuration2							
REG0x10	COL2_ILED3	LED3 Current in Color Configuration2							
REG0x11	COL3_ILED1	LED1 Current in Color Configuration3							
REG0x12	COL3_ILED2	LED2 Current in Color Configuration3							
REG0x13	COL3_ILED3	LED3 Current in Color Configuration3							
REG0x14	COL4_ILED1	LED1 Current in Color Configuration4							
REG0x15	COL4_ILED2	LED2 Current in Color Configuration4							
REG0x16	COL4_ILED3	LED3 Current in Color Configuration4							
REG0x17	PAT_TMR1	TRISE[3:0]				TINITIAL[3:0]			
REG0x18	PAT_TMR2	TFALL[3:0]				THOLD[3:0]			
REG0x19	PAT_TMR3	TOFF[3:0]				TPULSE[3:0]			
REG0x1A	PAT_CTRL1	CNT_GAIN0[3:0]				COL4_EN	COL3_EN	COL2_EN	COL1_EN
REG0x1B	PAT_CTRL2	COL4_CNT[1:0]		COL3_CNT[1:0]		COL2_CNT[1:0]		COL1_CNT[1:0]	
REG0x1C	PAT_CTRL3	CNT_GAIN1	LOOP_CNT[6:0]						
REG0x1D	PAT_GAM	Reserved							PAT_GAM
REG0x1E	PAT_STAT	PAT_STAT	COL4_STAT	COL3_STAT	COL2_STAT	COL1_STAT	PAT_TMR_STAT[2:0]		
REG0x1F	COL_UPDATE	Write “0x00” to 1Fh will update the data of COLx_ILEDy (x = 1, 2, 3, 4, y = 1, 2, 3), located at 0Bh ~16h.							
REG0x20	PWM_UPDATE	Write “0x00” to 20h will update the data of PFS and LED1/2/3_PWM, located at 01h[3] and 08h to 0Ah.							
REG0x21	PAT_UPDATE	Write “0x00” to 21h will update the data of PAT_TMR1/2/3, PAT_CTRL1/2/3, PAT_GAM, and PAT_STAT, located from 17h~1Eh.							
REG0x30	RESET	Write “0x00” to the Reset register, then SGM31030 will reset all registers to their default values.							

REGISTER MAPS (continued)

I²C Slave Address of SGM31030: 0x32

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

W: Write only bit(s)

REG0x00: Chip ID Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CHIP_ID[7:0]	00000011	R	Chip ID 00000011 = SGM31030

REG0x01: Global Control Register [Reset = 0x07]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5]	CHIPEN	0	R/W	Chip Enable 0 = Disable chip (default) 1 = Enable chip
D[4]	ECO_MODE	0	R/W	ECO Mode Enable 0 = Disable ECO mode. (default) 1 = Enable ECO mode. The chip will shut down if no LED outputs are detected after 30s. The chip can be reactivated by disabling ECO mode.
D[3]	PFS	0	R/W	PWM Frequency Select 0 = 200Hz (default) 1 = 400Hz PFS setting only applies in the PWM & current level mode.
D[2]	LED3_EN	1	R/W	LED3 Output Enable Control 0 = Disable 1 = Enable (default) LED3_EN will be masked if the chip is disabled, CHIPEN = 0.
D[1]	LED2_EN	1	R/W	LED2 Output Enable Control 0 = Disable 1 = Enable (default) LED2_EN will be masked if the chip is disabled, CHIPEN = 0.
D[0]	LED1_EN	1	R/W	LED1 Output Enable Control 0 = Disable 1 = Enable (default) LED1_EN will be masked if the chip is disabled, CHIPEN = 0.

REGISTER MAPS (continued)

REG0x02: LED Mode Configuration Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:4]	LED3_MODE[1:0]	00	R/W	LED3 Output Operation Mode 00 = PWM & current level mode (default) 01 = Pattern mode 10/11 = Current level mode
D[3:2]	LED2_MODE[1:0]	00	R/W	LED2 Output Operation Mode 00 = PWM & current level mode (default) 01 = Pattern mode 10/11 = Current level mode
D[1:0]	LED1_MODE[1:0]	00	R/W	LED1 Output Operation Mode 00 = PWM & current level mode (default) 01 = Pattern mode 10/11 = Current level mode

NOTE:
When LEDx works in PWM mode, pattern mode and current level mode, the output current is controlled by PWM, color setting and current level registers, respectively. In ECO mode, LED mode cannot be modified.

REG0x03: LED1 FADE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2]	LED1_FADE_OUT	0	R/W	LED1 Linear Fade-out Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-out is disable (default) 1 = PWM fade-out is enable, the dimming time decided by t_{FALL}
D[1]	LED1_FADE_IN	0	R/W	LED1 Linear Fade-in Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-in is disable (default) 1 = PWM fade-in is enable, the dimming time decided by t_{RISE}
D[0]	Reserved	0	R/W	Reserved

REG0x04: LED2 FADE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2]	LED2_FADE_OUT	0	R/W	LED2 Linear Fade-out Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-out is disable (default) 1 = PWM fade-out is enable, the dimming time decided by t_{FALL}
D[1]	LED2_FADE_IN	0	R/W	LED2 Linear Fade-in Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-in is disable (default) 1 = PWM fade-in is enable, the dimming time decided by t_{RISE}
D[0]	Reserved	0	R/W	Reserved

REG0x05: LED3 FADE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2]	LED3_FADE_OUT	0	R/W	LED3 Linear Fade-out Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-out is disable (default) 1 = PWM fade-out is enable, the dimming time decided by t_{FALL}
D[1]	LED3_FADE_IN	0	R/W	LED3 Linear Fade-in Enable Control, Only Active in PWM & Current Level Mode 0 = PWM fade-in is disable (default) 1 = PWM fade-in is enable, the dimming time decided by t_{RISE}
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x06: Global Current Control Register [Reset = 0x3F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6]	LCAI	0	R/W	Low Current Accuracy Improve 0 = 25mA as the maximum output current. (default) 1 = 6.25mA as the maximum output current to improve low current accuracy.
D[5:0]	GCC[5:0]	111111	R/W	Maximum Global Current Control GCC[5:0] bits control I_{OUT} as shown in Equation 5. $I_{OUT\_MAX} = \begin{cases} 25mA \times \frac{GCC}{63} \times \frac{COL}{255}, LCAI = 0 \\ 6.25mA \times \frac{GCC}{63} \times \frac{COL}{255}, LCAI = 1 \end{cases}$ (5) where I_{OUT} is the average current of the outputs; GCC is the decimal number of GCC[5:0]; COL is the decimal number of COLx_ILEDy[7:0] (x = 1, 2, 3, 4, y = 1, 2, 3) depending on the output channel and operating mode.

REG0x07: PWM Frequency Configuration Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2:0]	PFA[2:0]	000	R/W	PWM Frequency Adjust 000 = 0% (default) 001 = +12.5% 010 = +25% 011 = +37.5% 100 = -50% 101 = -37.5% 110 = -25% 111 = -12.5%

REG0x08: LED1 PWM Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LED1_PWM[7:0]	00000000	R/W	8-Bit PWM of LED1 Only used in PWM & current level mode. The output PWM is in full duty cycle if LED1_PWM[7:0] = 255.

REG0x09: LED2 PWM Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LED2_PWM[7:0]	00000000	R/W	8-Bit PWM of LED2 Only used in PWM & current level mode. The output PWM is in full duty cycle if LED2_PWM[7:0] = 255.

REG0x0A: LED3 PWM Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LED3_PWM[7:0]	00000000	R/W	8-Bit PWM of LED3 Only used in PWM & current level mode. The output PWM is in full duty cycle if LED3_PWM[7:0] = 255.

REGISTER MAPS (continued)

REG0x0B: LED1 Current Level and Color #1 Current Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL1_ILED1[7:0]	00000000	R/W	LED1 Current Output in Current Mode, and in the Pattern Mode of Color #1

REG0x0C: LED2 Current Level and Color #1 Current Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL1_ILED2[7:0]	00000000	R/W	LED2 Current Output in Current Mode, and in the Pattern Mode of Color #1

REG0x0D: LED3 Current Level and Color #1 Current Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL1_ILED3[7:0]	00000000	R/W	LED3 Current Output in Current Mode, and in the Pattern Mode of Color #1

REG0x0E: Color #2 LED1 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL2_ILED1[7:0]	00000000	R/W	LED1 Current Output in the Pattern Mode of Color #2

REG0x0F: Color #2 LED2 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL2_ILED2[7:0]	00000000	R/W	LED2 Current Output in the Pattern Mode of Color #2

REG0x10: Color #2 LED3 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL2_ILED3[7:0]	00000000	R/W	LED3 Current Output in the Pattern Mode of Color #2

REG0x11: Color #3 LED1 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL3_ILED1[7:0]	00000000	R/W	LED1 Current Output in the Pattern Mode of Color #3

REG0x12: Color #3 LED2 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL3_ILED2[7:0]	00000000	R/W	LED2 Current Output in the Pattern Mode of Color #3

REG0x13: Color #3 LED3 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL3_ILED3[7:0]	00000000	R/W	LED3 Current Output in the Pattern Mode of Color #3

REGISTER MAPS (continued)

REG0x14: Color #4 LED1 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL4_ILED1[7:0]	00000000	R/W	LED1 Current Output in the Pattern Mode of Color #4

REG0x15: Color #4 LED2 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL4_ILED2[7:0]	00000000	R/W	LED2 Current Output in the Pattern Mode of Color #4

REG0x16: Color #4 LED3 Current Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COL4_ILED3[7:0]	00000000	R/W	LED3 Current Output in the Pattern Mode of Color #4

REG0x17: Pattern Timer 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	TRISE[3:0]	0000	R/W	Rise Time (t_{RISE}) Selection 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.
D[3:0]	TINITIAL[3:0]	0000	R/W	Pattern Start Time ($t_{INITIAL}$) Selection 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.

REGISTER MAPS (continued)

REG0x18: Pattern Timer 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	TFALL[3:0]	0000	R/W	Fall Time (t_{FALL}) Selection 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.
D[3:0]	THOLD[3:0]	0000	R/W	Hold Time (t_{HOLD}) Selection 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.

REGISTER MAPS (continued)

REG0x19: Pattern Timer 3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	TOFF[3:0]	0000	R/W	Off Time (t_{OFF}) Selection 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.
D[3:0]	TPULSE[3:0]	0000	R/W	Time (t_{PULSE}) between Pulses 0000 = 0.04s (default) 0001 = 0.16s 0010 = 0.32s 0011 = 0.48s 0100 = 0.64s 0101 = 0.96s 0110 = 1.28s 0111 = 1.92s 1000 = 2.56s 1001 = 3.20s 1010 = 3.84s 1011 = 5.12s 1100 = 6.40s 1101 = 7.68s 1110 = 8.96s 1111 = 10.24s NOTE: This function takes effect after writing 0x00 to REG0x20 register.

REGISTER MAPS (continued)

REG0x1A: Pattern Control1 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	CNT_GAIN0[3:0]	0000	R/W	Pattern Loop Count Gain0 If CNT_GAIN0[3:0] = 0h, endless (default) If CNT_GAIN0[3:0] ≠ 0h, the loop count is CNT_GAIN1 × CNT_GAIN0 × LOOP_CNT. CNT_GAIN0 and LOOP_CNT are the decimal numbers of CNT_GAIN0[3:0] and LOOP_CNT[6:0], respectively.
D[3]	COL4_EN (1)	0	R/W	Color #4 Enable Selection 0 = color #4 disable (default) 1 = color #4 enable
D[2]	COL3_EN (1)	0	R/W	Color #3 Enable Selection 0 = color #3 disable (default) 1 = color #3 enable
D[1]	COL2_EN (1)	0	R/W	Color #2 Enable Selection 0 = color #2 disable (default) 1 = color #2 enable
D[0]	COL1_EN (1)	1	R/W	Color #1 Enable Selection 0 = color #1 disable 1 = color #1 enable (default)

NOTE:

1. These bits cannot be set to all zeros.

REG0x1B: Pattern Control2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	COL4_CNT[1:0]	00	R/W	Color #4 Cycle Time Selection 00 = endless (default) 01 = 1 time 10 = 2 times 11 = 3 times
D[5:4]	COL3_CNT[1:0]	00	R/W	Color #3 Cycle Time Selection 00 = endless (default) 01 = 1 time 10 = 2 times 11 = 3 times
D[3:2]	COL2_CNT[1:0]	00	R/W	Color #2 Cycle Time Selection 00 = endless (default) 01 = 1 time 10 = 2 times 11 = 3 times
D[1:0]	COL1_CNT[1:0]	00	R/W	Color #1 Cycle Time Selection 00 = endless (default) 01 = 1 time 10 = 2 times 11 = 3 times

REG0x1C: Pattern Control3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	CNT_GAIN1	0	R/W	Pattern Loop Count Gain1 0 = 1 time (default) 1 = 16 times
D[6:0]	LOOP_CNT[6:0]	0000000	R/W	Pattern Loop Count Setting If LOOP_CNT[6:0] = 0h, endless (default) If LOOP_CNT[6:0] ≠ 0h, the loop count is CNT_GAIN1 × CNT_GAIN0 × LOOP_CNT. CNT_GAIN0 and LOOP_CNT are the decimal numbers of CNT_GAIN0[3:0] and LOOP_CNT[6:0], respectively.

REGISTER MAPS (continued)

REG0x1D: Pattern GAM Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	0000000	R/W	Reserved
D[0]	PAT_GAM	0	R/W	Gamma Selection in Pattern Mode 0 = Gamma = 2.2 (default) 1 = Linearity

REG0x1E: Pattern State Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PAT_STAT	0	R	0 = Not running at Pattern (default) 1 = Running at pattern
D[6]	COL4_STAT	0	R	0 = Not running at Color #4 (default) 1 = Running at Color #4
D[5]	COL3_STAT	0	R	0 = Not running at Color #3 (default) 1 = Running at Color #3
D[4]	COL2_STAT	0	R	0 = Not running at Color #2 (default) 1 = Running at Color #2
D[3]	COL1_STAT	0	R	0 = Not running at Color #1 (default) 1 = Running at Color #1
D[2:0]	PAT_TMR_STAT[2:0]	000	R	000 = Running at $t_{INITIAL}$ (default) 001 = Running at t_{RISE} 010 = Running at t_{HOLD} 011 = Running at t_{FALL} 100 = Running at t_{PULSE} 101 = Running at t_{OFF}

REG0x1F: Color Update Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	COLOR_UPDATE[7:0]	00000000	R/W	Write “0x00” to 1Fh will update the data of COLx_ILEDy (x = 1, 2, 3, 4, y = 1, 2, 3), located at 0Bh ~16h.

REG0x20: PWM Update Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PWM_UPDATE[7:0]	00000000	R/W	Write “0x00” to 20h will update the data of PFS and LED1/2/3_PWM, located at 01h[3] and 08h to 0Ah.

REG0x21: PWM Time Update Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PWM_TM_UPDATE[7:0]	00000000	R/W	Write “0x00” to 21h will update the data of PAT_TMR1/2/3, PAT_CTRL1/2/3, PAT_GAM, and PAT_STAT, located from 17h~1Eh.

REG0x30: Reset Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	RESET[7:0]	00000000	W	Writes “0x00” to the Reset Register, then SGM31030 will reset all registers to the default values.

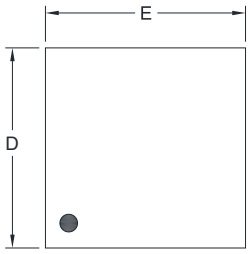
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

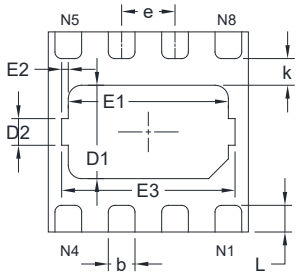
Changes from Original to REV.A (NOVEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

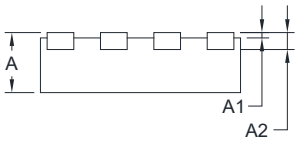
UTDFN-1.5×1.5-8L



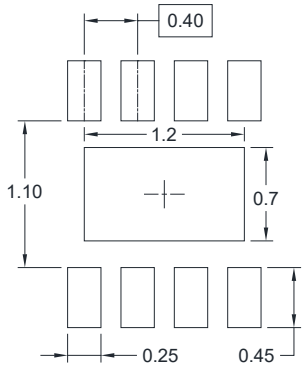
TOP VIEW



BOTTOM VIEW



SIDE VIEW



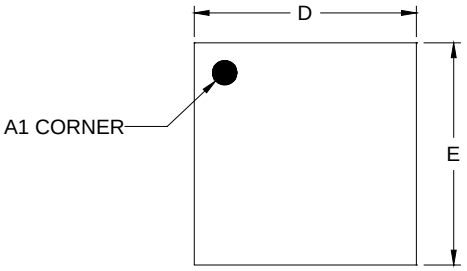
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.400	0.500	0.016	0.020
A1	0.000	0.050	0.000	0.002
A2	0.127 REF		0.005 REF	
D	1.450	1.550	0.057	0.061
D1	0.600	0.800	0.024	0.031
D2	0.200 REF		0.008 REF	
E	1.450	1.550	0.057	0.061
E1	1.100	1.300	0.043	0.051
E2	0.050 REF		0.002 REF	
E3	1.200	1.400	0.047	0.055
k	0.200 REF		0.008 REF	
b	0.150	0.250	0.006	0.010
e	0.400 BSC		0.016 BSC	
L	0.150	0.250	0.006	0.010

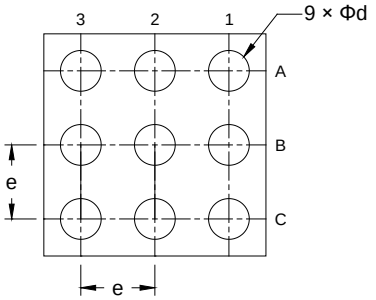
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

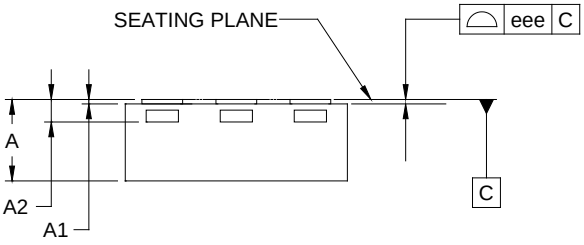
UTQFN-1.5×1.5-9AL



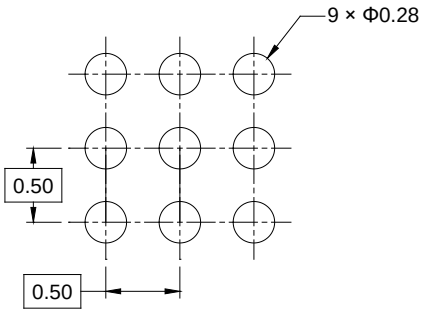
TOP VIEW



BOTTOM VIEW



SIDE VIEW



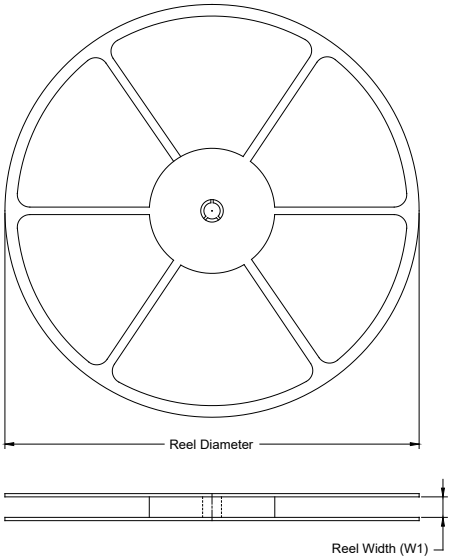
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.152 REF		
D	1.400	-	1.600
E	1.400	-	1.600
d	0.225	-	0.325
e	0.500 BSC		
eee	0.050		

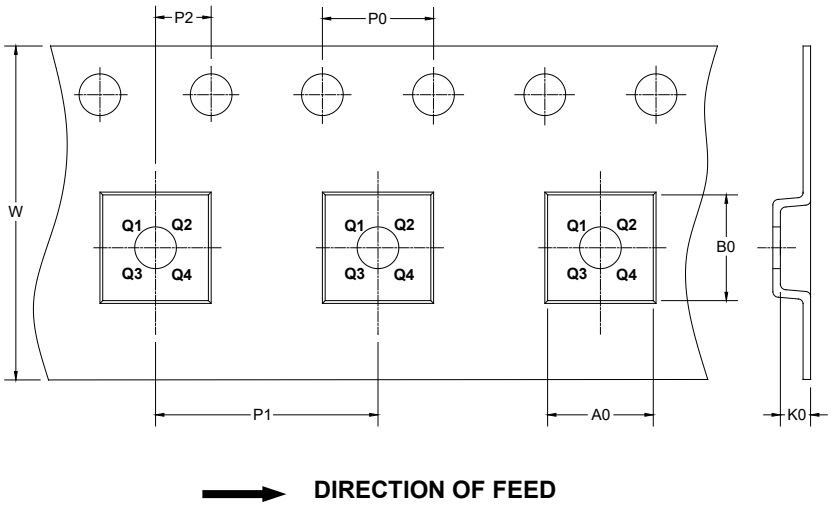
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



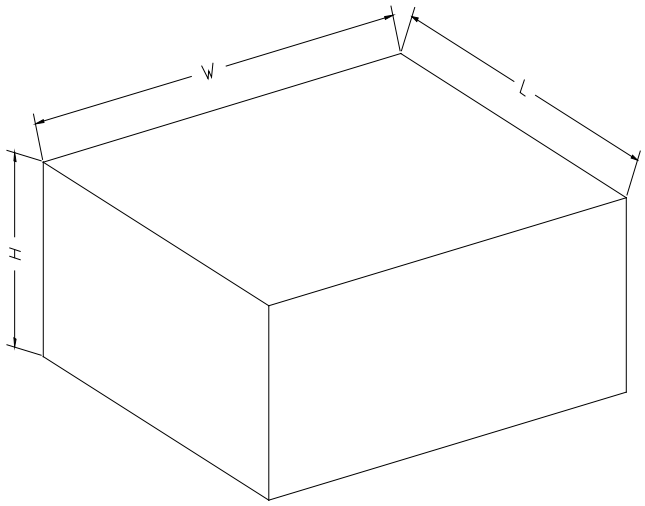
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.5×1.5-8L	7"	9.0	1.70	1.70	0.75	4.0	4.0	2.0	8.0	Q1
UTQFN-1.5×1.5-9AL	7"	9.0	1.70	1.70	0.75	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002